# ADuM2200/ADuM2201

## Dual-Channel Digital Isolators, 5 kV

## FEATURES

- High isolation voltage: 5000 V rms
- Enhanced system-level ESD performance per IEC 61000-4-x
- Low power operation
  - 5 V operation
    - 1.6 mA per channel maximum at 0 Mbps to 1 Mbps
    - 3.7 mA per channel maximum at 10 Mbps
  - 3.3 V operation
    - 1.4 mA per channel maximum at 0 Mbps to 1 Mbps
    - 2.4 mA per channel maximum at 10 Mbps
- 3.3 V/5 V level translation
- High temperature operation: 105°C and 125°C options
- High data rate: dc to 10 Mbps (NRZ)
- Precise timing characteristics
  - 3 ns maximum pulse width distortion
  - 3 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/µs
- 16-lead SOIC wide body package version (RW-16)
- 16-lead SOIC wide body enhanced creepage version (RI-16-2)
- Safety and regulatory approvals
  - UL 1577
    - $V_{ISO}$ = 5000 V rms for 1 minute.
  - IEC/EN/CSA 62368-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - $V_{IORM}$ = 645 V peak
- Qualified for automotive applications

## APPLICATIONS

- General-purpose, high voltage, multichannel isolation
- Medical equipment
- Power supplies
- RS-232/RS-422/RS-485 transceiver isolation
- Hybrid electric vehicles, battery monitors, and motor drives

## GENERAL DESCRIPTION

The ADuM2200/ADuM2201[1] are 2-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics that are superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. Typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM2200/ADuM2201 isolators provide two independent isolation channels in two channel configurations with data rates up to 10 Mbps (see the Ordering Guide). Both parts operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems, as well as enabling voltage translation functionality across the isolation barrier. The ADuM2200/ADuM2201 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

Similar to the ADuM3200/ADuM3201 isolators, the ADuM2200/ADuM2201 isolators contain various circuit and layout enhancements that provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM3200/ADuM3201 or ADuM2200/ADuM2201 products is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents pending.

Rev. H

## TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagrams ... 3
Specifications ... 4
Electrical Characteristics—5 V Operation ... 4
Electrical Characteristics—3.3 V Operation ... 5
Electrical Characteristics—Mixed 5 V/3.3 V Operation ... 6
Electrical Characteristics—Mixed 3.3 V/5 V Operation ... 7
Package Characteristics ... 8
Regulatory Information ... 9
Insulation and Safety-Related Specifications ... 10
DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics ... 10
Recommended Operating Conditions ... 11
Absolute Maximum Ratings ... 12
Maximum Continuous Working Voltage ... 12
ESD Caution ... 12
Pin Configurations and Function Descriptions ... 13
Typical Performance Characteristics ... 15
Applications Information ... 16
PCB Layout ... 16
Propagation Delay-Related Parameters ... 16
DC Correctness and Magnetic Field Immunity ... 16
Power Consumption ... 17
Insulation Lifetime ... 18
Outline Dimensions ... 19
Ordering Guide ... 19
Number of Inputs, Maximum Data Rate, Maximum Propagation, and Maximum Pulse Width Distortion Options ... 19
Automotive Products ... 20

## REVISION HISTORY

**1/2025—Rev. G to Rev. H**

Changes to Features Section ... 1
Moved Figure 1 and Figure 2 ... 3
Changes to Regulatory Information Section and Table 14 ... 9
Changes to Table 15 ... 10
Changed Insulation Characteristics (DIN V VDE V 0884-10 (VDE V 0884-10):2006-12) Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section ... 10
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section, Table 16, and Figure 3 Caption ... 10
Changes to Table 19 ... 12
Deleted Table 20 and Table 21; Renumbered Sequentially ... 12
Changes to Insulation Lifetime Section ... 18
Deleted Figure 16 to Figure 18; Renumbered Sequentially ... 18
Added Number of Inputs, Maximum Data Rate, Maximum Propagation, and Maximum Pulse Width Distortion Options ... 19

## FUNCTIONAL BLOCK DIAGRAMS

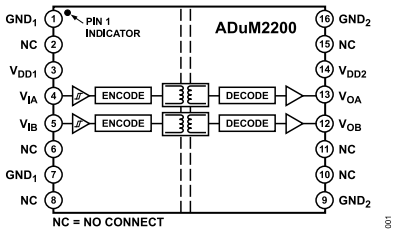


*Figure 1. ADuM2200*

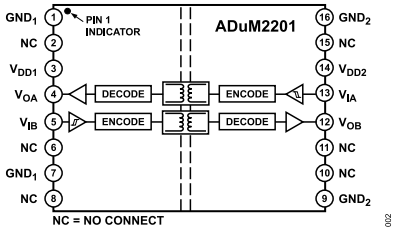


*Figure 2. ADuM2201*

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective grounds. 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 5.0 V.

*Table 1.*

| | | A Grade | | | B Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments** |
| SWITCHING SPECIFICATIONS | | | | | | | | | $C_L$ = 15 pF, CMOS levels |
| Pulse Width | PW | 1000 | | | 100 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 10 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 20 | | 150 | 20 | | 50 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 40 | | | 3 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | | | | 5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 100 | | | 15 | ns | Between any two units |
| Channel Matching | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | ns | |
| Opposing Directional | $t_{PSKOD}$ | | | 50 | | | 15 | ns | |

*Table 2.*

| | | 1 Mbps—A Grade, B Grade | | | 10 Mbps—B Grade | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| SUPPLY CURRENT (NO LOAD) | | | | | | | | |
| ADuM2200 | $I_{DD1}$ | | 1.3 | 1.8 | | 3.5 | 4.6 | mA |
| | $I_{DD2}$ | | 1.0 | 1.6 | | 2.0 | 2.8 | mA |
| ADuM2201 | $I_{DD1}$ | | 1.1 | 1.6 | | 3.1 | 4.2 | mA |
| | $I_{DD2}$ | | 1.3 | 1.9 | | 3.1 | 4.0 | mA |

*Table 3.*

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments**[1] |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | 5.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.5 | 4.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI (Q)}$ | | 0.4 | 0.8 | mA | All inputs at logic low |
| Quiescent Output Supply Current | $I_{DDO (Q)}$ | | 0.5 | 0.6 | mA | All inputs at logic low |
| Dynamic Input Supply Current | $I_{DDI (D)}$ | | 0.19 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO (D)}$ | | 0.05 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R$/$t_F$ | | | | | 10% to 90% |
| A Grade | | | 10 | | ns | |
| B Grade | | | 2.5 | | ns | |
| Common-Mode Transient Immunity[2] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |

## SPECIFICATIONS

[1] $I_{Ox}$ is the Channel x output current, where x = A or B, $V_{IxH}$ is the input side logic high, and $V_{IxL}$ is the input side logic low.

[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective grounds. 3.0 V ≤ $V_{DD1}$ ≤ 3.6 V, 3.0 V ≤ $V_{DD2}$ ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 3.3 V.

***Table 4.***

| | | A Grade | | | B Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments** |
| SWITCHING SPECIFICATIONS | | | | | | | | | $C_L$ = 15 pF, CMOS levels |
| Pulse Width | PW | 1000 | | | 100 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 10 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 20 | | 150 | 20 | | 60 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | | | | | | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| A Grade and B Grade | | | | 40 | | | 3 | ns | |
| WA Grade and WB Grade | | | | 40 | | | 4 | ns | |
| Change vs. Temperature | | | | | | 5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 100 | | | 22 | ns | Between any two units |
| Channel Matching | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | ns | |
| Opposing Directional | $t_{PSKOD}$ | | | 50 | | | 22 | ns | |

***Table 5.***

| | | 1 Mbps—A Grade, B Grade | | | 10 Mbps—B Grade | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| SUPPLY CURRENT (NO LOAD) | | | | | | | | |
| ADuM2200 | $I_{DD1}$ | | 0.8 | 1.3 | | 2.2 | 3.2 | mA |
| | $I_{DD2}$ | | 0.7 | 1.0 | | 1.3 | 1.7 | mA |
| ADuM2201 | $I_{DD1}$ | | 0.7 | 1.3 | | 1.9 | 2.5 | mA |
| | $I_{DD2}$ | | 0.8 | 1.6 | | 1.9 | 2.5 | mA |

***Table 6.***

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions/Comments**[1] |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | 3.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.5 | 2.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI\ (Q)}$ | | 0.3 | 0.5 | mA | All inputs at logic low |
| Quiescent Output Supply Current | $I_{DDO\ (Q)}$ | | 0.3 | 0.5 | mA | All inputs at logic low |
| Dynamic Input Supply Current | $I_{DDI\ (D)}$ | | 0.10 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO\ (D)}$ | | 0.03 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R$/$t_F$ | | | | | 10% to 90% |

## SPECIFICATIONS

*Table 6. (Continued)*

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments[1] |
|---|---|---|---|---|---|---|
| A Grade | | | 10 | | ns | |
| B Grade | | | 3 | | ns | |
| Common-Mode Transient Immunity[2] | \|CM\| | 25 | 35 | | kV/µs | $V_{Ix} = V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.1 | | Mbps | |

[1] $I_{Ox}$ is the Channel x output current, where x = A or B, $V_{IxH}$ is the input side logic high, and $V_{IxL}$ is the input side logic low.

[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All voltages are relative to their respective grounds. 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 3.0 V ≤ $V_{DD2}$ ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 3.3 V, $V_{DD2}$ = 5.0 V.

*Table 7.*

| | | A Grade | | | B Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Unit | Test Conditions/ Comments |
| SWITCHING SPECIFICATIONS | | | | | | | | | $C_L$ = 15 pF, CMOS levels |
| Pulse Width | PW | 1000 | | | 100 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 10 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 15 | | 150 | 15 | | 55 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | | | | | | $\|t_{PLH} - t_{PHL}\|$ |
| A Grade and B Grade | | | | 40 | | | 3 | ns | |
| WA Grade and WB Grade | | | | 40 | | | 4 | ns | |
| Change vs. Temperature | | | | | | 5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 50 | | | 22 | ns | Between any two units |
| Channel Matching | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | ns | |
| Opposing Directional | $t_{PSKOD}$ | | | 50 | | | 22 | ns | |

*Table 8.*

| | | 1 Mbps—A Grade, B Grade | | | 10 Mbps—B Grade | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |
| SUPPLY CURRENT (NO LOAD) | | | | | | | | |
| ADuM2200 | $I_{DD1}$ | | 1.3 | 1.8 | | 3.5 | 4.6 | mA |
| | $I_{DD2}$ | | 0.7 | 1.0 | | 1.3 | 1.7 | mA |
| ADuM2201 | $I_{DD1}$ | | 1.1 | 1.6 | | 3.1 | 4.2 | mA |
| | $I_{DD2}$ | | 0.8 | 1.6 | | 1.9 | 2.5 | mA |

*Table 9.*

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments[1] |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | $V_{DDx}$ | | V | $I_{Ox}$ = −20 µA, $V_{Ix} = V_{IxH}$ |
| | | $V_{DDx}$ − 0.5 | $V_{DDx}$ − 0.2 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix} = V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 µA, $V_{Ix} = V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix} = V_{IxL}$ |

## SPECIFICATIONS

*Table 9. (Continued)*

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments[1] |
|---|---|---|---|---|---|---|
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI (Q)}$ | | 0.4 | 0.8 | mA | All inputs at logic low |
| Quiescent Output Supply Current | $I_{DDO (Q)}$ | | 0.3 | 0.5 | mA | All inputs at logic low |
| Dynamic Input Supply Current | $I_{DDI (D)}$ | | 0.19 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO (D)}$ | | 0.03 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R/t_F$ | | | | | 10% to 90% |
| A Grade | | | 10 | | ns | |
| B Grade | | | 3 | | ns | |
| Common-Mode Transient Immunity[2] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |

[1] $I_{Ox}$ is the Channel x output current, where x = A or B, $V_{IxH}$ is the input side logic high, and $V_{IxL}$ is the input side logic low.

[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All voltages are relative to their respective grounds. 3.0 V ≤ $V_{DD1}$ ≤ 3.6 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 5.0 V, $V_{DD2}$ = 3.3 V.

*Table 10.*

| | | A Grade | | | B Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Unit | Test Conditions/Comments |
| SWITCHING SPECIFICATIONS | | | | | | | | | $C_L$ = 15 pF, CMOS levels |
| Pulse Width | PW | 1000 | | | 100 | | | ns | Within PWD limit |
| Data Rate | | | | 1 | | | 10 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 15 | | 150 | 15 | | 55 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | | | | | | $\|t_{PLH} - t_{PHL}\|$ |
| A Grade and B Grade | | | | 40 | | | 3 | ns | |
| WA Grade and WB Grade | | | | 40 | | | 4 | ns | |
| Change vs. Temperature | | | | | | 5 | | ps/°C | |
| Propagation Delay Skew | $t_{PSK}$ | | | 50 | | | 22 | ns | Between any two units |
| Channel Matching | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | ns | |
| Opposing Directional | $t_{PSKOD}$ | | | 50 | | | 22 | ns | |

*Table 11.*

| | | 1 Mbps—A Grade, B Grade | | | 10 Mbps—B Grade | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |
| SUPPLY CURRENT (NO LOAD) | | | | | | | | |
| ADuM2200 | $I_{DD1}$ | | 0.8 | 1.3 | | 2.2 | 3.2 | mA |
| | $I_{DD2}$ | | 1.0 | 1.6 | | 2.0 | 2.8 | mA |
| ADuM2201 | $I_{DD1}$ | | 0.7 | 1.3 | | 1.9 | 2.5 | mA |
| | $I_{DD2}$ | | 1.3 | 1.9 | | 3.1 | 4.0 | mA |

## SPECIFICATIONS

*Table 12.*

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments[1] |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 0.7 $V_{DDx}$ | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.3 $V_{DDx}$ | V | |
| Logic High Output Voltages | $V_{OH}$ | $V_{DDx}$ − 0.1 | $V_{DDx}$ | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.5 | $V_{DDx}$ − 0.2 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI (Q)}$ | | 0.3 | 0.5 | mA | All inputs at logic low |
| Quiescent Output Supply Current | $I_{DDO (Q)}$ | | 0.5 | 0.6 | mA | All inputs at logic low |
| Dynamic Input Supply Current | $I_{DDI (D)}$ | | 0.10 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO (D)}$ | | 0.05 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R/t_F$ | | | | | 10% to 90% |
| A Grade | | | 10 | | ns | |
| B Grade | | | 2.5 | | ns | |
| Common-Mode Transient Immunity[2] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.1 | | Mbps | |

[1] $I_{Ox}$ is the Channel x output current, where x = A or B, $V_{IxH}$ is the input side logic high, and $V_{IxL}$ is the input side logic low.

[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## PACKAGE CHARACTERISTICS

*Table 13.*

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Resistance (Input-to-Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input-to-Output)[1] | $C_{I-O}$ | | 2 | | pF | f = 1 MHz |
| Input Capacitance[2] | $C_I$ | | 4 | | pF | |
| IC Junction-to-Ambient Thermal Resistance | $\theta_{JA}$ | | 45 | | °C/W | |

[1] This device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

[2] Input capacitance is from any input data pin to ground.

## SPECIFICATIONS

### REGULATORY INFORMATION

The ADuM2200/ADuM2201 certification approvals are listed in Table 14. Refer to Table 19 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

*Table 14. ADuM2200/ADuM2201 Regulatory Information Table*

| UL | CSA | CQC | VDE |
|---|---|---|---|
| UL 1577[1]<br>Single Protection, 5000 V rms | RI-16-2 Package<br>IEC/EN/CSA 62368-1<br>Basic insulation, 870 V rms<br>Reinforced insulation, 435 V rms<br>IEC/CSA 60601-1<br>Reinforced insulation (2 MOPP), 250 V rms<br>IEC/CSA 61010-1<br>Basic insulation, 600 V rms, overvoltage category IV<br>Reinforced insulation, 300 V rms, overvoltage category II<br>RW-16 Package<br>IEC/EN/CSA 62368-1<br>Basic insulation, 780 V rms<br>Reinforced insulation, 390 V rms<br>IEC/CSA 60601-1<br>Reinforced insulation (2 MOPP), 125 V rms<br>IEC/CSA 61010-1<br>Basic insulation, 600 V rms, overvoltage category III<br>Reinforced insulation, 300 V rms, overvoltage category II | CQC GB4943.1<br>RI-16-2 Package<br>Basic Insulation, 600 V rms<br>Reinforced insulation, 400 V rms<br>RW-16 package<br>Basic Insulation, 600 V rms<br>Reinforced insulation, 380 V rms | DIN EN IEC 60747-17 (VDE 0884-17)<br>RI-16-2 Package[2]<br>Reinforced insulation, 645 V peak<br>RW-16 Package[3]<br>Reinforced insulation, 645 V peak |
| File E214100 | Certificate No. 205078 | Certificate No. CQC14001105917 | Certificate No. 40011599 |

[1] In accordance with UL 1577, each ADuM2200/ADuM2201 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 10 μA).

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM2200/ADuM2201 RI-16-2 is proof tested by applying an insulation test voltage ≥1209 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the components designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

[3] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM2200/ADuM2201 RW-16 is proof tested by applying an insulation test voltage ≥1209 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the components designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

## SPECIFICATIONS

### INSULATION AND SAFETY-RELATED SPECIFICATIONS

*Table 15.*

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 5000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance)[1, 2] | L(I01) | | | Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout |
| RW-16 Package | | 7.8 | mm | |
| RI-16-2 Package | | 8.7 | mm | |
| Minimum External Tracking (Creepage)[1] | L(I02) | | | Measured from input terminals to output terminals, shortest distance path along body |
| RW-16 Package | | 7.8 | mm | |
| RI-16-2 Package | | 8.7 | mm | |
| Minimum Internal Distance (Internal Clearance) | | 18 | um | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index)[3] | CTI | >400 | V | DIN IEC 112/VDE 0303, Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

[1] In accordance with IEC 62368-1 / IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

[3] CTI rating for the ADuM2200/ADuM2201 RI-16-2/ADuM2200/ADuM2201 RW_16 is >400 V and a Material Group II isolation group.

### DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. The asterisk (*) marking branded on the components designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

*Table 16. ADuM2200/ADuM2201 VDE Insulation Characteristics*

| Description | Test Conditions/Comments | Symbol | Characteristic | Unit |
|---|---|---|---|---|
| Overvoltage Category per IEC 60664-1 | | | | |
| ≤ 150 V rms | | | I to IV | |
| ≤ 300 V rms | | | I to IV | |
| ≤ 400 V rms | | | I to IV | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Repetitive Isolation Voltage | | $V_{IORM}$ | 645 | V peak |
| Maximum Working Insulation Voltage | | $V_{IOWM}$ | 456 | V rms |
| Input-to-Output Test Voltage, Method B1 | $V_{IORM}$ × 1.875 = $V_{pd(m)}$, 100% production test, $t_{ini}$ = $t_m$ = 1 sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1209 | V peak |
| Input-to-Output Test Voltage, Method A | | | | |
| After Environmental Tests Subgroup 1 | $V_{IORM}$ × 1.6 = $V_{pd(m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1032 | V peak |
| After Input and/or Safety Tests Subgroup 2 and Subgroup 3 | $V_{IORM}$ × 1.2 = $V_{pd(m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | $V_{pd(m)}$ | 774 | V peak |
| Maximum Transient Isolation Voltage | $V_{TEST}$ = 1.2 × $V_{IOTM}$, t =1s (100% production) | $V_{IOTM}$ | 6000 | V peak |
| Maximum Impulse Voltage | Surge voltage in air, waveform per IEC 61000-4-5 | $V_{IMP}$ | 6000 | V peak |
| Maximum Surge Isolation Voltage | $V_{TEST}$ ≥ 1.3 × $V_{IMP}$ (sample test), tested in oil, waveform per IEC 61000-4-5 | $V_{IOSM}$ | 10000 | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure; see Figure 3 | | | |
| Maximum Junction Temperature | | $T_S$ | 150 | °C |
| Total Power Dissipation at 25°C | | $P_S$ | 2.78 | W |
| Insulation Resistance at $T_S$ | $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

## SPECIFICATIONS

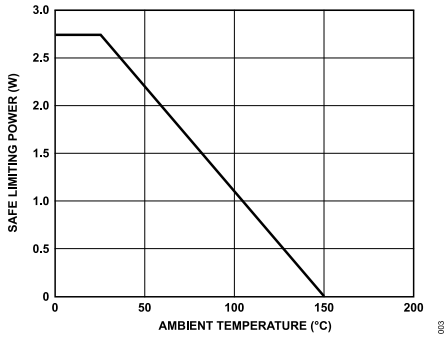


*Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)*

## RECOMMENDED OPERATING CONDITIONS

*Table 17.*

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | | | |
| A Grade and B Grade | | −40 | +105 | °C |
| WA Grade and WB Grade | | −40 | +125 | °C |
| Supply Voltages[1] | $V_{DD1}$, $V_{DD2}$ | 3.0 | 5.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

[1] All voltages are relative to their respective grounds.

## ABSOLUTE MAXIMUM RATINGS

*Table 18.*

| Parameter | Rating |
|---|---|
| Storage Temperature ($T_{ST}$) | −65°C to +150°C |
| Ambient Operating Temperature ($T_A$) | −40°C to +125°C |
| Supply Voltage ($V_{DD1}$, $V_{DD2}$)[1] | −0.5 V to +7.0 V |
| Input Voltage ($V_{IA}$, $V_{IB}$)[1, 2] | −0.5 V to $V_{DDI}$ + 0.5 V |
| Output Voltage ($V_{OA}$, $V_{OB}$)[1, 2] | −0.5 V to $V_{DDO}$ + 0.5 V |
| Average Output Current per Pin[3] | |
| Side 1 ($I_{O1}$) | −18 mA to +18 mA |
| Side 2 ($I_{O2}$) | −22 mA to +22 mA |
| Common-Mode Transients[4] | −100 kV/µs to +100 kV/µs |

1 All voltages are relative to their respective grounds.

2 $V_{DDI}$ and $V_{DDO}$ refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.

3 See Figure 3 for maximum rated current values for various temperatures.

4 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## MAXIMUM CONTINUOUS WORKING VOLTAGE

*Table 19. Maximum Continuous Working Voltage*

| Parameter | Max | Unit | Applicable Certification |
|---|---|---|---|
| AC Voltage | | | |
| Bipolar Waveform | 645 | V peak | Reinforced insulation rating per IEC 60747-17 ( VDE 0884-17)[1] |

1 Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

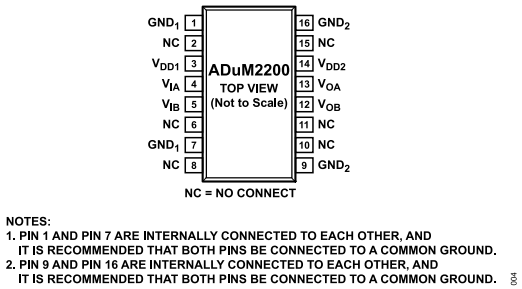


*Figure 4. ADuM2200 Pin Configuration*

*Table 20. ADuM2200 Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 7 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 1 and Pin 7 are internally connected to each other, and it is recommended that both pins be connected to a common ground. |
| 2 | NC | No Internal Connection. |
| 3 | $V_{DD1}$ | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 4 | $V_{IA}$ | Logic Input A. |
| 5 | $V_{IB}$ | Logic Input B. |
| 6 | NC | No Internal Connection. |
| 8 | NC | No Internal Connection. |
| 9, 16 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 16 are internally connected to each other, and it is recommended that both pins be connected to a common ground. |
| 10 | NC | No Internal Connection. |
| 11 | NC | No Internal Connection. |
| 12 | $V_{OB}$ | Logic Output B. |
| 13 | $V_{OA}$ | Logic Output A. |
| 14 | $V_{DD2}$ | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |
| 15 | NC | No Internal Connection. |

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

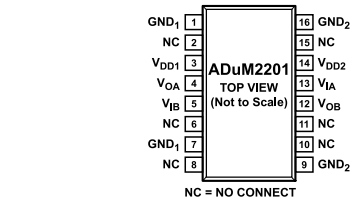


*Figure 5. ADuM2201 Pin Configuration*

*Table 21. ADuM2201 Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 7 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 1 and Pin 7 are internally connected to each other, and it is recommended that both pins be connected to a common ground. |
| 2 | NC | No Internal Connection. |
| 3 | $V_{DD1}$ | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 4 | $V_{OA}$ | Logic Output A. |
| 5 | $V_{IB}$ | Logic Input B. |
| 6 | NC | No Internal Connection. |
| 8 | NC | No Internal Connection. |
| 9, 16 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 16 are internally connected to each other, and it is recommended that both pins be connected to a common ground. |
| 10 | NC | No Internal Connection. |
| 11 | NC | No Internal Connection. |
| 12 | $V_{OB}$ | Logic Output B. |
| 13 | $V_{IA}$ | Logic Input A. |
| 14 | $V_{DD2}$ | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |
| 15 | NC | No Internal Connection. |

## TYPICAL PERFORMANCE CHARACTERISTICS

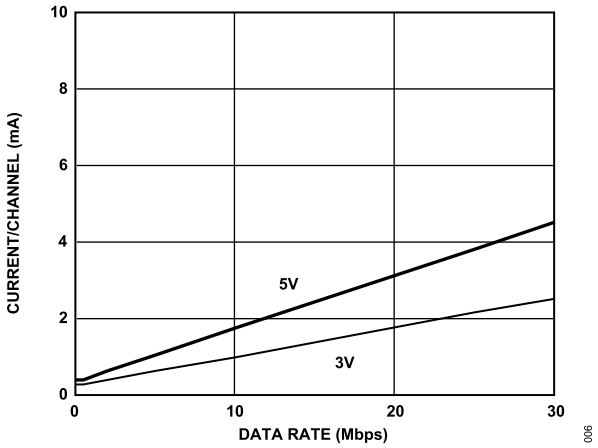


*Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)*

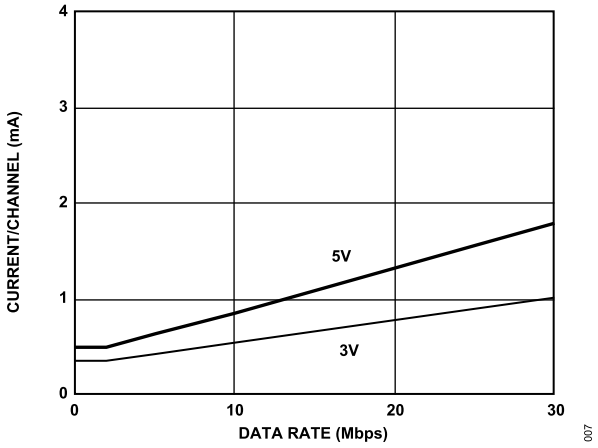


*Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)*

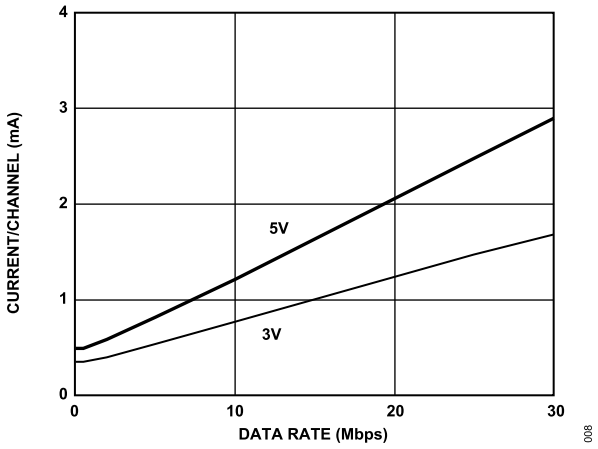


*Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)*

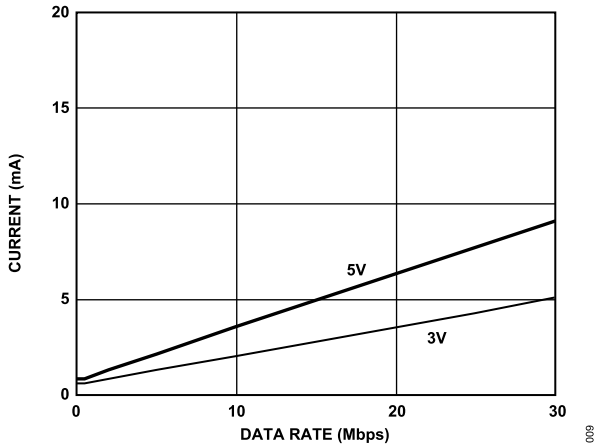


*Figure 9. Typical ADuM2200 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

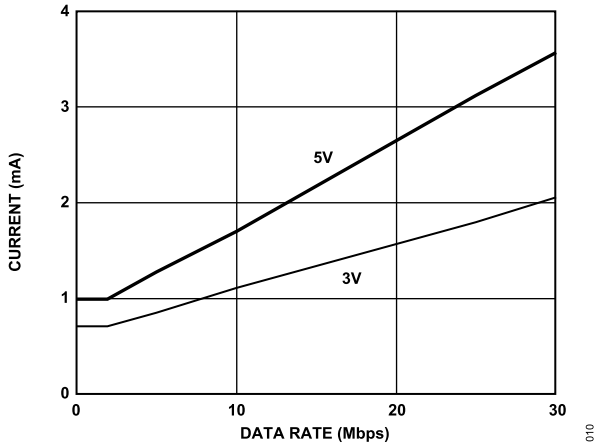


*Figure 10. Typical ADuM2200 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

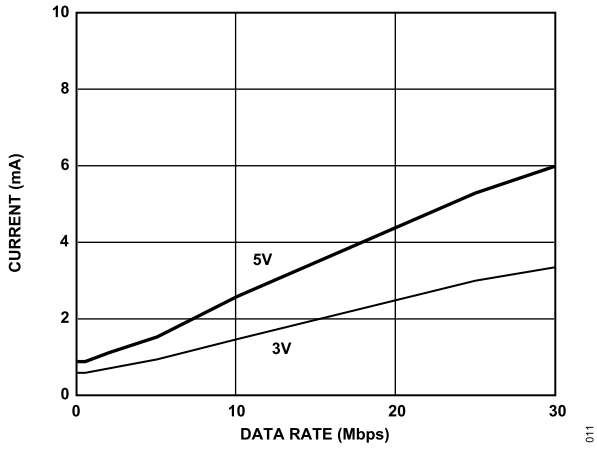


*Figure 11. Typical ADuM2201 $V_{DD1}$ or $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

## APPLICATIONS INFORMATION

### PCB LAYOUT

The ADuM2200/ADuM2201 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 12). Bypass capacitors are most conveniently connected between Pin 1 and Pin 3 for $V_{DD1}$ and between Pin 14 and Pin 16 for $V_{DD2}$. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 2 mm. Consider bypassing between Pin 3 and Pin 7 and between Pin 9 and Pin 14 unless the ground pair on each package side is connected close to the package.

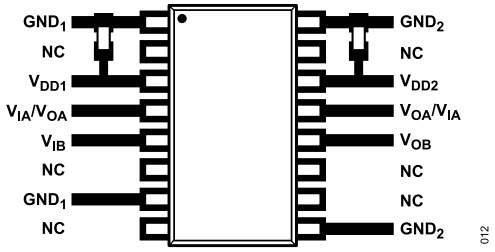


*Figure 12. Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur affects all pins equally on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings for the device as specified in Table 18, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

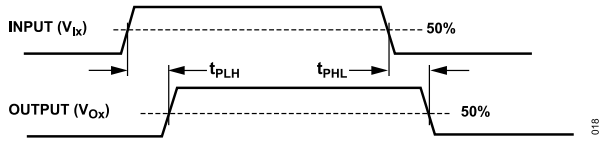


*Figure 13. Propagation Delay Parameters*

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM2200/ADuM2201 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM2200/ADuM2201 components operated under the same conditions.

### DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, and the isolator output is forced to a default state by the watchdog timer circuit (see Table 21 and #unique_5/unique_5_Connect_42_ID3703).

The limitation on the magnetic field immunity of the ADuM2200/ADuM2201 is set by the condition in which induced voltage in the transformer receiving coil is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM2200/ADuM2201 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \ldots, N \quad (1)$$

where:
$\beta$ is the magnetic flux density (gauss).
$r_n$ is the radius of the $n^{th}$ turn in the receiving coil (cm).
$N$ is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM2200/ADuM2201 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 14.

## APPLICATIONS INFORMATION

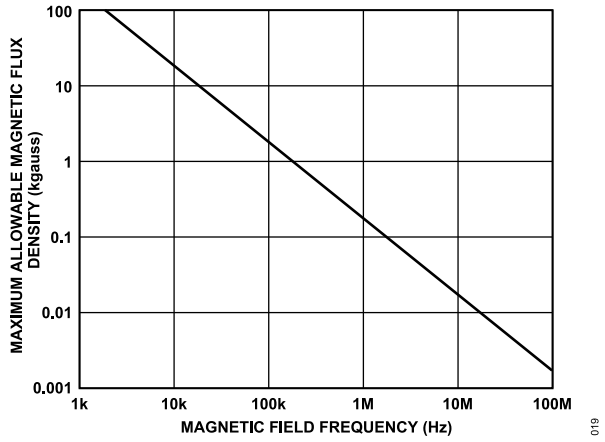


*Figure 14. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM2200/ADuM2201 transformers. Figure 15 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 15, the ADuM2200/ADuM2201 are immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current placed 5 mm away from the ADuM2200/ADuM2201 is required to affect the operation of the component.

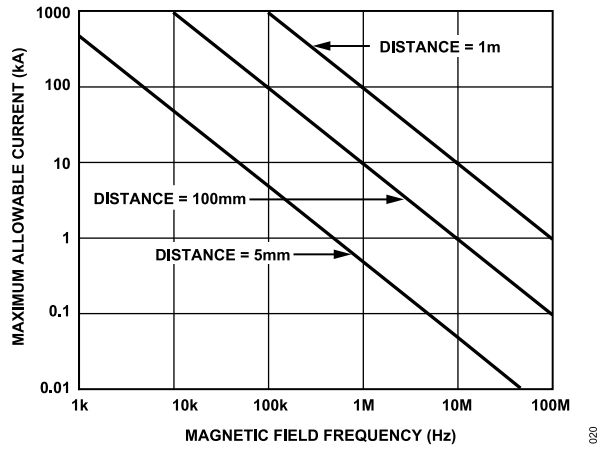


*Figure 15. Maximum Allowable Current for Various Current-to-ADuM2200/ADuM2201 Spacings*

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

### POWER CONSUMPTION

The supply current at a given channel of the ADuM2200/ADuM2201 isolators is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \quad f \leq 0.5f_r \tag{2}$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \quad f > 0.5f_r \tag{3}$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \quad f \leq 0.5f_r \tag{4}$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \quad f > 0.5f_r \tag{5}$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).
$C_L$ is the output load capacitance (pF).
$V_{DDO}$ is the output supply voltage (V).
$f$ is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
$f_r$ is the input stage refresh rate (Mbps).

To calculate the total $I_{DD1}$ and $I_{DD2}$, the supply currents for each input and output channel corresponding to $I_{DD1}$ and $I_{DD2}$ are calculated and totaled.

Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 provide total $I_{DD1}$ and $I_{DD2}$ as a function of data rate for the ADuM2200/ADuM2201 channel configurations.

## APPLICATIONS INFORMATION

### INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM2200/ADuM2201 devices.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 19 summarize the maximum continuous working voltages as per IEC 60747-17. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

## OUTLINE DIMENSIONS

| Package Drawing (Option) | Package Type | Package Description |
|---|---|---|
| RW-16 | SOIC_W | 16-Lead Standard Small Outline Package |
| RI-16-2 | SOIC_IC | 16-Lead Standard Small Outline Package, with Increased Creepage |

For the latest package outline information and land patterns (footprints), go to Package Index.

## ORDERING GUIDE

| Model[1, 2, 3] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADuM2200ARIZ | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM2200ARWZ | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM2200WARWZ | −40°C to +125°C | 16-Lead SOIC_W | RW-16 |
| ADuM2200BRIZ | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM2200BRWZ | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM2200WBRWZ | −40°C to +125°C | 16-Lead SOIC_W | RW-16 |
| ADuM2201ARIZ | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM2201ARWZ | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM2201WARWZ | −40°C to +125°C | 16-Lead SOIC_W | RW-16 |
| ADuM2201BRIZ | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM2201BRWZ | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM2201WBRWZ | −40°C to +125°C | 16-Lead SOIC_W | RW-16 |

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

[3] Tape and reel is available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.

## NUMBER OF INPUTS, MAXIMUM DATA RATE, MAXIMUM PROPAGATION, AND MAXIMUM PULSE WIDTH DISTORTION OPTIONS

| Model[1, 2, 3] | Number of Inputs, $V_{DD1}$ Side | Number of Inputs, $V_{DD2}$ Side | Maximum Data Rate (Mbps) | Maximum Propagation Delay, 5 V (ns) | Maximum Pulse Width Distortion (ns) |
|---|---|---|---|---|---|
| ADuM2200ARIZ | 2 | 0 | 1 | 150 | 40 |
| ADuM2200ARWZ | 2 | 0 | 1 | 150 | 40 |
| ADuM2200WARWZ | 2 | 0 | 1 | 150 | 40 |
| ADuM2200BRIZ | 2 | 0 | 10 | 50 | 3 |
| ADuM2200BRWZ | 2 | 0 | 10 | 50 | 3 |
| ADuM2200WBRWZ | 2 | 0 | 10 | 50 | 3 |
| ADuM2201ARIZ | 1 | 1 | 1 | 150 | 40 |
| ADuM2201ARWZ | 1 | 1 | 1 | 150 | 40 |
| ADuM2201WARWZ | 1 | 1 | 1 | 150 | 40 |
| ADuM2201BRIZ | 1 | 1 | 10 | 50 | 3 |
| ADuM2201BRWZ | 1 | 1 | 10 | 50 | 3 |
| ADuM2201WBRWZ | 1 | 1 | 10 | 50 | 3 |

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

[3] Tape and reel is available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.

## OUTLINE DIMENSIONS

### AUTOMOTIVE PRODUCTS

The ADuM2200W and ADuM2201W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.