Narrow-Band and Wideband RF Transceiver with Integrated Application Processor

FEATURES

- Integrated 1 Tx × 2 Rx RF transceiver
- Operating frequency range of 70 MHz to 6000 MHz
- Transmitter and wideband receiver signal bandwidth from 12 kHz to 40 MHz
- Narrowband receiver signal bandwidth from 12 kHz to 2 MHz
- 2 fully integrated, fractional-N, RF synthesizers
- 2 fully integrated, fractional-N, RF PLLs to control external VCO banks
- Supports external LO
- LVDS and CMOS synchronous serial data interface options
- Low power monitor and sleep modes
- Fully integrated DPD for TDD narrowband waveforms
- User-programmable ARM core with 928 kB memory
- Interfaces include 2× UART, 2× I^2S, I^2C, QSPI, SPI-M, JTAG
- Library of hardware accelerators
- Fully programmable via a 4-wire SPI
- Package: 196-ball, 10 mm × 10 mm, CSP_BGA

APPLICATIONS

- Land Mobile Radios
- Mobile Satellite and Satellite IoT
- Wireless microphones
- Mission critical communications systems
- Smart Meters
- Factory Automation

GENERAL DESCRIPTION

The ADRV9104 is a highly integrated RF transceiver with an integrated application processor that has a single transmitter, dual receivers, integrated synthesizers, and digital signal processing functions. Its a high performance, highly linear, high dynamic range transceiver designed for the lowest power consumption to support portable, and battery powered equipment. The ADRV9104 operates from 70 MHz to 6000 MHz and covers the VHF (from 70MHz),UHF, industrial, scientific, and medical (ISM) bands, and cellular frequency bands in narrow-band (kHz) and wideband operation up to 40 MHz. The ADRV9104 is capable of both TDD and uncalibrated FDD operation.

The transceiver has three direct conversion signal paths (1Tx and 2Rx) with state-of-the-art noise figure and linearity. The dedicated Narrow Band Receiver path can support up to 2MHz of RF signal BW. The dedicated wide band Receiver path can support up to 40MHz of RF signal BW. Each receiver and transmitter subsystem includes quadrature error correction (QEC), programmable digital filters, DC offset correction on the Rx paths and LO leakage suppression on the Tx path. In addition, functions such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs), are integrated to provide additional monitoring and control capability.

The transmitter has internal modulator functions that can support for typical Land Mobile Radio (LMR) standards, such as Analog FM, Digital Mobile Radio (DMR), P25. The modulator integrates the symbol mapping, interpolation and pulse shaping functions which allow the basedband processor to send 2bit symbols to ADRV9014.

The fully integrated phase-locked loops (PLLs) provide high performance, low power, fractional-N frequency synthesis for the transmitter, receiver, and clock sections. Careful design and layout techniques provide the isolation required in high performance personal radio applications.

All voltage-controlled oscillator (VCO) and loop filter components are integrated to minimize the external component count. The internal PLLs provide local oscillators (LOs) and have flexible configuration options and include fast lock modes. The fully integrated PLLs also have the option of operating with one or more external VCOs to provide ultra low noise LOs for the transmitter and receivers.

The transceiver includes low power sleep and monitor modes to save power and extend the battery life of portable devices while monitoring communications, it has the capability to monitor the DMR and Analog FM signal simultaneously with the narrow-band receiver channel when monitor mode is enabled. For some modes, ADRV9104 can operate form DEV_CLK only with the internal Clock PLL powered down.

The fully integrated, low power digital predistortion (DPD) is optimized for narrow-band TDD signals and enables linearization of high efficiency power amplifiers.

The ADRV9104 hosts a second processor, Processor Subsystem 2 (PS2), for users application specific programming. The ARM M4 has 928kB of useable memory, hardware accelerators, peripheral interfaces and runs up to 200MHz. This application processor can be used to implement modem like features on the transceiver customized to individual use cases.

The ADRV9104 core can be powered directly from 1.0 V and 1.8 V regulators and is controlled via a standard 4-wire serial port. High data rate and low data rate interfaces are supported using configurable CMOS or low voltage differential signaling (LVDS) serial synchronous interface (SSI) choice. The ADRV9104 is packaged in a 10 mm × 10 mm, 0.65 pitch 196-ball chip scale package ball grid array (CSP_BGA).

Rev. PrC

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FUNCTIONAL BLOCK DIAGRAM

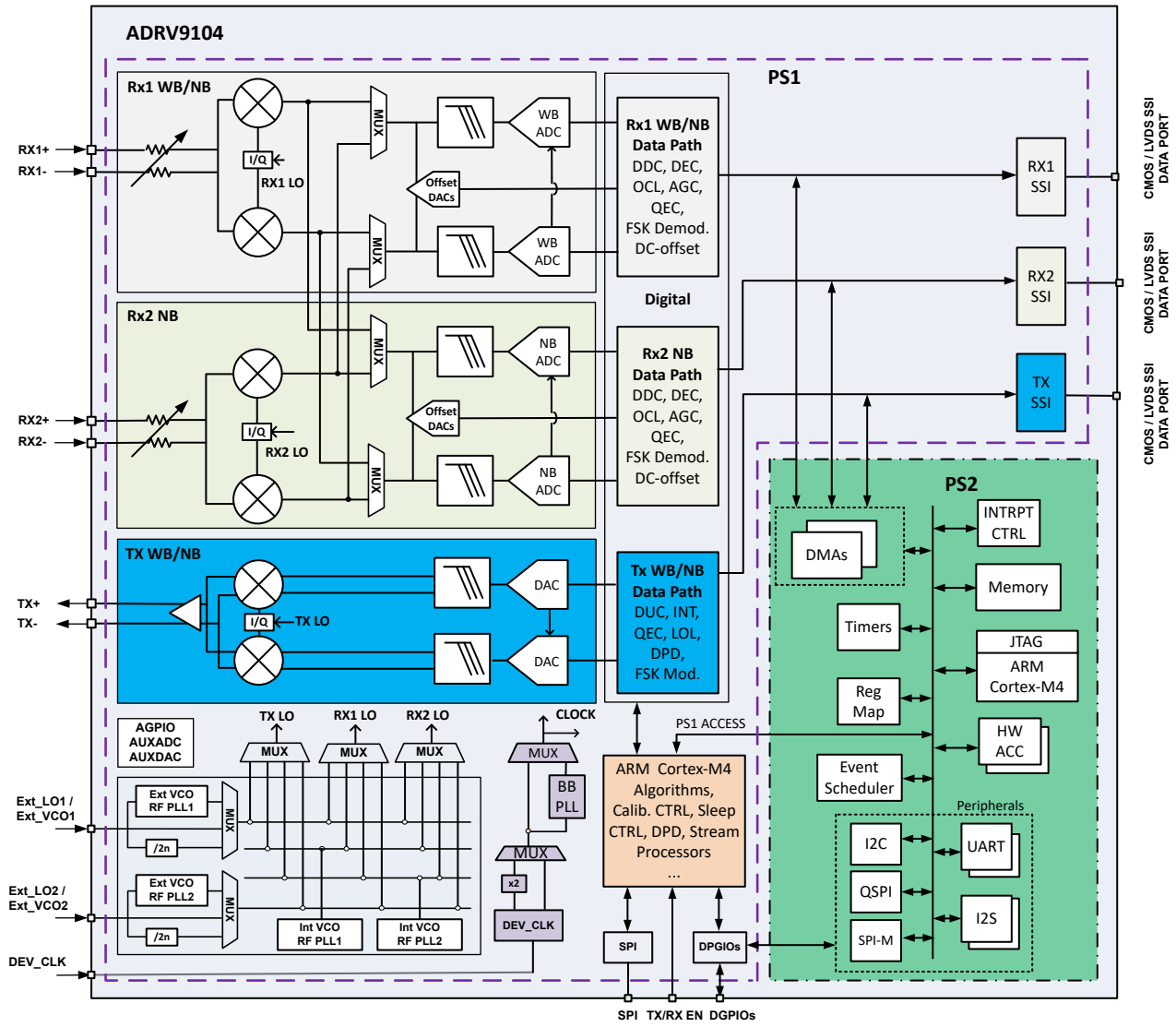


Figure 1. Functional Block Diagram

SPECIFICATIONS

Electrical characteristics are at the operating ambient temperature range, VDDA_1P0 = 1.0 V, VDDA_1P8 = 1.8 V, VDD_1P0 = 1.0 V, VDD_1P8 = 1.8 V. The following values are not de-embedded. The specification tables below are populated with preliminary measurement results, taken at 25°C averaged across multiple parts, and are subject to change as characterization on the device continues and more qualified data is obtained.

TRANSMITTER SPECIFICATIONS

All values in the transmitter specification table have been measured while the part was in NB mode only.

Table 1. Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CENTER FREQUENCY		70		6000	MHz	
BANDWIDTH FLATNESS			0.1		dB	
DEVIATION FROM LINEAR PHASE			1		Degree	
POWER CONTROL RANGE						
IQ Mode			42		dB	LO of 900MHz
Direct Modulation Mode			12		dB	LO of 900MHz. Only through internal PLL
POWER CONTROL RESOLUTION						
IQ Mode			0.05		dB	
IN BAND NOISE FLOOR						
100kHz			−135		dBm/Hz	0dB Attenuation
1MHz			−138		dBm/Hz	0dB Attenuation
OUT OF BAND NOISE FLOOR						
10MHz			−146		dBm/Hz	0dB Attenuation
100MHz			−148		dBm/Hz	0dB Attenuation
IMAGE REJECTION WITH INITIALIZATION CALIBRATION						Internal LO, 0 dB transmitter Attenuation, −6dBFs, 4.1Khz offset continuous wave Signal output
Narrow-Band						
70 MHz			76		dBc	
136 MHz			84		dBc	
380 MHz			87		dBc	
520 MHz			83		dBc	
941 MHz			74		dBc	
CONTINUOUS WAVE FULL-SCALE OUTPUT POWER						Full scale CW output and 0 dB transmitter attenuation. Backoff of 0.2dB
70MHz			7.9		dBm	
136MHz			8.3		dBm	
380MHz			8.3		dBm	
520MHz			8.3		dBm	
941MHz			8.2		dBm	
OUTPUT IMPEDANCE	ZOUT		50		Ω	Differential
MAXIMUM OUTPUT LOAD VOLTAGE STANDING WAVE RATIO (VSWR)			TBD		Ω	Use the maximum value to ensure adequate calibration.
OUTPUT RETURN LOSS						Unmatched differential port return loss. From simulation, no trace or balun included.
70 MHz			29		dB	
136 MHz			29		dB	
380 MHz			26		dB	
520 MHz			24		dB	
941 MHz			20		dB	

SPECIFICATIONS

Table 1. Transmitter (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT THIRD-ORDER INTERCEPT POINT	OIP3					Internal LO, 0 dB transmitter attenuation. Continuous wave tones at 4.1 kHz and 5.1 kHz, −7 dBFS/tone.
70MHz			30.8		dBm	
136MHz			31.8		dBm	
380MHz			32.5		dBm	
520 MHz			32.3		dBm	
941MHz			33.9		dBm	
CARRIER LEAKAGE WITH INITIALIZATION CALIBRATION						Internal LO, 0 dB transmitter Attenuation, −6dBFs, 4.1Khz offset continuous wave Signal output
Narrow-Band						
70 MHz			−74.9		dBm	
136 MHz			−71.7		dBm	
380 MHz			−71.7		dBm	
520 MHz			−74.1		dBm	
941 MHz			−68.2		dBm	

RECEIVER SPECIFICATIONS

Table 2. Receiver (Rx2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CENTER FREQUENCY		70		6000	MHz	
MAXIMUM GAIN						
70 MHz			22.2		dB	
136 MHz			22.3		dB	
380 MHz			22.6		dB	
520 MHz			22.3		dB	
941 MHz			22.6		dB	
ATTENUATION RANGE FROM MAXIMUM GAIN			34		dB	
Attenuation Accuracy						
Gain Step			0.5		dB	Attenuator steps from 0 dB to 30 dB.
			1		dB	Attenuator steps from 30 dB to 34 dB.
Gain Step Error			0.1		dB	Attenuator steps from 0 dB to 30 dB.
			TBD			Attenuator steps from 30 dB to 34 dB.
FREQUENCY RESPONSE						
Peak-to-Peak Gain Deviation			1		dB	
RECEIVER BANDWIDTH		12		2000	kHz	
RECEIVER ALIAS BAND REJECTION		80			dB	This performance is achieved because of the digital filters
CONTINUOUS WAVE FULL-SCALE INPUT POWER	FSIP					This continuous wave signal level corresponds to the input power at maximum gain that produces 0 dBFS at the ADC output, this level increases dB for dB with attenuation, backoff by at least −1 dBFS is required
70 MHz			−11.8		dBm	
136 MHz			−12.5		dBm	
380 MHz			−12.2		dBm	
520.MHz			−12.5		dBm	
941 MHz			−12.3		dBm	
INPUT IMPEDANCE			100		Ω	Differential
INPUT PORT RETURN LOSS						Values from simulation, without board trace or balun
70 MHz			29		dB	

SPECIFICATIONS

Table 2. Receiver (Rx2) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
136 MHz			28		dB	
380 MHz			26		dB	
520 MHz			26		dB	
941 MHz			26		dB	
NOISE FIGURE	NF					Measured at max gain vs LO
70 MHz			14		dB	
136 MHz			13		dB	
380 MHz			13		dB	
520 MHz			13		dB	
941 MHz			12		dB	
SECOND-ORDER INPUT INTERMODULATION INTERCEPT POINT						Max Receiver Gain, One tone at 50Khz carrier frequency offset, second tone at 492Khz carrier frequency offset, tone output power is −9dBFs/tone
Rx2 Narrow-Band	IIP2LB					
70 MHz			97.0		dBm	
136 MHz			97.3		dBm	
380 MHz			88.6		dBm	
520 MHz			85.5		dBm	
941 MHz			80.8		dBm	
THIRD-ORDER INPUT INTERMODULATION INTERCEPT POINT, DIFFERENCE PRODUCT						Max Receiver Gain, Two tone at 50Khz/100Khz carrier frequency offset respectively, tone output power is −9 dBFs/tone
Rx2 Narrow-Band	LB − IIP3DIFF					
70 MHz			28.9		dBm	
136 MHz			26.8		dBm	
380 MHz			25.6		dBm	
520 MHz			24.4		dBm	
941 MHz			23.1		dBm	
THIRD-ORDER HARMONIC DISTORTION						Max Receiver Gain, Input continuous wave signal at Carrier frequency + 294KHz (2/3 IF), tone output power is −1dBFS
Rx2 Narrow-Band	HD3LB					
70 MHz			122.7		dBc	
136 MHz			126.3		dBc	
380 MHz			109.8		dBc	
520 MHz			108.7		dBc	
941 MHz			105.4		dBc	
SECOND-ORDER HARMONIC DISTORTION						Max Receiver Gain, Input continuous wave signal at Carrier frequency + 221KHz (1/2 IF), tone output power is −1dBFS
Rx2 Narrow-Band	HD2LB					
70 MHz			103.5		dBc	
136 MHz			102.5		dBc	
380 MHz			96.9		dBc	
520 MHz			94.9		dBc	
941 MHz			95.4		dBc	
IMAGE REJECTION						Ext LO. Gain sweep from index 255 to 195. Tone is input at 3k, amplitude adjusted to measure −10dB on data capture.
Narrow-Band						
70 MHz			105		dBc	
136 MHz			103		dBc	

SPECIFICATIONS

Table 2. Receiver (Rx2) (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
380 MHz			103		dBc	
520 MHz			101		dBc	
941 MHz			103		dBc	
RECEIVER INPUT LO LEAKAGE AT MAXIMUM GAIN						
70 MHz			TBD		dBm	
136 MHz			TBD		dBm	
380 MHz			TBD		dBm	
520 MHz			TBD		dBm	
941 MHz			TBD		dbm	
SIGNAL ISOLATION						
Tx to Rx2 Isolation						
70 MHz			TBD		dB	
136 MHz			TBD		dB	
380 MHz			TBD		dB	
520 MHz			TBD		dB	
941 MHz			TBD		dB	

INTERNAL LO, EXTERNAL LO, AND DEVICE CLOCK

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOCAL OSCILLATOR						
LO Frequency Step				2.2	Hz	For 38.4 MHz DEV_CLK, use the equation DEV_CLK/((223 − 15) × 2) to calculate, assuming the LO divider is 2
LO Reference Spurs			−80		dBc	LO < 1 GHz, PLL bandwidth = 300 kHz
LOCAL OSCILLATOR WITH HIGH PERFORMANCE MODE						
Integrated Phase Noise						
136 MHz LO			TBD		°rms	
520 MHz LO			TBD		°rms	
941 MHz LO			TBD		°rms	
Phase Noise						
136 MHz LO			TBD			
520 MHz LO			TBD			
941 MHz LO			TBD			
LO PHASE SYNCHRONIZATION						
Initial Phase Synchronization Accuracy			TBD		ps	
EXTERNAL LO INPUT						
Input Frequency						
2x VCO/LO Input		140		12000	MHz	
1x VCO/LO Input		250		1000	MHz	
Input Signal Power		−6	0		dBm	100 Ω matching at the device differential input. Divider set to 4 by default.
Input Signal Differential Phase Balance				20	Degrees	Do not exceed 20 degrees to ensure adequate quadrature error correction.
Input Signal Differential Amplitude Balance				1	dB	

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Signal Duty Cycle Error				2.5	%	
Input Impedance			100		Ω	Differential
REFERENCE CLOCK (DEV_CLK_IN SIGNAL)						
Differential mode						
Frequency Range		10		307.2	MHz	
Signal Level		0.2		0.4	V p-p	AC-coupled, for optimal spurious performance and to meet the specified PLL performance parameters, use a 400 mV p-p (800 mV p-p differential) input clock
Single-Ended Mode						
Frequency Range		10		80	MHz	
Signal Level		0.2		1	V p-p	AC-coupled, for optimal spurious performance and to meet the specified PLL performance parameters, use a 1V p-p input clock.
REFERENCE CLOCK (XTAL)						
Frequency Range		20		80	MHz	
CLOCK OUTPUT (DEV_CLK_OUT SIGNAL)						
Frequency Range		10		80	MHz	

EXTERNAL VCO CHARGE PUMP

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHARGE PUMP(CP)						
CP Current Sink and Source						
High Value			6.4		mA	
Low Value			0.1		mA	
Absolute Accuracy			TBD		%	
ICP Three-State Leakage			TBD		nA	
Sink and Source Current Matching			TBD		%	
ICP vs. VCP			TBD		%	
ICP vs. Temperature			TBD		%	

DIGITAL INTERFACES AND AUXILIARY CONVERTERS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AUXILIARY ADC CONVERTERS					
Resolution		10		Bits	
Input Voltage					
Minimum		0.05		V	
Maximum		0.95		V	
AUXILIARY DAC CONVERTERS					
Resolution		12		Bits	
Output Voltage					
Minimum		0.05		V	
Maximum		VDDA_1P8 − 0.05		V	
Drive Capability		10		mA	

SPECIFICATIONS

Table 4. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL SPECIFICATIONS (CMOS-SSI SIGNALS)					
Logic Inputs					
Input Voltage					
High Level	VDIG_1P8 × 0.65		VDIG_1P8 + 0.18	V	
Low Level	−0.30		VDIG_1P8 × 0.35	V	
Logic Outputs Voltage					
Output Voltage					
High Level	VDIG_1P8 − 0.45			V	
Low Level			0.45	V	
Drive Capability		10		mA	
DIGITAL SPECIFICATIONS (DIGITAL GPIO SIGNALS)					
Logic Inputs					
Input Voltage					
High Level	VDIG_1P8 × 0.65		VDIG_1P8 + 0.18	V	
Low Level	−0.30		VDIG_1P8 × 0.35	V	
Logic Outputs					
Output Voltage					
High Level	VDIG_1P8 − 0.45			V	
Low Level			0.45	V	
Drive Capability		10		mA	
DATAPORT SPECIFICATIONS (LVDS SSI, MCS+/MCS−)					
Logic Inputs					
Input Voltage Range	825		1675	mV	
Input Differential Voltage Threshold	−100		+100	mV	
Receiver Differential Input Impedance		100		Ω	
Logic Outputs					
Output Voltage					
High			1390	mV	
Low	1000			mV	
Differential		300		mV	
Offset		1200		mV	
Output Current			4.1	mA	
Clock Signal Duty Cycle	45	50	55	%	
Output Rise/Fall Time		0.371		ns	
DIGITAL SPECIFICATIONS (ANALOG GPIO SIGNALS)					
Logic Inputs					
Input Voltage					
High Level	VDDA_1P8 × 0.65		VDDA_1P8 + 0.18	V	
Low Level	−0.30		VDDA_1P8 × 0.35	V	
Logic Outputs					
Output Voltage					
High Level	VDDA_1P8 − 0.45			V	
Low Level			0.45	V	

SPECIFICATIONS

Table 4. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Drive Capability		10		mA	

POWER SUPPLY SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS				
VDDA_1P0[1] Analog Supplies		1.0		V
VDD_1P0[2] Digital Supply		1.0		V
VDDA_1P8[3] Analog Supplies		1.8		V
VDD_1P8[4] Digital Supply		1.8		V

[1] VDDA_1P0 refers to all analog 1.0 V supplies, including VANA1_1P0,VANA2_1P0 , VRFSYN1_1P0, VRFSYN2_1P0, VCLKSYN_1P0, VRFLO1_1P0, VRFLO2_1P0, VCONV1_1P0, VCONV2_1P0, VAGPIO_1P0, VRX1LO_1P0, VRX2LO_1P0, VCLKVCO_1P0, VTXLO_1P0, VDEVCLK_1P0, VEXTLO1_1P0, VEXTLO2_1P0.

[2] VDD_1P0 refers to all digital 1.0 V supplies including VDIG_1P0.

[3] VDD_1P8 refers to all analog 1.8 V supplies including VAGPIO_1P8, VCONV1_1P8, VCONV2_1P8, VANA1_1P8, VANA2_1P8, VRFVCO1_1P8, VRFVCO2_1P8.

[4] VDD_1P8 refers to all digital 1.8 V supplies including VDIG_1P8.

POWER CONSUMPTION ESTIMATES (TYPICAL VALUES)

The values in Table 6 are based on the following configuration: DEV_CLK: 38.4Mhz, Input Sample Rate: 24KSPS, DAC Sample Rate: 38.4Mhz, 4X EXT LO Mode with Tx channel power on only.

Table 6. Tx Power Consumption

	Supply (mA)				
Conditions	VDDA_1P0 Analog Supplies	VDD_1P0 Digital Supply	VDDA_1P8 Analog Supplies	VDD_1P8 Digital Supply	Total Average Power (mW)
Tx Attenuation: 0 dB RF PLL is Enabled for EXT VCO	170	22	141	1.9	450
Tx Attenuation: 10 dB RF PLL is Enabled for EXT VCO	170	22	67.2	1.9	316

The values in Table 7 are based on the following configuration: DEV_CLK: 38.4Mhz, with Tx channel power on only.

Table 7. Tx Power Consumption with Internal LO

	Supply (mA)				
Conditions	VDDA_1P0 Analog Supplies	VDD_1P0 Digital Supply	VDDA_1P8 Analog Supplies	VDD_1P8 Digital Supply	Total Average Power (mW)
Tx Attenuation: 0 dB Input Sample Rate: 2.4MSPS, DAC Sample Rate: 38.4Mhz, Internal LO Mode at 450MHz	204.6	24.7	193.5	5.4	588
Tx Attenuation: 10 dB Input Sample Rate: 2.4MSPS, DAC Sample Rate: 38.4Mhz, Internal LO Mode at 450MHz	204.2	24.6	114.3	5.2	444
Tx Attenuation: 0 dB Input Sample Rate: 30.72MSPS, DAC Sample Rate: 552.96Mhz, Internal LO Mode at 450MHz	302.8	215.5	231.9	34.1	997
Tx Attenuation: 10 dB Input Sample Rate: 30.72MSPS, DAC Sample Rate: 552.96Mhz, Internal LO Mode at 450MHz	302.8	215.7	155.9	33.6	859.6

SPECIFICATIONS

The values in Table 8 are based on the following configuration: DEV_CLK: 38.4Mhz, ADC Sample Rate: 38.4Mhz, Output Sample Rate: 24Khz, 4X EXT LO Mod, with Rx channel power on only.

Table 8. Rx Power Consumption

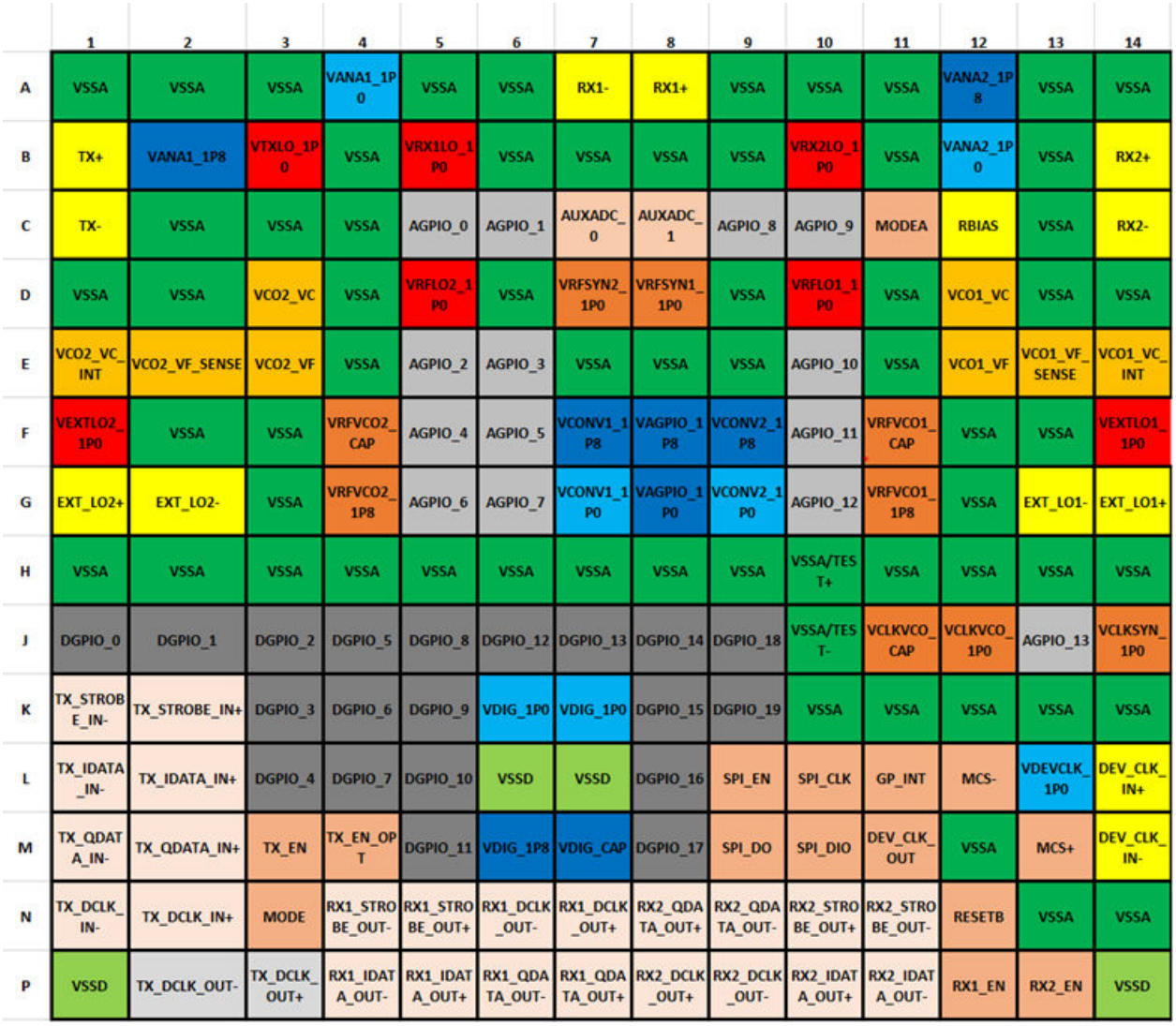
	Supply (mA)				
Conditions	**VDDA_1P0 Analog Supplies**	**VDD_1P0 Digital Supply**	**VDDA_1P8 Analog Supplies**	**VDD_1P8 Digital Supply**	**Total Average Power (mW)**
RF PLL is Enabled for EXT VCO	45.2	22.5	19	1.5	105

The values in Table 9 are based on the following configuration: DEV_CLK: 38.4Mhz, with Rx channel power on only.

Table 9. Rx Power Consumption with Internal LO

	Supply (mA)				
Conditions	**VDDA_1P0 Analog Supplies**	**VDD_1P0 Digital Supply**	**VDDA_1P8 Analog Supplies**	**VDD_1P8 Digital Supply**	**Total Average Power (mW)**
Rx2 NB enabled, Sample Rate: 2.4MSPS, ADC Sample Rate: 38.4Mhz, Internal LO Mode at 450MHz	55	27.6	51.8	4.2	183.4
Rx1 WB enabled, Sample Rate: 30.72MSPS, ADC Sample Rate: 1105.92Mhz, Internal LO Mode at 450MHz	134.5	190.4	97.7	20	536.8

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	VSSA	VSSA	VANA1_1P0	VSSA	VSSA	RX1-	RX1+	VSSA	VSSA	VSSA	VANA2_1P8	VSSA	VSSA
B	TX+	VANA1_1P8	VTXLO_1P0	VSSA	VRX1LO_1P0	VSSA	VSSA	VSSA	VSSA	VRX2LO_1P0	VSSA	VANA2_1P0	VSSA	RX2+
C	TX-	VSSA	VSSA	VSSA	AGPIO_0	AGPIO_1	AUXADC_0	AUXADC_1	AGPIO_8	AGPIO_9	MODEA	RBIAS	VSSA	RX2-
D	VSSA	VSSA	VCO2_VC	VSSA	VRFLO2_1P0	VSSA	VRFSYN2_1P0	VRFSYN1_1P0	VSSA	VRFLO1_1P0	VSSA	VCO1_VC	VSSA	VSSA
E	VCO2_VC_INT	VCO2_VF_SENSE	VCO2_VF	VSSA	AGPIO_2	AGPIO_3	VSSA	VSSA	VSSA	AGPIO_10	VSSA	VCO1_VF	VCO1_VF_SENSE	VCO1_VC_INT
F	VEXTLO2_1P0	VSSA	VSSA	VRFVCO2_CAP	AGPIO_4	AGPIO_5	VCONV1_1P8	VAGPIO_1P8	VCONV2_1P8	AGPIO_11	VRFVCO1_CAP	VSSA	VSSA	VEXTLO1_1P0
G	EXT_LO2+	EXT_LO2-	VSSA	VRFVCO2_1P8	AGPIO_6	AGPIO_7	VCONV1_1P0	VAGPIO_1P0	VCONV2_1P0	AGPIO_12	VRFVCO1_1P8	VSSA	EXT_LO1-	EXT_LO1+
H	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA/TEST+	VSSA	VSSA	VSSA	VSSA
J	DGPIO_0	DGPIO_1	DGPIO_2	DGPIO_5	DGPIO_8	DGPIO_12	DGPIO_13	DGPIO_14	DGPIO_18	VSSA/TEST-	VCLKVCO_CAP	VCLKVCO_1P0	AGPIO_13	VCLKSYN_1P0
K	TX_STROBE_IN-	TX_STROBE_IN+	DGPIO_3	DGPIO_6	DGPIO_9	VDIG_1P0	VDIG_1P0	DGPIO_15	DGPIO_19	VSSA	VSSA	VSSA	VSSA	VSSA
L	TX_IDATA_IN-	TX_IDATA_IN+	DGPIO_4	DGPIO_7	DGPIO_10	VSSD	VSSD	DGPIO_16	SPI_EN	SPI_CLK	GP_INT	MCS-	VDEVCLK_1P0	DEV_CLK_IN+
M	TX_QDATA_IN-	TX_QDATA_IN+	TX_EN	TX_EN_OPT	DGPIO_11	VDIG_1P8	VDIG_CAP	DGPIO_17	SPI_DO	SPI_DIO	DEV_CLK_OUT	VSSA	MCS+	DEV_CLK_IN-
N	TX_DCLK_IN-	TX_DCLK_IN+	MODE	RX1_STROBE_OUT-	RX1_STROBE_OUT+	RX1_DCLK_OUT-	RX1_DCLK_OUT+	RX2_QDATA_OUT+	RX2_QDATA_OUT-	RX2_STROBE_OUT+	RX2_STROBE_OUT-	RESETB	VSSA	VSSA
P	VSSD	TX_DCLK_OUT-	TX_DCLK_OUT+	RX1_IDATA_OUT-	RX1_IDATA_OUT+	RX1_QDATA_OUT-	RX1_QDATA_OUT+	RX2_DCLK_OUT+	RX2_DCLK_OUT-	RX2_IDATA_OUT+	RX2_IDATA_OUT-	RX1_EN	RX2_EN	VSSD

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Type	Mnemonic	Description
A1, A2, A3, A5, A6, A9, A10, A11, A13, A14, B4, B6 to B9, B11, B13, C2, C3, C4, C13, D1, D2, D4, D6, D9, D11, D13, D14, E4, E7, E8, E9, E11, F2, F3, F12, F13, G3, G12, H1 to H9, H11 to H14, K10 to K14, M12, N13, N14	Input	VSSA	Analog Ground
A4	Input	VANA1_1P0	1.0 V Analog Supply for RX1 TIA, TX Baseband Filter.
A7, A8	Input	RX1-, RX1+	Differential Input for Receiver Channel 1 (Wide Band). If unused, connect RX1− and RX1+ to VSSA via a capacitor.
A12	Input	VANA2_1P8	1.8 V Analog Supply for RX2 Mixer, RX2 TIA, and Internal References.
B1, C1	Output	TX+, TX-	Differential Output for Transmitter Channel. If unused, do not connect TX+ and TX−.
B2	Input	VANA1_1P8	1.8 V Analog Supply for RX1 Mixer, RX1 TIA, TX Mixer, TX Baseband Filter.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Type	Mnemonic	Description
B3	Input	VTXLO_1P0	1.0 V Analog Supply for TX LO Distribution and TX Upconverter.
B5	Input	VRX1LO_1P0	1.0 V Analog Supply for RX1 LO Distribution, RX1 Mixer.
B10	Input	VRX2LO_1P0	1.0 V Analog Supply for RX2 LO Distribution, RX2 Mixer.
B12	Input	VANA2_1P0	1.0 V Analog Supply for RX2 TIA
B14, C14	Input	RX2+, RX2-	Differential Input for Receiver Channel 2 (Narrow Band). If unused, connect RX2- and RX2+ to VSSA via a capacitor.
C5, C6, E5, E6, F5, F6, G5, G6, C9, C10, E10, F10, G10, J13	Input/ Output	AGPIO_xx	GPIOs Signals Referenced to VAGPIO_1P8 1.8 V Supply, AGPIO_0 to AGPIO_3 pins can also function as auxiliary DAC outputs. If unused, do not connect AGPIO_xx.
C7	Input	AUXADC_0	Input to Auxiliary ADC0. If unused, do not connect AUXADC_0.
C8	Input	AUXADC_1	Input to Auxiliary ADC1. If unused, do not connect AUXADC_1.
C11	Input	MODEA	Use MODEA to configure the boot up option for the DEV_CLK_IN± inputs and the DEV_CLK_OUT output. Connect MODEA to VSSA to enable the differential clock receiver at the DEV_CLK_IN± pins. Connect MODEA to 1.8V supply to enable single ended clock at DEV_CLK_IN+. Connect MODEA to voltage level higher than any VSSA (level TBD) to enable the crystal oscillator resonator at both of the DEV_CLK_IN± pins.
C12	Input	RBIAS	Bias Resistor Connection. RBIAS generates an internal current based on an external 1% resistor. Connect a 4.99 kΩ resistor between RBIAS and VSSA (analog ground).
D3	Output	VCO2_VC	External VCO2 Coarse tuning Voltage output
D5	Input	VRFLO2_1P0	1.0 V Analog Supply for RF LO2 Generation
D7	Input	VRFSYN2_1P0	1.0 V Analog Supply for RF PLL2
D8	Input	VRFSYN1_1P0	1.0 V Analog Supply for RF PLL1
D10	Input	VRFLO1_1P0	1.0 V Analog Supply for RF LO1 Generation
D12	Output	VCO1_VC	External VCO1 Coarse tuning Voltage output
E1	Output	VCO2_VC_INT	External VCO2 Coarse tuning Voltage Integration
E2	Input	VCO2_VF_SENSE	External VCO2 Fine tuning Voltage Sense input
E3	Output	VCO2_VF	External VCO2 Fine tuning Voltage output
E12	Output	VCO1_VF	External VCO1 Fine tuning Voltage output
E13	Input	VCO1_VF_SENSE	External VCO1 Fine tuning Voltage Sense input
E14	Output	VCO1_VC_INT	External VCO1 Coarse tuning Voltage Integration
F1	Input	VEXTLO2_1P0	1.0 V Analog Supply for External LO2
F4	Output	VRFVCO2_CAP	1.6 V Internal Supply Node for RF PLL2 Circuitry. Bypass VRFVCO2_CAP with a 4.7 µF capacitor.
F7	Input	VCONV1_1P8	1.8 V Analog Supply for TX DAC, RX1 ADC.
F8	Input	VAGPIO_1P8	1.8 V Analog Supply for DEV_CLK, MCS, Auxiliary DACs, Auxiliary ADCs, and AGPIO Signals.
F9	Input	VCONV2_1P8	1.8 V Analog Supply for RX2 ADC.
F11	Output	VRFVCO1_CAP	1.6 V Internal Supply Node for RF PLL1 Circuitry. Bypass VRFVCO1_CAP with a 4.7 µF capacitor.
F14	Input	VEXTLO1_1P0	1.0 V Analog Supply for External LO1
G1, G2	Input	EXT_LO2+, EXT_LO2-	External LO/External VCO Input port 2 (LO2). In differential mode, the input frequency could be 2x or higher than the desired carrier frequency. For the carrier frequency range of 250 MHz (TBD) to 1 GHz, 1x multiplier is available. In single ended mode, the input frequency must be 2x or higher than the desired carrier frequency, EXT_LO2- is not used in single ended mode, it should be AC grounded. If External LO/VCO function is unused, connect EXT_LO2+, EXT_LO2- to VSSA.
G4	Input	VRFVCO2_1P8	1.8 V Analog Supply for RF VCO2, RF PLL2(for External VCO2).
G7	Input	VCONV1_1P0	1.0 V Analog Supply for TX DAC, RX1 ADC.
G8	Input	VAGPIO_1P0	1.0 V Analog Supply for Auxiliary DACs, Auxiliary ADCs, and AGPIO_xx Signals.
G9	Input	VCONV2_1P0	1.0 V Analog Supply for RX2 ADC.
G11	Input	VRFVCO1_1P8	1.8 V Analog Supply for RF VCO1, RF PLL1(for External VCO1).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Type	Mnemonic	Description
G14, G13	Input	EXT_LO1+, EXT_LO1-	External LO/External VCO Input port 1 (LO1). In differential mode, the input frequency could be 2x or higher than the desired carrier frequency. For the carrier frequency range of 250 MHz (TBD) to 1 GHz, 1x multiplier is available. In single ended mode, the input frequency must be 2x or higher than the desired carrier frequency, EXT_LO1- is not used in single ended mode, it should be AC grounded. If External LO/VCO function is unused, connect EXT_LO1+, EXT_LO1- to VSSA.
H10	Input	VSSA/TEST+	Connect VSSA/TEST+ to VSSA for normal operation.
J10	Input	VSSA/TEST-	Connect VSSA/TEST- to VSSA for normal operation.
J1 to J9, K3, K4, K5, K8, K9, L3, L4, L5, L8, M5, M8	Input/ Output	DGPIO_xx	Digital GPIO. VDIG_1P8 supplies 1.8 V to DGPIO_xx. If unused, do not connect DGPIO_xx.
J11	Output	VCLKVCO_CAP	0.8 V Internal Supply Node for Clock PLL. Bypass VCLKVCO_CAP with a 4.7 µF capacitor.
J12	Input	VCLKVCO_1P0	1.0 V Analog Supply for Clock PLL VCO, Clock Generation.
J14	Input	VCLKSYN_1P0	1.0 V Analog Supply for Clock PLL.
K1	Input	TX_STROBE_IN-	In LVDS SSI mode, TX_STROBE_IN− is the TX strobe input negative side. In CMOS SSI mode, TX_STROBE_IN− is not used. If unused, do not connect TX_STROBE_IN−.
K2	Input	TX_STROBE_IN+	In LVDS SSI mode, TX_STROBE_IN+ is the TX strobe input positive side. In CMOS SSI mode, TX_STROBE_IN+ is the TX strobe input. If unused, do not connect TX_STROBE_IN+.
K6, K7	Input	VDIG_1P0	1.0 V Digital Core Supply. Connect Pin K6 and Pin K7 together. Use a wide trace to connect the VDIG_1P0 pins to a separate power supply domain. Provide reservoir capacitance close to the chip.
L1	Input	TX_IDATA_IN-	In LVDS SSI mode, TX_IDATA_IN− is the TX I sample data input negative side or the TX I and Q sample data input negative side. In CMOS SSI mode, TX_IDATA_IN− is the TX Data Input 0 or the TX I and Q sample data input. If unused, do not connect TX_IDATA_IN−.
L2	Input	TX_IDATA_IN+	In LVDS SSI mode, TX_IDATA_IN+ is the TX I sample data input positive side or the TX I and Q sample data input positive side. In CMOS SSI mode, TX_IDATA_IN+ is the TX Data Input 1. If unused, do not connect TX_IDATA_IN+.
L6, L7, P1, P14	Input	VSSD	Digital Ground
L9	Input	SPI_EN	Active Low Serial Data Bus Chip Select.
L10	Input	SPI_CLK	Serial Data Bus Clock Input.
L11	Output	GP_INT	General Purpose Digital Interrupt Output Signal. If unused, do not connect GP_INT.
L12, M13	Input	MCS-, MCS+	Multichip Synchronization Reference Inputs. If unused, connect MCS+ and MCS− to VSSA.
L13	Input	VDEVCLK_1P0	1.0 V Analog Supply for DEV_CLK circuitry
L14, M14	Input	DEV_CLK_IN+, DEV_CLK_IN-	Device Clock Input. DEV_CLK_IN± can operate as differential, single-ended, or be connected to the external crystal oscillator. In single-ended mode, apply the clock signal to the DEV_CLK_IN+ pin and leave the DEV_CLK_IN− pin unconnected.
M1	Input	TX_QDATA_IN-	In LVDS SSI mode, TX_QDATA_IN− is the TX Q sample data input negative side. In CMOS SSI mode, TX_QDATA_IN− is the TX Data Input 2. If unused, do not connect TX_QDATA_IN−.
M2	Input	TX_QDATA_IN+	In LVDS SSI mode, TX_QDATA_IN+ is the TX Q sample data input positive side. In CMOS SSI mode, TX_QDATA_IN+ is the TX Data Input 3. If unused, do not connect TX_QDATA_IN+.
M3	Input	TX_EN	Enable Input for Transmitter Channel. If unused, connect TX_EN to VSSA
M4	Input	TX_EN_OPT	Optional Enable Input for Transmitter wideband Channel if two independent Pins control for narrow-band channel and wideband channel respectively is needed. If unused, connect to VSSA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Type	Mnemonic	Description
M6	Input	VDIG_1P8	1.8 V Digital Supply Input for Data Port Interface (CMOS-SSI and LVDS SSI Mode), SPI Signals, Control Input and Output Signals, and DGPIO Interface.
M7	Output	VDIG_CAP	0.9 V Internal Supply Node for Digital Circuitry. Bypass VDIG_CAP with a 4.7 µF capacitor.
M9	Output	SPI_DO	Serial Data Output. If unused in SPI 3-wire mode, do not connect SPI_DO.
M10	Input/ Output	SPI_DIO	Serial Data Input in 4-Wire Mode or Input and Output in 3-Wire Mode.
M11	Output	DEV_CLK_OUT	Single-Ended Device Clock Output. DEV_CLK_OUT provides a DEV_CLK signal or the divided version to the baseband IC. If unused, do not connect DEV_CLK_OUT.
N1	Input	TX_DCLK_IN-	In LVDS SSI mode, TX_DCLK_IN− is the TX data clock input negative side. In CMOS SSI mode, TX_DCLK_IN− is not used. If unused, do not connect TX_DCLK_IN−.
N2	Input	TX_DCLK_IN+	In LVDS SSI mode, TX_DCLK_IN+ is the TX data clock input positive side. In CMOS SSI mode, TX_DCLK_IN+ is the TX data clock input. If unused, do not connect TX_DCLK_IN+.
N3	Input	MODE	Joint Test Action Group (JTAG) Boundary Scan Pin. If unused, connect MODE to VSSA.
N4	Output	RX1_STROBE_OUT-	In LVDS SSI mode, RX1_STROBE_OUT− is the RX1 strobe output negative side. In CMOS SSI mode, RX1_STROBE_OUT− is not used. If unused, do not connect RX1_STROBE_OUT−.
N5	Output	RX1_STROBE_OUT+	In LVDS SSI mode, RX1_STROBE_OUT+ is the RX1 strobe output positive side. In CMOS SSI mode, RX1_STROBE_OUT+ is the RX1 strobe output. If unused, do not connect RX1_STROBE_OUT+.
N6	Output	RX1_DCLK_OUT-	In LVDS SSI mode, RX1_DCLK_OUT− is the RX1 data clock output negative side. In CMOS SSI mode, RX1_DCLK_OUT− is not used. If unused, do not connect RX1_DCLK_OUT−.
N7	Output	RX1_DCLK_OUT+	In LVDS SSI mode, RX1_DCLK_OUT+ is the RX1 data clock output positive side. In CMOS SSI mode, RX1_DCLK_OUT+ is the RX1 data clock output. If unused, do not connect RX1_DCLK_OUT+.
N8	Output	RX2_QDATA_OUT+	In LVDS SSI mode, RX2_QDATA_OUT+ is the RX2 Q sample data output positive side. In CMOS SSI mode, RX2_QDATA_OUT+ is the RX2 Data Output 3. If unused, do not connect RX2_QDATA_OUT+.
N9	Output	RX2_QDATA_OUT-	In LVDS SSI mode, RX2_QDATA_OUT− is the RX2 Q sample data output negative side. In CMOS SSI mode, RX2_QDATA_OUT− is the RX2 Data Output 2. If unused, do not connect RX2_QDATA_OUT−.
N10	Output	RX2_STROBE_OUT+	In LVDS SSI mode, RX2_STROBE_OUT+ is the RX2 strobe output positive side. In CMOS SSI mode, RX2_STROBE_OUT+ is the RX2 strobe output. If unused, do not connect RX2_STROBE_OUT+.
N11	Output	RX2_STROBE_OUT-	In LVDS SSI mode, RX2_STROBE_OUT− is the RX2 strobe output negative side. In CMOS SSI mode, RX2_STROBE_OUT− is not used. If unused, do not connect RX2_STROBE_OUT−.
N12	Input	RESETB	Active Low Chip Reset
P2	Output	TX_DCLK_OUT-	In LVDS SSI mode, TX_DCLK_OUT- is the TX reference clock output negative side. In CMOS SSI mode, TX_DCLK_OUT- is not used. If unused, do not connect TX_DCLK_OUT-.
P3	Output	TX_DCLK_OUT+	In LVDS SSI mode, TX_DCLK_OUT+ is the TX SSI reference clock output positive side. In CMOS SSI mode, TX_DCLK_OUT+ is the TX SSI reference clock output. If unused, do not connect TX_DCLK_OUT+.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Type	Mnemonic	Description
P4	Output	RX1_IDATA_OUT-	In LVDS SSI mode, RX1_IDATA_OUT− is the RX1 I sample data output negative side or the RX1 I and Q sample data output negative side. In CMOS SSI mode, RX1_IDATA_OUT− is the RX1 Data Output 0 or the RX1 I and Q sample data output. If unused, do not connect RX1_IDATA_OUT-.
P5	Output	RX1_IDATA_OUT+	In LVDS SSI mode, RX1_IDATA_OUT+ is the RX1 I sample data output positive side or the RX1 I and Q sample data output positive side. In CMOS SSI mode, RX1_IDATA_OUT+ is the RX1 Data Output 1. If unused, do not connect RX1_IDATA_OUT+.
P6	Output	RX1_QDATA_OUT-	In LVDS SSI mode, RX1_QDATA_OUT− is the RX1 Q sample data output negative side. In CMOS SSI mode, RX1_QDATA_OUT− is the RX1 Data Output 2. If unused, do not connect RX1_QDATA_OUT−.
P7	Output	RX1_QDATA_OUT+	In LVDS SSI mode, RX1_QDATA_OUT+ is the RX1 Q sample data output positive side. In CMOS SSI mode, RX1_QDATA_OUT+ is the RX1 Data Output 3. If unused, do not connect RX1_QDATA_OUT+.
P8	Output	RX2_DCLK_OUT+	In LVDS SSI mode, RX2_DCLK_OUT+ is the RX2 data clock output positive side. In CMOS SSI mode, RX2_DCLK_OUT+ is the RX2 data clock output. If unused, do not connect RX2_DCLK_OUT+.
P9	Output	RX2_DCLK_OUT-	In LVDS SSI mode, RX2_DCLK_OUT− is the RX2 data clock output negative side. In CMOS SSI mode, RX2_DCLK_OUT− is not used. If unused, do not connect RX2_DCLK_OUT−.
P10	Output	RX2_IDATA_OUT+	In LVDS SSI mode, RX2_IDATA_OUT+ is the RX2 I sample data output positive side of the differential pair or the RX2 I and Q sample data output positive side of the differential pair. In CMOS SSI mode, RX2_IDATA_OUT+ is the RX2 Data Output 1. If unused, do not connect RX2_IDATA_OUT+.
P11	Output	RX2_IDATA_OUT-	In LVDS SSI mode, RX2_IDATA_OUT− is the RX2 I sample data output on the negative side or the RX2 I and Q sample data output on the negative side. In CMOS SSI mode, RX2_IDATA_OUT− is the RX2 Data Output 0 or the RX2 I and Q sample data output. If unused, do not connect RX2_IDATA_OUT−.
P12	Input	RX1_EN	Enable Input for Receiver channel 1. If unused, connect RX1_EN to VSSA.
P13	Input	RX2_EN	Enable Input for Receiver channel 2. If unused, connect RX2_EN to VSSA.

THEORY OF OPERATION

The ADRV9104 is a low-power optimized Software Defined Radio (SDR) with extended capabilities for modem functionalities that can be configured for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide transmit and receive functions in a single device. Programmability allows the transmitter channel and two receiver channels to be used in TDD and FDD systems for mobile radio and cellular standards. The ADRV9104 contains serial interface links that consist of LVDS and a CMOS synchronous serial interface (LSSI/CSSI). Both receiver and transmitter channels provide a low pin count and reliable data interface to a field-programmable gate array (FPGA) or other integrated baseband solutions.

TRANSMITTER

The ADRV9104 uses a direct conversion transmitter architecture that provides all the digital processing, mixed signal, PLL, and RF blocks necessary to implement a direct conversion system.

The ADRV9104 has an optional, fully programmable, 128-tap FIR. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each DAC has an adjustable sample rate and is linear up to full scale. The configurable digital datapath design allows the transmitter to support narrow band or wide band applications.

The DAC output produces baseband analog signals. The I and Q signals are first filtered to remove sampling artifacts and then fed to the up conversion mixers. At the mixer stage, the I and Q signals are recombined and upconverted to the carrier frequency for transmission to the output stage. The transmit chain provides a wide attenuation adjustment range with fine granularity to help designers optimize the signal-to-noise ratio (SNR).

RECEIVER

ADRV9104 contains two receiver paths: Rx1 WB/NB is a wide to narrow band path with up to 40 MHz RF bandwidth; Rx2 NB is a dedicated low power narrow band path with up to 2 MHz RF bandwidth. Both receivers, Rx1 WB/NB and Rx2 NB, are a fully integrated, direct conversion receiver signal chains with digital NCOs enabling support for low IF mode. The receiver subsystems consist of a resistive input network for gain control followed by a current mode passive mixer. The output current of the mixer is converted to a voltage by a transimpedance amplifier and then digitized by the ADC. There is a wide band, high performance Σ-Δ ADC on Rx channel 1 and a narrow band, high performance Σ-Δ ADC on Rx channel 2. The digital baseband that provides the required filtering and decimation follows these ADCs. The mixer architecture is linear and inherently wideband, which facilitates impedance matching. The differential input impedance of the receiver inputs is 100 Ω. To achieve gain control, a programmed gain index map is implemented. This gain map distributes attenuation among the various receiver blocks for optimal performance at each power level. The gain range is 34 dB. The ADRV9104 is a wideband architecture transceiver that relies on the ADC high dynamic range to receive signals and interference at the same time. Filtering provided by the receive LPF attenuates ADC alias images.

The receive LPF characteristic is flat and not intended to provide rejection of close in blockers.

The ADC output can be conditioned further by a series of decimation filters and a fully programmable, FIR filter with additional decimation settings. The sample rate of each digital filter block automatically adjusts with each change of the decimation factors to produce the desired output data rate.

The receiver supports Intermediate Frequency (IF) receive architecture where the LO frequency is offset by that of the receive carrier frequency. The IF signal at the mixer and LPF output is digitalized by ADC, the digital down converter with the NCO down converts the IF signal to baseband. The ADRV9104 makes no assumptions about high-side or low-side injection.

CLOCK INPUT

The ADRV9104 requires an external reference clock be applied to its DEV_CLK_IN± pins. This supplied reference clock serves as the basis from which all internal ADRV9104 clocks are derived. The ADRV9104 offers multiple reference input clocking options. The reference input clock pins on the device are labeled DEV_CLK_IN±. If a differential input clock is provided, the clock signal must be ac-coupled with the input range limited from 10 MHz to 307.2MHz. The ADRV9104 can also accept an external crystal (XTAL) as a clock source. The frequency range of the supported crystal is between 20 MHz to 80 MHz. The external crystal connection must be dc-coupled. If a differential clock is not available, a single-ended, ac-coupled, 1 V p-p (maximum) CMOS signal can be applied to the DEV_CLK_IN+ pin with the DEV_CLK_IN− pin unconnected. The maximum clock frequency in this mode is limited to 80 MHz.

SYNTHESIZERS

The ADRV9104 offers two distinct PLL paths, an RF PLL for the high frequency RF path and a baseband PLL for the digital and sampling clocks of the data converters.

THEORY OF OPERATION

RF PLL

The PLL structure in the ADRV9104 is unique as it includes two internal RF PLLs with fully integrated on-chip VCOs and two internal RF PLLs fit for external VCOs. The flexible internal LO mapping circuits support the use of internal LO signals, external LO signals and external VCO signals. Any of these sources can be routed to any or all the RF channels. This flexibility enables the ADRV9104 to meet various applications that require versatility.

The internal LO is generated by an on-chip VCO, which is tunable over a frequency range of 6.5 GHz to 13 GHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable. The VCO outputs are steered through a combination of frequency dividers to produce in-phase and quadrature phase LO signals in the 70 MHz to 6 GHz frequency range.

An external LO signal can be applied to the external LO inputs of the ADRV9104 to generate the LO signals in quadrature for the RF path. If the external LO path is chosen, the input frequency range is between 140 MHz and 12 GHz.

Alternatively, the ADRV9104 internal PLLs can interface with external VCO design, the external VCO outputs are applied to the ADRV9104 external LO inputs and are phase locked to the reference clock through the internal programmable factional-N PLLs. This allows integration of custom VCO designs for maximum versatility in LO generation.

BASEBAND PLL

The ADRV9104 contains a baseband PLL synthesizer that generates all baseband and data port related clocks. The ADRV9104 has the option to disable the baseband PLL and utilizes the reference clock input, or reference clock input with doubler, to generate all baseband and data port related clocks.

GPIO PINS

Digital General-Purpose Inputs/Outputs (DGPIOs)

The ADRV9104 GPIO signals referenced to the VDIG_1P8 supply are intended to interface with digital circuitry and can be configured for numerous functions. Some of these pins, when configured as outputs, are used by the baseband processor as real-time signals to provide a number of internal settings and measurements. This configuration allows the baseband processor to monitor receiver performance in different situations. Signals used for manual gain mode, calibration flags, state machine states, and various receiver parameters are among the outputs that can be monitored on these pins. In addition, certain pins can be configured as inputs and used in various functions, such as setting the receiver gain or transmitter attenuation in real time.

The PS2 subsystem has the ability to map other functions to the GPIOs to operate the PS2 ARM digital interrupt and other PS2 peripherals. Any of the 20 DGPIOs can be set to inputs for the PS2 interrupt.

Analog General-Purpose Inputs/Outputs (AGPIOs)

The AGPIO pins are intended to interface with system blocks that perform analog functions. The AGPIO pins referenced to the VAGPIO_1P8 supply provide control signals to the external components, such as the low noise amplifier (LNA) or digital step attenuator (DSA). The selected AGPIO pins provide an alternate auxiliary DAC functionality.

AUXILIARY CONVERTERS

Auxiliary ADC Inputs (AUXADC_x)

The ADRV9104 contains four auxiliary ADCs with the corresponding inputs connected to four dedicated input pins (AUXADC_x). This block can monitor system voltages without additional components. The auxiliary ADC is 10 bits with an input voltage range of 0.05 V to 0.95 V. When enabled, the auxiliary ADC is free running. An API function allows the user to read back the last value latched by the ADC.

Auxiliary DACs Outputs (AUXDAC_x)

The ADRV9104 contains four identical auxiliary DACs (AUXDAC_x) that can supply bias voltages, analog control voltages, or other system functionality. The auxiliary DACs (AUXDAC_0 to AUXDAC_3) are multiplexed with the AGPIO_xx pins. The auxiliary DACs are 12 bits and have an output voltage range of approximately 0.05 V to VDDA_1P8 − 0.05 V and have a current drive of 10 mA. The auxiliary DACs generate ramp up and ramp down patterns that can be loaded into the ADRV9104 and then triggered based on state of dedicated DGPIO pin.

SPI

The ADRV9104 uses an SPI to communicate with the baseband processor. This interface can be configured either as a 4-wire interface with dedicated receive and transmit ports, or as a 3-wire interface with a bidirectional data communications port. This bus allows the baseband processor to set all device control parameters using a simple address data serial bus protocol. Write commands follow a 24-bit format. The first bit sets the bus direction of the bus transfer. The next 15 bits set the address where the data is written. The final eight bits contain the data transferred to the specific register address. Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DIO pin and the final eight bits are read from the ADRV9104 either on the SPI_DO pin in 4-wire mode or on the SPI_DIO pin in 3-wire mode.

THEORY OF OPERATION

PROCESSOR SUBSYSTEM 2 (PS2)

The ADRV9104 enables users to jump start designs for a flexible wireless connectivity by implementing various protocol stack layers from physical (PHY) to upper layers (L1/L2/L3). The ADRV9104 PS2 contains dedicated hardware accelerators to support all major PHY layer functions, enabling development for a wide range of wireless applications.

The ADRV9104 PS2 block diagram is shown in Figure 1, which consists of the transceiver component (ADRV9104 PS1) and the extended open ARM Cortex-M4 processor-based PS2 for the functions of the modem upper protocol stack layer.

By bringing an ARM Cortex-M4 subsystem with 928 kB of memory, a variety of peripherals, and flexible and scalable hardware accelerators for protocol stack functions together, the ADRV9104 PS2 gives developers more design choices for rapid deployment of applications requiring wireless connectivity.

The ADRV9104 PS2 main features include the following:

- An ARM processor Cortex-M4 subsystem
- 928 kB of useable memory
- Direct memory access (DMA) controllers to transfer data between PS2 memory, SSI, the PS1 data path and peripherals
- A variety of peripherals: SPI-M, SPI-S, I^2C, I^2S, Q-SPI, UART
- Timers and system event scheduler
- Dedicated PHY hardware accelerators (DSP and communication)

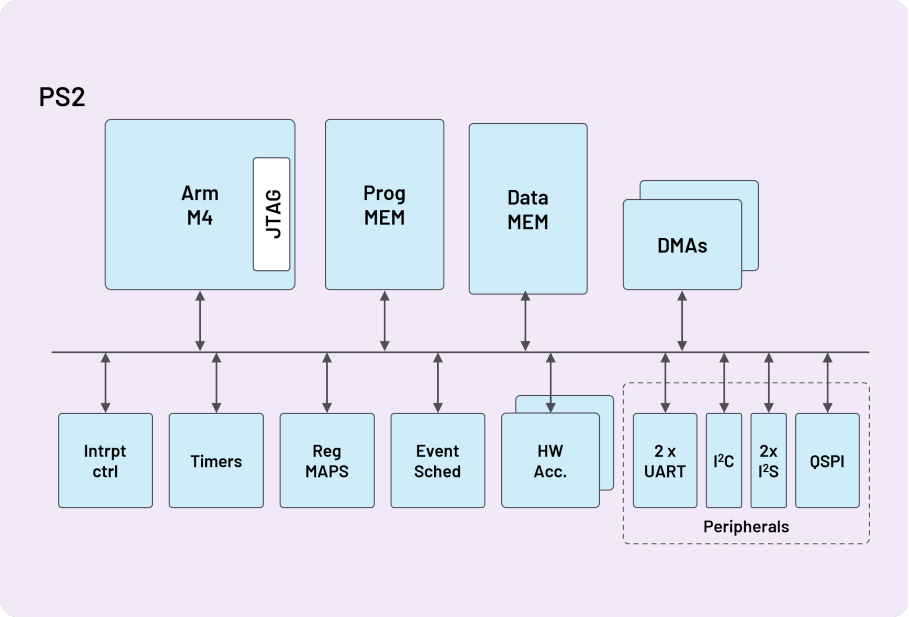


Figure 3. PS2 Block Diagram

THEORY OF OPERATION

DIGITAL DATA INTERFACE

The ADRV9104 data interface supports both CMOS and LVDS electrical interfaces. The CSSI is intended for narrow RF signal bandwidths, and the LVDS synchronous serial interface (LSSI) can support the full RF bandwidth of the ADRV9104. Table 11 provides a high level overview.

All signal lanes support both electrical interfaces, but concurrent operation of both interfaces is not supported. Additionally, each receive and transmit channel has a dedicated set of lanes for transferring information. The receive and transmit channels cannot be reconfigured to an alternative ball configuration that is different from how it has been assigned by design.

CSSI

The CSSI supports two modes of operation, 1-lane serialized data or 4-lane data. In either case, the maximum clock frequency supported by the CMOS configuration is 80 MHz.

For the CSSI in 1-lane data mode, 16 bits of I data and 16 bits of Q data (a total of 32 data bits) are serialized on a single lane. Figure 4 shows a graphical overview of the CSSI in 1-lane data mode.

For the CSSI in 4-lane data mode, the I and Q digital data is spread across four data lanes. The 16 bits of I data and 16 bits of Q data are split into 8 bits and sent over one of four data lanes. For example, Lane 0 would have 8 LSB bits of I data, Lane 1 would have 8 MSB bits of I data, Lane 2 would have 8 LSB bits of Q data, and Lane 3 would have 8 MSB bits of Q data.

The CSSI in 4-lane data mode supports both a full rate clock and a double data rate (DDR) clock. The DDR clock mode allows data to be latched on both the rising and falling edges, which enables twice the available RF bandwidth, as shown in Figure 5.

CSSI Receive

In the receive CMOS configuration, two additional signal lanes are required for the strobe and clock signals in addition to the data lane requirement as described for the CSSI in 1-lane mode and the CSSI in 4-lane mode, which allows a total of three signal lanes for the CSSI in 1-lane data mode and six total signal lanes for the CSSI in 4-lane data mode.

RXx_DCLK_OUT is an output clock signal that synchronizes the data and strobe output signals. RXx_STROBE_OUT is a strobe output signal that indicates the first bit of the serial data stream. The RXx_STROBE_OUT signal can be configured to indicate the start of the I and Q samples. For a 16-bit data sample, the RXx_STROBE_OUT signal is high for one clock cycle and low for 31 clock cycles. Alternatively, the RXx_STROBE_OUT signal can be configured to be high for I data duration and low for Q data duration. In this case, for a 16-bit data sample, the RXx_STROBE_OUT signal is high for 16 clock cycles (I data) and low for 16 clock cycles (Q data).

CSSI Transmit

For the transmit CMOS configuration, three additional signal lanes are required for the strobe, clock input, and clock output in addition to the data lane requirement as described for the CSSI in 1-lane data mode and the CSSI in 4-lane data mode, which allows a total of four signal lanes for the CSSI in 1-lane data mode and seven total signal lanes for the CSSI in 4-lane data mode.

TX_DCLK_IN is an input clock to the ADRV9104 that synchronizes to the data inputs (TX_DATA_IN) and strobe inputs (TX_STROBE_IN). TX_STROBE_IN is an input signal that indicates the first bit of the serial data sample. Similar to the receive path, the transmit strobe has two configuration options. The TX_DCLK_OUT is an output clock from the ADRV9104 to the external baseband device to generate the TX_DCLK_IN, TX_STROBE_IN, and TX_DATA_IN signals.

LSSI

The LSSI supports the higher RF channel bandwidths and requires differential signal pairs. In LSSI mode, there are two data transfer formats, 1-lane data mode, where both the I and Q data are serialized on a single differential pair, or 2-lane data mode, where the I and Q data occupy separate differential pairs. The selection of either 1-lane data mode or 2-lane data mode depends on the RF channel bandwidth. To capture the maximum 40 MHz RF bandwidth of the ADRV9104, select the LSSI in 2-lane data mode. In either case, the maximum clock frequency supported by the LSSI configuration is 491.52 MHz and the clock type is DDR. Refer to Figure 6 for more details.

Table 11. ADRV9104 Data Port Interface Modes

Interface Mode	Data Lanes per Channel	Serialization Factor per Data Lane	Maximum Data Lane Rate (MHz)	Maximum Clock Rate (MHz)	Maximum RF Bandwidth (MHz)	Sample Rate for I and Q Data (MHz)	Data Type[1]	Figure Reference
CSSI in 1-Lane Data	1	32	80	80	1.25	2.5	Normal	Figure 4
CSSI in 1-Lane Data	1	32	160	80	2.5	5	DDR	
CSSI in 4-Lane Data	4	8	80	80	5	10	Normal	
CSSI in 4-Lane Data	4	8	160	80	10	20	DDR	Figure 5

THEORY OF OPERATION

Table 11. ADRV9104 Data Port Interface Modes (Continued)

Interface Mode	Data Lanes per Channel	Serialization Factor per Data Lane	Maximum Data Lane Rate (MHz)	Maximum Clock Rate (MHz)	Maximum RF Bandwidth (MHz)	Sample Rate for I and Q Data (MHz)	Data Type[1]	Figure Reference
LSSI in 1-Lane Data	1	32	983.04	491.52	20	30.72	DDR	
LSSI in 2-Lane Data	2	16	983.04	491.52	40	61.44	DDR	Figure 6

[1] Normal data type refers to data on the rising edges, and DDR is double data rate, where data is available on the rising and falling edges of the input clock.

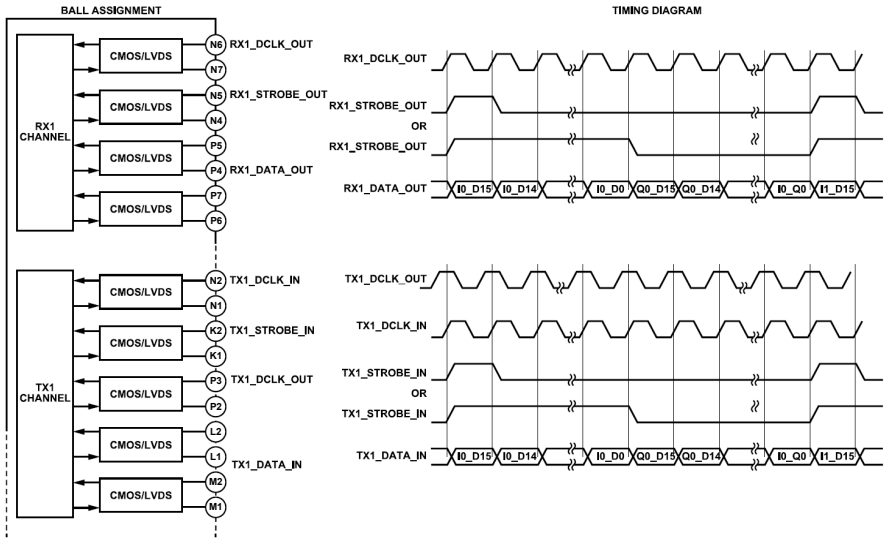


Figure 4. CSSI in 1-Lane Data Mode

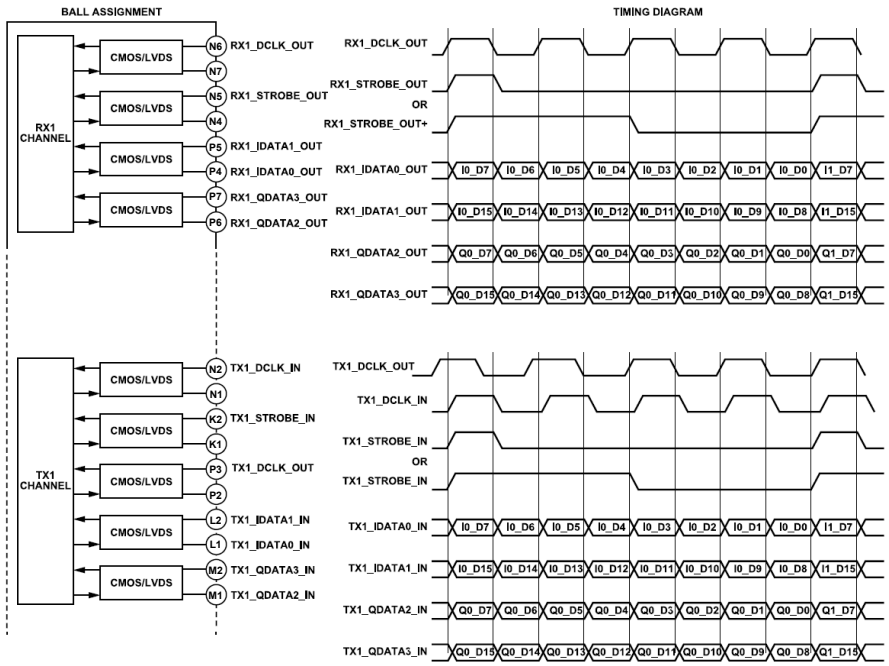


Figure 5. CSSI in 4-Lane Data Mode, DDR

THEORY OF OPERATION

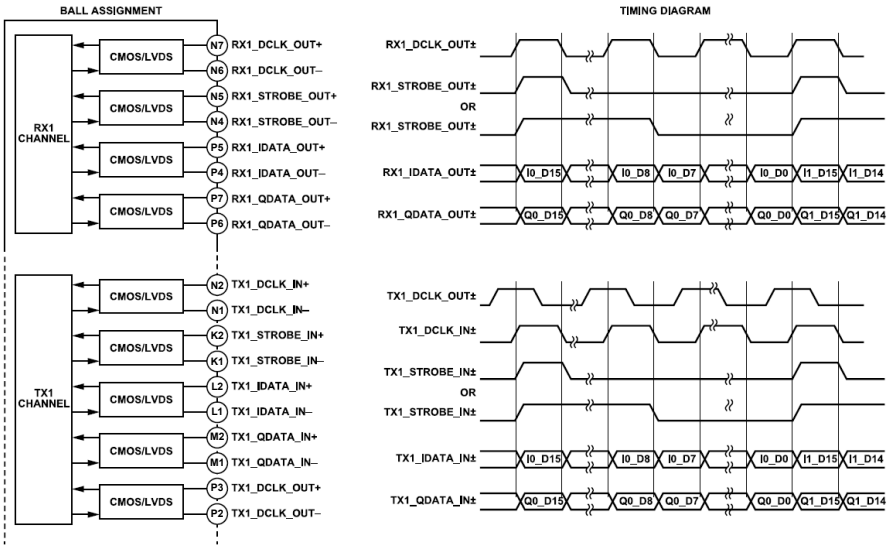


Figure 6. LSSI in 2-Lane Data Mode, DDR

OUTLINE DIMENSIONS

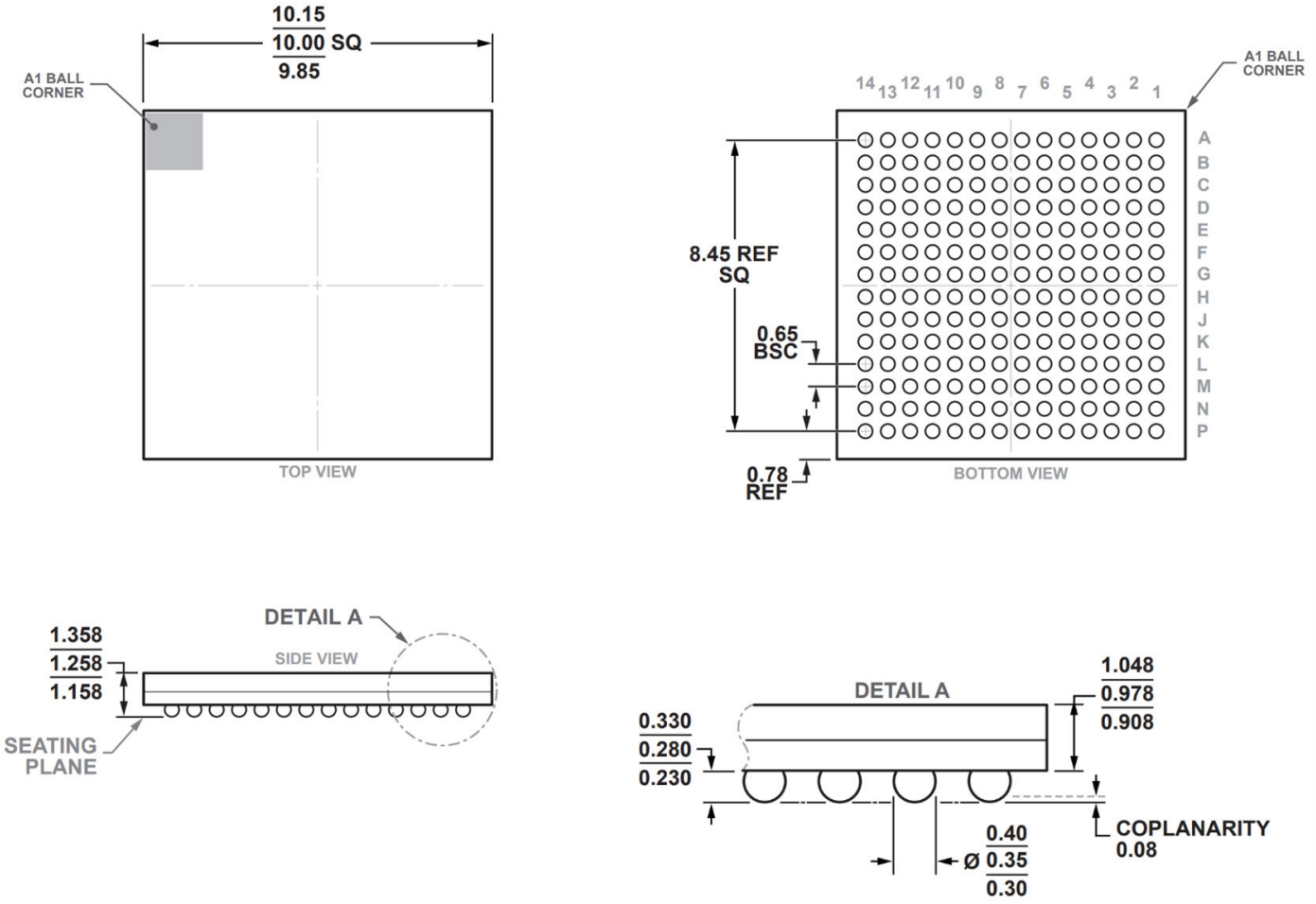


Figure 7. 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-196-19)
Dimensions shown in millimeters