

Monolithic 4T4R/8T8R Split 7.2a O-RU SoC

FEATURES

- ▶ Overall
 - ▶ O-RAN-compliant split 7.2x Category A RU System on a Chip (SoC)
 - ▶ 4 Tx/4 Rx/1 ORx using the ADRV9061
 - ▶ Extendible to 8 Tx/8 Rx/2 ORx using the ADRV9061/ADRV9062
 - ▶ Support for TDD and FDD operation
 - ▶ Support for NR FR1, LTE, and NB-IoT air interfaces
 - ▶ Support for single-band and multiband operation
 - ▶ Integrated ARM Cortex-A55 quad-core supporting Linux
- ▶ Bandwidth and frequency
 - ▶ Tunable RF range: 500MHz to 4830MHz
 - ▶ Tunable LO range: 600MHz to 4500MHz
 - ▶ Maximum Tx large signal bandwidth: 660MHz
 - ▶ Maximum Tx synthesis bandwidth: 800MHz
 - ▶ Maximum Rx bandwidth: 660MHz
 - ▶ Maximum ORx bandwidth: 800MHz
 - ▶ Maximum occupied bandwidth per antenna: 400MHz
- ▶ Clocking and synchronization
 - ▶ 2 integrated fractional-N RF synthesizers
 - ▶ Multichip phase sync for all LOs and baseband clocks
 - ▶ IEEE1588 PTP and SyncE (enhanced O-RU support)
- ▶ Digital front end (DFE)
 - ▶ Integrated DPD engine optimized for state-of-the-art macro power amplifiers
 - ▶ Support for DPD model switching for better dynamic performance
 - ▶ Support for charge trapping correction for GaN power amplifiers

- ▶ Integrated CFR engine
- ▶ Integrated PIMC
- ▶ Low PHY and fronthaul
 - ▶ FFT and IFFT
 - ▶ PRACH extraction
 - ▶ OFDM phase compensation
 - ▶ Integrated antenna calibration
- ▶ O-RAN-compliant 7.2x Category A eCPRI
- ▶ Fronthaul data compression
- ▶ Interfaces
 - ▶ Two fronthaul Ethernet ports supporting 10G or 25G
 - ▶ Interface to DDR4 memory
 - ▶ Interface to flash memory (QSPI/eMMC/SD card)
 - ▶ 6 SPI ports, 8 I²C ports, 5 UART ports, 16 pulse-width modulation (PWM), 1G Ethernet
 - ▶ Integrated chip-to-chip interface to support up to 8T8R by tiling two devices
 - ▶ Integrated 10G and 25G Ethernet switch
- ▶ Security
 - ▶ MACsec supporting AES-128/AES-256 encryption
 - ▶ Integrated support for secure boot, secure update, and life cycle management provided by tiny enclave
 - ▶ Power saving features
 - ▶ Discontinuous Tx and Rx with symbol granularity
 - ▶ Deep sleep mode

APPLICATIONS

- ▶ 4G/5G O-RAN TDD/FDD multiband small cell and macro base stations

FUNCTIONAL BLOCK DIAGRAM

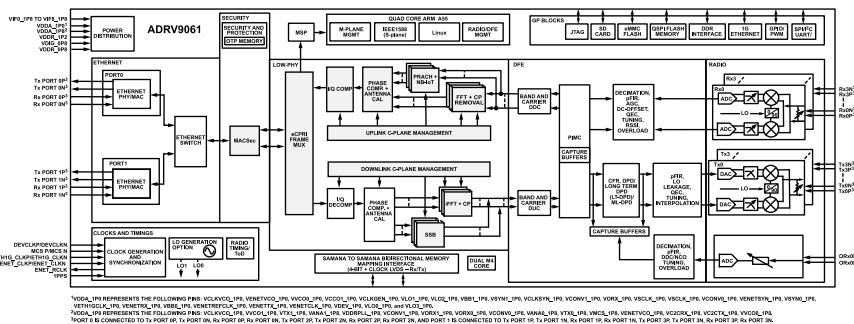


Figure 1. Block Diagram for 4T4R Configuration (ADRV9061), See Figure 478 for the Configuration (ADRV9061/ADRV9062)

For more information about the ADRV9061/ADRV9062, contact Analog Devices, Inc., at ADRV906x_Info@analog.com.

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DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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