Data Sheet

ADRV9042

8T8R SoC with DFE, 400 MHz iBW RF Transceiver

FEATURES

- Highly integrated transceiver
- 8 transmit (Tx), 8 receive (Rx), and 2 observation receivers (ORx)
- LO tuning range: 600 MHz to 7125 MHz
- RF range: 500 MHz to 7455 MHz[1]
- Zero-IF architecture reduces system size, weight, and power (SWaP)
  - Initial and run time calibrations maintain high performance
- Dual fully integrated fractional-N RF synthesizers
- Dual external LO inputs supporting operation up to 6 GHz.
- Multichip phase synchronization for all local oscillator (LO) and baseband clocks
- Single and multiband (N × 2T2R/4T4R) capability
- 4 individual band profiles within tunable range (band profiles define bandwidth and aggregate sampling rate of a channel)
- Fully integrated DPD supporting up to 400 MHz iBW/OBW
- Supports up to 660 MHz instantaneous BW, 400 MHz occupied BW on RF front end with DFE enabled
- Supports up to 400 MHz instantaneous/occupied BW with DFE disabled
- Supports JESD204B and JESD204C digital interface
- Simplifying thermal and power consumption challenges
  - 10.44 W power consumption for the TDD mode, full DFE features enabled use case with 100 MHz iBW/OBW[2]
  - 125°C maximum junction temperature for intermittent operation, 110°C for continuous (operating lifetime impact at >110°C can be offset by operation at <110°C based on acceleration factors)
- Fully integrated DFE (DPD, CDUC, CDDC, and CFR) engine reduces FPGA resources, halves SERDES lane rate, and simplifies designs
  - DPD adaptation engine for power amplifier linearization
  - CDUC/CDDC—maximum of 8 component carriers (CCs) per each transmitter/receiver channel
  - Multistage CFR engine
- Low power monitor and sleep modes

APPLICATIONS

- Tactical communications
- Phased array radars
- Electronic warfare
- Wireless test and measurement
- Portable instruments
- Time division duplexing (TDD)
- Frequency division duplexing (FDD)

FUNCTIONAL BLOCK DIAGRAM

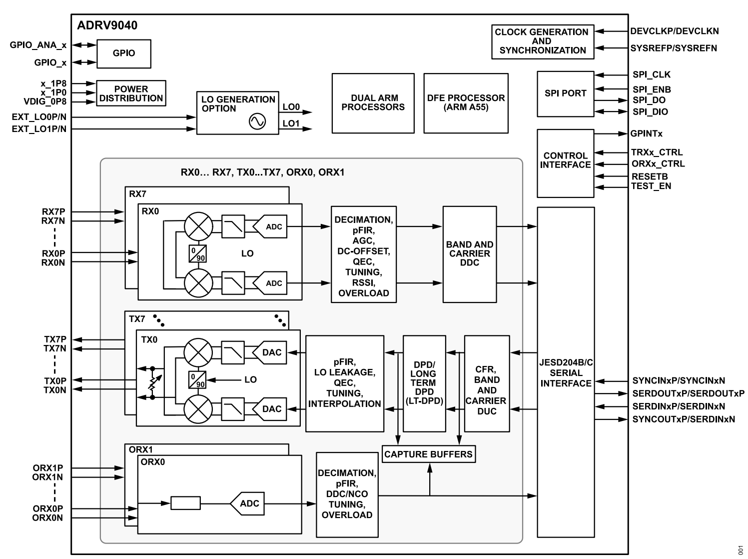

Figure 1. Functional Block Diagram

[1] The relationship between the LO and RF ranges can be expressed as: RF range = LO tuning range ± (large signal bandwidth/2).

[2] Power consumption values shown are for a typical use case. Power consumption depends heavily on the device configuration (use case). Please refer to the power analysis tab in the EVAL-ADRV904X evaluation software (ACE) to estimate the power consumption for the specified use case.

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GENERAL DESCRIPTION

The ADRV9042 is a highly integrated, RF transceiver with an integrated, digital front end (DFE) designed for use in instrumentation and aerospace, defense applications, and advanced communications systems. The transceiver contains eight transmitters, two observation receivers, eight receivers, integrated LO and clock synthesizers, and digital signal processing functions. The ADRV9042 is a high performance and low power radio with DFE support that has been designed for use in general-purpose applications operating from low frequencies. The ADRV9042 has a tuning range from 600 MHz to 7125 MHz and covers all UHF, industrial, scientific, and medical (ISM) and cellular frequency bands including WiFi 6E. Support beyond these frequencies can be enabled via external upconverters and downconverters available at Analog Devices, Inc.

The receiver and transmitter signal paths use a zero-IF (ZIF) architecture that provides wide bandwidth with dynamic range suitable for contiguous and noncontiguous multicarrier applications. The ZIF architecture has the benefits of low power plus RF frequency and bandwidth agility. The lack of aliases and out-of-band images eliminate anti-aliasing and image filters, which reduces both system size and cost, also making band independent solutions possible.

The device also includes two wide-bandwidth observation path receiver subsystems to monitor transmitter outputs. This transceiver subsystem includes automatic and manual attenuation control, DC offset correction, quadrature error correction (QEC), and digital filtering. General-purpose inputs and outputs (GPIOs) that provide an array of digital control options are also integrated.

Multiband capability is enabled by additional LO dividers and wideband operation, which allows four individuals band profiles within the tunable range; therefore, maximizing use case flexibility.

The transceiver has fully integrated DFE functionality, which includes carrier digital upconversion and downconversion (CDUC and CDDC), crest factor reduction (CFR), digital predistortion (DPD), closed-loop gain control (CLGC), and voltage standing wave ratio (VSWR) monitor.

The CDUC feature of the ADRV9042 filters and places individual component carriers within the band of interest. The CDDC feature, with its eight parallel paths, processes each carrier individually before sending over the serial data interface.

The CDUC and CDDC reduce serialization/deserialization (SERDES) interface data rates in noncontiguous carrier configurations. This integration also reduces power compared to an equivalent field-programmabel gate array (FPGA)-based implementation.

The CFR engine of the ADRV9042 reduces the peak-to-average ratio (PAR) of the input signal, which enables higher efficiency transmit line ups while reducing the processing load on baseband processors.

The transceiver also contains a fully integrated digital predistortion (DPD) engine for use in power amplifier linearization. The DPD enables the high-efficiency power amplifiers, which reduce system power consumption and the number of SERDES lanes interfacing with the baseband processors. The DPD engine incorporates a dedicated long-term DPD (LT-DPD) block, which provides the support for gallium nitride (GaN) power amplifiers. The ADRV9042 tackles the charge-trapping property of GaN power amplifiers with its LT-DPD block; therefore, improving the emissions and error vector magnitude (EVM). The transceiver includes an ARM Cortex-A55 quad core processor to independently serve DPD, CLGC, and VSWR monitor features. The dedicated processor, together with the DPD engine, provides industry leading DPD performance.

The serial data interface consists of eight serializer and deserializer lanes. The interface supports the JESD204C standards, and both fixed and floating-point data formats are supported. The floating-point format allows internal automatic gain control (AGC) to be transparent to the baseband processor.

The ADRV9042 is powered directly from 0.8 V, 1.0 V, and 1.8 V regulators and is controlled through a standard serial port interface (SPI). The comprehensive power-down modes are included to minimize the power consumption in normal use. The device is packaged in a 27 mm × 20 mm, 736-ball grid array, thermally enhanced (BGA_ED).

SPECIFICATIONS

Electrical characteristics at ambient temperature range; all RF specifications based on measurements that include printed circuit board (PCB) and matching circuit losses, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMITTERS						
Center Frequency		600		7125	MHz	
Large Signal Bandwidth						
				660[1, 2]	MHz	LO frequency ≥ 1200 MHz
				400	MHz	900 MHz ≤ LO frequency ≥ 1200 MHz
				200	MHz	LO frequency ≤ 900 MHz
Synthesis Bandwidth						
				800	MHz	LO frequency ≥ 1200 MHz
				600	MHz	LO frequency < 1200 MHz
Input Data Rate						Supported data rates over JESD: 30.72, 61.44, 122.88, 184.32, 245.76, 368.64, and 491.52
		7.68		491.52	MSPS	CDUC enabled
		61.44		491.52	MSPS	CDUC bypassed
Full-Scale Output Power	P_{OUT}					Continuous wave output power at 0 dBFS, 0 dB transmitter attenuation; 1 MHz tone
850 MHz			5		dBm	
1800 MHz			4.5		dBm	
2600 MHz			4.5		dBm	
3500 MHz			3.5		dBm	
4500 MHz			2.5		dBm	
5600 MHz			2		dBm	
6300 MHz			2		dBm	
7100 MHz			2		dBm	
Flicker Noise						
1 kHz Offset from LO			−137		dBFS/Hz	
P_{OUT} Temperature Slope			−30		mdB/°C	Valid over full power-control range
Power Control Range			32		dB	Signal-to-noise ratio (SNR) maintained for 0 dB to 20 dB RF attenuation
Power Control Resolution			0.05		dB	
Attenuation Accuracy						
			0.1		dB	Valid over full power-control range for any 4 dB step
			±0.04		dB	Monotonic
Phase Change vs. RF Attenuation			3		Degrees	Uncorrected, valid over full power-control range, LO = 3500 MHz
RF Delay Variation with Temperature			1.2		ps/°C	Valid over full power-control range
Peak-to-Peak Gain Deviation						Includes compensation by programmable finite impulse response (FIR) filter, measured with 800 MHz synthesis bandwidth use case
200 MHz RF Bandwidth			0.2		dB	
400 MHz RF Bandwidth			0.4		dB	
660 MHz RF Bandwidth			1		dB	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
800 MHz RF Bandwidth			1.5		dB	
Peak-to-Peak Gain Deviation Narrow Band						
20 MHz RF Bandwidth			0.1		dB	Any 20 MHz bandwidth span within the large signal bandwidth; includes compensation by programmable FIR filter
Deviation from Linear Phase						Measured with 800 MHz synthesis bandwidth use case
100 MHz RF Bandwidth			±1		Degrees	
450 MHz RF Bandwidth			±5		Degrees	
800 MHz RF Bandwidth			±10		Degrees	
Error Vector Magnitude	EVM					Phase-locked loop (PLL) optimized for integrated noise measured using long term evolution (LTE) 20 MHz signal; PLL loop filter bandwidth (LFBW) approximately 500 kHz
850 MHz			0.10		%	
1800 MHz			0.12		%	
2600 MHz			0.26		%	
3500 MHz			0.38		%	
4500 MHz			0.28		%	
5600 MHz			0.52		%	
6300 MHz			0.70		%	
7100 MHz			0.90		%	
Adjacent Channel Leakage Ratio (LTE)	ACLR					20 MHz LTE at −12 dBFS
850 MHz			−67		dBc	
1800 MHz			−67		dBc	
2600 MHz			−67		dBc	
3500 MHz			−65		dBc	
4500 MHz			−62		dBc	
5600 MHz			−60		dBc	
6300 MHz			−57		dBc	
7100 MHz			−57		dBc	
In-Band Noise Floor						In-band noise falls dB for dB with attenuation until limited by the thermal noise floor
0 dB Attenuation			−157		dBFS/Hz	
20 dB Attenuation			−154		dBFS/Hz	
Out-of-Band Noise Floor			−158		dBFS/Hz	0 dB attenuation; 3 × synthesis bandwidth/2 offset
Interpolation Images						
Large Signal Bandwidth			−70		dBc	
Synthesis Bandwidth			−55		dBc	
Second- and Third-Order In-Band Harmonic Distortion	HD2/HD3					−12 dBFS continuous wave signal, HD product falling inside the large signal bandwidth, 30 MHz baseband frequency
850 MHz			−75		dBc	
1800 MHz			−75		dBc	
2600 MHz			−70		dBc	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
3500 MHz			−70		dBc	
4500 MHz			−70		dBc	
5600 MHz			−67		dBc	
6300 MHz			−65		dBc	
7100 MHz			−65		dBc	
Second- and Third-Order Out-of-Band Harmonic Distortion	HD2/HD3					−12 dBFS continuous wave signal, HD product falling outside the large signal bandwidth
850 MHz			−70		dBc	
1800 MHz			−70		dBc	
2600 MHz			−65		dBc	
3500 MHz			−65		dBc	
4500 MHz			−65		dBc	
5600 MHz			−63		dBc	
6300 MHz			−60		dBc	
7100 MHz			−60		dBc	
Third-Order Intermodulation Products	IM3					Two −15 dBFS carriers within the large signal bandwidth
850 MHz			−70		dBc	
1800 MHz			−70		dBc	
2600 MHz			−65		dBc	
3500 MHz			−65		dBc	
4500 MHz			−65		dBc	
5600 MHz			−64		dBc	
6300 MHz			−62		dBc	
7100 MHz			−60		dBc	
Image Rejection						
Within Large-Signal Bandwidth						Quadrature error correction (QEC) active, up to 20 dB of attenuation
			65		dBc	LO < 5000 MHz
			60		dBc	5000 MHz ≤ LO ≤ 6300 MHz
			50		dBc	LO > 6300 MHz
Beyond Large-Signal Bandwidth			40		dBc	Assumes that the distortion power density is 25 dB below the desired power density
Output Impedance	Z_{OUT}		100		Ω	Differential – nominal
Maximum Output Load Voltage Standing Wave Ratio (VSWR)				3		Maximum value to ensure adequate calibration
Output Return Loss			10		dB	
LO Leakage Power						LO leakage (LOL) correction active
Carrier Offset from LO						
850 MHz			−84		dBFS	
1800 MHz			−84		dBFS	
2600 MHz			−84		dBFS	
3500 MHz			−84		dBFS	
4500 MHz			−82		dBFS	
5600 MHz			−82		dBFS	
6300 MHz			−82		dBFS	
7100 MHz			−82		dBFS	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Carrier on LO						
850 MHz			−71		dBFS	
1800 MHz			−71		dBFS	
2600 MHz			−71		dBFS	
3500 MHz			−71		dBFS	
4500 MHz			−71		dBFS	
5600 MHz			−71		dBFS	
6300 MHz			−71		dBFS	
7100 MHz			−71		dBFS	
Spurious-Free Dynamic Range	SFDR		−70		dBc	Within signal bandwidth; −6 dBFS continuous wave signal with 0 dB transmitter attenuation; single LO use case; nonintermodulation related spurs; does not include harmonic distortion, LO leakage, image, interpolation, and converter clock products
RECEIVERS						
Center Frequency		600		7125	MHz	
Signal Bandwidth						
				660[1, 2]	MHz	LO frequency ≥ 1200 MHz
				400	MHz	900 MHz ≤ LO frequency ≤ 1200 MHz
				200	MHz	LO frequency ≤ 900 MHz
Output Data Rate						Supported data rates over JESD: 30.72, 61.44, 122.88, 184.32, 245.76, 368.64, and 491.52
		7.68		491.52	MSPS	CDDC enabled
		61.44		491.52	MSPS	CDDC bypassed
Full-Scale Input Power	P_{FS}					Continuous wave input, produces 0 dBFS; 0 dB receiver attenuation
850 MHz			−11.5		dBm	
1800 MHz			−10.7		dBm	
2600 MHz			−10.4		dBm	
3500 MHz			−9.9		dBm	
4500 MHz			−9.7		dBm	
5600 MHz			−10.0		dBm	
6300 MHz			−9.5		dBm	
7100 MHz			−9.0		dBm	
Attenuation Control						
Gain Range			32		dB	
Analog Gain Step Size			0.5		dB	Attenuator steps from 0 dB to 6 dB
			1		dB	Attenuator steps from 6 dB to 32 dB
Residual Gain Step Error			0.1		dB	Attenuator steps from 0 dB to 20 dB
			0.2		dB	Attenuator steps from 20 dB to 32 dB
Gain Temperature Slope						
LO ≤ 5000 MHz			3		mdB/°C	
LO > 5000 MHz			4		mdB/°C	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Phase Change vs. Receiver Gain						Uncorrected, valid over full gain-control range
850 MHz			3		Degrees	
1800 MHz			6		Degrees	
2600 MHz			9		Degrees	
3500 MHz			12		Degrees	
4500 MHz			16		Degrees	
5600 MHz			19		Degrees	
6300 MHz			22		Degrees	
7100 MHz			25		Degre63	
RF Delay Variation with Temperature			1		ps/°C	Valid over full gain-control range
Peak-to-Peak Gain Deviation						Over signal bandwidth, includes compensation by programmable FIR filter
200 MHz RF Bandwidth			1		dB	
400 MHz RF Bandwidth			1		dB	
660 MHz RF Bandwidth			1		dB	
Receiver Decimation Image Rejection		80			dB	Due to digital filters
Receiver Alias Band Rejection			70		dB	Rejection of signals within the ADC alias band
Input Impedance	Z_{IN}		100		Ω	Differential
Maximum Source VSWR				3		
Input Port Return Loss			10		dB	
Receiver Input LO Leakage at Maximum Gain						Leakage decreases dB for dB with attenuation over full attenuation range
850 MHz			−70		dBm	
1800 MHz			−65		dBm	
2600 MHz			−65		dBm	
3500 MHz			−65		dBm	
4500 MHz			−65		dBm	
5600 MHz			−65		dBm	
6300 MHz			−60		dBm	
7100 MHz			−75		dBm	
Image Rejection			−75		dBc	QEC active up to −1 dBFS
Noise Spectral Density	N_0					Offset = 40 MHz, spot
850 MHz			−151.7		dBFS/Hz	
1800 MHz			−151.5		dBFS/Hz	
2600 MHz			−151.1		dBFS/Hz	
3500 MHz			−150.5		dBFS/Hz	
4500 MHz			−150.7		dBFS/Hz	
5600 MHz			−150.3		dBFS/Hz	
6300 MHz			−149.7		dBFS/Hz	
7100 MHz			−149.5		dBFS/Hz	
Noise Figure						0 dB attenuation
850 MHz			10.5		dB	
1800 MHz			11.8		dB	
2600 MHz			12.5		dB	
3500 MHz			13.5		dB	
4500 MHz			13.8		dB	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
5600 MHz			14.0		dB	
6300 MHz			14.5		dB	
7100 MHz			15.0		dB	
Noise Figure Ripple					dB	Peak-to-peak deviation in noise figure over large signal bandwidth
200 MHz RF Bandwidth			1		dB	
400 MHz RF Bandwidth			1.5		dB	
660 MHz RF Bandwidth			2		dB	
Second-Order Harmonic Distortion	HD2					HD2 products occurring anywhere in-band
200 MHz RF Bandwidth			−76		dBc	−3.5 dBFS continuous wave signal
400 MHz RF Bandwidth			−75		dBc	−2.5 dBFS continuous wave signal
660 MHz RF Bandwidth			−73		dBc	−1 dBFS continuous wave signal
Third-Order Harmonic Distortion	HD3					HD3 products occurring on band-edge
200 MHz RF Bandwidth			−72		dBc	−2.5 dBFS continuous wave signal, 600 MHz < LO < 1200 MHz
			−70		dBc	−1 dBFS continuous wave signal, LO ≥ 1200 MHz
400 MHz RF Bandwidth			−67		dBc	− 2.5 dBFS continuous wave signal, LO < 1200 MHz
			−64		dBc	−1 dBFS continuous wave signal, LO ≥ 1200 MHz
660 MHz RF Bandwidth			−59		dBc	−1 dBFS continuous wave signal, LO < 2200 MHz
			−60		dBc	−1 dBFS continuous wave signal, LO ≥ 2200 MHz
Fourth-Order Harmonic Distortion	HD4		−90		dBc	−1 dBFS continuous wave signal, HD4 products occurring anywhere in-band
Fifth-Order Harmonic Distortion	HD5					HD5 products occurring on band-edge
200 MHz RF Bandwidth			−80		dBc	−3.5 dBFS continuous wave signal
400 MHz RF Bandwidth			−80		dBc	−2.5 dBFS continuous wave signal
660 MHz RF Bandwidth			−79		dBc	−1 dBFS continuous wave signal
Second-Order Intermodulation Products	IM2					
850 MHz			−77		dBc	Two continuous wave tones at −8.5 dBFS, 200 MHz signal bandwidth
1800 MHz			−77		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth
2600 MHz			−77		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth
3500 MHz			−77		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth
4500 MHz			−77		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth
5600 MHz			−77		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth
6300 MHz			−76		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth
7100 MHz			−76		dBc	Two continuous wave tones at −7 dBFS, 660 MHz signal bandwidth

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Third-Order Intermodulation Products	IM3					
850 MHz			−66		dBc	Two continuous wave tones at −9.5 dBFS, 200 MHz signal bandwidth
1800 MHz			−60		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
2600 MHz			−61		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
3500 MHz			−61		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
4500 MHz			−61		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
5600 MHz			−61		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
6300 MHz			−58		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
7100 MHz			−58		dBc	Two continuous wave tones at −7 dBFS, 600 MHz signal bandwidth
Receiver Band Spurs Referenced to RF Input at Maximum Gain			−95		dBm	TDD mode; no more than one spur at this level per 10 MHz of receiver bandwidth; excludes converter clock spurs; no input signal applied; non-IoT
Spurious-Free Dynamic Range	SFDR		−70		dBc	Within signal bandwidth; single LO; −1 dBFS input; nonintermodulation related spurs; does not include harmonic distortion
OBSERVATION RECEIVERS						Measurement are taken with 5898.25 MHz sampling frequency for less than 5 GHz frequency and 7863.42 MHz sampling frequency for greater than 5 GHz frequency
Center of Input Frequency Range		600		7125	MHz	
Signal Bandwidth						
				800	MHz	LO frequency > 1200 MHz
				600	MHz	LO frequency ≤ 1200 MHz
Output Data Rate		122.88		983.04	MSPS	Supported data rates: 122.88 MSPS, 184.32 MSPS, 245.76 MSPS, 368.64 MSPS, 491.52 MSPS, 737.28 MSPS, and 983.04 MSPS
Maximum Observation Receiver Input Power				16	dBm	Specified at the pin, peak power for modulated signals with a peak to average ratio (PAR) ≥ 7 dB; For continuous wave, it is reduced to 10 dBm
Full-Scale Input Power	P_{FS}					Continuous wave input power, which produces 0 dBFS; 0 dB observation receiver attenuation; no external attenuator
850 MHz			5.5		dBm	
1800 MHz			5.3		dBm	
2600 MHz			6.1		dBm	
3500 MHz			7.5		dBm	
4500 MHz			7.5		dBm	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
5600 MHz			8		dBm	
6300 MHz			10		dBm	
7100 MHz			11		dBm	
Gain Range			16		dB	Limited by maximum input power of 16 dBm at device under test (DUT) input pins
Gain Step			1		dB	
Peak-to-Peak Gain Deviation						Within signal bandwidth, includes compensation by programmable FIR filter
200 MHz RF Bandwidth			0.4		dB	
400 MHz RF Bandwidth			0.6		dB	
600 MHz RF Bandwidth			0.8		dB	
800 MHz RF Bandwidth			1		dB	
Peak-to-Peak Gain Deviation Narrow Band						
20 MHz RF Bandwidth			0.1		dB	Any 20 MHz bandwidth span within the large signal bandwidth; includes compensation by programmable FIR filter
Deviation from Linear Phase			±2		Degrees	800 MHz RF bandwidth
Input Impedance	Z_{IN}		100		Ω	Differential
Input Source VSWR				3		
Input Port Return Loss			10		dB	
Third-Order Intermodulation Product	IM3					Two tones; each at −13 dBFS, ORx attenuation ≤ 12 dB is recommended to achieve performance
LO < 5000 MHz			−70		dBc	
LO ≥ 5000 MHz to < 6000 MHz			−65		dBc	
LO ≥ 6000 MHz			−62		dBc	
Second-Order Harmonic Distortion	HD2					0 dB observation receiver attenuation, ORx attenuation ≤ 12 dB recommended to achieve performance
LO < 5000 MHz						
−1 dBFS			−51		dBc	
−10 dBFS			−60		dBc	
LO ≥ 5000 MHz						
−1 dBFS			−46		dBc	
−10 dBFS			−55		dBc	
Third-Order Harmonic Distortion	HD3					0 dB observation receiver attenuation, ORx attenuation ≤ 12 dB recommended to achieve performance
LO < 5000 MHz						
−1 dBFS			−52		dBc	
−10 dBFS			−70		dBc	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LO ≥ 5000 MHz						
−1 dBFS			−47		dBc	
−10 dBFS			−65		dBc	
Spurious-Free Dynamic Range	SFDR		−65		dBFS	Within signal bandwidth; −10 dBFS input; nonintermodulation related spurs; does not include harmonic distortion; limited by continuous wave spur at N × sampling frequency (f_S)/4
			−70		dBFS	Within signal bandwidth; −10 dBFS input; nonintermodulation related spurs; does not include harmonic distortion; does not include f_S/4 spur, limited by clock spurs at input frequency (f_{IN}) ± f_S/4
			−75		dBFS	−10 dBFS input; not including clock spurs at f_{IN} ± f_S/4
Noise Spectral Density	N_0					0 dB observation receiver attenuation; tone power −20 dBFS or lower
2949.12 MHz Sampling Frequency			−144		dBFS/Hz	
3932.16 MHz Sampling Frequency			−145		dBFS/Hz	
5898.24 MHz Sampling Frequency			−147		dBFS/Hz	
7864.32 MHz Sampling Frequency			−148		dBFS/Hz	
CHANNEL TO CHANNEL ISOLATION						
Tx to Tx Isolation						
850 MHz			75		dB	
1800 MHz			75		dB	
2600 MHz			69		dB	
3500 MHz			67		dB	
4500 MHz			66		dB	
5600 MHz			65		dB	
6300 MHz			65		dB	
7100 MHz			63		dB	
Tx to Rx Isolation						
850 MHz			70		dB	
1800 MHz			70		dB	
2600 MHz			65		dB	
3500 MHz			63		dB	
4500 MHz			61		dB	
5600 MHz			60		dB	
6300 MHz			60		dB	
7100 MHz			60		dB	
Tx to ORx Isolation						
850 MHz			75		dB	
1800 MHz			75		dB	
2600 MHz			74		dB	
3500 MHz			70		dB	
4500 MHz			67		dB	
5600 MHz			65		dB	
6300 MHz			65		dB	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
7100 MHz			65		dB	
Rx to Rx Isolation						
850 MHz			75		dB	
1800 MHz			75		dB	
2600 MHz			75		dB	
3500 MHz			63		dB	
4500 MHz			62		dB	
5600 MHz			60		dB	
6300 MHz			60		dB	
7100 MHz			60		dB	
Rx to ORx Isolation						
850 MHz			75		dB	
1800 MHz			75		dB	
2600 MHz			75		dB	
3500 MHz			75		dB	
4500 MHz			70		dB	
5600 MHz			70		dB	
6300 MHz			70		dB	
7100 MHz			70		dB	
ORx to ORx Isolation						
850 MHz			75		dB	
1800 MHz			75		dB	
2600 MHz			75		dB	
3500 MHz			75		dB	
4500 MHz			75		dB	
5600 MHz			75		dB	
6300 MHz			75		dB	
7100 MHz			75		dB	
LO SYNTHESIZER (LO)						
LO Spectral Purity			−80		dBc	TDD mode; not including integer boundary spurs
LO Path Delay Slope vs. Temperature			1.2		ps/°C	Half a VCO cycle worst-case
Integrated Phase Noise—Wide Band						Integrated from 1 kHz to 50 MHz; PLL bandwidth optimized for integrated phase noise; PLL LFBW approximately 500 kHz
850 MHz			0.03		°RMS	
1800 MHz			0.06		°RMS	
2600 MHz			0.1		°RMS	
3500 MHz			0.13		°RMS	
4500 MHz			0.19		°RMS	
5600 MHz			0.23		°RMS	
6300 MHz			0.46		°RMS	
7100 MHz			0.50		°RMS	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Spot Phase Noise—Wide Band						PLL bandwidth optimized for integrated phase noise; PLL LFBW approximately 500 kHz
850 MHz						
100 kHz Offset			−127		dBc/Hz	
1 MHz Offset			−139		dBc/Hz	
10 MHz Offset			−160		dBc/Hz	
1800 MHz						
100 kHz Offset			−115.9		dBc/Hz	
1 MHz Offset			−133.5		dBc/Hz	
10 MHz Offset			−156.5		dBc/Hz	
2600 MHz						
100 kHz Offset			−116.6		dBc/Hz	
1 MHz Offset			−126		dBc/Hz	
10 MHz Offset			−151.7		dBc/Hz	
3500 MHz						
100 kHz Offset			−114.2		dBc/Hz	
1 MHz Offset			−126.6		dBc/Hz	
10 MHz Offset			−151		dBc/Hz	
4500 MHz						
100 kHz Offset			−111		dBc/Hz	
1 MHz Offset			−121.8		dBc/Hz	
10 MHz Offset			−148.4		dBc/Hz	
5600 MHz						
100 kHz Offset			−110		dBc/Hz	
1 MHz Offset			−119		dBc/Hz	
10 MHz Offset			−146		dBc/Hz	
6300 MHz						
100 kHz Offset			−108		dBc/Hz	
1 MHz Offset			−117		dBc/Hz	
10 MHz Offset			−144		dBc/Hz	
7100 MHz						
100 kHz Offset			−105		dBc/Hz	
1 MHz Offset			−114		dBc/Hz	
10 MHz Offset			−142		dBc/Hz	
Spot Phase Noise—Narrow Band						PLL bandwidth optimized to minimize phase noise at >200 kHz; PLL LFBW approximately 70 kHz; numbers met for DEVCLKx ≥ 122.88 MHz
900 MHz						
100 kHz Offset			−114		dBc/Hz	
200 kHz Offset			−125		dBc/Hz	
250 kHz Offset			−128		dBc/Hz	
400 kHz Offset			−134		dBc/Hz	
600 kHz Offset			−139		dBc/Hz	
1 MHz Offset			−144		dBc/Hz	
1.2 MHz Offset			−146		dBc/Hz	
1.8 MHz Offset			−150		dBc/Hz	
6 MHz Offset			−158		dBc/Hz	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
10 MHz Offset			−160		dBc/Hz	
1800 MHz						
100 kHz Offset			−109		dBc/Hz	
200 kHz Offset			−118		dBc/Hz	
250 kHz Offset			−121		dBc/Hz	
400 kHz Offset			−127		dBc/Hz	
600 kHz Offset			−132		dBc/Hz	
1 MHz Offset			−138		dBc/Hz	
1.2 MHz Offset			−140		dBc/Hz	
1.8 MHz Offset			−144		dBc/Hz	
6 MHz Offset			−154		dBc/Hz	
10 MHz Offset			−156		dBc/Hz	
2600 MHz						
100 kHz Offset			−100		dBc/Hz	
1 MHz Offset			−130		dBc/Hz	
10 MHz Offset			−150		dBc/Hz	
3500 MHz						
100 kHz Offset			−90		dBc/Hz	
1 MHz Offset			−123		dBc/Hz	
10 MHz Offset			−148		dBc/Hz	
4500 MHz						
100 kHz Offset			−95		dBc/Hz	
1 MHz Offset			−128		dBc/Hz	
10 MHz Offset			−150		dBc/Hz	
5600 MHz						
100 kHz Offset			−92		dBc/Hz	
1 MHz Offset			−124		dBc/Hz	
10 MHz Offset			−146		dBc/Hz	
6300 MHz						
100 kHz Offset			TBD		dBc/Hz	
1 MHz Offset			TBD		dBc/Hz	
10 MHz Offset			TBD		dBc/Hz	
7100 MHz						
100 kHz Offset			TBD		dBc/Hz	
1 MHz Offset			TBD		dBc/Hz	
10 MHz Offset			TBD		dBc/Hz	
EXTERNAL LO INPUT						
Input Frequency		3.55		12	GHz	
Input Signal Power		0		6	dBm	
Allowable Input Signal Differential Phase Imbalance		−15		+15	degree	To ensure adequate quadrature error correction
Allowable Input Signal Differential Amplitude Imbalance				1.5	dB	
Input Signal Duty Cycle Error				2.5	%	
Input Impedance			100		Ω	On-chip AC coupling is provided
Supported LO Divider Ratio						Frequency division ratio of external LO to mixer, only powers of two supported; Tx LO range between 3.0 Ghz to 3.55 GHz is not currently

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
						supported when using external LO input for Tx LO source
Tx LO ≤ 3.00 GHz		4		32		
Tx LO ≥ 3.55 GHz		2		2		
Rx		2		32		
CLOCK SYNTHESIZER						
Integrated Phase Noise—Wide Band						1 kHz to 100 MHz, PLL bandwidth optimized for low jitter (491.52 MHz phase/frequency detector (f_{PFD})).
2949.12 MHz Sample Clock			0.13		°RMS	
3932.16 MHz Sample Clock			0.15		°RMS	
Integrated Phase Noise—Narrow Band						1 kHz to 10 MHz, PLL bandwidth optimized for low phase noise at > 800 kHz
2949.12 MHz Sample Clock			0.82		°RMS	
3932.16 MHz Sample Clock			0.87		°RMS	
Spot Phase Noise—Wide Band						1 kHz to 100 MHz, PLL bandwidth optimized for low jitter (491.52 MHz f_{PFD})
2949.12 MHz Sample Clock						
100 kHz Offset			−115.7		dBc/Hz	
1 MHz Offset			−122.6		dBc/Hz	
10 MHz Offset			−150.6		dBc/Hz	
3932.16 MHz Sample Clock						
100 kHz Offset			−111.3		dBc/Hz	
1 MHz Offset			−123.6		dBc/Hz	
10 MHz Offset			−148.5		dBc/Hz	
Spot Phase Noise—Narrow Band						1 kHz to 10 MHz, PLL bandwidth optimized for low phase noise at > 800 kHz
2949.12 MHz Sample Clock						
100 kHz Offset			−95.5		dBc/Hz	
800 kHz Offset			−125		dBc/Hz	
1 MHz Offset			−127.7		dBc/Hz	
3 MHz Offset			−139.8		dBc/Hz	
10 MHz Offset			−150.8		dBc/Hz	
3932.16 MHz Sample Clock						
100 kHz Offset			−95.6		dBc/Hz	
800 kHz Offset			−125.4		dBc/Hz	
1 MHz Offset			−127.5		dBc/Hz	
3 MHz Offset			−138.1		dBc/Hz	
10 MHz Offset			−148.4		dBc/Hz	
REFERENCE CLOCK (DEVCLK_IN SIGNAL)						
Frequency Range		61.44		491.52	MHz	
Slew Rate		1.5			V/ns	
Signal Level (Differential)		0.35		1.9	V p-p	AC-coupled, common-mode voltage internally supplied; for best spurious performance and to meet the specified PLL performance

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
						parameters, use a 1.9 V p-p input clock
Input Impedance			100		Ω	Needs external AC coupling
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)						
Logic Compliance			LVDS			Alternative signal formats, such as low voltage positive emitter coupled logic (LVPECL), can be supported through the use of external components, as long as they adhere to the specification and maximum pin voltage limits
Differential Input Voltage	V_{OD}	0.5	0.7	0.9	V p-p	DC-coupled low voltage differential signaling (LVDS)
Input Common Mode Voltage	V_{OC}	1.125		1.375	V	Common-mode supplied by LVDS driver
Input Resistance (Differential)			48		kΩ	
Input Capacitance (Differential)			1		pF	
Input Offset Range		30		220	mV	Programmable input offset used to prevent SYSREF toggling if LVDS driver has been turned off
Device Clock to SYSREF Setup Time		320			ps	
Device Clock to SYSREF Hold Time		180			ps	
DIGITAL SPECIFICATIONS (COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR (CMOS))						
Logic Inputs						
Input Voltage						
High Level		VIF × 0.65		VIF + 0.18	V	Power supply specifications shown in Table 2
Low Level		−0.30		VIF × 0.35	V	
Input Current						
High Level		−10		+10	μA	
Low Level		−10		+10	μA	
Logic Outputs						
Output Voltage						
High Level		(VIF × 0.95) – 0.45			V	2 mA drive current at default drive strength
		(VIF × 0.95) – 0.11			V	0.5 mA drive current at default drive strength
		VIF x 0.95			V	<20 μA drive current at default drive strength
Low Level				0.45	V	
Drive Capability			2		mA	
DIGITAL SPECIFICATIONS (LVDS)						
Logic Inputs						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled
Logic Outputs						
Output Voltage						

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
High				1375	mV	
Low		1025			mV	
Differential			225		mV	
Offset			1200		mV	
DIGITAL SPECIFICATIONS (GPIO_ANA)						
Logic Inputs						
Input Voltage						
High Level		VDDA_1P8 × 0.65		VDDA_1P8 + 0.18	V	Power supply specifications shown in Table 2
Low Level		−0.30		VDDA_1P8 × 0.35	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		(VDDA_1P8 × 0.95) – 0.45			V	2 mA drive current at default drive strength
		(VDDA_1P8 × 0.95) – 0.11			V	0.5 mA drive current at default drive strength
		VDDA_1P8 x 0.95			V	<20 µA drive current at default drive strength
Low Level				0.45	V	
Drive Capability			2		mA	

[1] Maximum bandwidth supported in CDUC/CDDC bypass mode is 400 MHz instantaneous bandwidth/occupied bandwidth (iBW/oBW).

[2] Maximum bandwidth supported in CDUC/CDDC enabled mode is 660 MHz/400 MHz iBW/oBW.

Figure 2 shows the LVDS input levels for SYSREF.

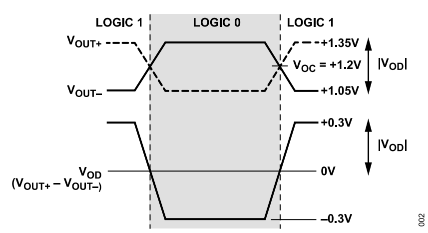

Figure 2. LVDS Input Levels for SYSREF

SPECIFICATIONS

POWER SUPPLY SPECIFICATIONS

Table 2. Power Supply Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CHARACTERISTICS						
VDIG_0P8 Supply		0.76	0.8	0.84	V	±5%
VDDA_1P0 Supply		0.975	1	1.025	V	±2.5%
VDDA_1P8 Supply		1.71	1.8	1.89	V	±5%
VIF Supply		1.71	1.8	1.89	V	±5%

DIGITAL INTERFACE AND TIMING SPECIFICATIONS

Table 3. Digital Interface and Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL PERIPHERAL INTERFACE (SPI) TIMING						
Write SPI_CLK Period	t_{CP}	20			ns	
SPI_CLK High Pulse Width	t_{MP}	5			ns	
SPI_EN Setup to First SPI_CLK Rising Edge	t_{SC}	0.5			ns	
Last SPI_CLK Falling Edge to SPI_EN Hold	t_{HC}	0.5			ns	
SPI_DIO Data Input Setup to SPI_CLK	t_S	1			ns	
SPI_DIO Data Input Hold to SPI_CLK	t_H	1			ns	
SPI_CLK Falling Edge to Output Data Delay	t_{CO}	4		6	ns	3- or 4-wire mode
Bus Turnaround Time After Baseband Processor Drives Last Address Bit	t_{HZM}	$t_{CO\ MIN}$		$t_{CO\ MAX}$	ns	3-wire mode
Bus Turnaround Time After Transceiver Drives Last Data Bit (Must be in Terms of Baseband Processor)	t_{HZS}	$t_{CO\ MIN}$		$t_{CO\ MAX}$	ns	3-wire mode
DIGITAL TIMING						
TRXx_CTRL Pulse Width		10[1]			µs	
ORX_CTRL_x Pulse Width		10[1]			µs	
TRXx_CTRL to Valid Data			2[2]		µs	
ORX_CTRL_x to Valid Data			1.5		µs	
JESD204B/JESD204C DATA OUTPUT TIMING						
Unit Interval	UI	41.1		407	ps	
Data Rate per Channel (Nonreturn to Zero (NRZ))						
JESD204B		4915.2		14745.6	Mbps	
JESD204C		4055.04		24330.24	Mbps	
Rise Time	t_R	17	26		ps	20% to 80% in 100 Ω load
Fall Time	t_F	17	26		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Differential Output Voltage	V_{DIFF}	360	466	1000	mV p-p	Differential
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	
Differential Termination Impedance	Z_{RDIFF}	80	100	120	Ω	

SPECIFICATIONS

Table 3. Digital Interface and Timing Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
JESD204B/JESD204C DATA INPUT TIMING						
Unit Interval	UI	41.1		407	ps	
Data Rate per Channel (NRZ)						
JESD204B		4915.2		14745.6	Mbps	
JESD204C		4055.04		24330.24	Mbps	
Input Common-Mode Voltage	V_{CM}	0.05		1.65	V	AC-coupled
Differential Input Voltage	V_{DIFF}	125		1000	mV p-p	Differential
Differential Termination Impedance	Z_{RDIFF}	80	106	120	Ω	

[1] The pulse width mentioned is for digital timing. For calibrations to run, the minimum Tx_ENABLE and ORx_ENABLE pulse with must be 17 µs and Rx_ENABLE pulse width must be 35 µs.

[2] Minimum time for sending data from field programmable gate array (FPGA) after Tx_EN and Rx_EN are applied.

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
VDDA_1P8 to VSSA	−0.2 V to +1.98 V
VDIG_0P8 to VSSD, VSSA	−0.2 V to +1.05 V
VDDA_1P0 to VSSA	−0.2 V to see Table 8
VIF Referenced Logic Inputs and Outputs to VSSD	−0.3 V to VIF + 0.3 V
JESD204B/JESD204C Logic Outputs to VSSA	−0.2 V to +1.1 V
JESD204B/JESD204C Logic Inputs to VSSA	−0.2 V to +1.1 V
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into Receiver Ports	For limits vs. survival time, see Table 7
Maximum Input Power into Observation Receiver Port	20 dBm[1]
Junction Temperature Range	−40°C to +125°C[2]
Junction Temperature Range for Continuous Operation	−40°C to +110°C
Storage Temperature Range	−65°C to +150°C

1 For modulated signals with PAR ≥ 7 dB and observation receiver attenuation ≥ 6 dB. For lower attenuation, the max rating decreases dB to dB. For continuous wave, it is 14 dBm for all observation receiver attenuations.

2 Operation up to 125°C is supported, but specification compliance is only guaranteed up to 110°C. Operation above 110°C can impact device operating lifetime. To avoid a reduction in operating lifetime by operating above 110°C, the device must operate at a temperature below 110°C for a period. Use the following equation to calculate lifetime: Lifetime = $(\Sigma(time_T \times AF_T) \times 10)$, where: $time_T$ refers to time spent at discrete temperatures on Table 6 in terms of duty cycle, and AF_T are acceleration factors taken from Table 5. Note that the maximum lifetime is 10 years.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 5. Acceleration Factors for High Temperature Operation

Operating Junction Temperature (°C)	Acceleration Factor (AF)
125	3.32
120	2.25
115	1.51
110	1
105	0.89
100	0.79
95	0.70
90	0.62
85	0.56
80	0.48

The following example shows how the equation and the acceleration factor values are used to understand whether operating lifetime is degraded or not. An example scenario is shown in Table 6, which indicates the time that the device spends on a certain junction temperature with a duty cycle.

Table 6. Example Scenario to Estimate Impact of Accelerating Factor on Lifetime

Operating Junction Temperature (°C)	Duty Cycle
125	0.05 (5%)
120	0.1 (10%)
95	0.4 (40%)
90	0.45 (45%)

With values from Table 5 and Table 6, the condition for operating lifetime of 10 years is satisfied and there is no degradation:

$$20 - (((0.05 \times 3.32) + (0.1 \times 2.25) + (0.4 \times 0.70) + (0.45 \times 0.62)) \times 10) = 10.5$$

To the extent that the customer operates the hardware under the condition $T_J > 110°C$, the customer represents and warrants that they first consult with an Analog Devices field representative. To support any failure analysis made by Analog Devices, the customer further warrants that it provides relevant historical logs, reasonably requested by Analog Devices. In the absence of relevant historical logs being made available by the customer, Analog Devices determines at its sole discretion by analyzing various technical indicators whether or not the customer has operated the device within guidance mentioned in footnote 2.

Analog Devices represents and warrants that performance of its hardware products meets its provided specifications, only to the extent that the customer has operated the device as per footnote 2 and in accordance with Analog Devices' standard warranty. If the customer operates the hardware beyond the lifetime determined as per footnote 2, Analog Devices does not warrant that the hardware operates as expected, operate without malfunction, damage, or failure, or perform in a manner consistent with its provided specifications. In such circumstances, Analog Devices further assumes no liability for the hardware's operation.

Table 7. Maximum Input Power into Receiver Ports vs. Lifetime

RF Port Input Power (Continuous Wave Signal)	Lifetime	
	ATTEN = 32 dB	ATTEN = 0 dB
7 dBm	>10 years	>10 years
10 dBm	>10 years	>10 years
20 dBm	>10 years	70 hours
21 dBm	>10 years	24 hours
24 dBm	>10 years	24 hours

ABSOLUTE MAXIMUM RATINGS

Table 8. VDDA_1P0 Voltage vs. Duty Cycle to Maintain 10-Year Lifetime

VDDA_1P0 (V)	Required Duty Cycle to Maintain 10 Year Lifetime (%)
1	100.0
1.01	100.0
1.02	100.0
1.03	100.0
1.04	100.0
1.05	98.8
1.06	66.5
1.07	45.0
1.08	30.5
1.09	20.7
1.1	14.2
1.11	9.7
1.12	6.7
1.13	4.6
1.14	3.2
1.15	2.2
1.16	1.5
1.17	1.1
1.18	0.8
1.19	0.5
1.2	0.4

REFLOW PROFILE

The transceiver reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal resistance values specified in Table 9 are calculated based on JEDEC specs (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 9. Thermal Resistance Values

Package Type	θ_{JA} (°C/W)	$\theta_{JC\ TOP}$ (°C/W)	θ_{JB} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)
BP-736-2	8.98	0.29	2.01	0.24	1.92

Note: Using enhanced heat removal (PCB, heatsink, airflow, etc.) techniques, improve the thermal resistance values.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human Body Model (HBM) as per ANSI/ESDA/JEDDEC JS-001.
Charged Device Model (CDM) as per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRV9042

Table 10. ADRV9042, 736-Ball BGA_ED

ESD Model	Withstand Threshold (V)	Class
HBM	±1000	1B
CDM	±165[1]	C0B

[1] All pins except transmitter channel pins and EXT LO pins rated at ±250 V CDM classification test level (Class C1).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

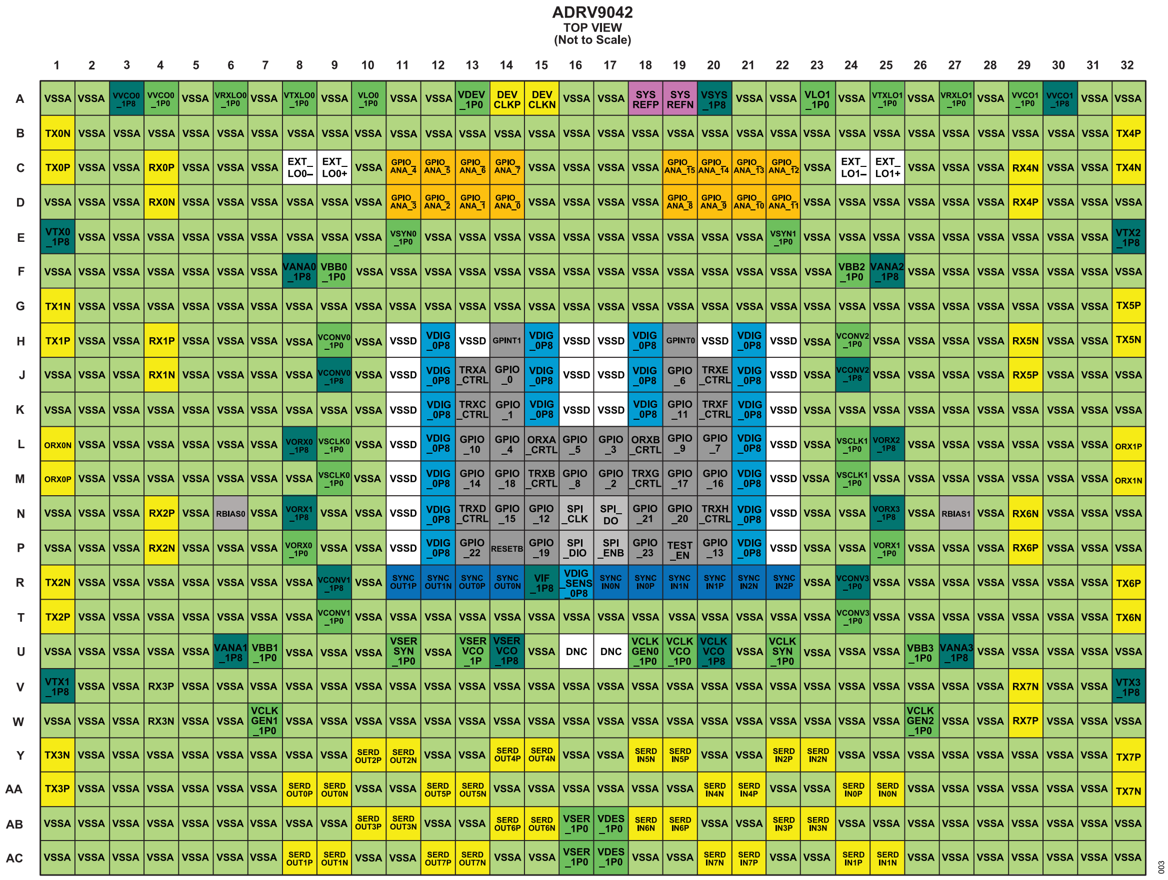

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, A2, A5, A7, A9, A11, A12, A16, A17, A21, A22, A24, A26, A28, A31, A32, B2 to B31, C2, C3, C5 to C7, C10, C15 to C18, C23, C26 to C28, C30 to C31, D1, D2, D3, D5 to D10, D15 to D18, D23 to D28, D30 to D32, E2 to E10, E12 to E21, E23 to E31, F1 to F7, F10 to F23, F26 to F32, G2 to G31, H2, H3, H5 to H8, H10, H23, H25 to H28, H30, H31, J1 to J3, J5 to J8, J10, J23, J25 to J28, J30 to J32, K1 to K10, K23 to K32, L2 to L7, L26 to L31, M2 to M8, M25 to M31, N1 to N3, N5, N7, N9, N10, N23, N24, N26, N28, N30 to N32, P1 to P3, P5 to P7, P9, P10, P23, P24, P26 to P28, P30 to P32, R2 to R8, R10, R23, R25 to R31, T2 to T8, T10 to T23, T25 to T31, U1 to U5, U8 to U10, U12, U15, U21, U23 to U25, U28 to U32, V2, V3, V5 to V28, V30, V31, W1 to W3, W5, W6, W8 to W25, W27, W28, W30 to W32, Y2 to Y9, Y12, Y13, Y16, Y17, Y20, Y21, Y24 to Y31, AA2 to AA7, AA10, AA11, AA14 to AA19, AA22, AA23, AA26 to AA31, AB1 to AB9, AB12, AB13, AB20, AB21, AB24 to AB32, AC1	VSSA	I	Analog Ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
to AC7, AC10, AC11, AC14, AC15, AC18, AC19, AC22, AC23, AC26 to AC32			
L10, M10	VSSA	I	Analog Ground. Return pin for VSCLK0_1P0, connect decoupling capacitor between L9, M9, and L10, M10.
L23, M23	VSSA	I	Analog Ground. Return pin for VSCLK1_1P0, connect decoupling capacitor between L23, M23, and L24, M24.
A3	VVCO0_1P8	I	1.8 V Supply Voltage. Requires local bypass to ground.
A4	VVCO0_1P0	O	1.0 V Internal Supply Node. Bypass this pin with a 4.7 µF ceramic capacitor.
A30	VVCO1_1P8	I	1.8 V Supply Voltage. Requires local bypass to ground.
A29	VVCO1_1P0	O	1.0 V Internal Supply Node. Bypass this pin with a 4.7 µF ceramic capacitor.
A6	VRXLO0_1P0	I	1.0 V Supply Voltage.
A8	VTXLO0_1P0	I	1.0 V Supply Voltage.
A10	VLO0_1P0	I	1.0 V Supply Voltage.
A23	VLO1_1P0	I	1.0 V Supply voltage.
A25	VTXLO1_1P0	I	1.0 V Supply Voltage.
A27	VRXLO1_1P0	I	1.0 V Supply Voltage.
B1, C1	TX0N, TX0P	O	Differential Output for Transmitter Channel 0. Do not connect if unused.
C8, C9	EXT_LO0−, EXT_LO0+	I	Differential External LO Input 0. Do not connect if unused.
C24, C25	EXT_LO1−, EXT_LO1+	I	Differential External LO Input 1. Do not connect if unused.
B32, C32	TX4P, TX4N	O	Differential Output for Transmitter Channel 4. Do not connect if unused.
C4, D4	RX0P, RX0N	I	Differential Input for Receiver Channel 0. Do not connect if unused.
F8	VANA0_1P8	I	1.8 V Supply Voltage.
F9	VBB0_1P0	I	1.0 V Supply Voltage.
U7	VBB1_1P0	I	1.0 V Supply Voltage.
F24	VBB2_1P0	I	1.0 V Supply Voltage.
U26	VBB3_1P0	I	1.0 V Supply Voltage.
U6	VANA1_1P8	I	1.8 V Supply Voltage.
F25	VANA2_1P8	I	1.8 V Supply Voltage.
U27	VANA3_1P8	I	1.8 V Supply Voltage.
C29, D29	RX4N, RX4P	I	Differential Input for Receiver Channel 4. Do not connect if unused.
D14, D13, D12, D11, C11, C12, C13, C14, D19, D20, D21, D22, C22, C21, C20, C19	GPIO_ANA_0, GPIO_ANA_1, GPIO_ANA_2, GPIO_ANA_3, GPIO_ANA_4, GPIO_ANA_5, GPIO_ANA_6, GPIO_ANA_7, GPIO_ANA_8, GPIO_ANA_9, GPIO_ANA_10, GPIO_ANA_11, GPIO_ANA_12, GPIO_ANA_13, GPIO_ANA_14, GPIO_ANA_15	I/O	General-Purpose Inputs and Outputs Referenced to 1.8 V. If unused, these pins can be connected to VSSA with a 10 kΩ resistor or configured as outputs, driven low, and left disconnected.
E11	VSYN0_1P0	I	1.0 V Supply Voltage.
A14, A15	DEVCLKP, DEVCLKN	I	Device Clock Differential Input.
E22	VSYN1_1P0	I	1.0 V Supply Voltage.
G1, H1	TX1N, TX1P	O	Differential Output for Transmitter Channel 1. Do not connect if unused.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
A13	VDEV_1P0	I	1.0 V Supply Voltage.
A20	VSYS_1P8	I	1.8 V Supply Voltage.
G32, H32	TX5P, TX5N	O	Differential Output for Transmitter Channel 5. Do not connect if unused.
H4, J4	RX1P, RX1N	I	Differential Input for Receiver Channel 1. Do not connect if unused.
A18, A19	SYSREFP, SYSREFN	I	LVDS System Reference Clock Inputs for the SERDES Interface.
H29, J29	RX5N, RX5P	I	Differential Input for Receiver Channel 5. Do not connect if unused.
H9	VCONV0_1P0	I	1.0 V Supply Voltage.
J13, K13, N13, M15, M18, J20, K20, N20	TRXA_CTRL, TRXC_CTRL, TRXD_CTRL, TRXB_CTRL, TRXG_CTRL, TRXE_CTRL, TRXF_CTRL, TRXH_CTRL	I	Transceiver Control Pins.
J14, K14, M17, L17, L14, L16, J19, L20, M16, L19, L13, K19, N15, P20, M13, N14, M20, M19, M14, P15, N19, N18, P13, P18	GPIO_0 to GPIO_23	I/O	General-Purpose Digital Inputs and Outputs. See Figure 3 to match the ball location to the GPIO_n signal name. If unused, these pins can be connected to VSSD with a 10 kΩ resistor or configured as outputs, driven low, and left disconnected.
H24	VCONV2_1P0	I	1.0 V Supply Voltage.
J9	VCONV0_1P8	I	1.8 V Supply Voltage.
J24	VCONV2_1P8	I	1.8 V Supply Voltage.
L1, M1	ORX0N, ORX0P	I	Differential Input for Observation Receiver Channel 0. Do not connect if unused
L8	VORX0_1P8	I	1.8 V Supply Voltage.
L15, L18	ORXA_CTRL, ORXB_CTRL	I	Observation Receiver Control Pins.
H11, J11, K11, L11, M11, N11, P11, H13, H16, J16, K16, H17, J17, K17, H20, H22, J22, K22, L22, M22, N22, P22	VSSD	I	Digital Ground.
H12, J12, K12, L12, M12, N12, P12, H15, J15, K15, H18, J18, K18, H21, J21, K21, L21, M21, N21, P21	VDIG_0P8	I	0.8 V Supply Voltage.
R16	VDIG_SENS_0P8	O	Sense Output for 0.8 V Supply.
N8	VORX1_1P8	I	1.8 V Supply Voltage.
L25	VORX2_1P8	I	1.8 V Supply Voltage.
N25	VORX3_1P8	I	1.8 V Supply Voltage.
L32, M32	ORX1P, ORX1N	I	Differential Input for Observation Receiver Channel 1. Do not connect if unused.
L9, M9	VSCLK0_1P0	I	1.0 V Supply Voltage.
L24, M24	VSCLK1_1P0	I	1.0 V Supply Voltage.
N4, P4	RX2P, RX2N	I	Differential Input for Receiver Channel 2. Do not connect if unused.
N29, P29	RX6N, RX6P	I	Differential Input for Receiver Channel 6. Do not connect if unused.
P8	VORX0_1P0	I	1.0 V Supply Voltage.
P25	VORX1_1P0	I	1.0 V Supply Voltage.
R1, T1	TX2N, TX2P	O	Differential Output for Transmitter Channel 2. Do not connect if unused.
R9	VCONV1_1P8	I	1.8 V Supply Voltage.
R24	VCONV3_1P8	I	1.8 V Supply Voltage.
R32, T32	TX6P, TX6N	O	Differential Output for Transmitter Channel 6. Do not connect if unused.
T9	VCONV1_1P0	I	1.0 V Supply Voltage.
P14	RESETB	I	Active Low Chip Reset.
P19	TEST_EN	I	Test Input Used for JTAG Boundary Scan. Pull high to enable boundary scan, connect to VSSA if unused.
T24	VCONV3_1P0	I	1.0 V Supply Voltage.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
V4, W4	RX3P, RX3N	I	Differential Input for Receiver Channel 3. Do not connect if unused.
R11, R12	SYNCOUT1P, SYNCOUT1N	O	LVDS Sync Signal Output 1. Do not connect if unused.
H19, H14	GPINT0, GPINT1	O	General-Purpose Interrupt Pins.
N16	SPI_CLK	I	SPI Clock.
P16	SPI_DIO	I/O	SPI Data In/Out.
N17	SPI_DO	O	SPI Data Out.
P17	SPI_ENB	I	Active Low SPI Enable.
V29, W29	RX7N, RX7P	I	Differential Input for Receiver Channel 7. Do not connect if unused.
N6, N27	RBIAS0, RBIAS1	I	Bias Resistor Connection. This pin generates an internal current based on an external 0.1% resistor. Connect a 4.99 kΩ resistor between this pin and the analog ground (VSSA).
R13, R14	SYNCOUT0P, SYNCOUT0N	O	LVDS Sync Signal Output 0. Do not connect if unused.
R15	VIF_1P8	I	1.8 V Supply Voltage.
R17, R18	SYNCIN0N, SYNCIN0P	I	LVDS Sync Signal Input 0. Connect to VSSA if unused.
R19, R20	SYNCIN1N, SYNCIN1P	I	LVDS Sync Signal Input 1. Connect to VSSA if unused.
U22	VCLKSYN_1P0	I	1.0 V Supply Voltage.
Y1, AA1	TX3N, TX3P	O	Differential Output for Transmitter Channel 3. Do not connect if unused.
U13	VSERVCO_1P0	O	1.0 V Internal Supply Node. Bypass this pin with a 4.7 µF ceramic capacitor.
U14	VSERVCO_1P8	I	1.8 V Supply Voltage.
U16, U17	DNC	N/A	Do Not Connect.
R21, R22	SYNCIN2N, SYNCIN2P	I	LVDS Sync Signal Input 2. Connect to VSSA if unused.
U19	VCLKVCO_1P0	O	1.0 V Internal Supply Node. Bypass this pin with a 4.7 µF ceramic capacitor.
U20	VCLKVCO_1P8	I	1.8 V Supply Voltage.
U18	VCLKGEN0_1P0	I	1.0 V Supply Voltage.
W7	VCLKGEN1_1P0	I	1.0 V Supply Voltage.
W26	VCLKGEN2_1P0	I	1.0 V Supply Voltage.
Y32, AA32	TX7P, TX7N	O	Differential Output for Transmitter Channel 7. Do not connect if unused.
E1	VTX0_1P8	I	1.8 V Supply Voltage.
V1	VTX1_1P8	I	1.8 V Supply Voltage.
E32	VTX2_1P8	I	1.8 V Supply Voltage.
V32	VTX3_1P8	I	1.8 V Supply Voltage.
Y10, Y11	SERDOUT2P, SERDOUT2N	O	SERDES Differential Output 1. Do not connect if unused.
Y14, Y15	SERDOUT4P, SERDOUT4N	O	SERDES Differential Output 4. Do not connect if unused.
Y18, Y19	SERDIN5N, SERDIN5P	I	SERDES Differential Output 5. Do not connect if unused.
Y22, Y23	SERDIN2P, SERDIN2N	I	SERDES Differential Output 1. Do not connect if unused.
AA8, AA9	SERDOUT0P, SERDOUT0N	O	SERDES Differential Output 0. Do not connect if unused.
AA12, AA13	SERDOUT5P, SERDOUT5N	O	SERDES Differential Output 5. Do not connect if unused.
U11	VSERSYN_1P0	I	1.0 V Supply Voltage.
AA20, AA21	SERDIN4N, SERDIN4P	I	SERDES Differential Input 4. Do not connect if unused.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
AA24, AA25	SERDIN0P, SERDIN0N	I	SERDES Differential Input 0. Do not connect if unused.
AB10, AB11	SERDOUT3P, SERDOUT3N	O	SERDES Differential Output 3. Do not connect if unused.
AB14, AB15	SERDOUT6P, SERDOUT6N	O	SERDES Differential Output 6. Do not connect if unused.
AB16, AC16	VSER_1P0	I	1.0 V Supply Voltage.
AB17, AC17	VDES_1P0	I	1.0 V Supply Voltage.
AB18, AB19	SERDIN6N, SERDIN6P	I	SERDES Differential Input 6. Do not connect if unused.
AB22, AB23	SERDIN3P, SERDIN3N	I	SERDES Differential Input 3. Do not connect if unused.
AC8, AC9	SERDOUT1P, SERDOUT1N	O	SERDES Differential Output 2. Do not connect if unused.
AC12, AC13	SERDOUT7P, SERDOUT7N	O	SERDES Differential Output 7. Do not connect if unused.
AC20, AC21	SERDIN7N, SERDIN7P	I	SERDES Differential Input 7. Do not connect if unused.
AC24, AC25	SERDIN1P, SERDIN1N	I	SERDES Differential Input 2. Do not connect if unused.

[1] I is input, O is output, I/O is input/output, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

850 MHZ BAND

The temperature settings refer to the die temperature. All LO frequencies set to 850 MHz, unless otherwise noted. The observation receiver measurements are taken with 5898.24 MHz sampling frequency, unless otherwise noted. The receiver linearity performance for receiver attenuation settings higher than 20 dB is limited by measurement setup.

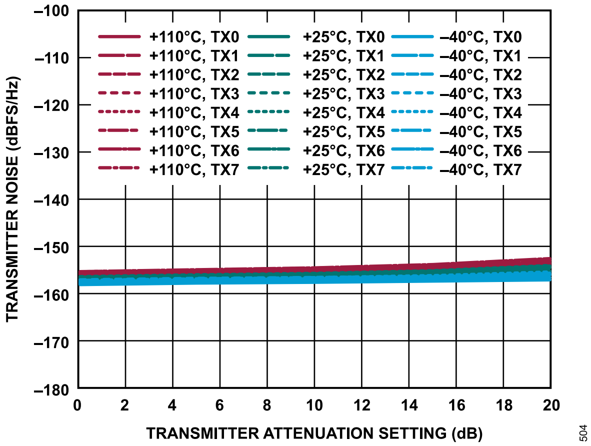

Figure 4. Transmitter Noise vs. Transmitter Attenuation Setting, 100 MHz Offset

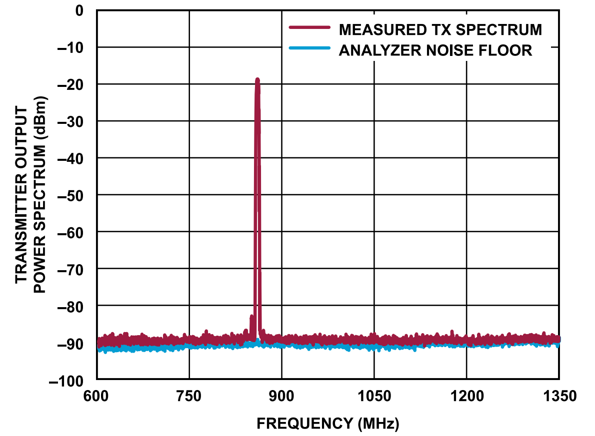

Figure 6. Transmitter Output Power Spectrum vs. Frequency, Tx0, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth

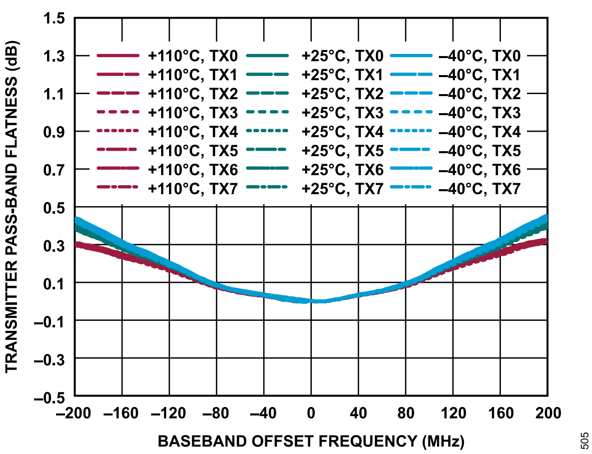

Figure 5. Transmitter Pass-Band Flatness vs. Baseband Offset Frequency

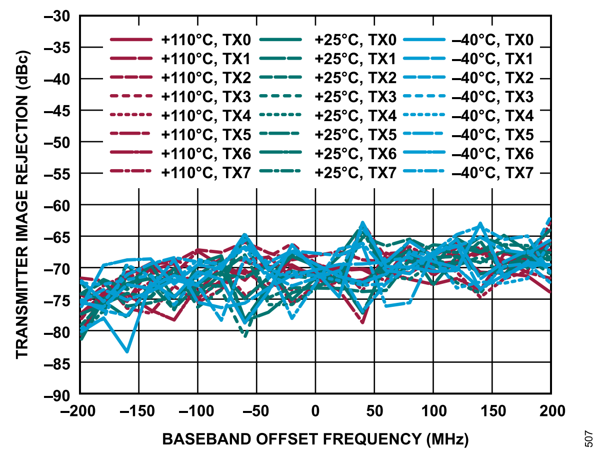

Figure 7. Transmitter Image Rejection vs. Baseband Offset Frequency, −6 dBFS Continuous Wave Signal

TYPICAL PERFORMANCE CHARACTERISTICS

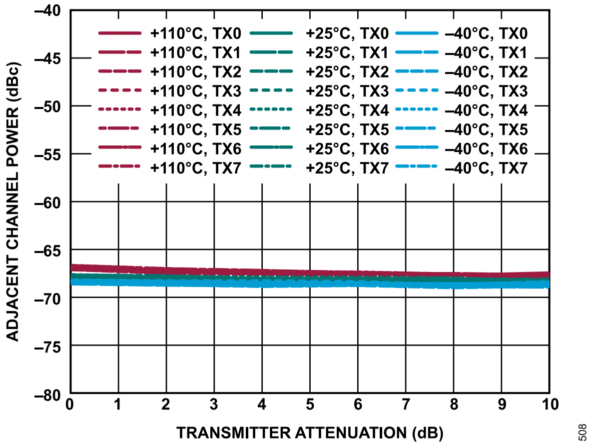

Figure 8. Adjacent Channel Power vs. Transmitter Attenuation, 190 MHz Offset, 20 MHz LTE, PAR = 12 dB

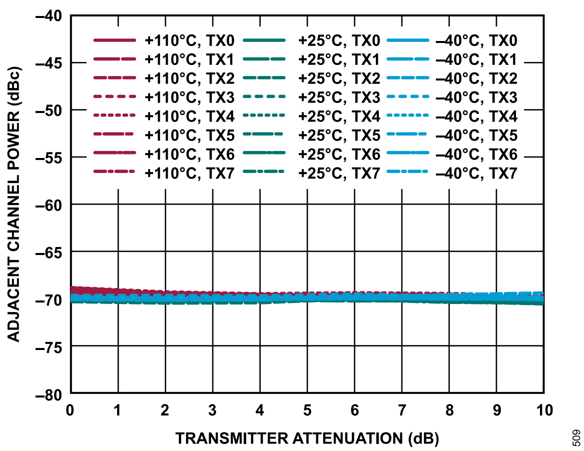

Figure 9. Adjacent Channel Power vs. Transmitter Attenuation, −10 MHz Offset, 20 MHz LTE, PAR = 12 dB

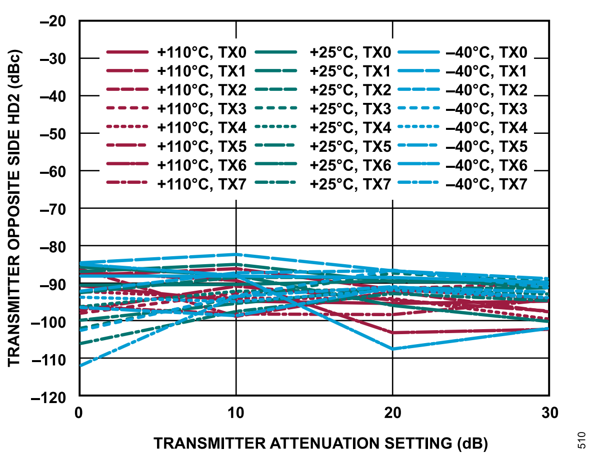

Figure 10. Transmitter Opposite Side Second Harmonic Distortion (HD2) vs. Transmitter Attenuation Setting, 30 MHz Offset, −12 dBFS Continuous Wave Signal

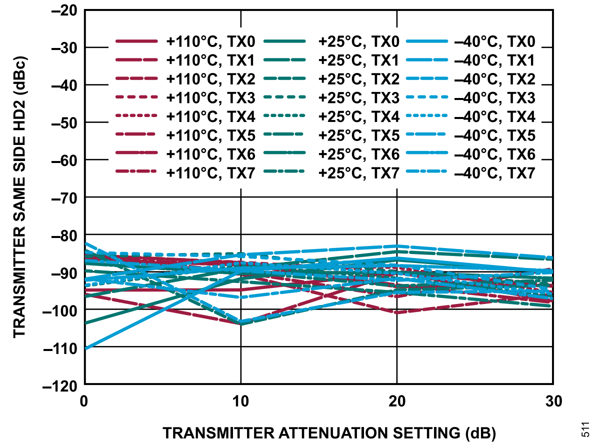

Figure 11. Transmitter Same Side HD2 vs. Transmitter Attenuation Setting, 30 MHz Offset, −12 dBFS Continuous Wave Signal

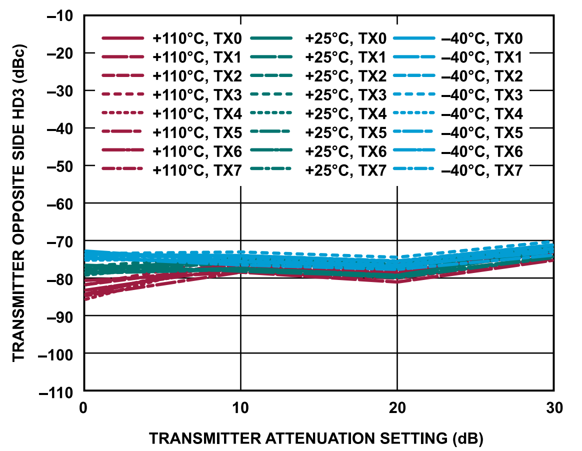

Figure 12. Transmitter Opposite Side Third Harmonic Distortion (HD3) vs. Transmitter Attenuation Setting, 30 MHz Offset, −12 dBFS Continuous Wave Signal

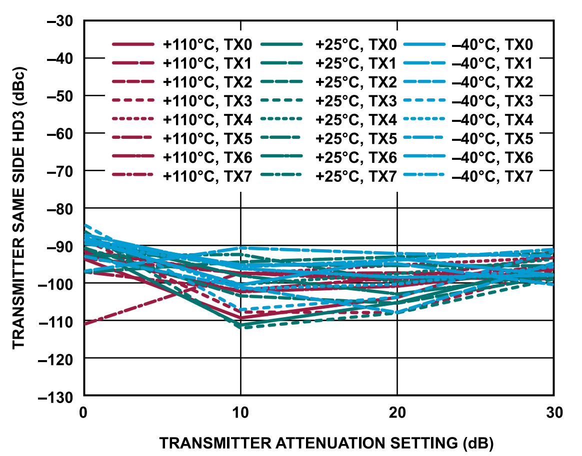

Figure 13. Transmitter Same Side HD3 vs. Transmitter Attenuation Setting, 30 MHz Offset, −12 dBFS Continuous Wave Signal

TYPICAL PERFORMANCE CHARACTERISTICS

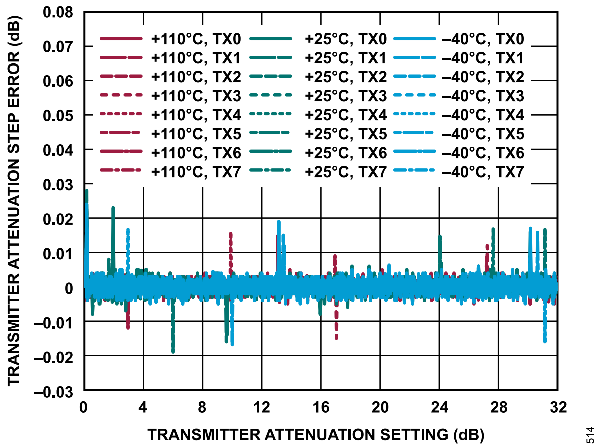

Figure 14. Transmitter Attenuation Step Error vs. Transmitter Attenuation Setting, 30 MHz Offset, −12 dBFS Continuous Wave Signal

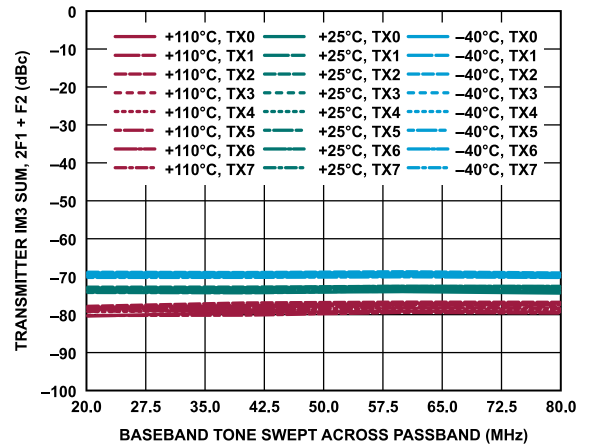

Figure 17. Transmitter IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

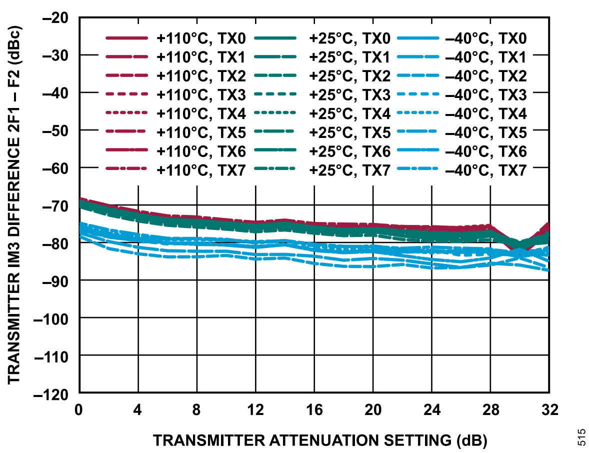

Figure 15. Transmitter IM3, 2f1 − f2 vs. Transmitter Attenuation Setting, −15 dBFS Signal Level per Tone, f1 = 180 MHz Offset, f2 = 185 MHz Offset

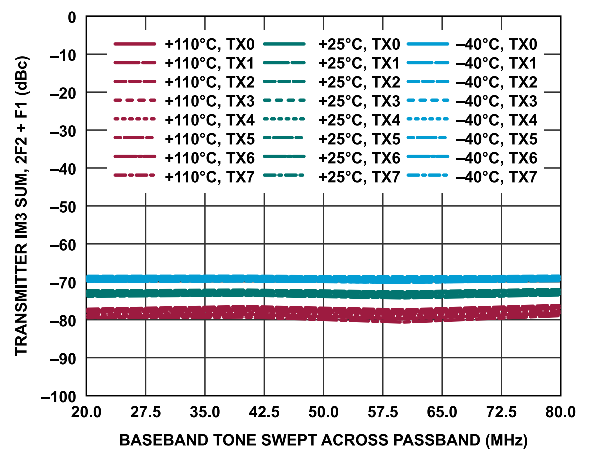

Figure 18. Transmitter IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

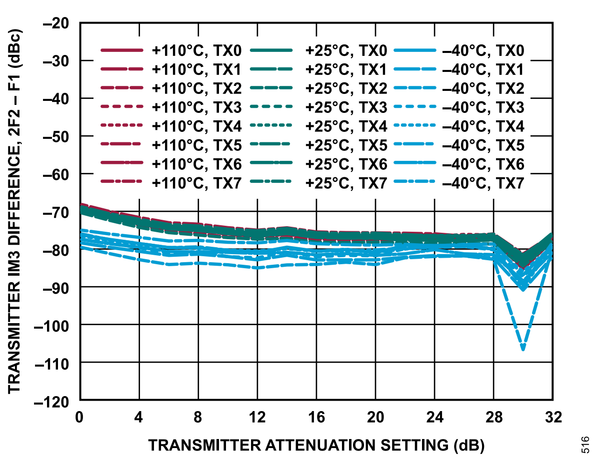

Figure 16. Transmitter IM3, 2f2 − f1 vs. Transmitter Attenuation Setting, −15 dBFS Signal Level per Tone, f1 = 180 MHz Offset, f2 = 185 MHz Offset

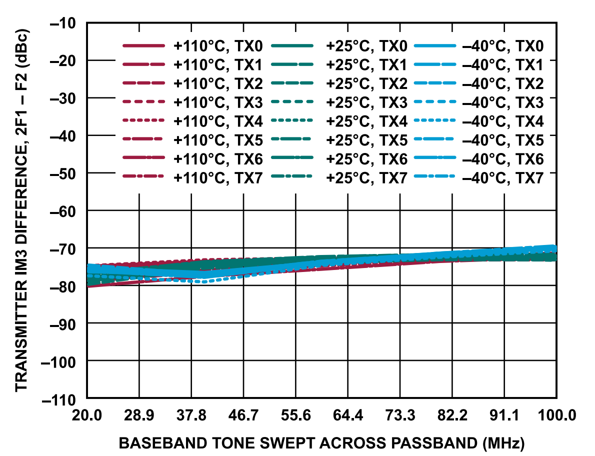

Figure 19. Transmitter IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

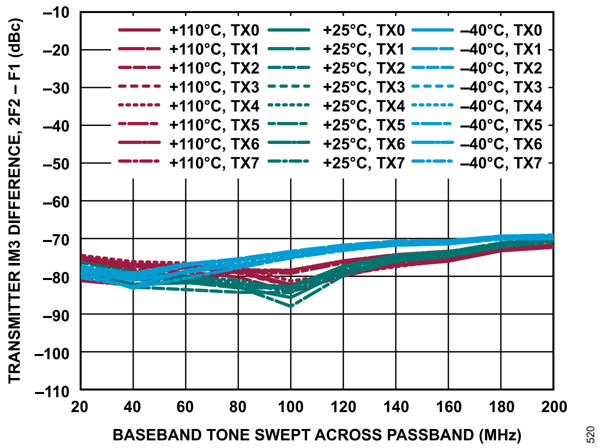

Figure 20. Transmitter IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

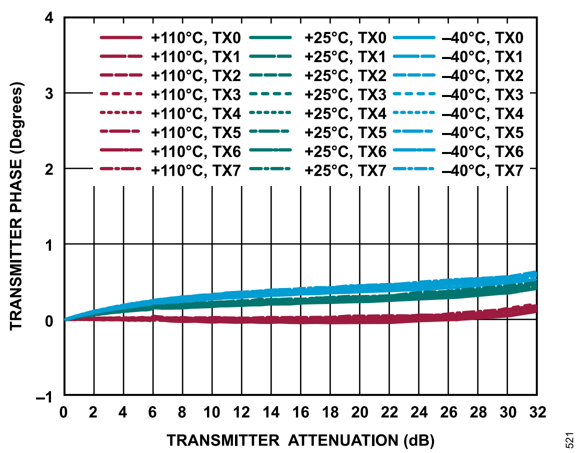

Figure 21. Transmitter Phase vs. Transmitter Attenuation

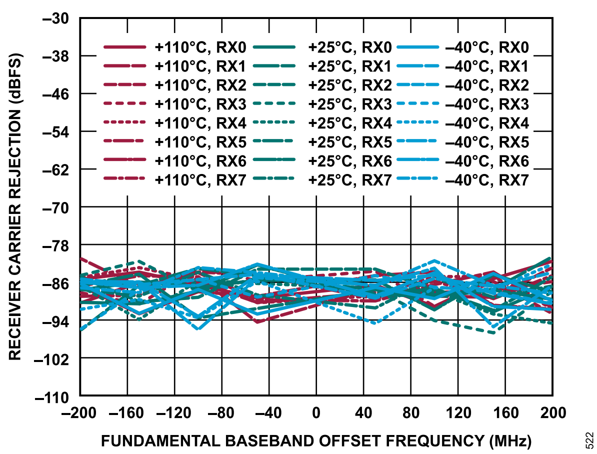

Figure 22. Receiver Carrier Rejection vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

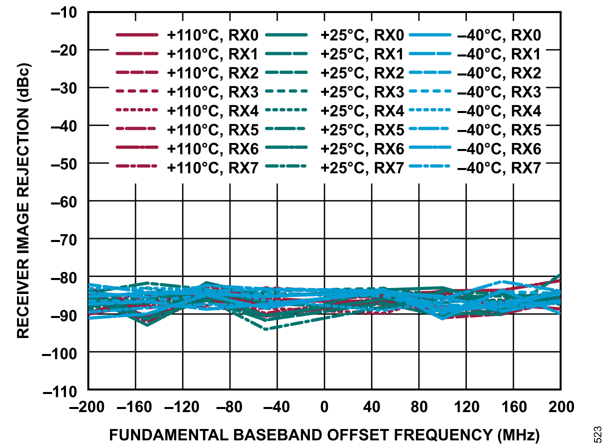

Figure 23. Receiver Image Rejection vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

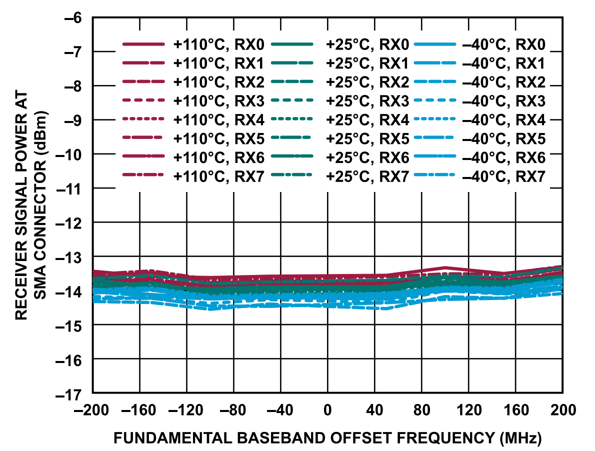

Figure 24. Receiver Signal Power at SMA Connector vs. Fundamental Baseband Offset Frequency, −1 dBFs Input Signal (Match Is Not De-Embedded)

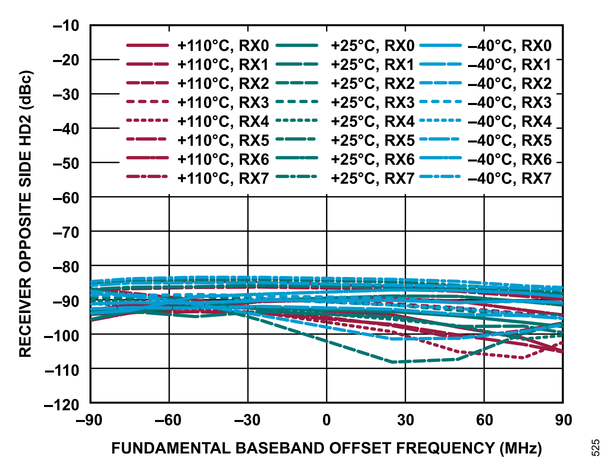

Figure 25. Receiver Opposite Side HD2 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

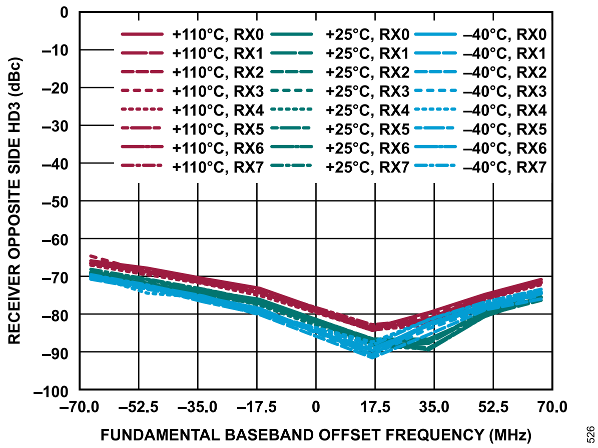

Figure 26. Receiver Opposite Side HD3 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

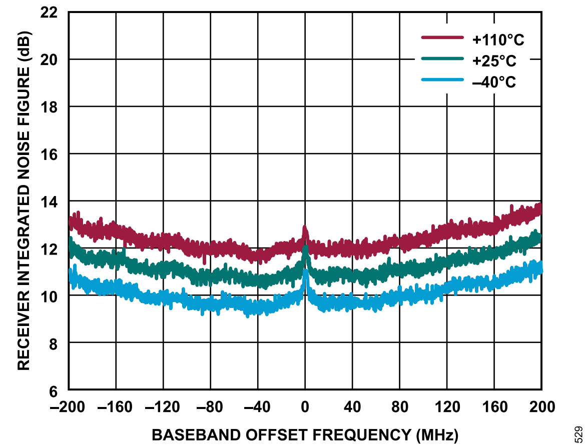

Figure 29. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 kHz Integration Steps, 983.04 MSPS Sample Rate

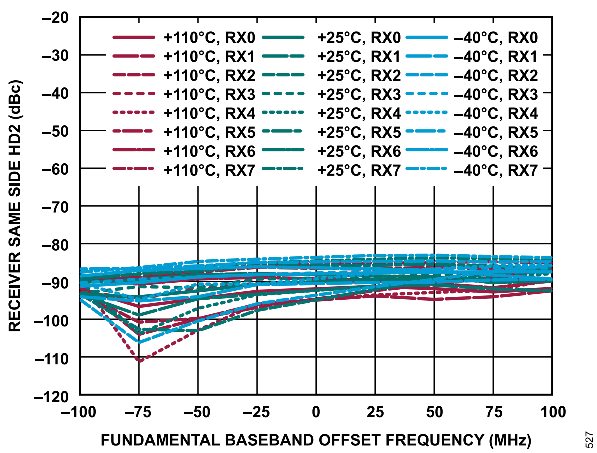

Figure 27. Receiver Same Side HD2 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

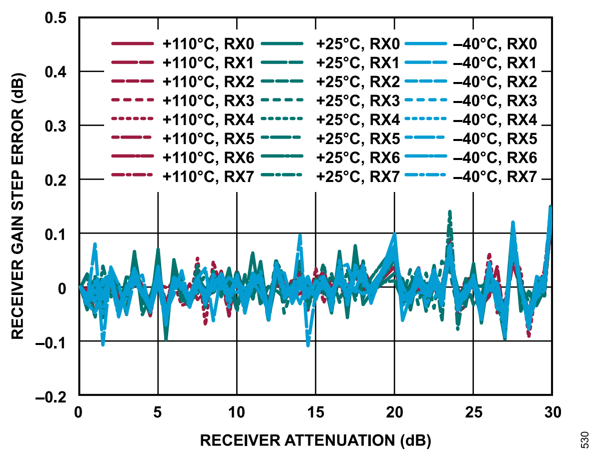

Figure 30. Receiver Gain Step Error vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

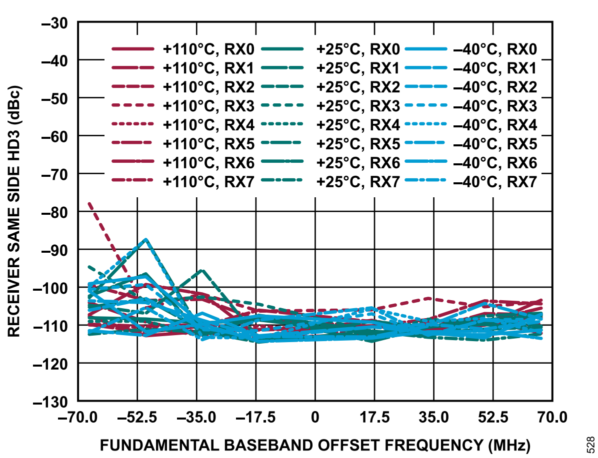

Figure 28. Receiver Same Side HD3 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

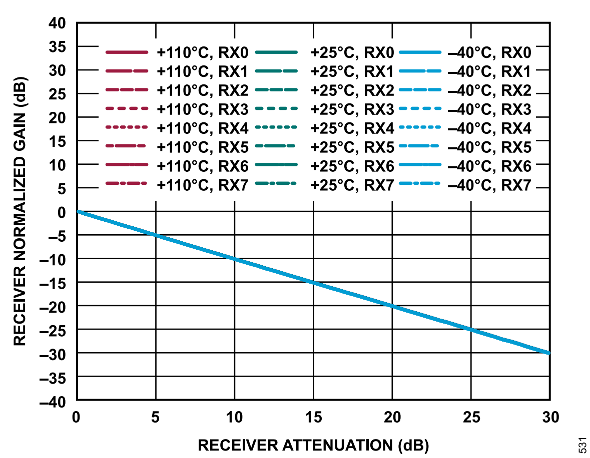

Figure 31. Receiver Normalized Gain vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

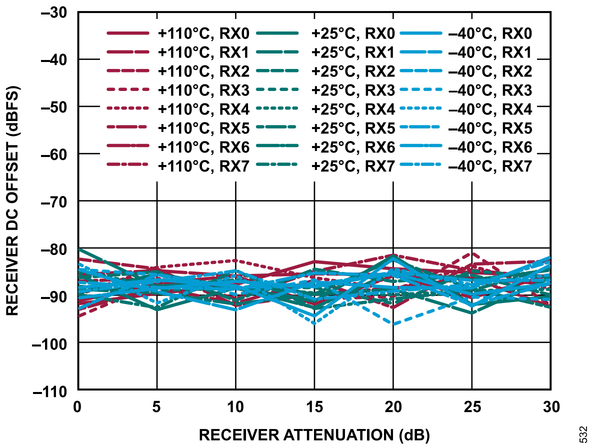

Figure 32. Receiver DC Offset vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

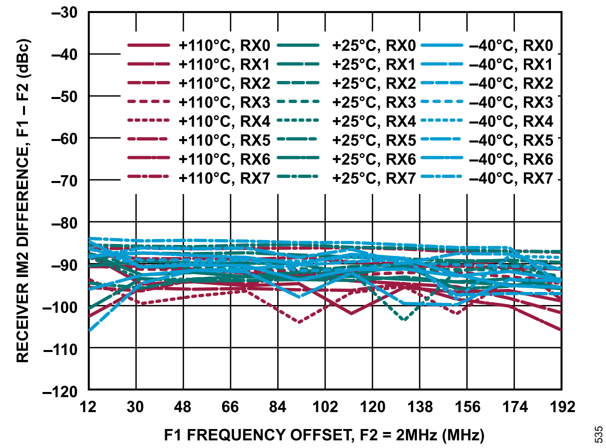

Figure 35. Receiver IM2, f1 − f2 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

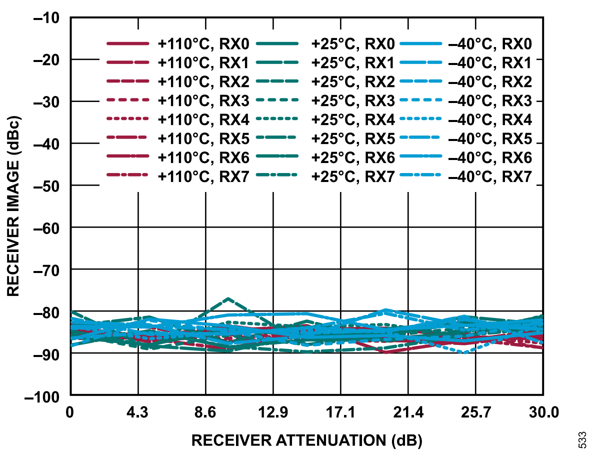

Figure 33. Receiver Image vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

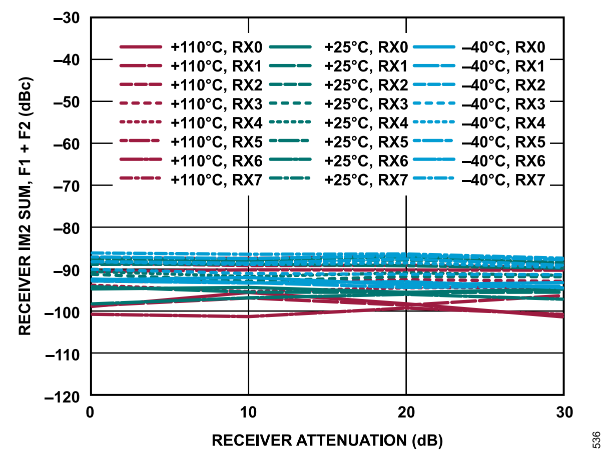

Figure 36. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 192 MHz Offset, f2 = 2 MHz Offset

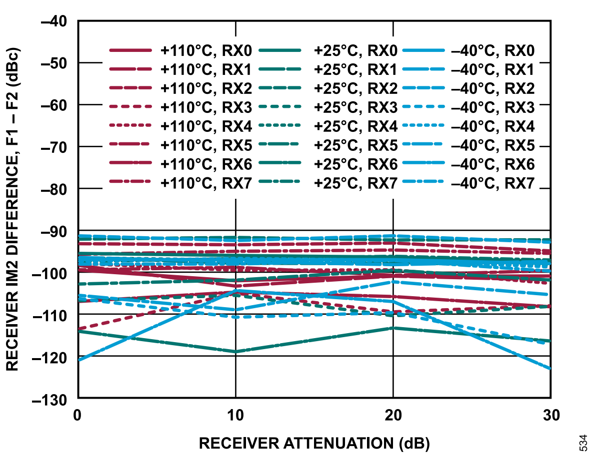

Figure 34. Receiver IM2, f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 192 MHz Offset, f2 = 2 MHz Offset

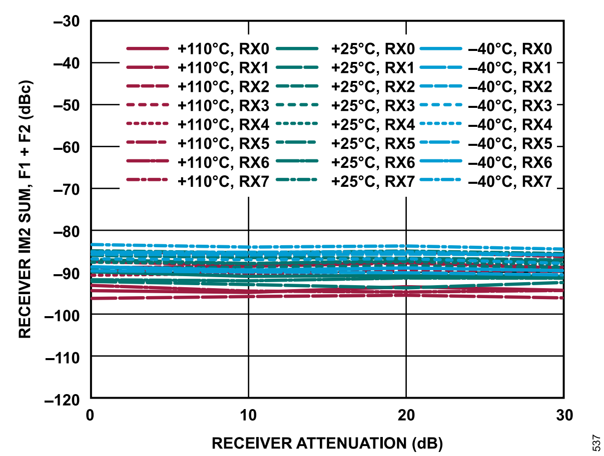

Figure 37. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 101 MHz Offset, f2 = 99 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

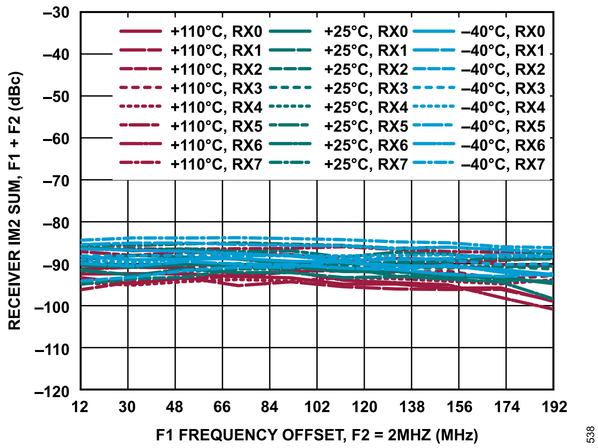

Figure 38. Receiver IM2, f1 + f2 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

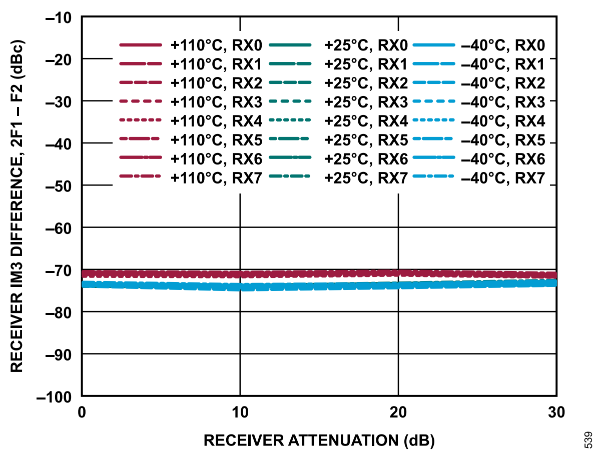

Figure 39. Receiver IM3, 2f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 101 MHz Offset, f2 = 2 MHz Offset

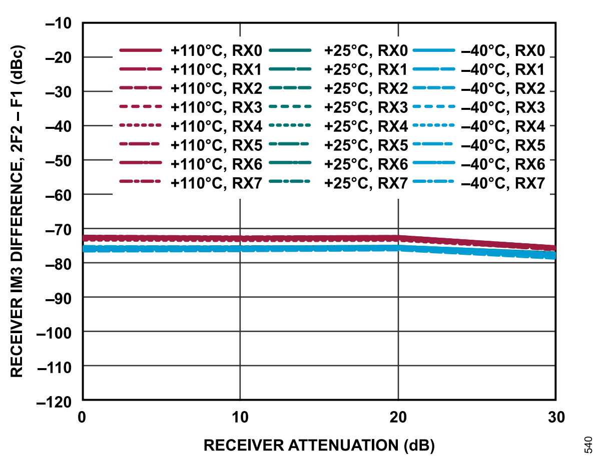

Figure 40. Receiver IM3, 2f2 − f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 101 MHz Offset, f2 = 2 MHz Offset

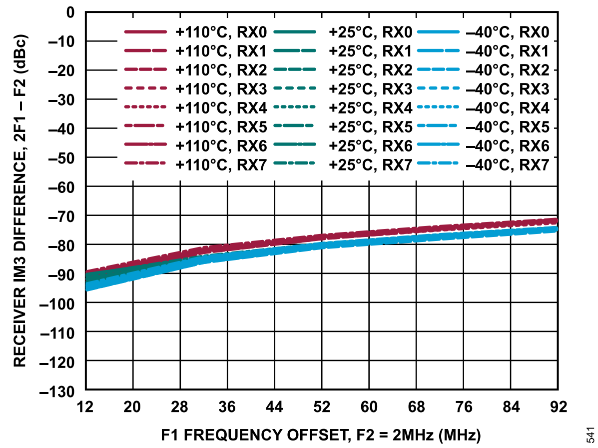

Figure 41. Receiver IM3, 2f1 − f2 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

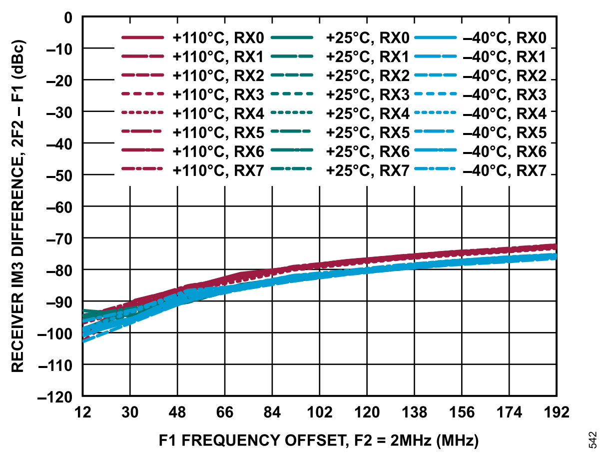

Figure 42. Receiver IM3, 2f2 − f1 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

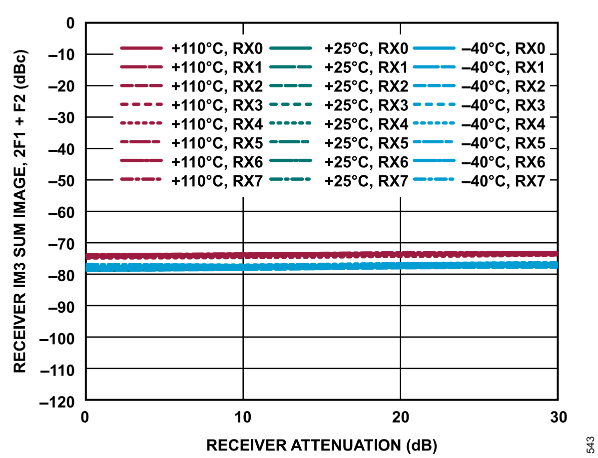

Figure 43. Receiver IM3, 2f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 99 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

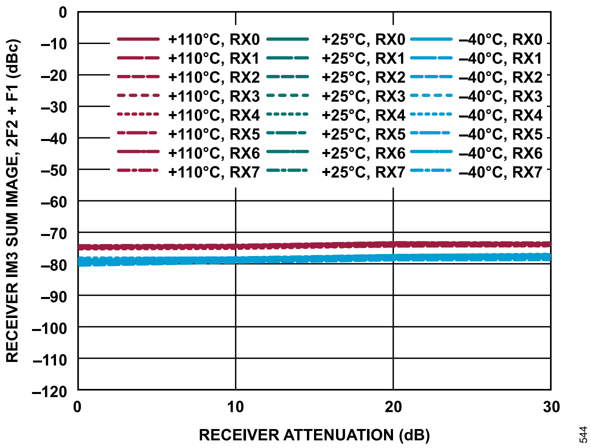

Figure 44. Receiver IM3, 2f2 + f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 99 MHz Offset, f2 = 2 MHz Offset

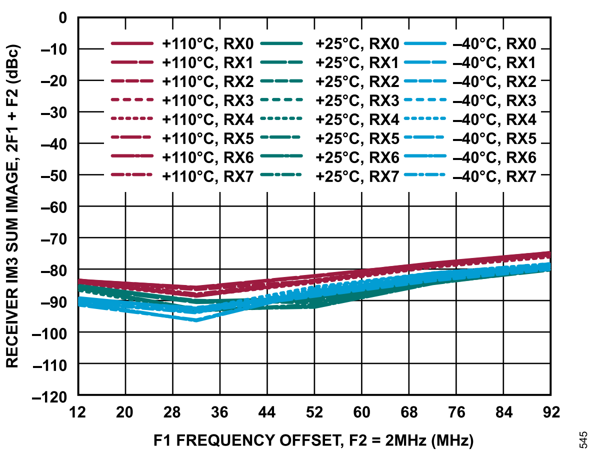

Figure 45. Receiver IM3, 2f1 + f2 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

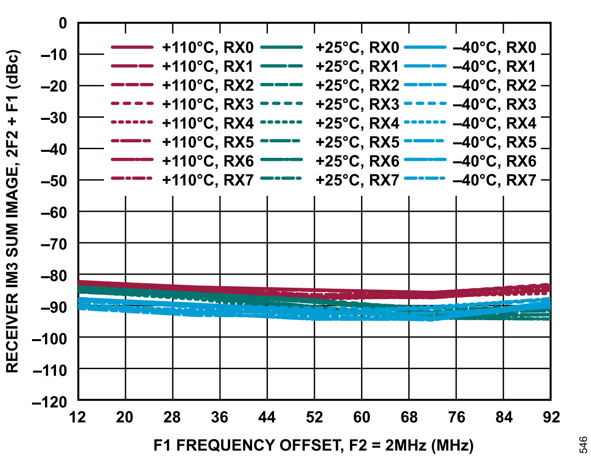

Figure 46. Receiver IM3, 2f2 + f1 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

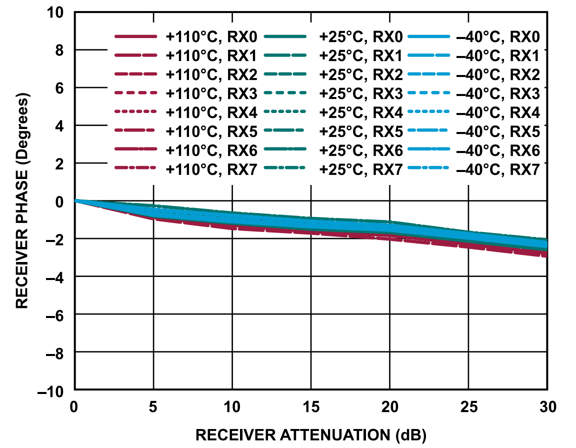

Figure 47. Receiver Phase vs. Receiver Attenuation

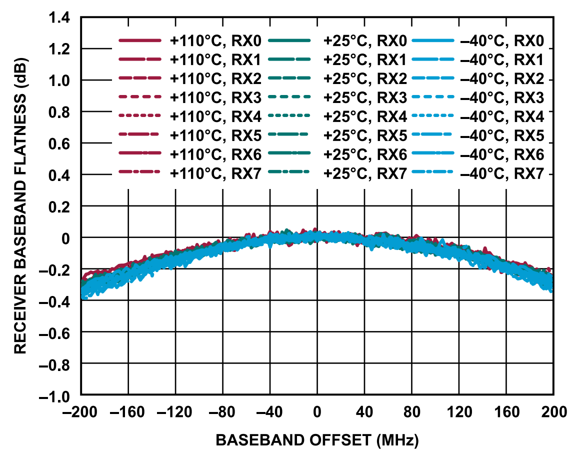

Figure 48. Receiver Baseband Flatness vs. Baseband Offset

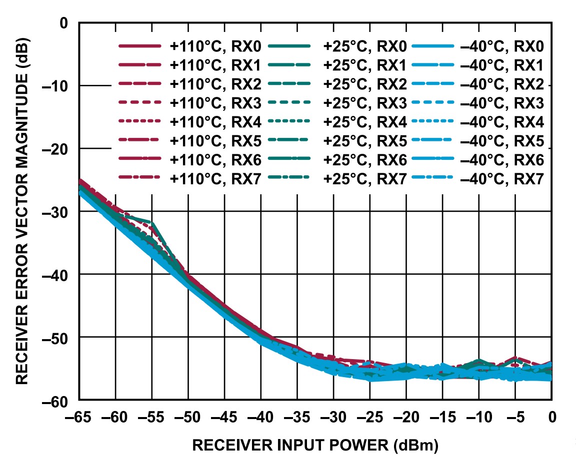

Figure 49. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Centered Around DC, TDD Mode, AGC Enabled

TYPICAL PERFORMANCE CHARACTERISTICS

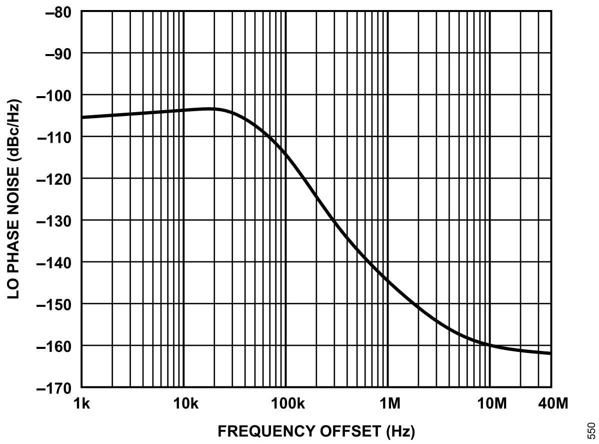

Figure 50. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 60 kHz, Phase Margin = 55°

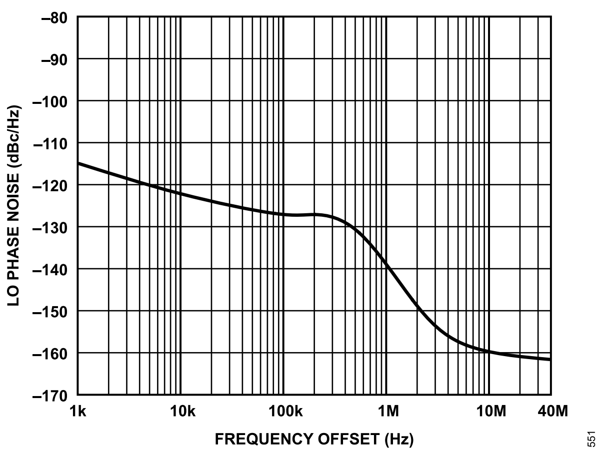

Figure 51. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 55°

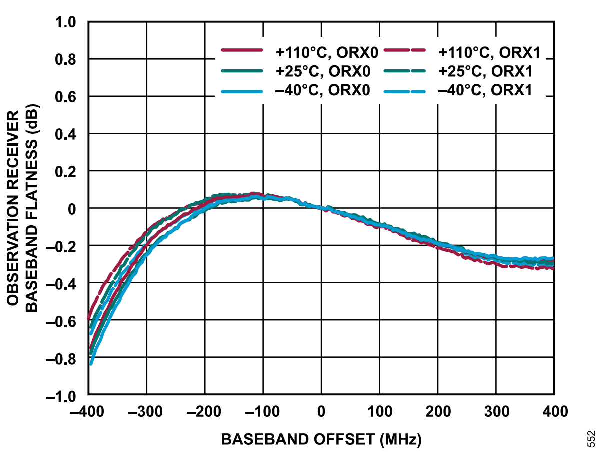

Figure 52. Observation Receiver Baseband Flatness vs. Baseband Offset

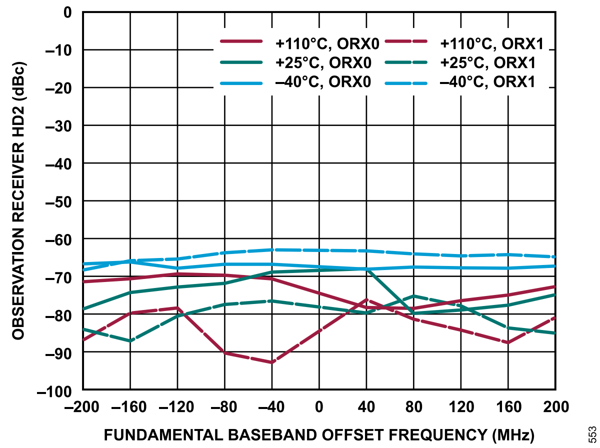

Figure 53. Observation Receiver HD2 vs. Fundamental Baseband Offset Frequency, −10 dBFS Input Signal

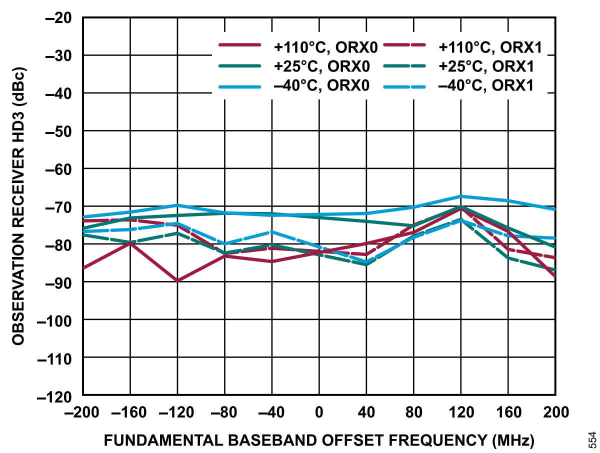

Figure 54. Observation Receiver HD3 vs. Fundamental Baseband Offset Frequency, −10 dBFS Input Signal

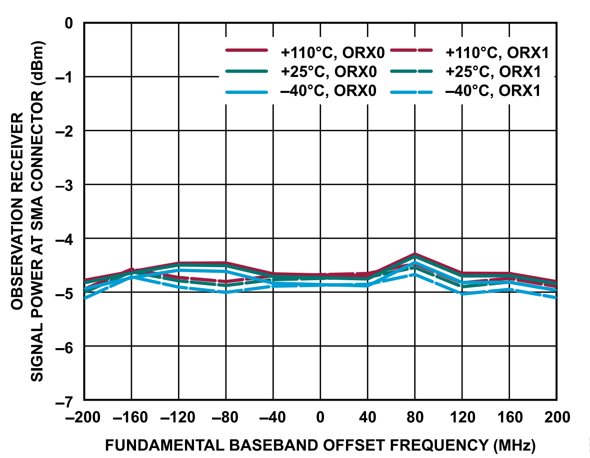

Figure 55. Observation Receiver Signal Power at SMA Connector vs. Fundamental Baseband Offset Frequency, −10 dBFS Input Signal (Match Is Not De-Embedded)

TYPICAL PERFORMANCE CHARACTERISTICS

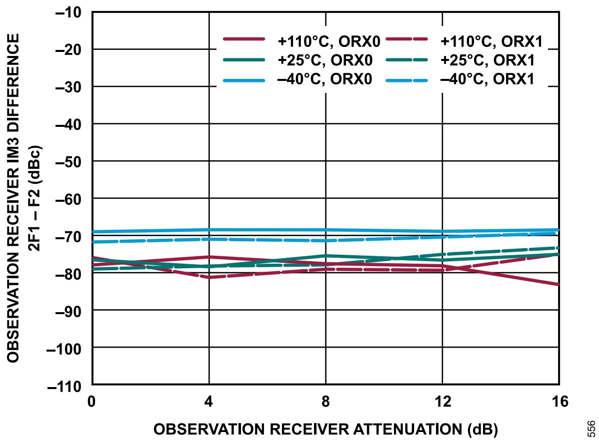

Figure 56. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 852 MHz, f2 = 862 MHz

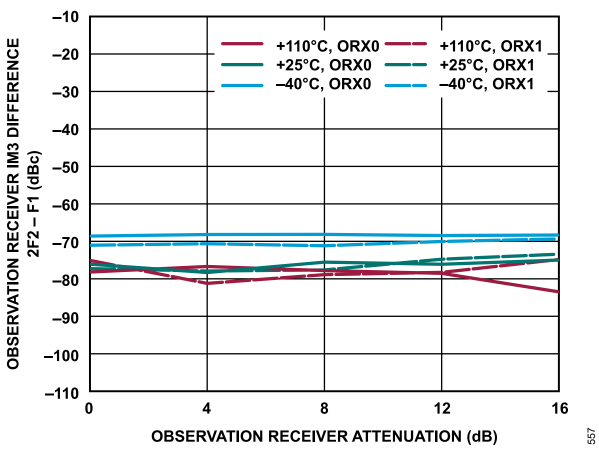

Figure 57. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 852 MHz, f2 = 862 MHz

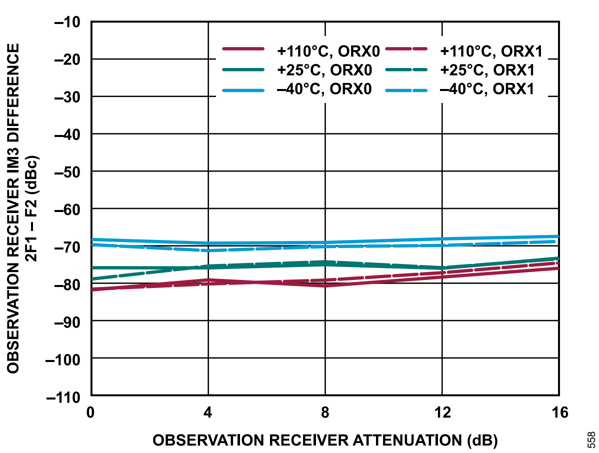

Figure 58. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 852 MHz, f2 = 1062 MHz

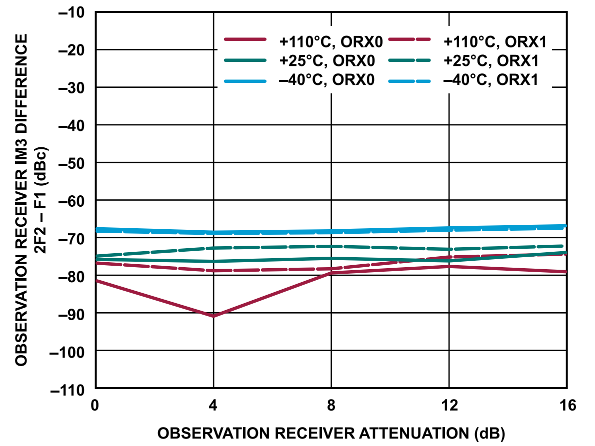

Figure 59. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 852 MHz, f2 = 1062 MHz

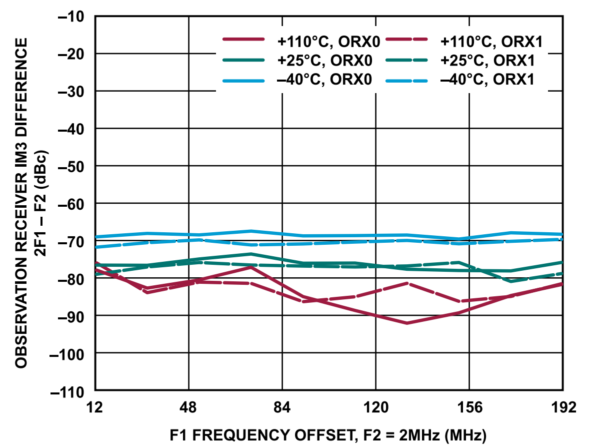

Figure 60. Observation Receiver IM3, 2f1 − f2 vs. Frequency Offset, −13 dBFS Signal Level per Tone, f2 = 2 MHz

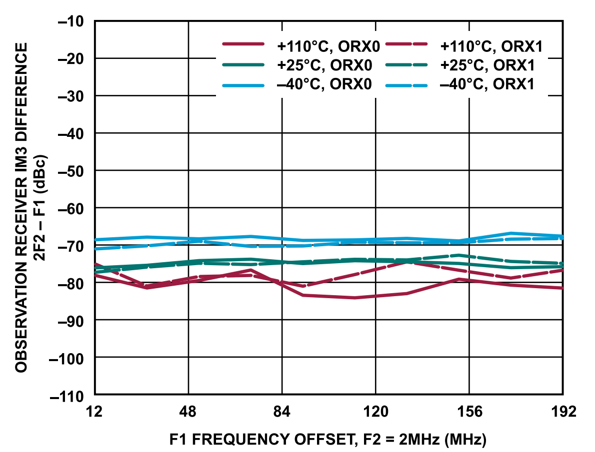

Figure 61. Observation Receiver IM3, 2f2 − f1 vs. Frequency Offset, −13 dBFS Signal Level per Tone, f2 = 2 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

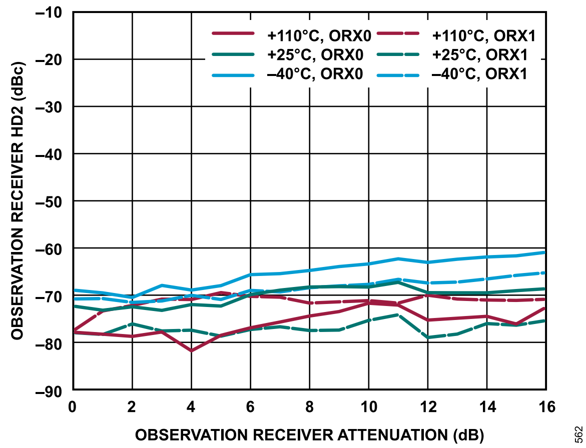

Figure 62. Observation Receiver HD2 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

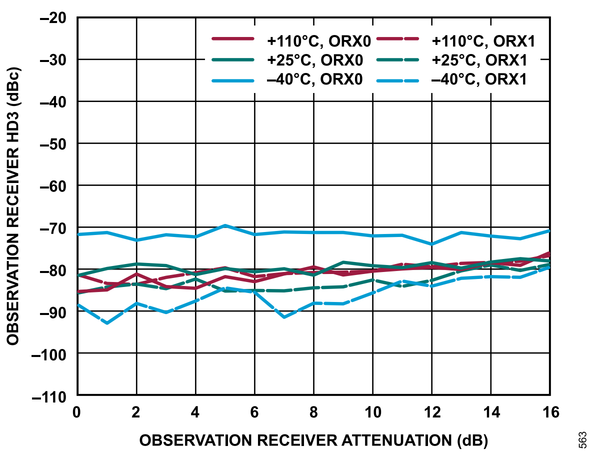

Figure 63. Observation Receiver HD3 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

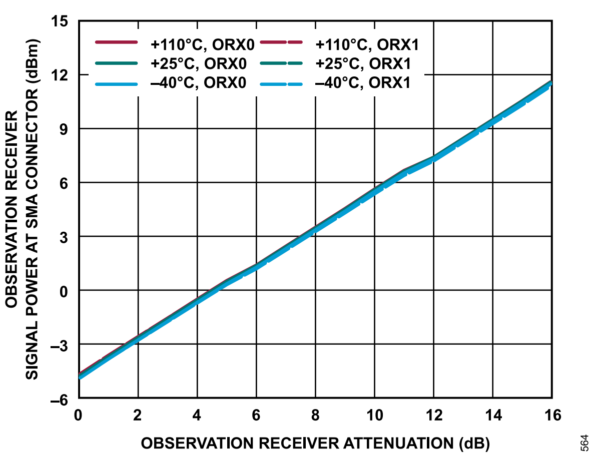

Figure 64. Observation Receiver Signal Power at SMA Connector vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

1800 MHZ BAND

The temperature settings refer to the die temperature. All LO frequencies set to 1800 MHz, unless otherwise noted. The observation receiver measurements are taken with 5898.24 MHz sampling frequency, unless otherwise noted. The receiver linearity performance for receiver attenuation settings higher than 20 dB is limited by measurement setup.

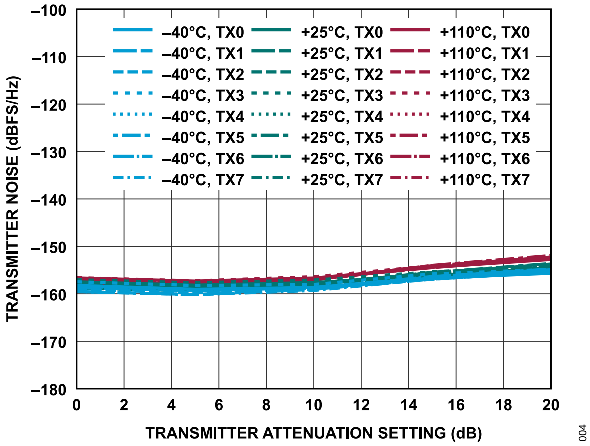

Figure 65. Transmitter Noise vs. Transmitter Attenuation, 150 MHz Offset

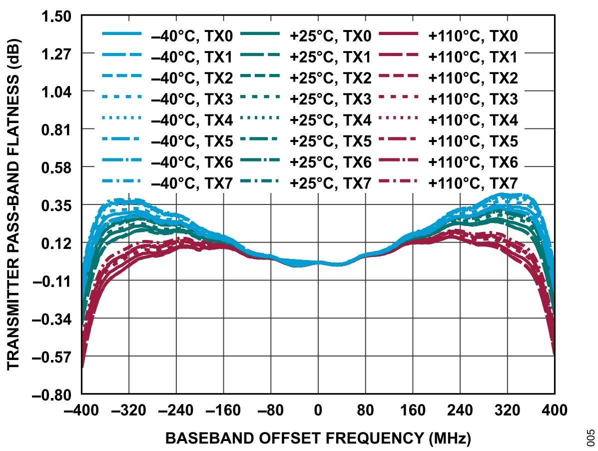

Figure 66. Transmitter Pass−Band Flatness vs. Baseband Offset Frequency

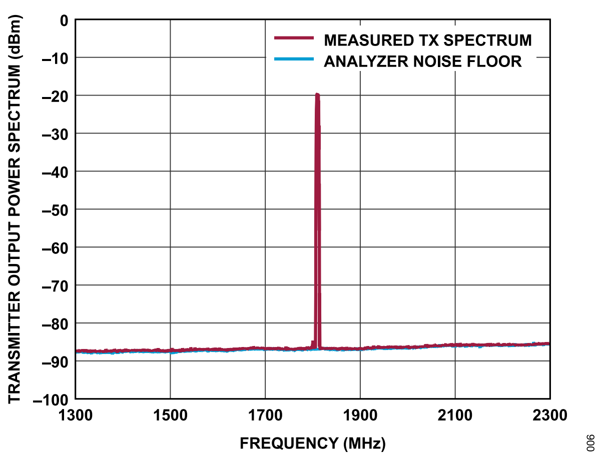

Figure 67. Transmitter Output Power Spectrum, Tx0, 5MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T_J = 25°C

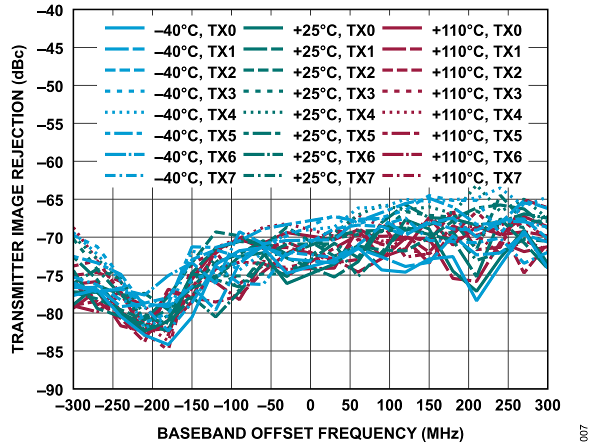

Figure 68. Transmitter Image Rejection vs. Baseband Offset Frequency, −6 dBFS Continuous Wave Signal

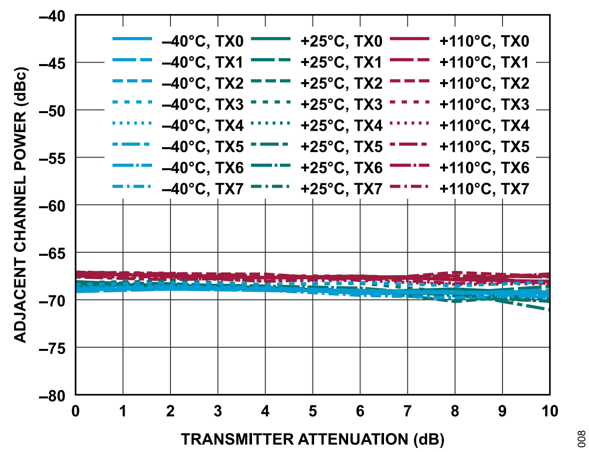

Figure 69. Adjacent Channel Power vs. Transmitter Attenuation, 290 MHz Offset, 20 MHz LTE, PAR = 12 dB

TYPICAL PERFORMANCE CHARACTERISTICS

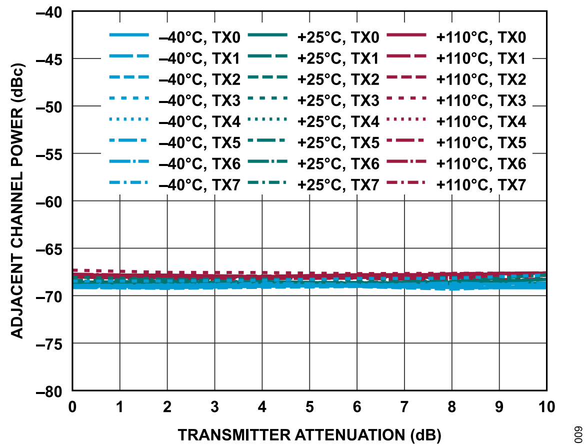

Figure 70. Adjacent Channel Power vs. Transmitter Attenuation, −10 MHz Offset, 20 MHz LTE, PAR = 12 dB

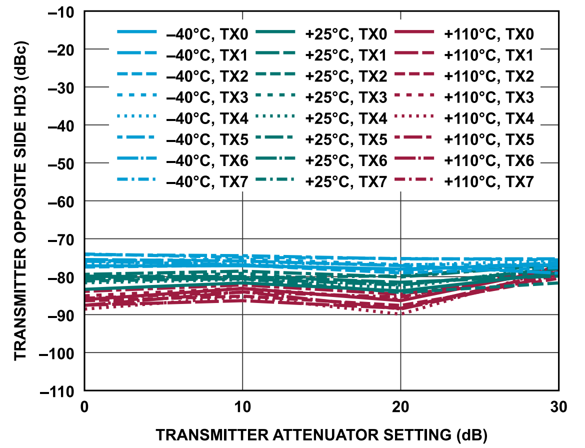

Figure 73. Transmitter Opposite Side Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

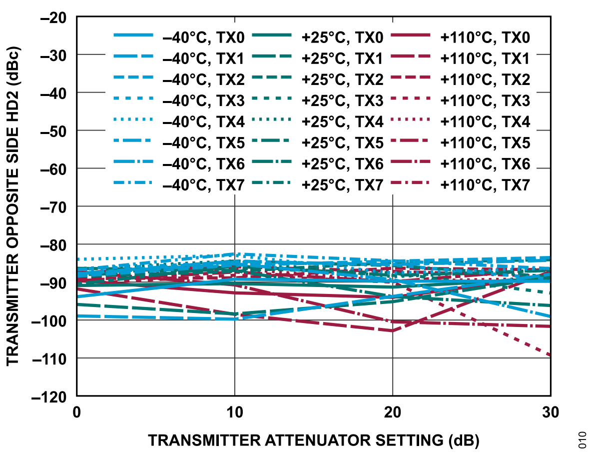

Figure 71. Transmitter Opposite Side Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

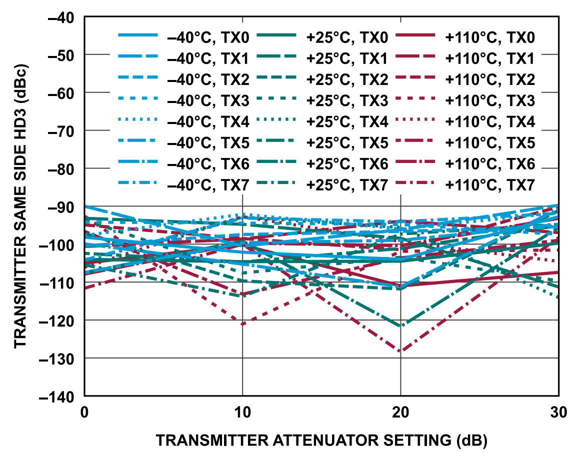

Figure 74. Transmitter Same Side HD3 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

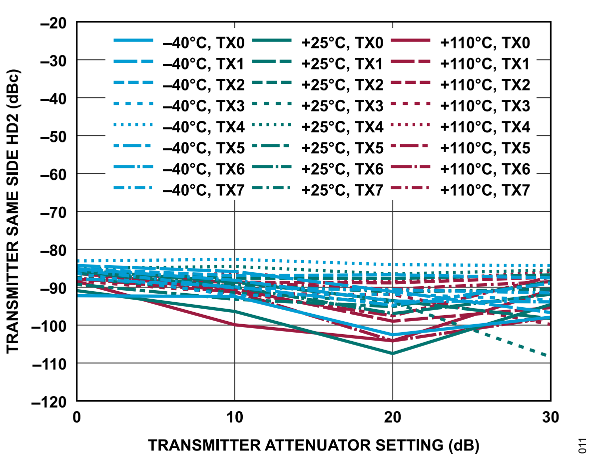

Figure 72. Transmitter Same Side HD2 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

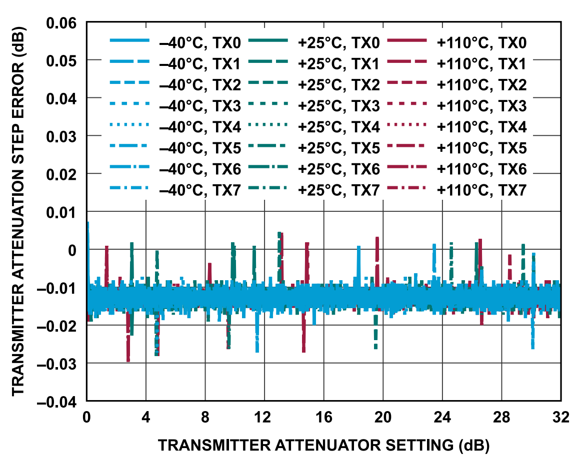

Figure 75. Transmitter Attenuation Step Error vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

TYPICAL PERFORMANCE CHARACTERISTICS

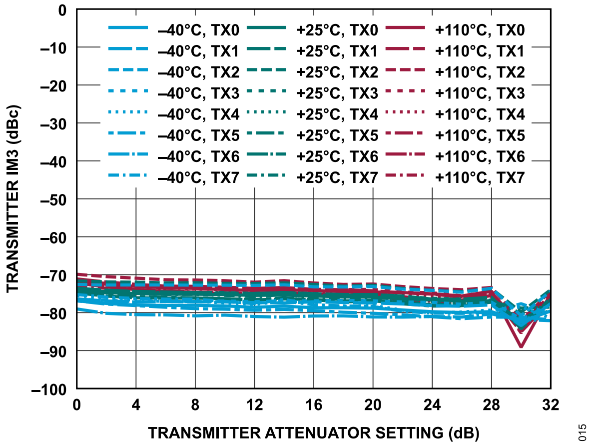

Figure 76. Transmitter IM3, 2f1 − f2 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

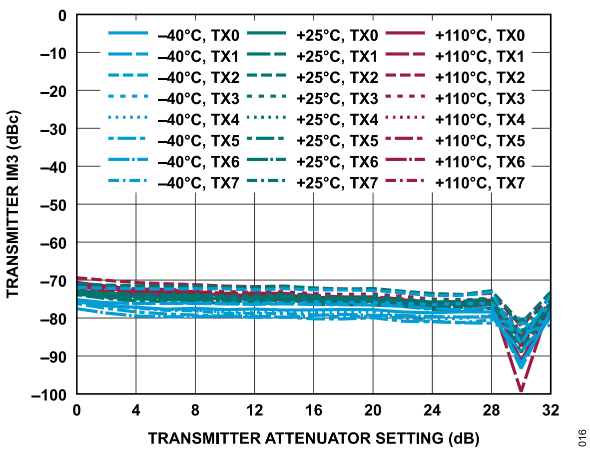

Figure 77. Transmitter IM3, 2f2 − f1 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

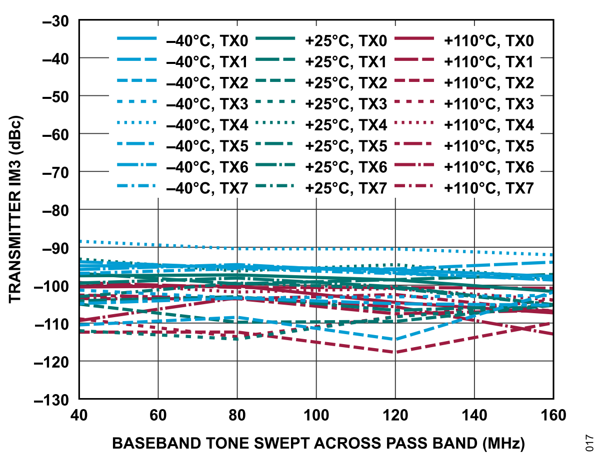

Figure 78. Transmitter IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

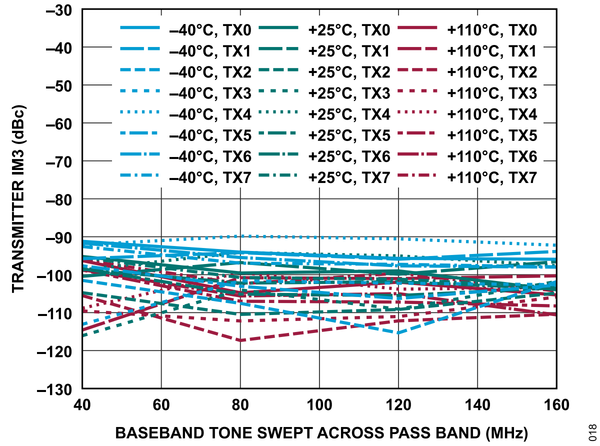

Figure 79. Transmitter IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

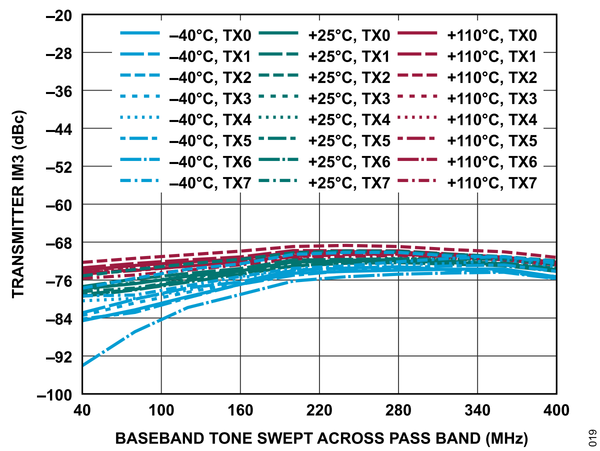

Figure 80. Transmitter IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

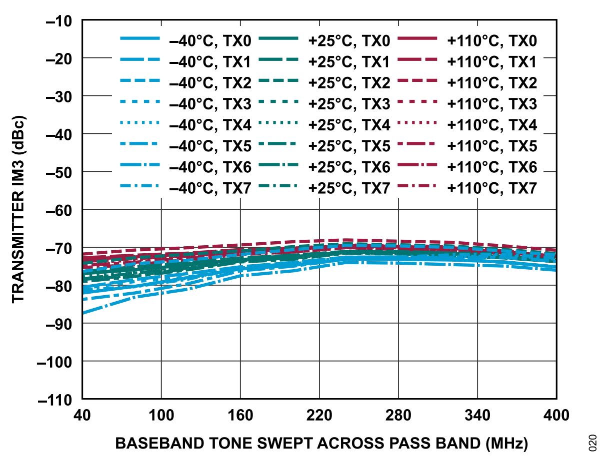

Figure 81. Transmitter IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

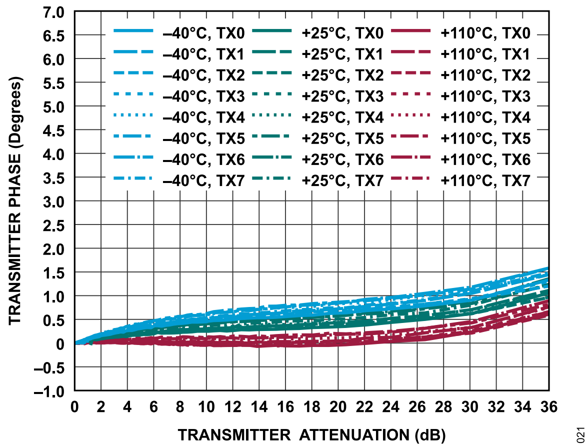

Figure 82. Transmitter Phase vs. Transmitter Attenuation

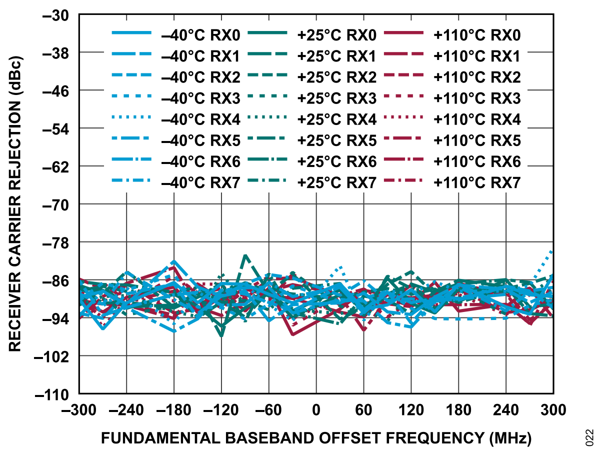

Figure 83. Receiver Carrier Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

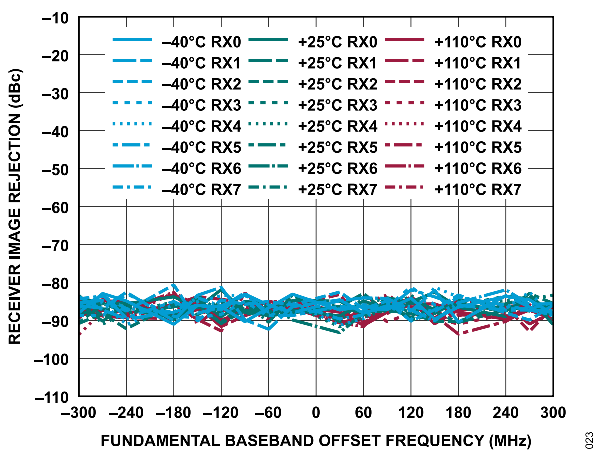

Figure 84. Receiver Image Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

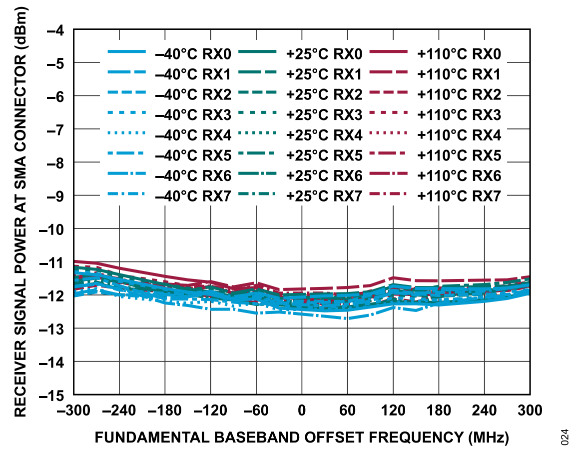

Figure 85. Receiver Signal Power at SMA Connector vs. Baseband Offset Frequency, −1 dBFS Input Signal (Match Is Not De−Embedded)

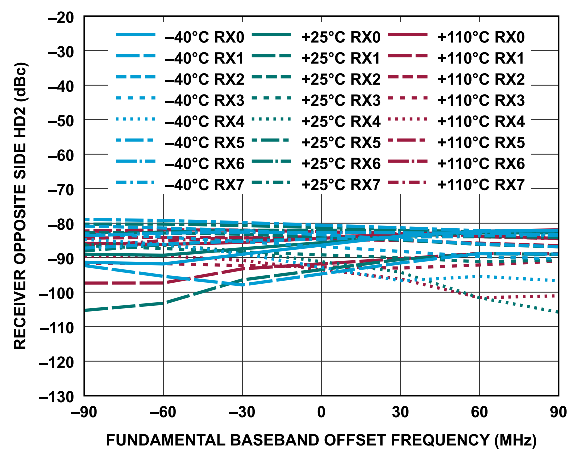

Figure 86. Receiver Opposite Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

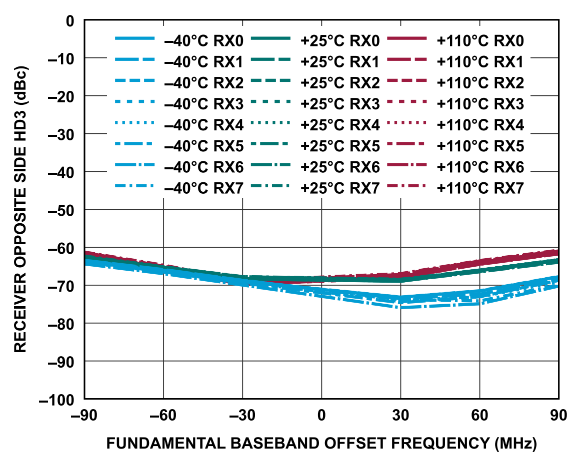

Figure 87. Receiver Opposite Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

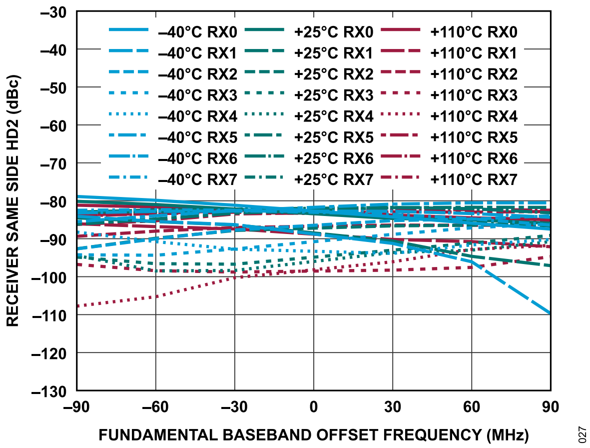

Figure 88. Receiver Same Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

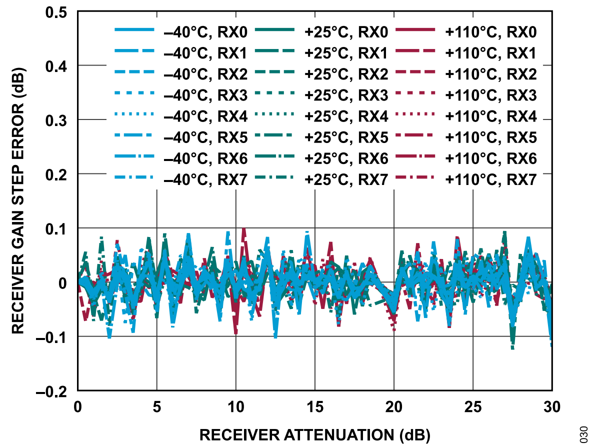

Figure 91. Receiver Gain Step Error vs. Attenuation, 30 MHz Offset, −1 dBFS Input Signal

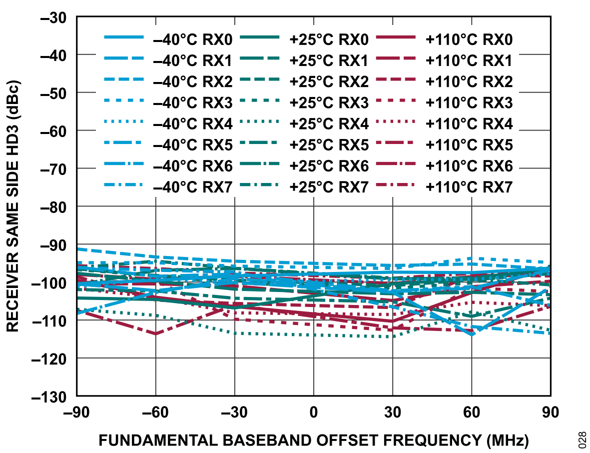

Figure 89. Receiver Same Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

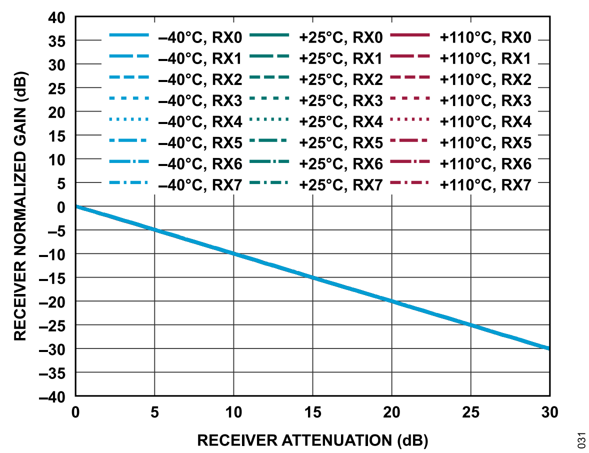

Figure 92. Receiver Normalized Gain vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

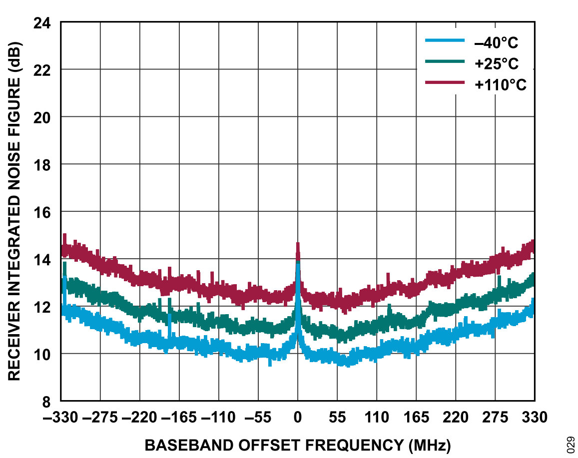

Figure 90. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 kHz Integration Steps, 983.04 MSPS Sample Rate

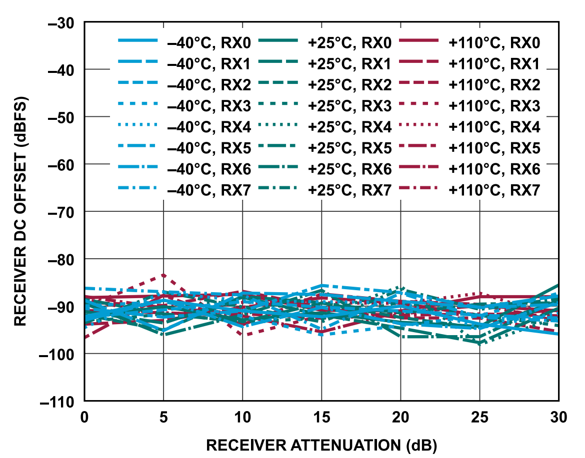

Figure 93. Receiver DC Offset vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

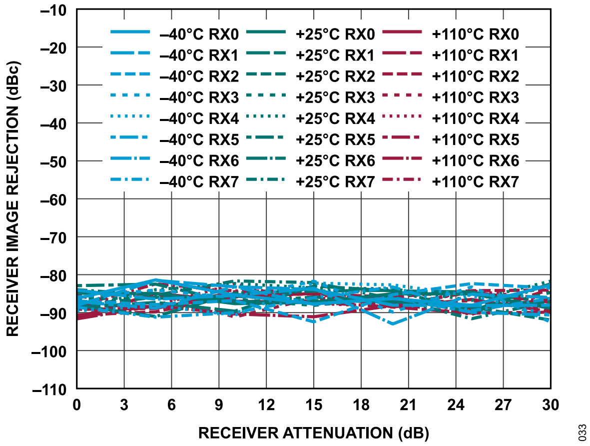

Figure 94. Receiver Image vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

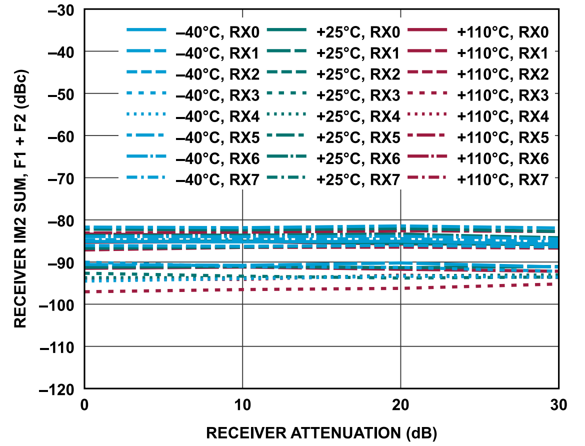

Figure 97. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

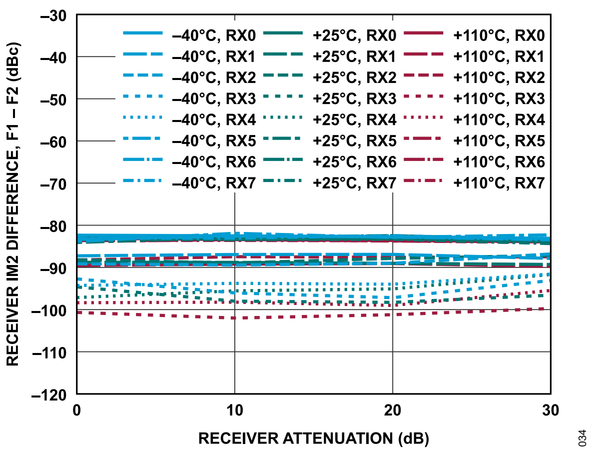

Figure 95. Receiver IM2, f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

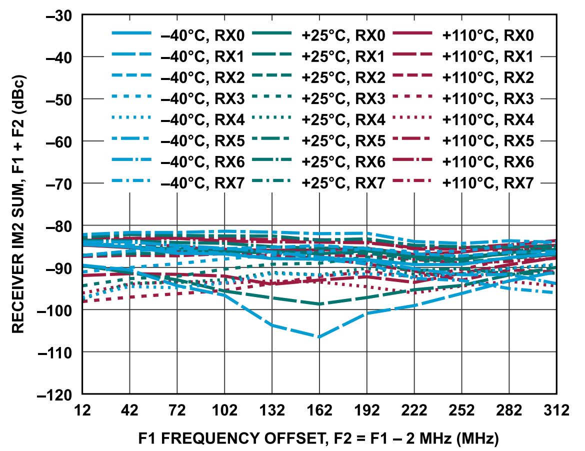

Figure 98. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 282 MHz Offset, f2 = 2 MHz Offset

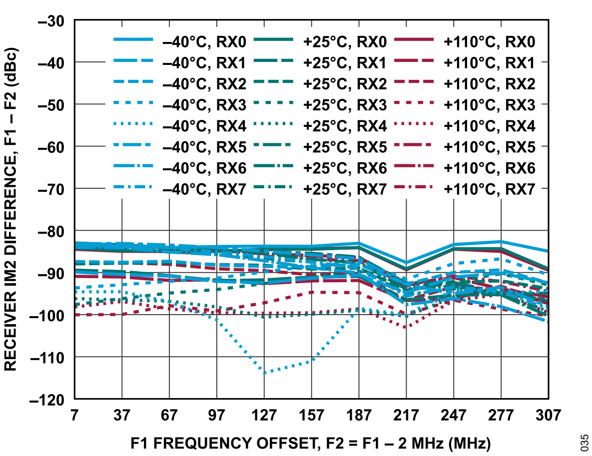

Figure 96. Receiver IM2, f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

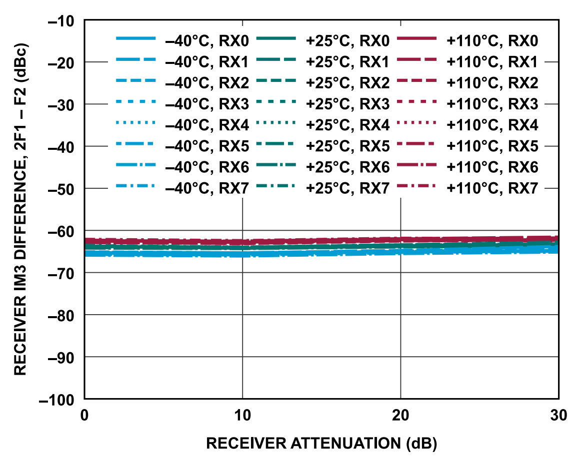

Figure 99. Receiver IM2, f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

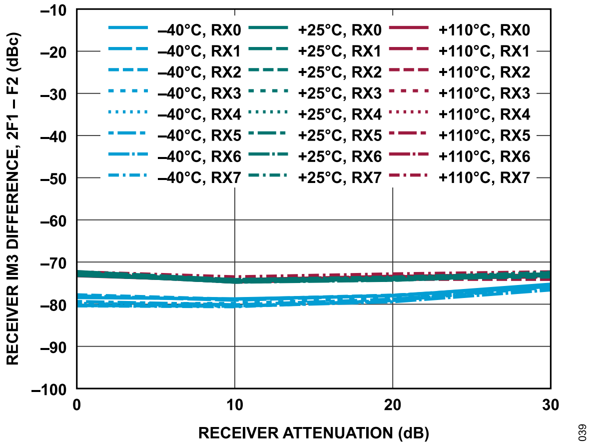

Figure 100. Receiver IM3, 2f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

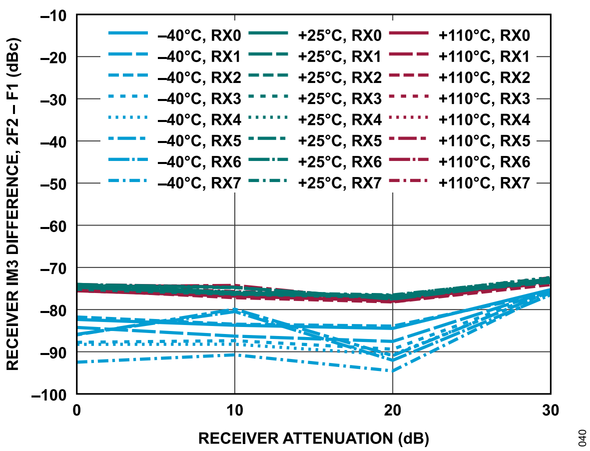

Figure 101. Receiver IM3, 2f2 − f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

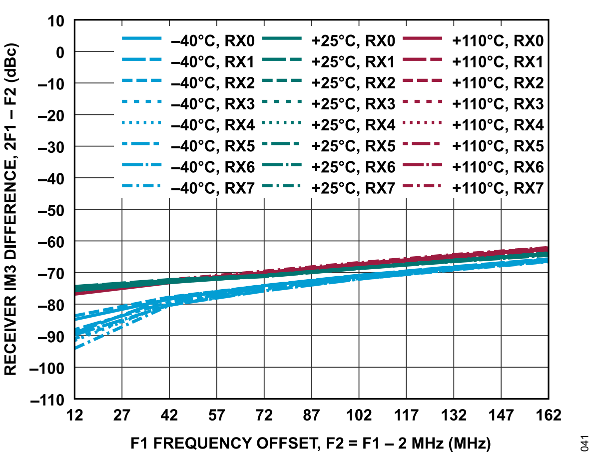

Figure 102. Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

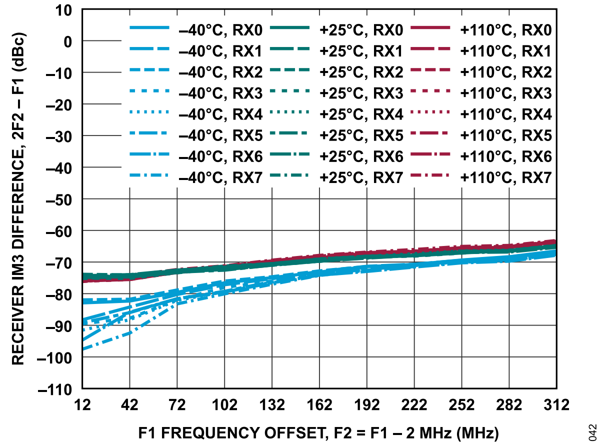

Figure 103. Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

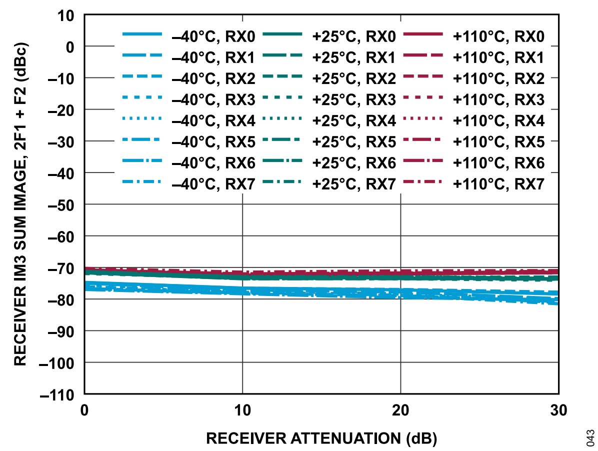

Figure 104. Receiver IM3, 2f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

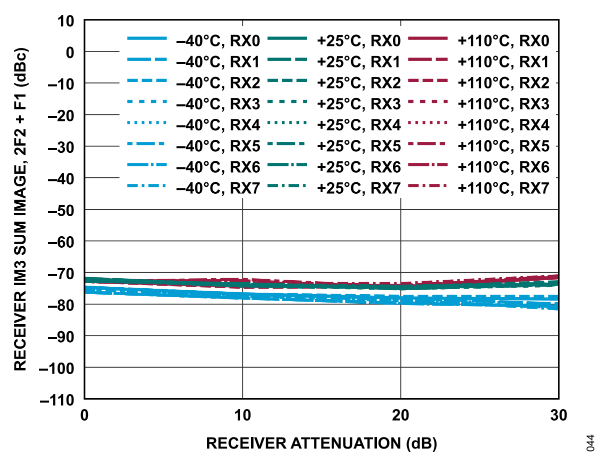

Figure 105. Receiver IM3, 2f2 + f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

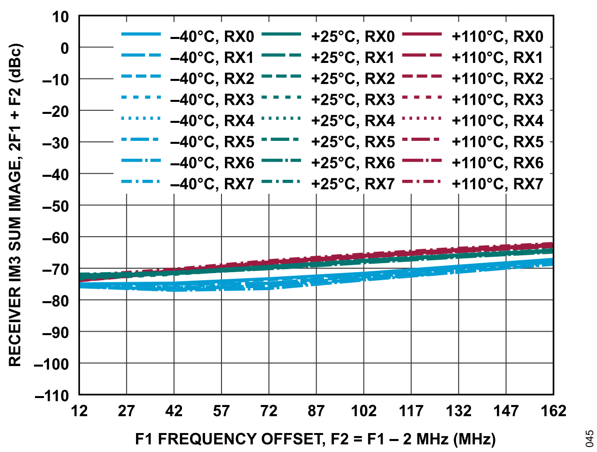

Figure 106. Receiver IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

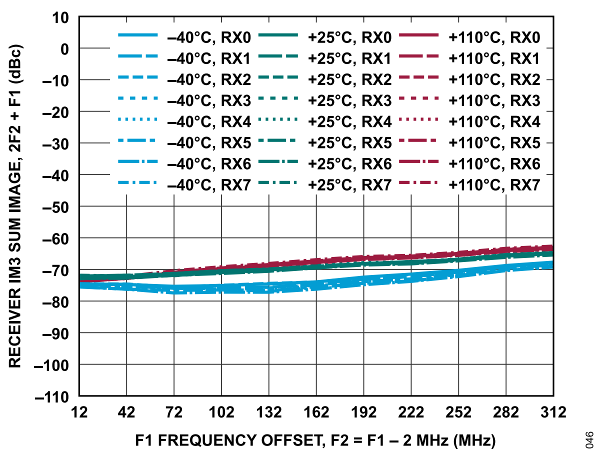

Figure 107. Receiver IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

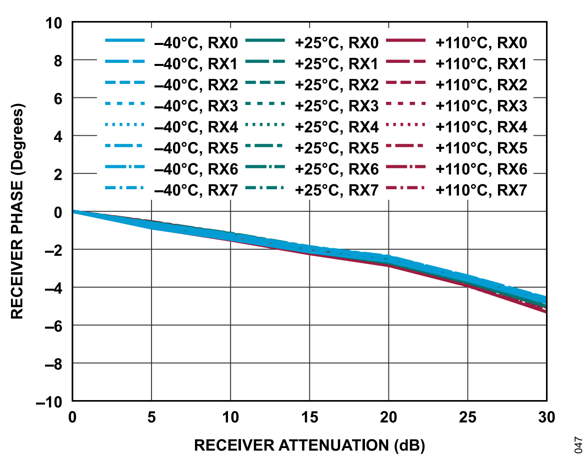

Figure 108. Receiver Phase vs. Receiver Attenuation

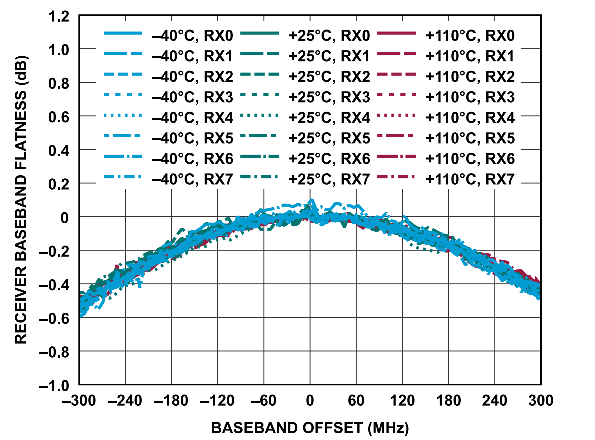

Figure 109. Receiver Baseband Flatness vs. Baseband Offset

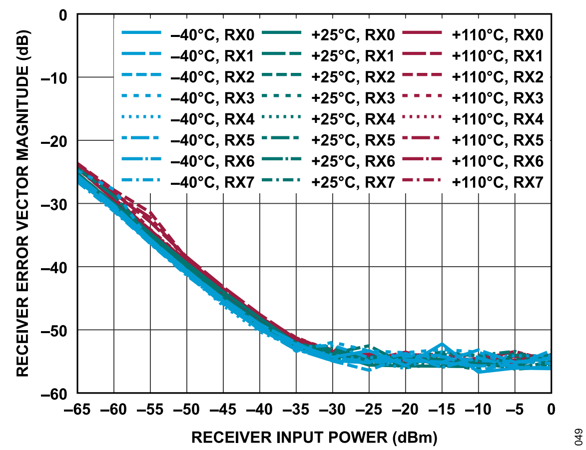

Figure 110. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Centered Around DC, TDD Mode, AGC Enabled

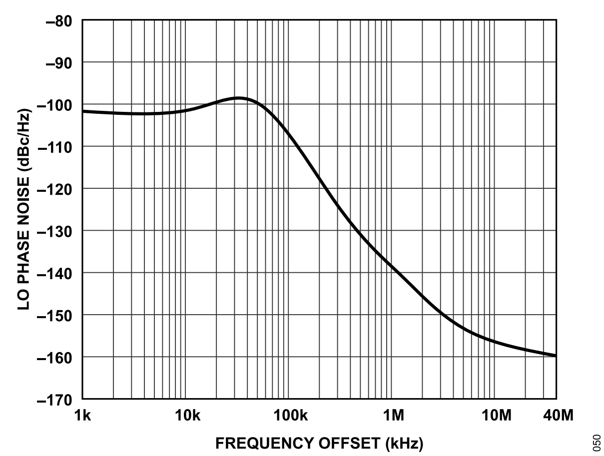

Figure 111. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 60 kHz, Phase Margin = 55º

TYPICAL PERFORMANCE CHARACTERISTICS

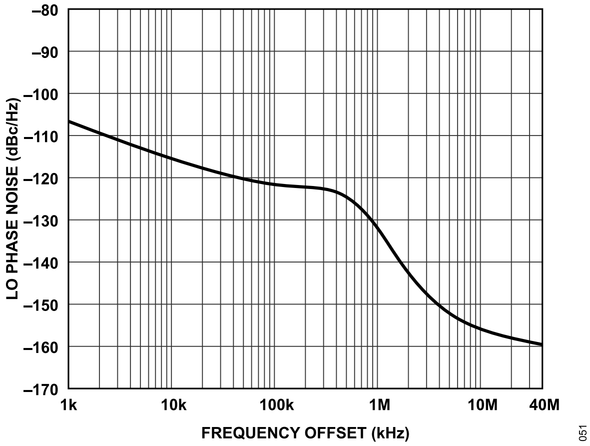

Figure 112. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 55°

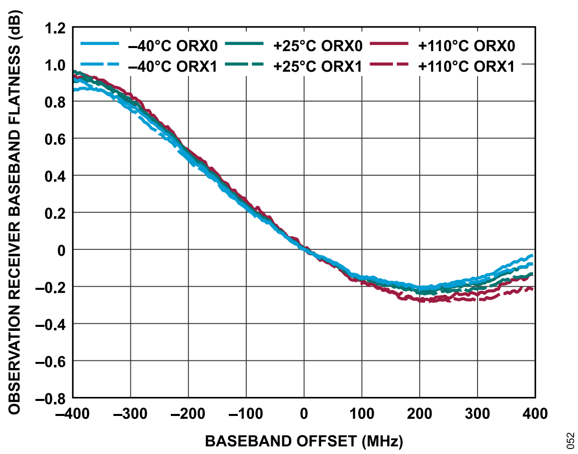

Figure 113. Observation Receiver Baseband Flatness vs. Baseband Offset

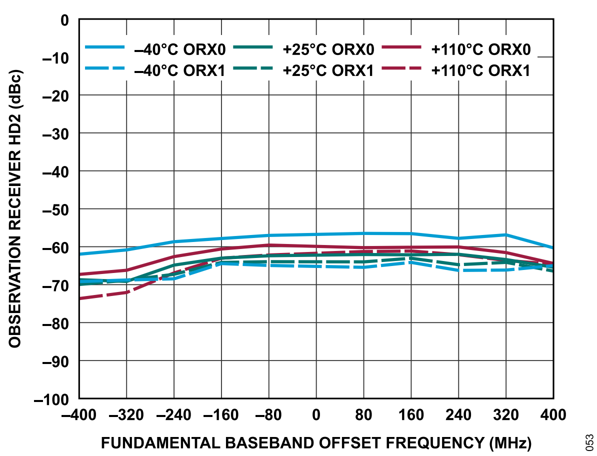

Figure 114. Observation Receiver HD2 vs. Baseband Offset Frequency, −10 dBFS Input Signal

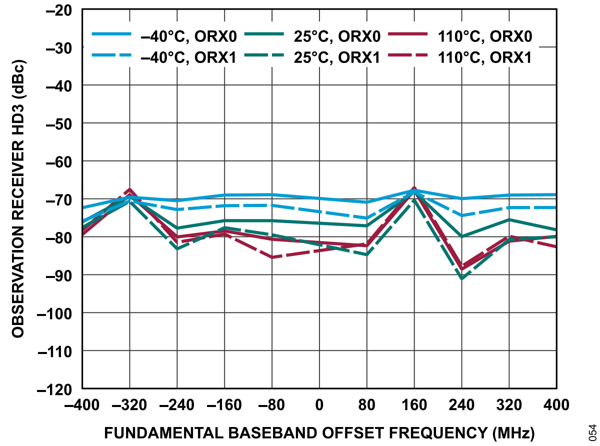

Figure 115. Observation Receiver HD3 vs. Baseband Offset Frequency, −10 dBFS Input Signal

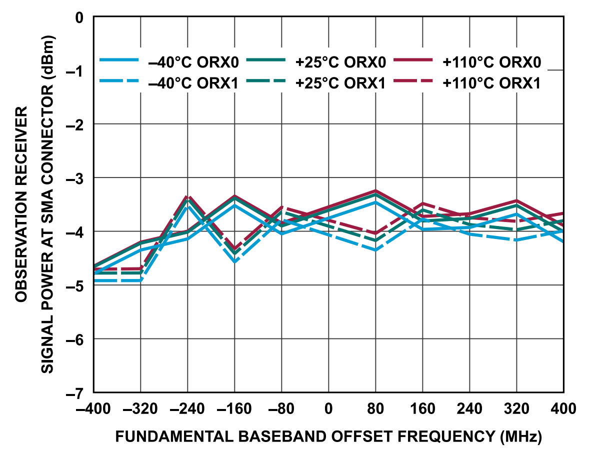

Figure 116. Observation Receiver Signal Power at SMA Connector vs. Baseband Frequency, −10 dBFS Input Signal (Match Is Not De−Embedded)

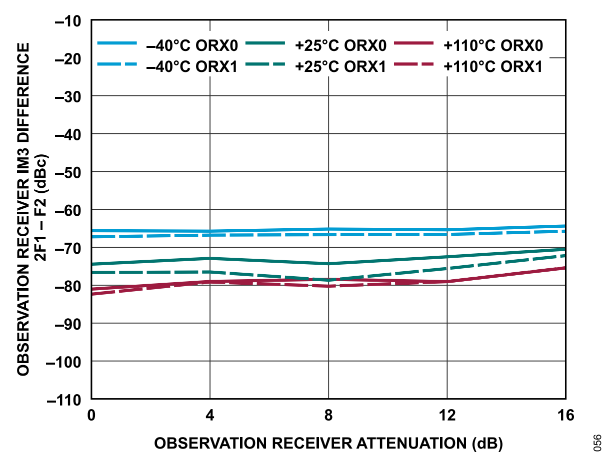

Figure 117. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 1802 MHz, f2 = 1812 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

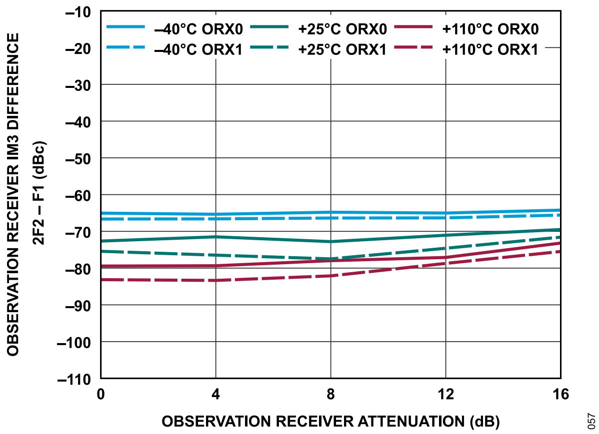

Figure 118. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 1802 MHz, f2 = 1812 MHz

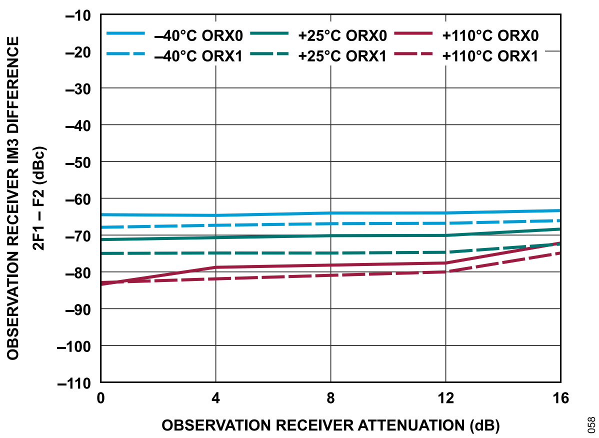

Figure 119. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 1802 MHz, f2 = 2012 MHz

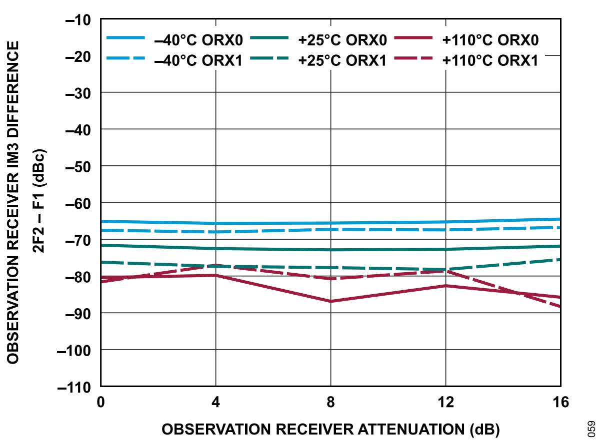

Figure 120. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 1802 MHz, f2 = 2012 MHz

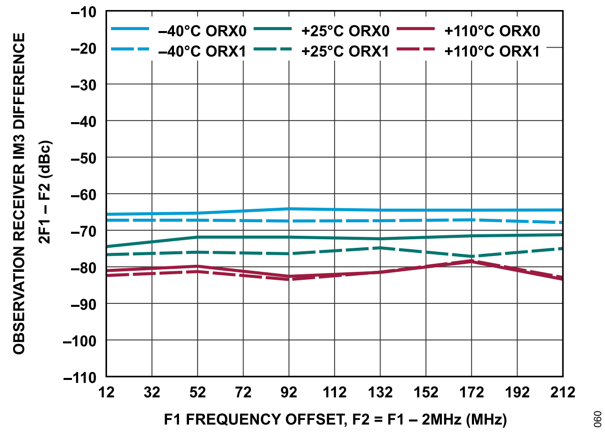

Figure 121. Observation Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 1802 MHz

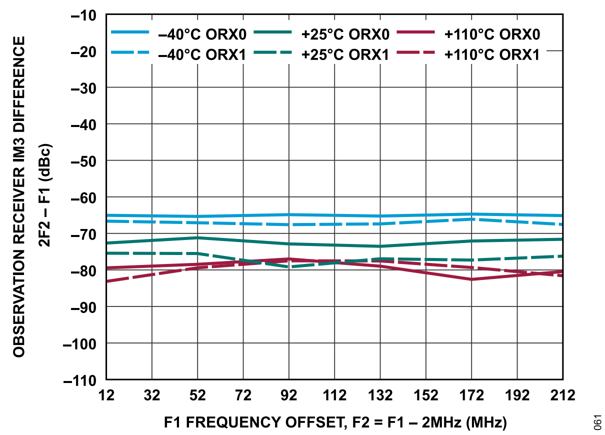

Figure 122. Observation Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 1802 MHz

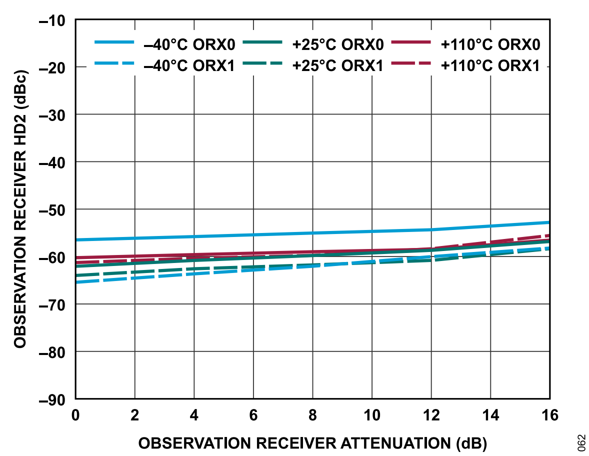

Figure 123. Observation Receiver HD2 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

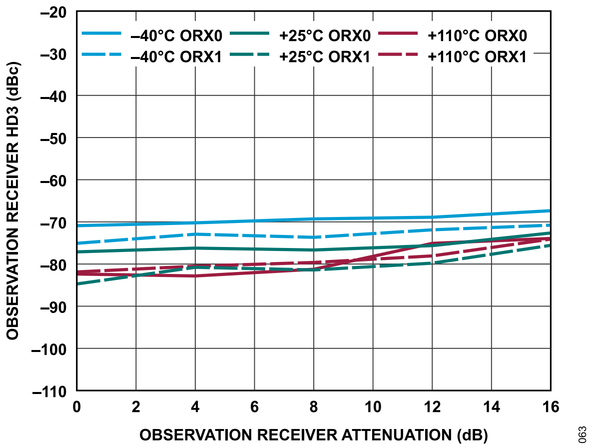

Figure 124. Observation Receiver HD3 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

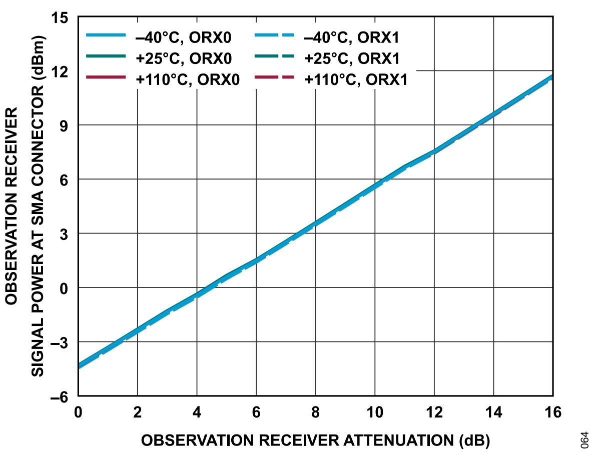

Figure 125. Observation Receiver Signal Power at SMA Connector vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

2600 MHZ BAND

The temperature settings refer to the die temperature. All LO frequencies set to 2600 MHz, unless otherwise noted. The observation receiver measurements are taken with 5898.24 MHz sampling frequency, unless otherwise noted.

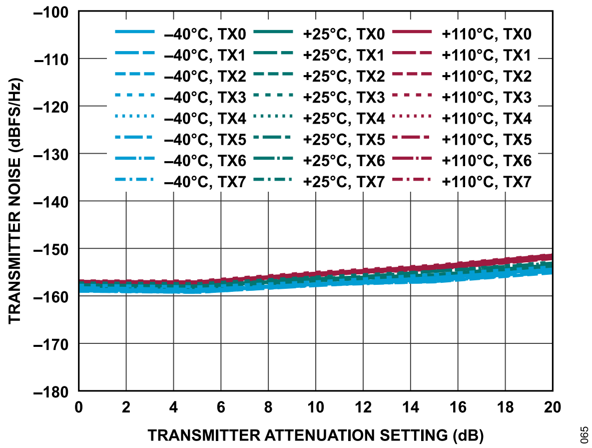

Figure 126. Transmitter Noise vs. Transmitter Attenuation, 150 MHz Offset

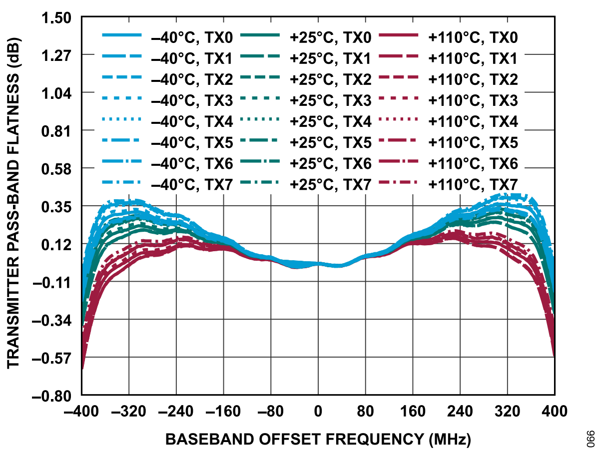

Figure 127. Transmitter Pass−Band Flatness vs. Baseband Offset Frequency

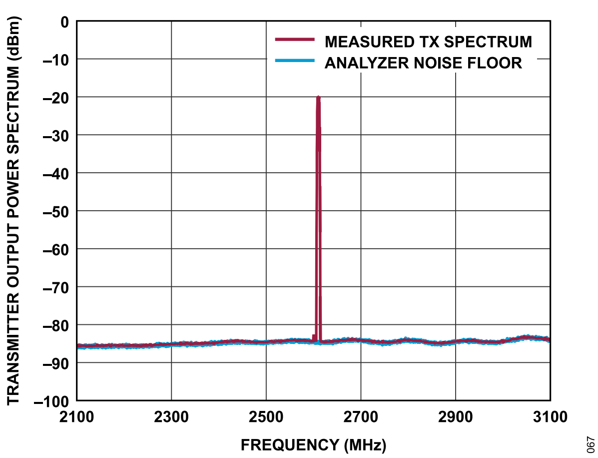

Figure 128. Transmitter Output Power Spectrum, Tx0, 5MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T_J = 25°C

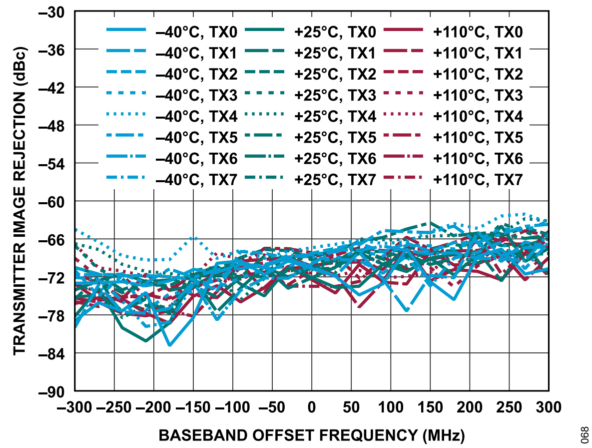

Figure 129. Transmitter Image Rejection vs. Baseband Offset Frequency, −6 dBFS Continuous Wave Signal

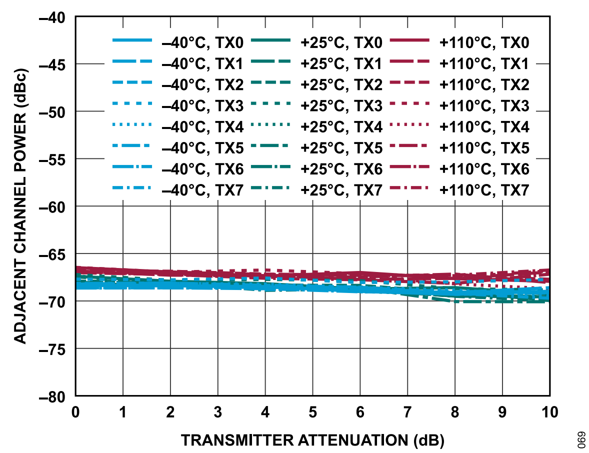

Figure 130. Adjacent Channel Power vs. Transmitter Attenuation, 290 MHz Offset, 20 MHz LTE, PAR = 12 dB

TYPICAL PERFORMANCE CHARACTERISTICS

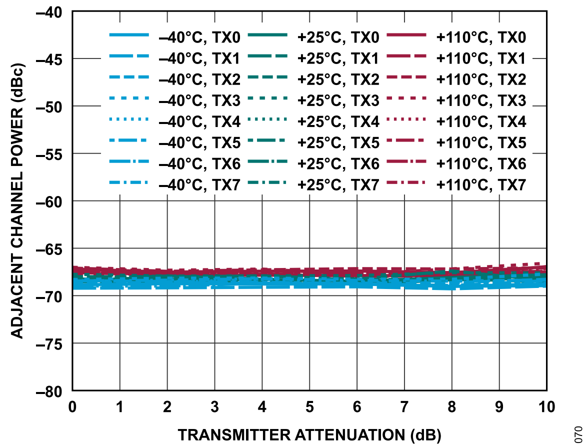

Figure 131. Adjacent Channel Power vs. Transmitter Attenuation, −10 MHz Offset, 20 MHz LTE, PAR = 12 dB

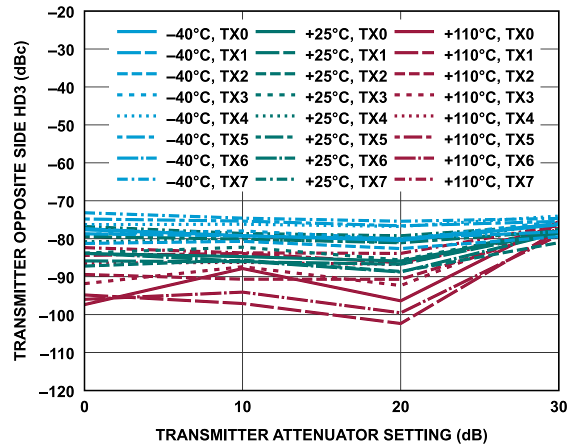

Figure 134. Transmitter Opposite Side Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

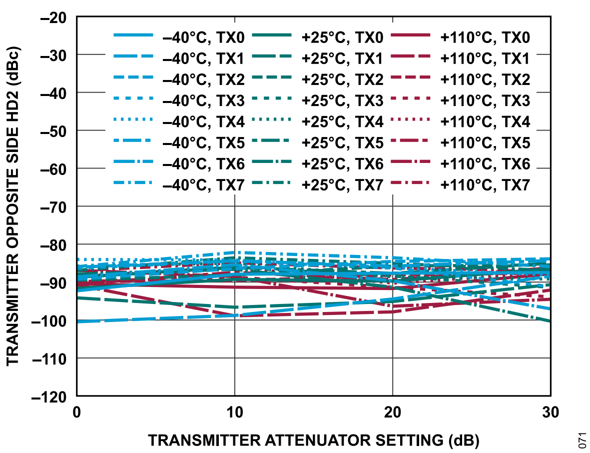

Figure 132. Transmitter Opposite Side Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

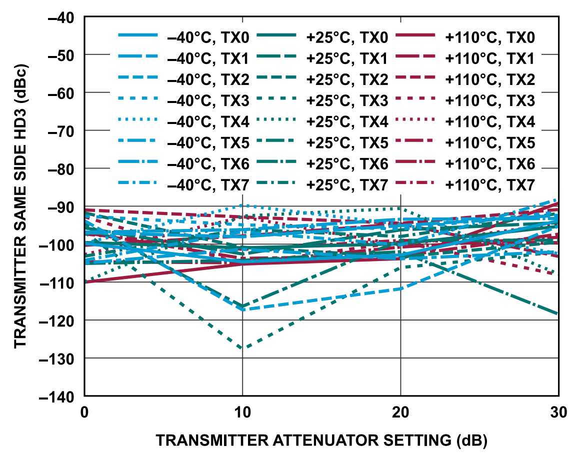

Figure 135. Transmitter Same Side HD3 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

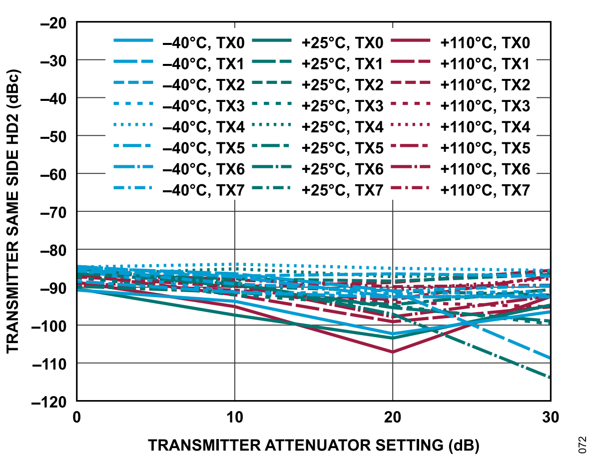

Figure 133. Transmitter Same Side HD2 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

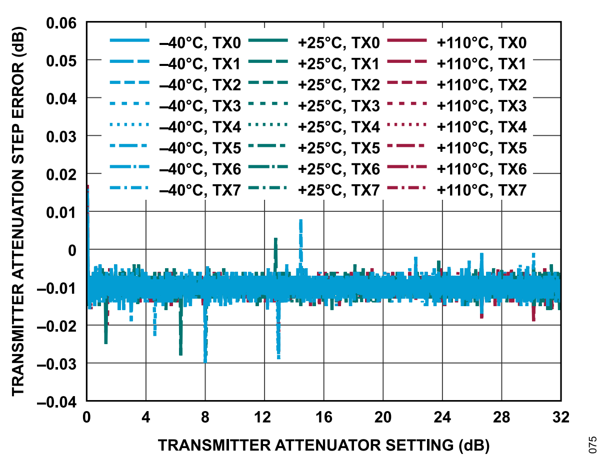

Figure 136. Transmitter Attenuation Step Error vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

TYPICAL PERFORMANCE CHARACTERISTICS

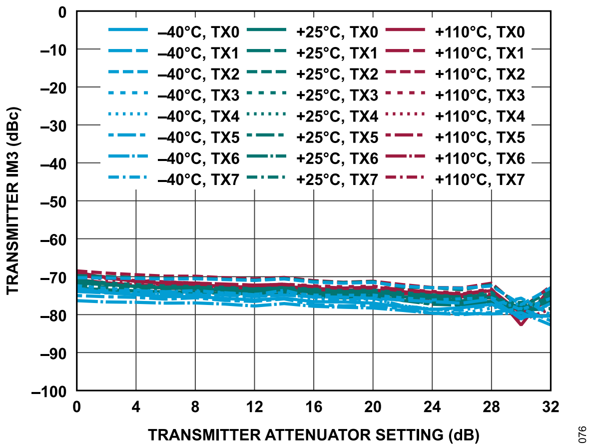

Figure 137. Transmitter IM3, 2f1 − f2 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

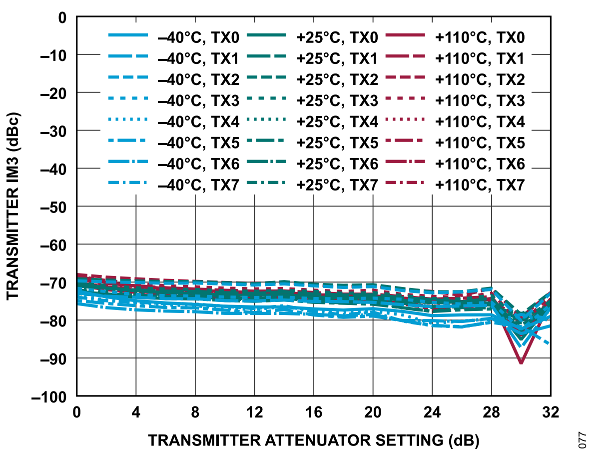

Figure 138. Transmitter IM3, 2f2 − f1 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

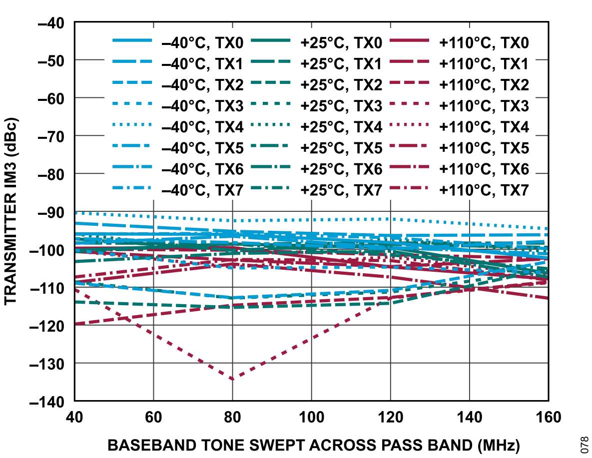

Figure 139. Transmitter IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

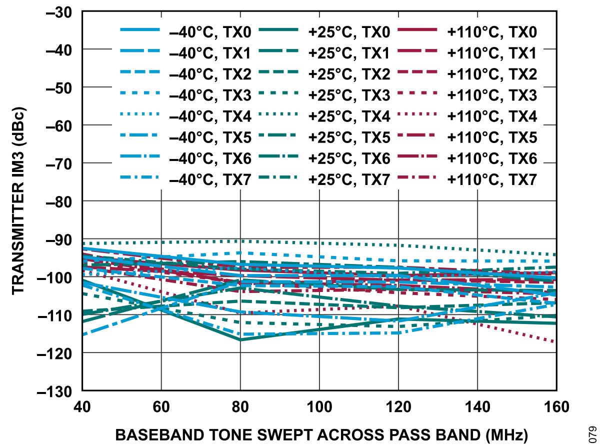

Figure 140. Transmitter IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

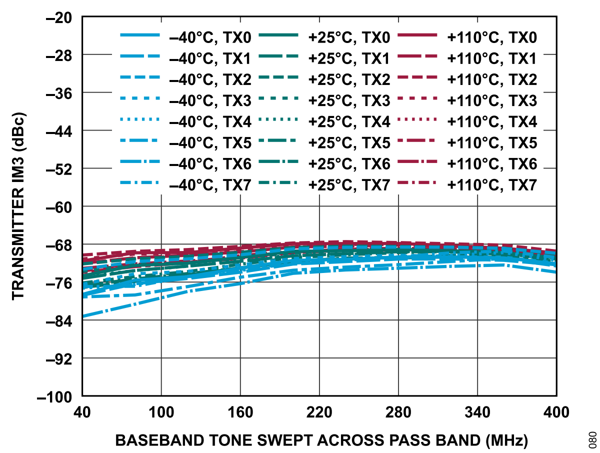

Figure 141. Transmitter IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

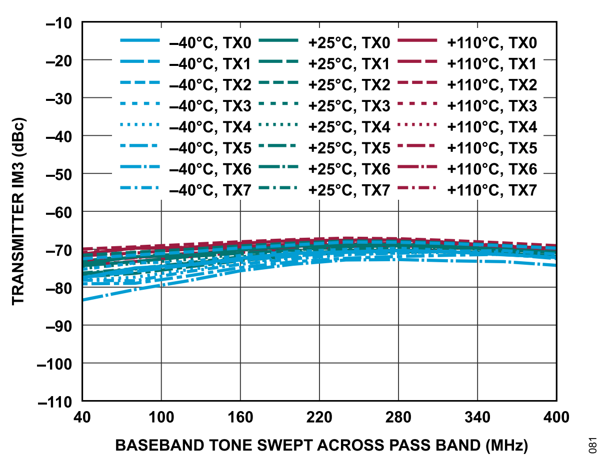

Figure 142. Transmitter IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

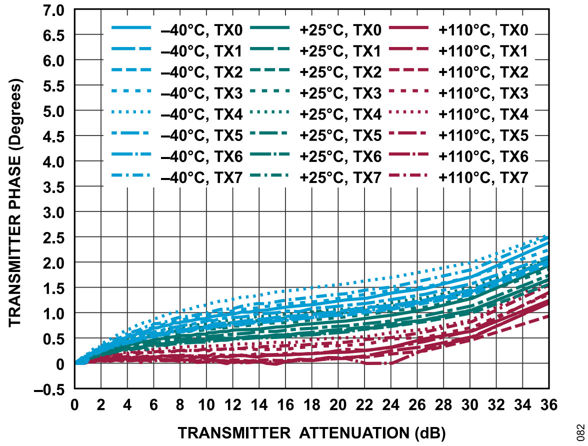

Figure 143. Transmitter Phase vs. Transmitter Attenuation

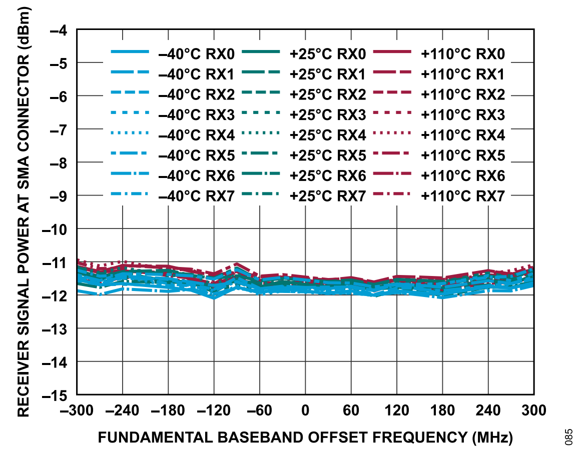

Figure 146. Receiver Signal Power at SMA Connector vs. Baseband Offset Frequency, −1 dBFS Input Signal (Match Is Not De−Embedded)

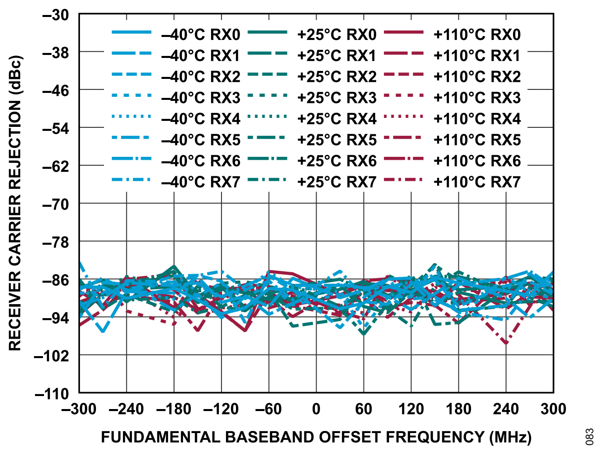

Figure 144. Receiver Carrier Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

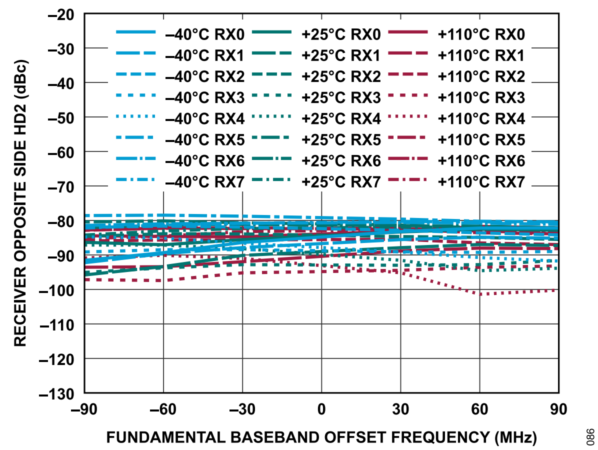

Figure 147. Receiver Opposite Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

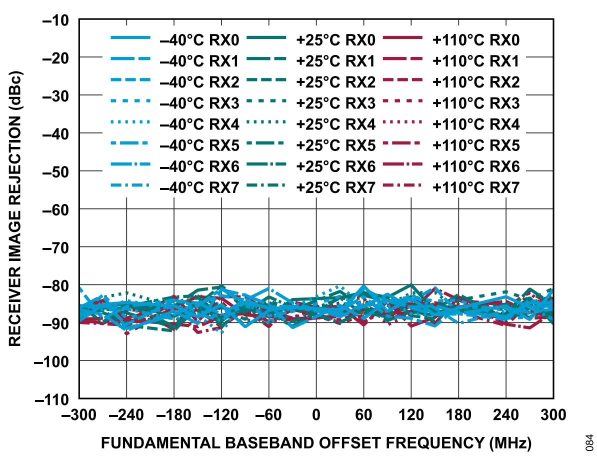

Figure 145. Receiver Image Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

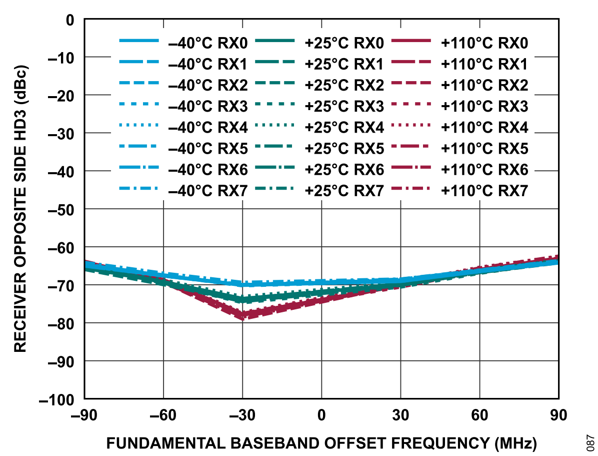

Figure 148. Receiver Opposite Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

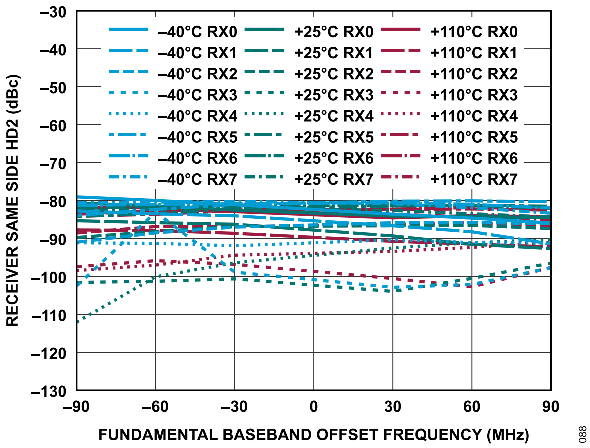

Figure 149. Receiver Same Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

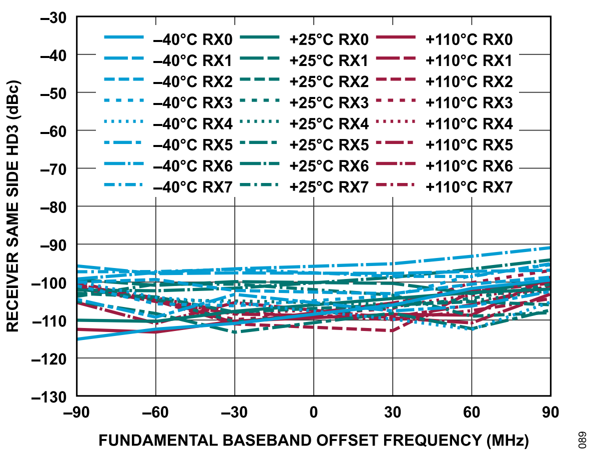

Figure 150. Receiver Same Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

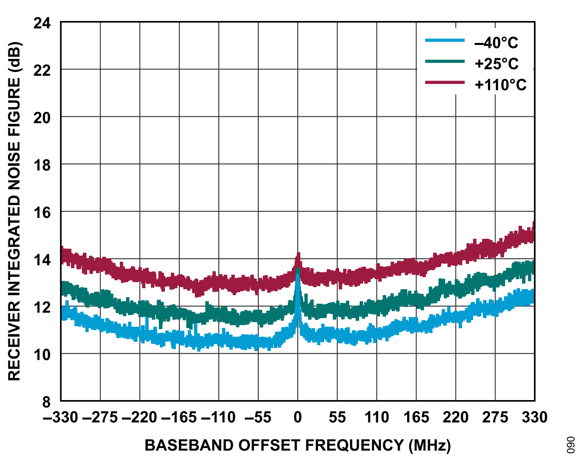

Figure 151. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 kHz Integration Steps, 983.04 MSPS Sample Rate

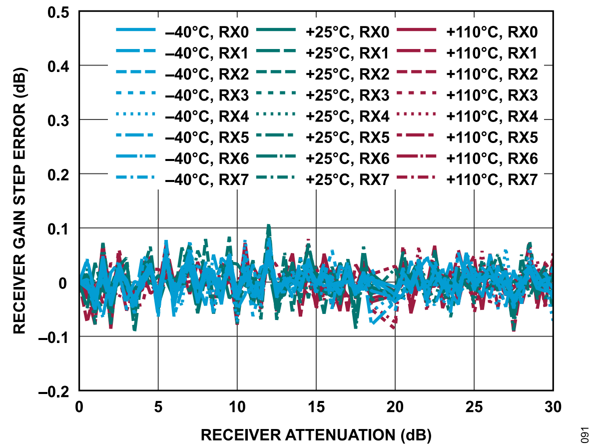

Figure 152. Receiver Gain Step Error vs. Attenuation, 30 MHz Offset, −1 dBFS Input Signal

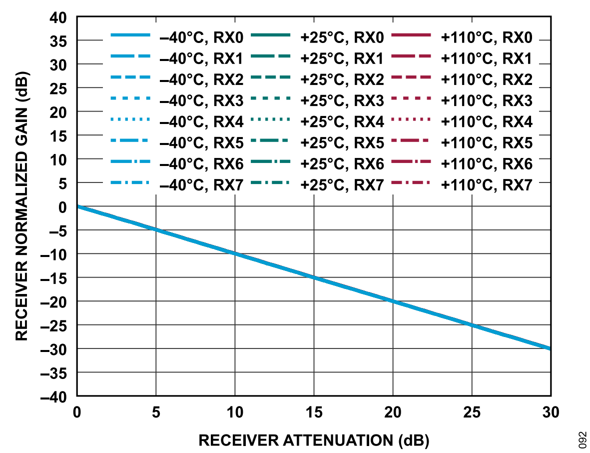

Figure 153. Receiver Normalized Gain vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

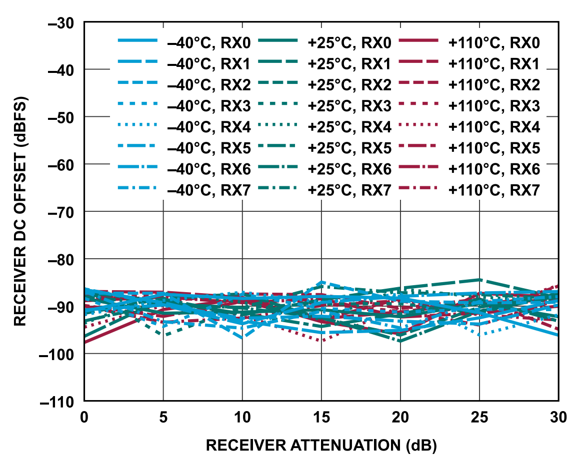

Figure 154. Receiver DC Offset vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

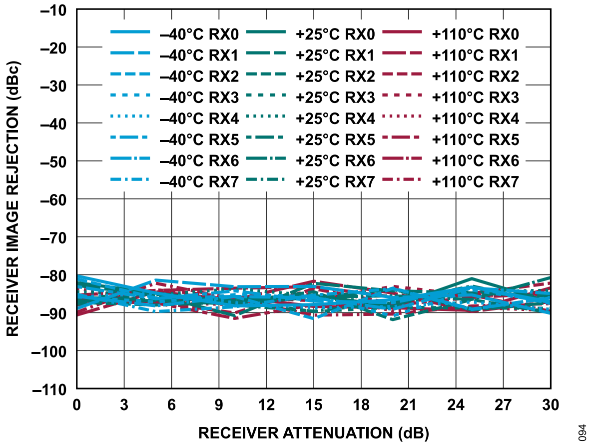

Figure 155. Receiver Image vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

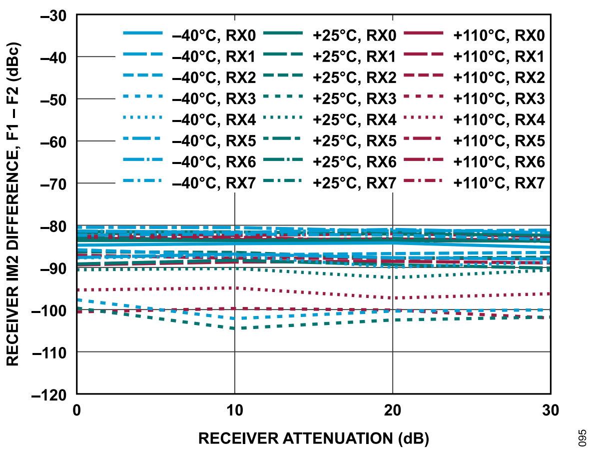

Figure 156. Receiver IM2, f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

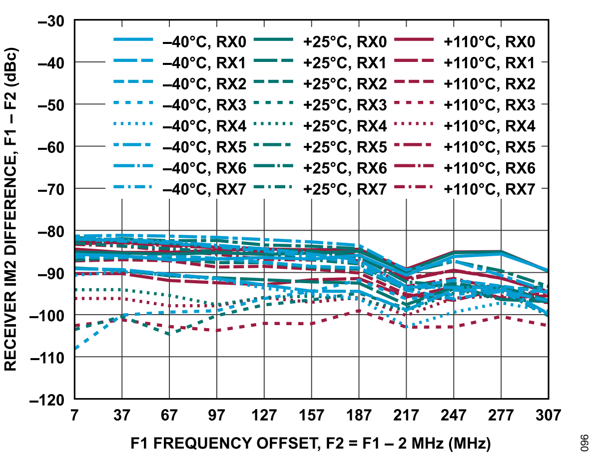

Figure 157. Receiver IM2, f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

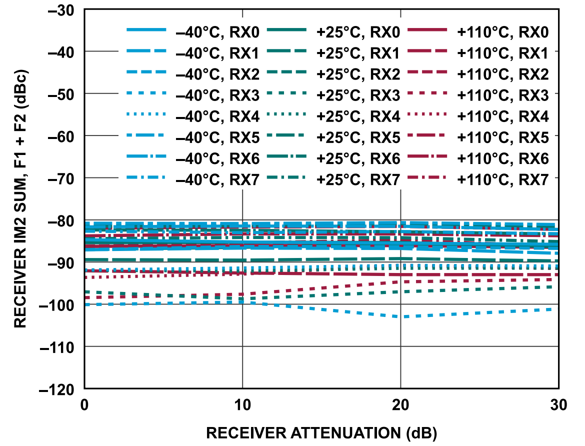

Figure 158. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

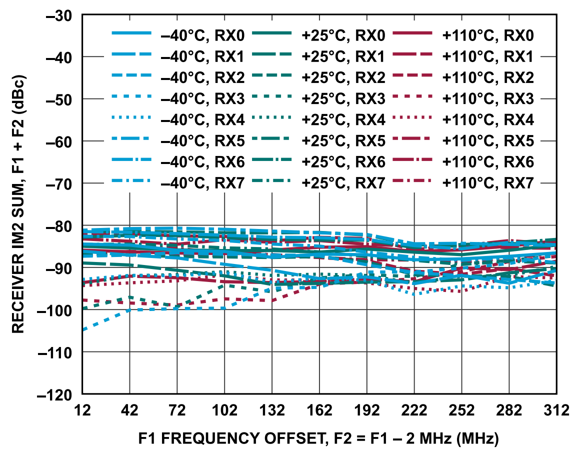

Figure 159. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 282 MHz Offset, f2 = 2 MHz Offset

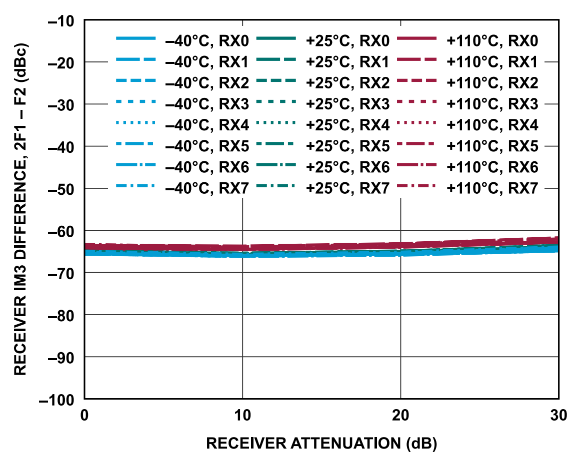

Figure 160. Receiver IM2, f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

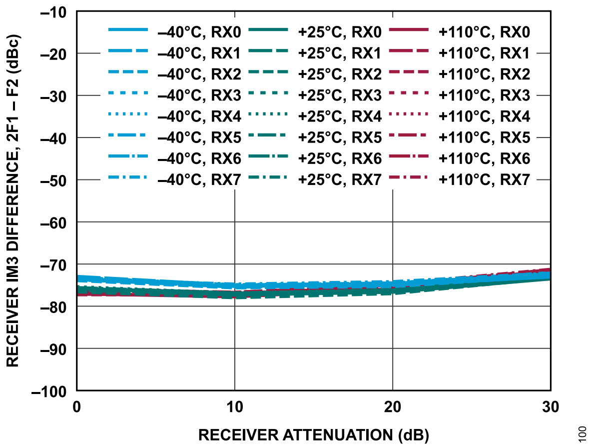

Figure 161. Receiver IM3, 2f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

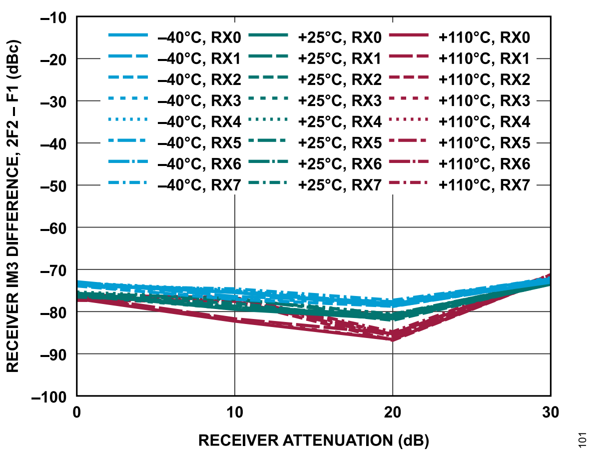

Figure 162. Receiver IM3, 2f2 − f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

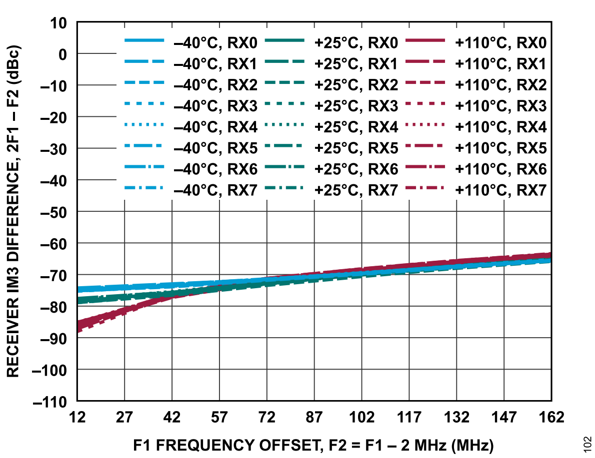

Figure 163. Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

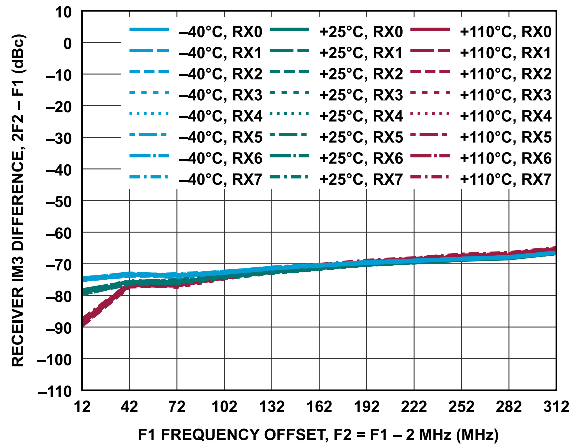

Figure 164. Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

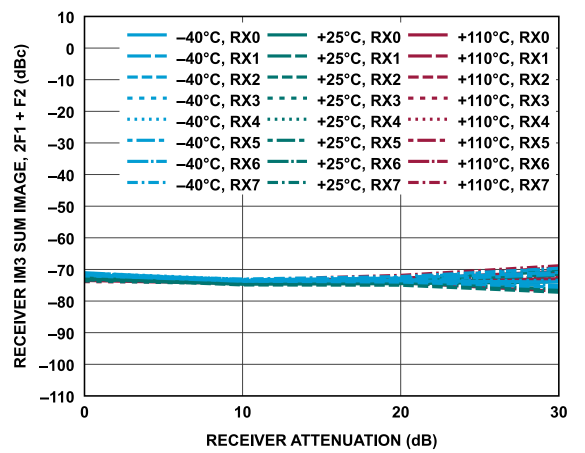

Figure 165. Receiver IM3, 2f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

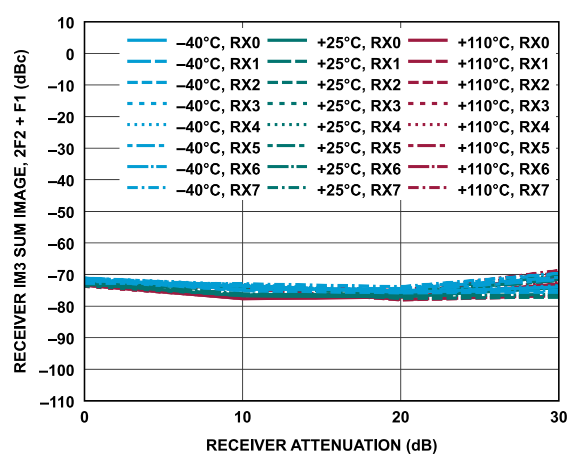

Figure 166. Receiver IM3, 2f2 + f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

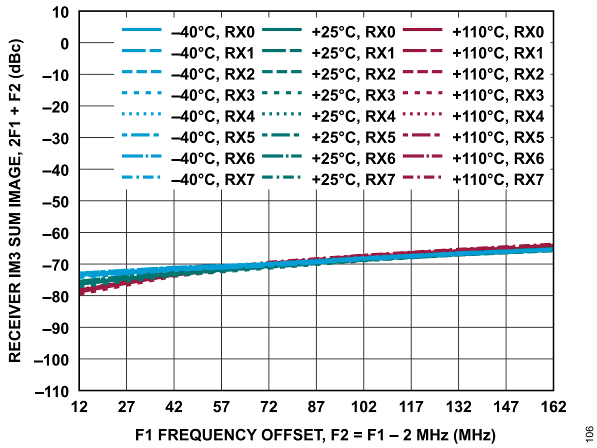

Figure 167. Receiver IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

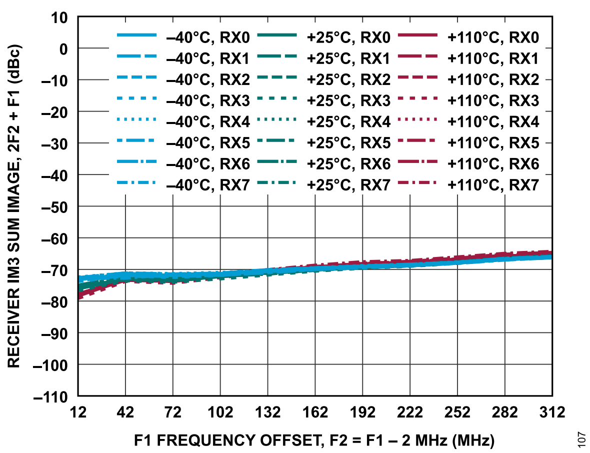

Figure 168. Receiver IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

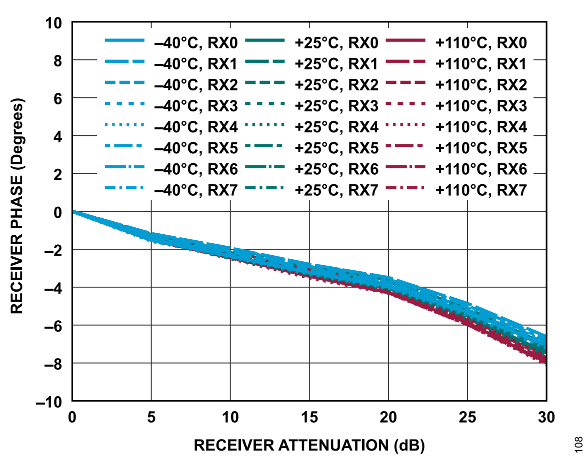

Figure 169. Receiver Phase vs. Receiver Attenuation

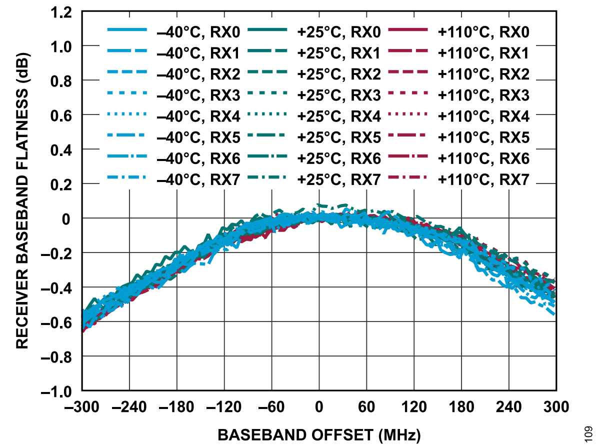

Figure 170. Receiver Baseband Flatness vs. Baseband Offset

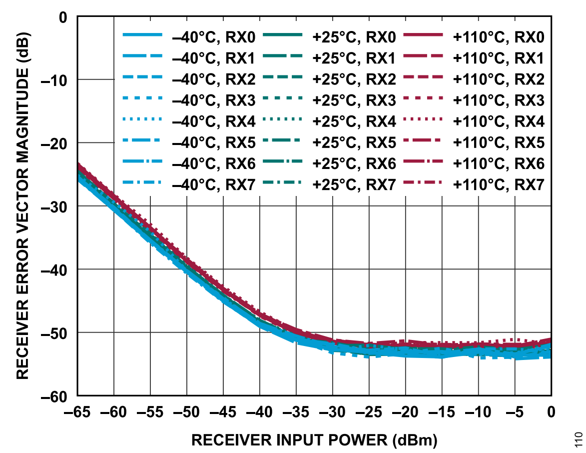

Figure 171. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Centered Around DC, TDD Mode, AGC Enabled

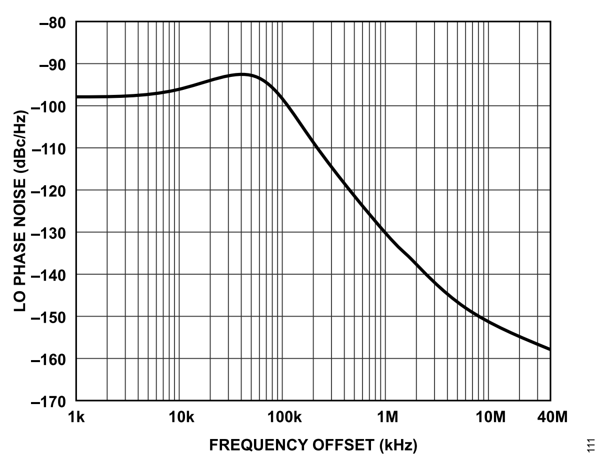

Figure 172. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 60 kHz, Phase Margin = 55°

TYPICAL PERFORMANCE CHARACTERISTICS

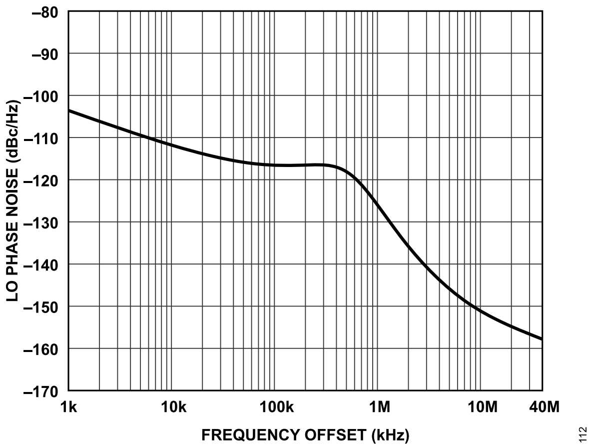

Figure 173. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 55°

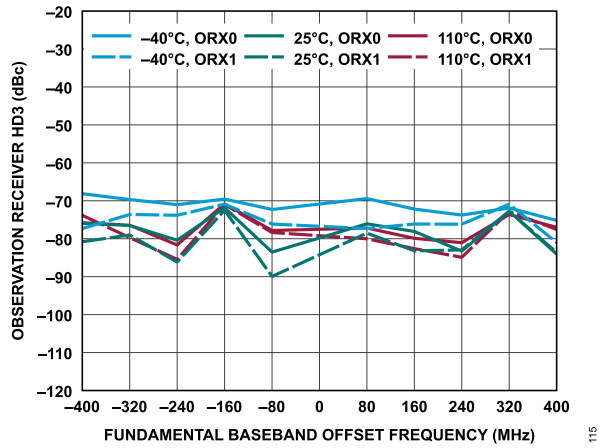

Figure 176. Observation Receiver HD3 vs. Baseband Offset Frequency, −10 dBFS Input Signal

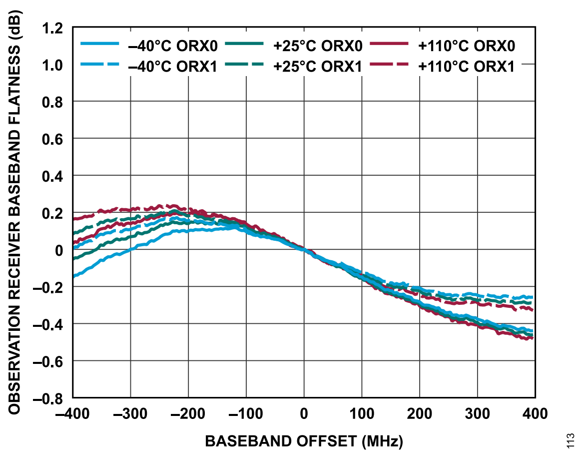

Figure 174. Observation Receiver Baseband Flatness vs. Baseband Offset

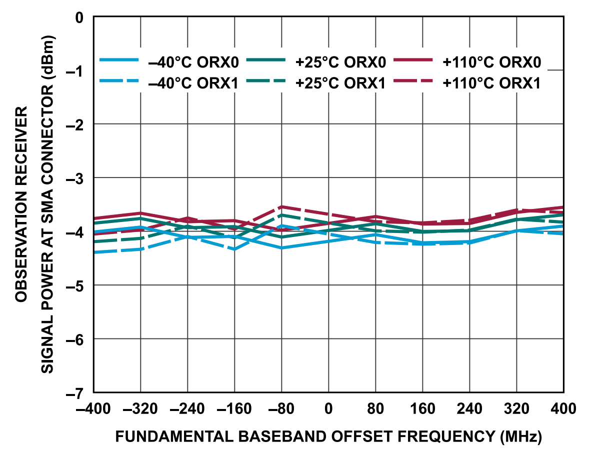

Figure 177. Observation Receiver Signal Power at SMA Connector vs. Baseband Frequency, −10 dBFS Input Signal (Match Is Not De−Embedded)

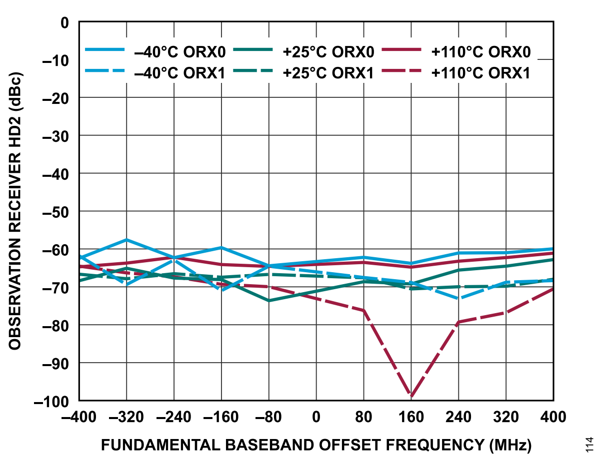

Figure 175. Observation Receiver HD2 vs. Baseband Offset Frequency, −10 dBFS Input Signal

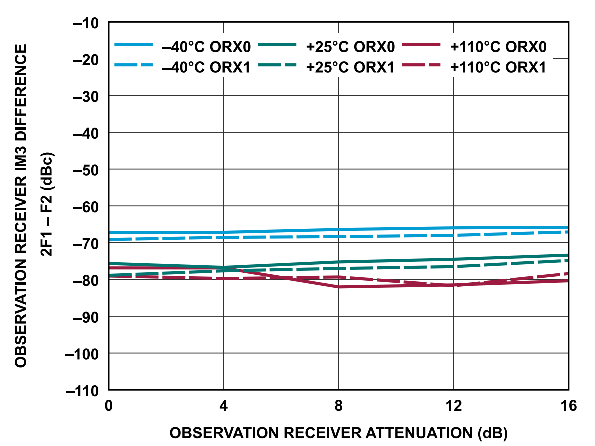

Figure 178. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 2602 MHz, f2 = 2612 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

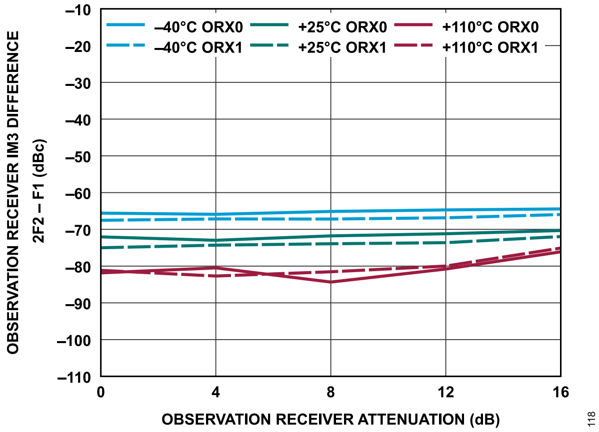

Figure 179. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 2602 MHz, f2 = 2612 MHz

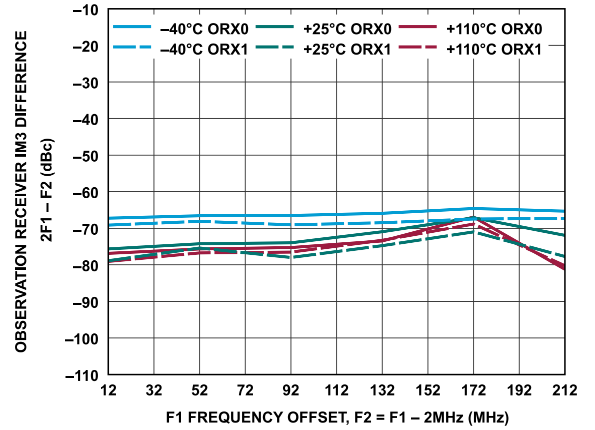

Figure 182. Observation Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 2602 MHz

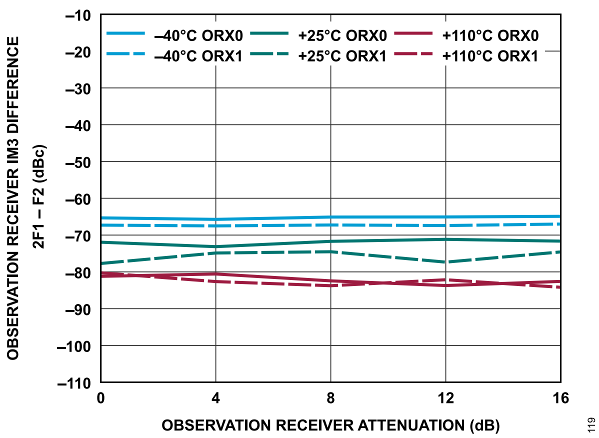

Figure 180. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 2602 MHz, f2 = 2812 MHz

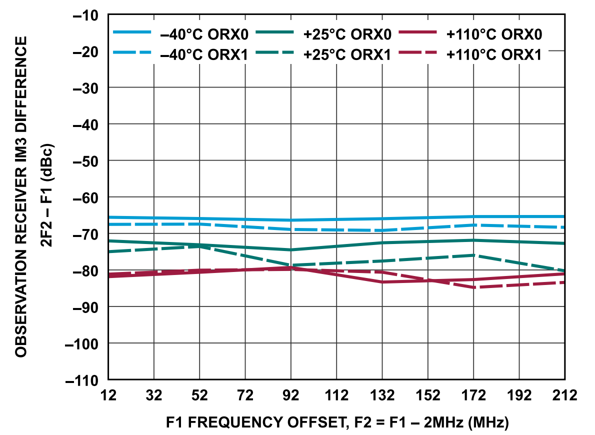

Figure 183. Observation Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 2602 MHz

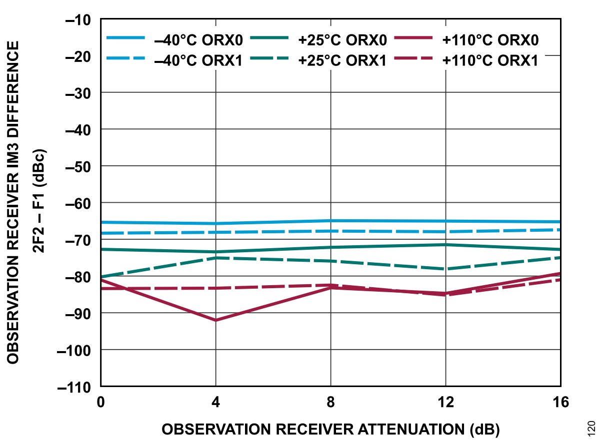

Figure 181. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 2602 MHz, f2 = 2812 MHz

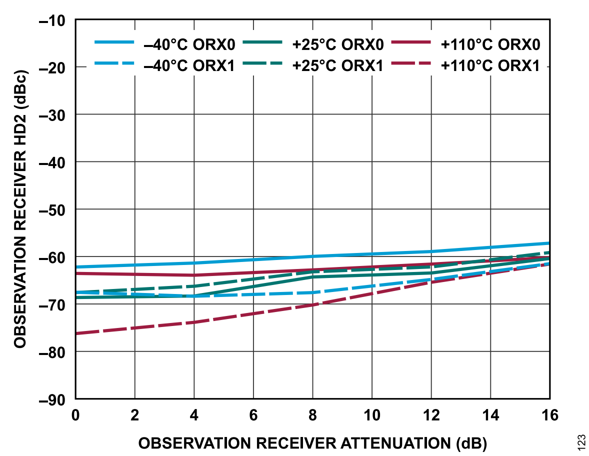

Figure 184. Observation Receiver HD2 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

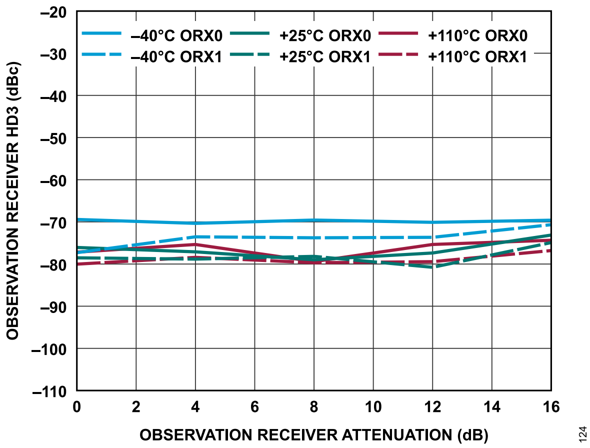

Figure 185. Observation Receiver HD3 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

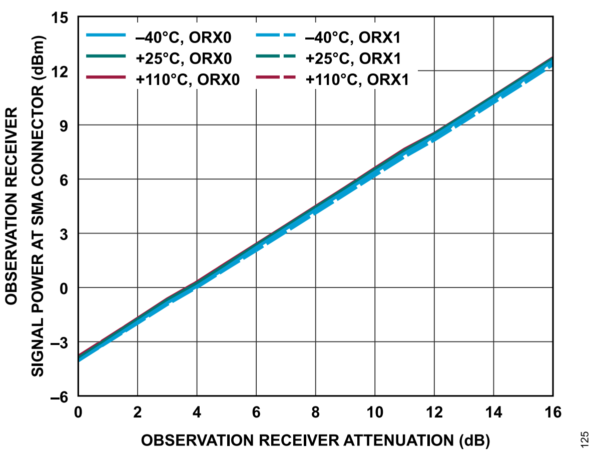

Figure 186. Observation Receiver Signal Power at SMA Connector vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

3500 MHZ BAND

The temperature settings refer to the die temperature. All LO frequencies set to 3500 MHz, unless otherwise noted. The observation receiver measurements are taken with 5898.24 MHz sampling frequency, unless otherwise noted.

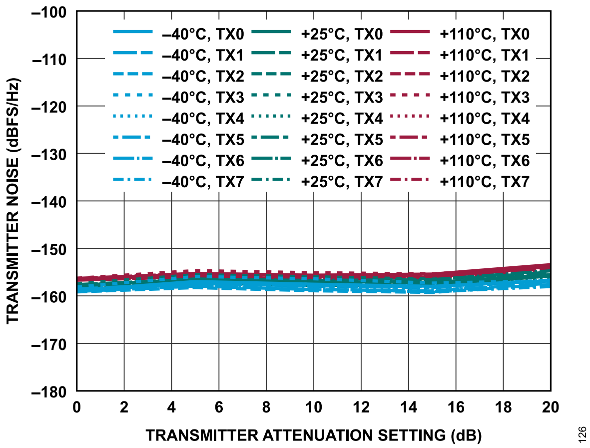

Figure 187. Transmitter Noise vs. Transmitter Attenuation, 150 MHz Offset

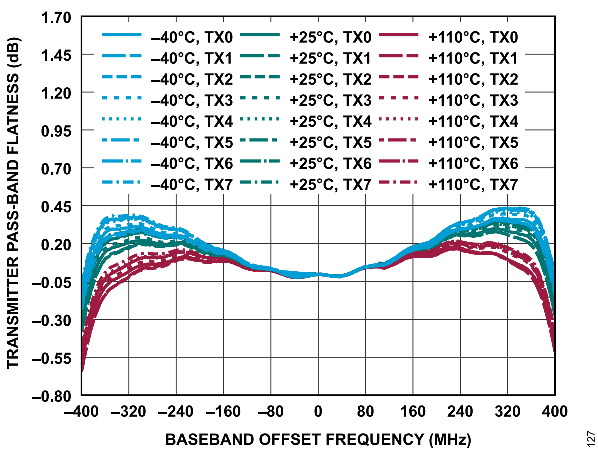

Figure 188. Transmitter Pass−Band Flatness vs. Baseband Offset Frequency

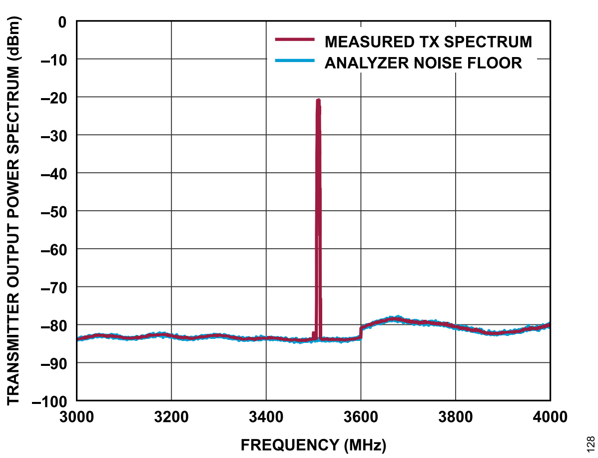

Figure 189. Transmitter Output Power Spectrum, Tx0, 5MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T_J = 25°C

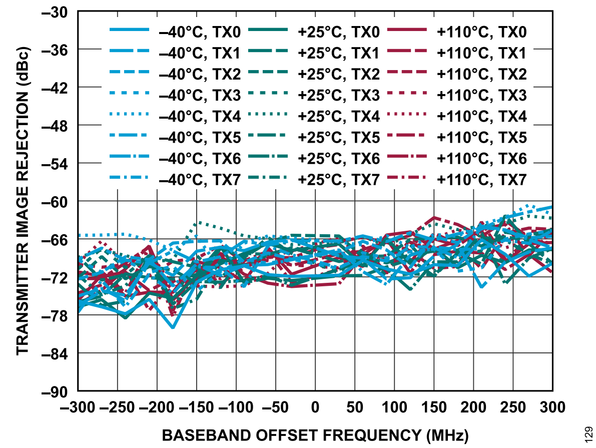

Figure 190. Transmitter Image Rejection vs. Baseband Offset Frequency, −6 dBFS Continuous Wave Signal

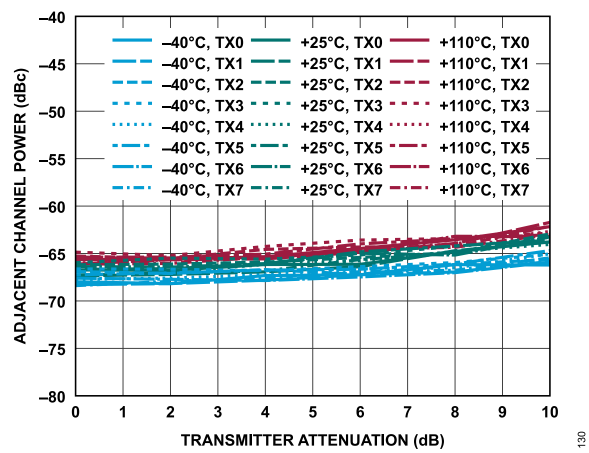

Figure 191. Adjacent Channel Power vs. Transmitter Attenuation, 290 MHz Offset, 20 MHz LTE, PAR = 12 dB

TYPICAL PERFORMANCE CHARACTERISTICS

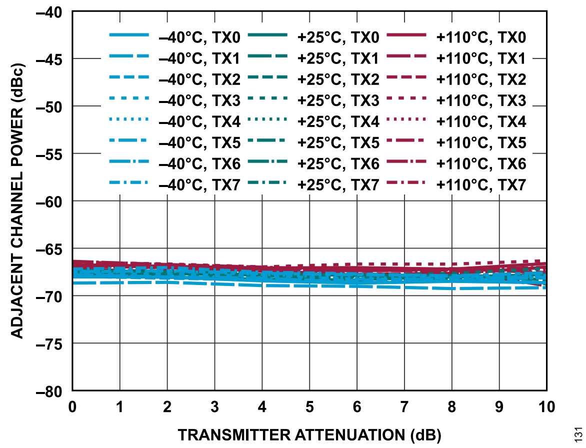

Figure 192. Adjacent Channel Power vs. Transmitter Attenuation, −10 MHz Offset, 20 MHz LTE, PAR = 12 dB

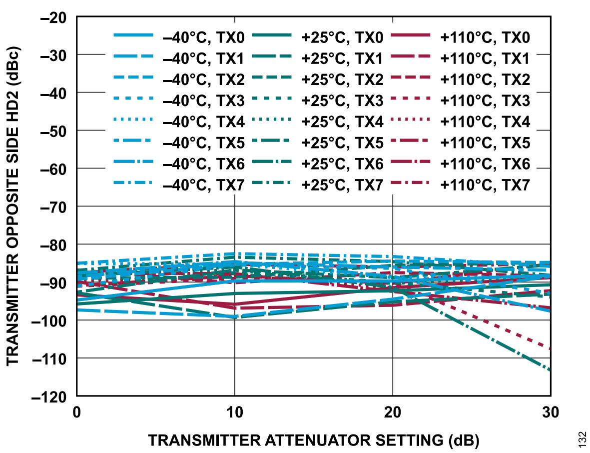

Figure 193. Transmitter Opposite Side Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

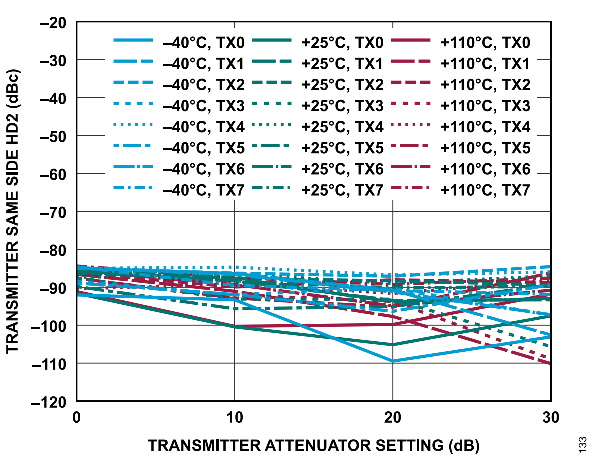

Figure 194. Transmitter Same Side HD2 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

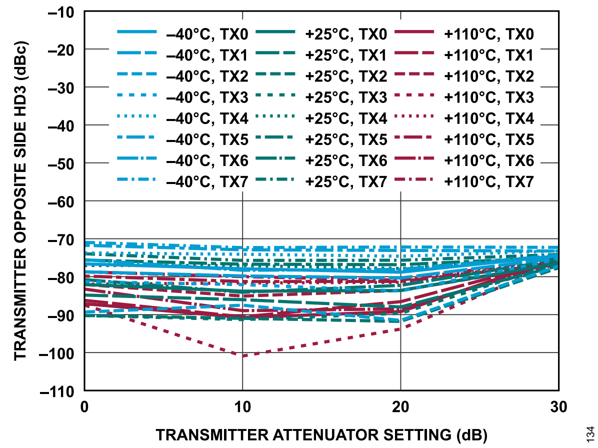

Figure 195. Transmitter Opposite Side HD3 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

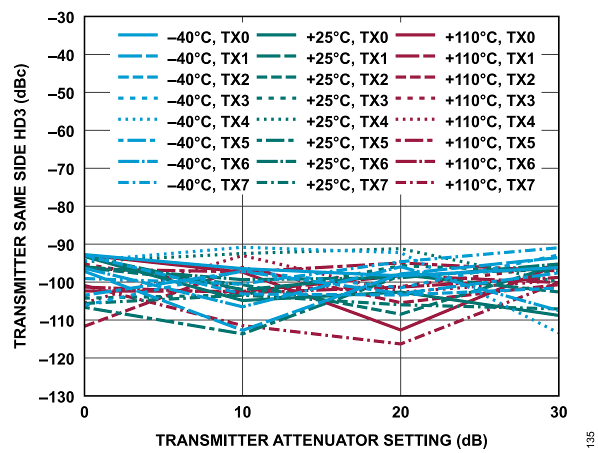

Figure 196. Transmitter Same Side HD3 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

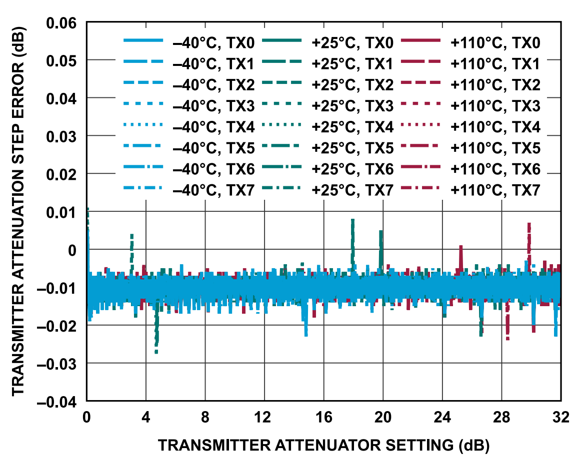

Figure 197. Transmitter Attenuation Step Error vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

TYPICAL PERFORMANCE CHARACTERISTICS

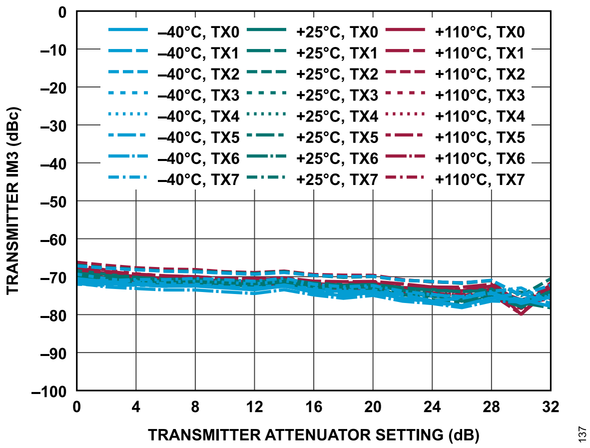

Figure 198. Transmitter IM3, 2f1 − f2 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

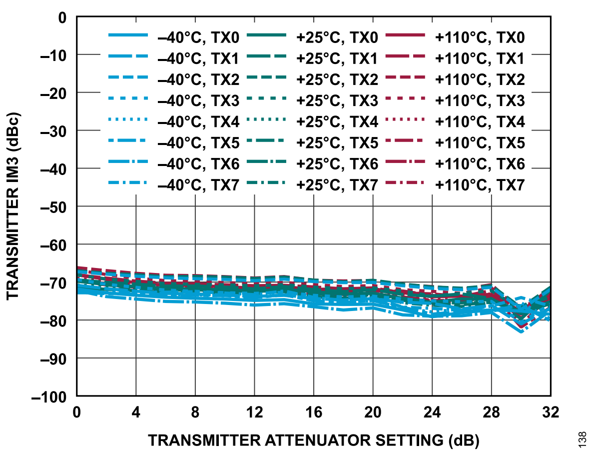

Figure 199. Transmitter IM3, 2f2 − f1 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

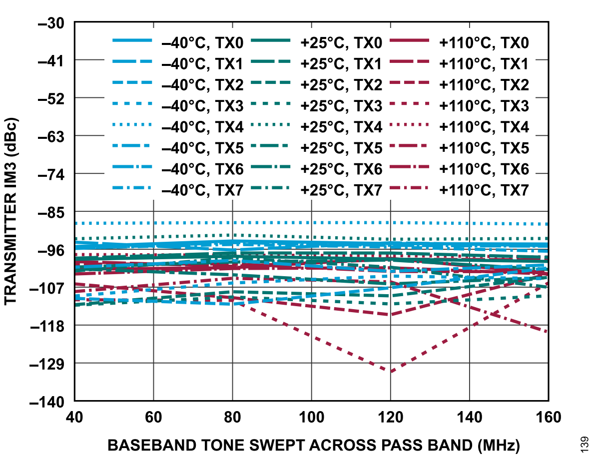

Figure 200. Transmitter IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

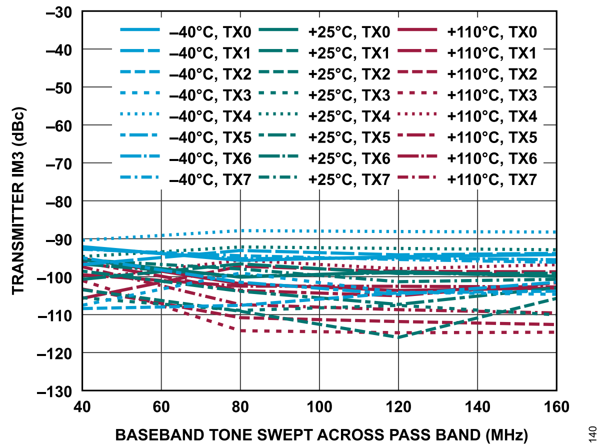

Figure 201. Transmitter IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

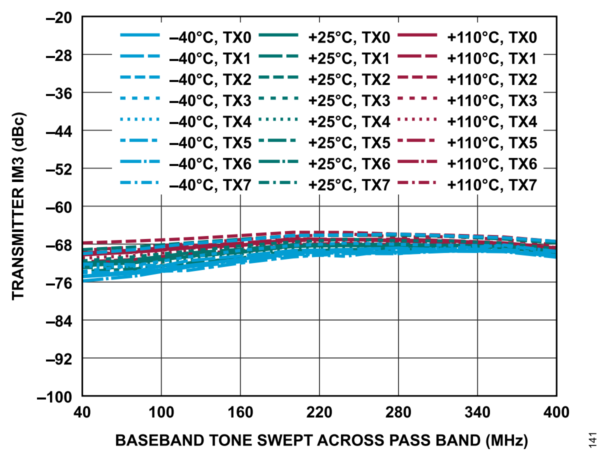

Figure 202. Transmitter IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

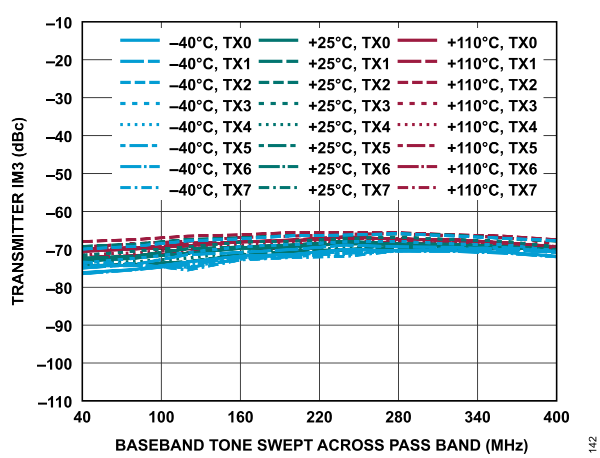

Figure 203. Transmitter IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

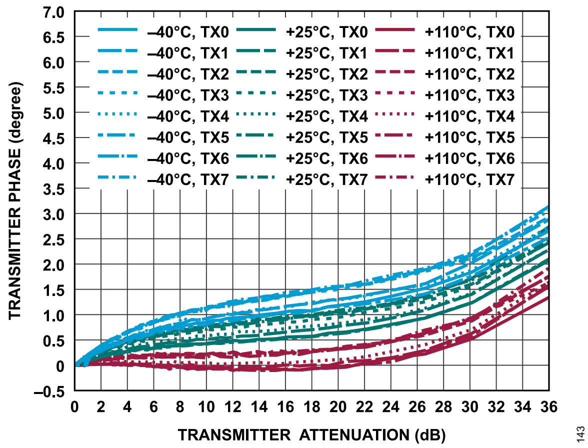

Figure 204. Transmitter Phase vs. Transmitter Attenuation

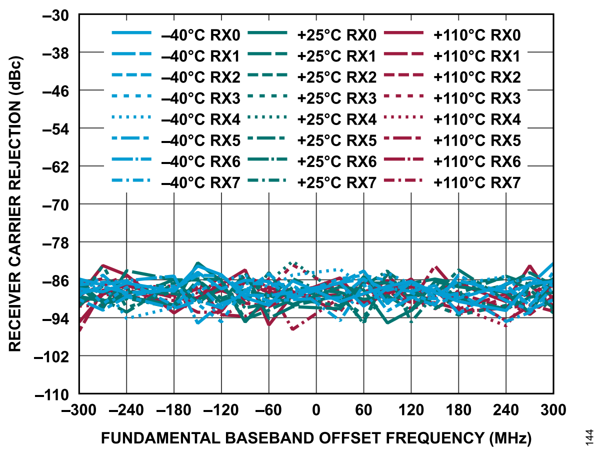

Figure 205. Receiver Carrier Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

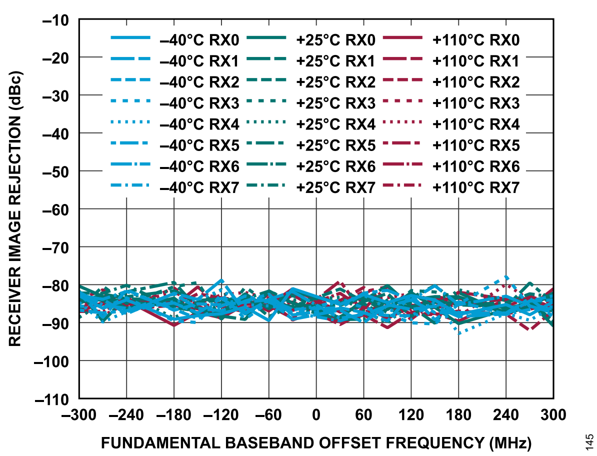

Figure 206. Receiver Image Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

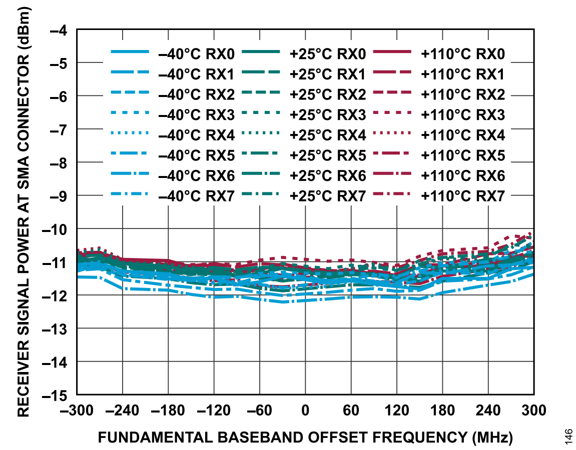

Figure 207. Receiver Signal Power at SMA Connector vs. Baseband Offset Frequency, −1 dBFS Input Signal (Match Is Not De−Embedded)

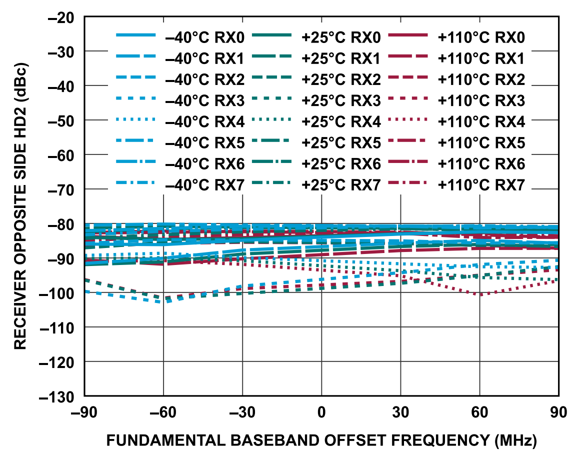

Figure 208. Receiver Opposite Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

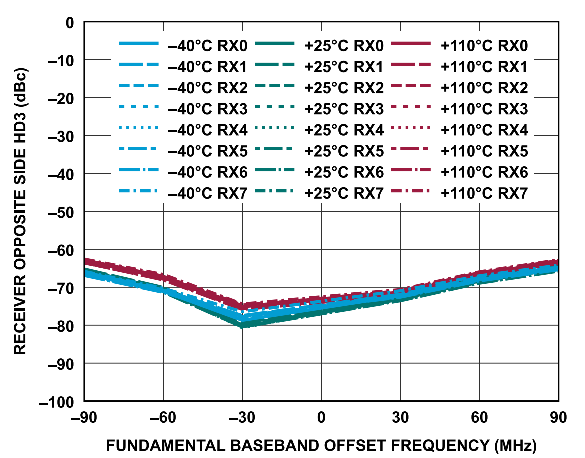

Figure 209. Receiver Opposite Side Third Harmonic Distortion (HD3) vs. Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

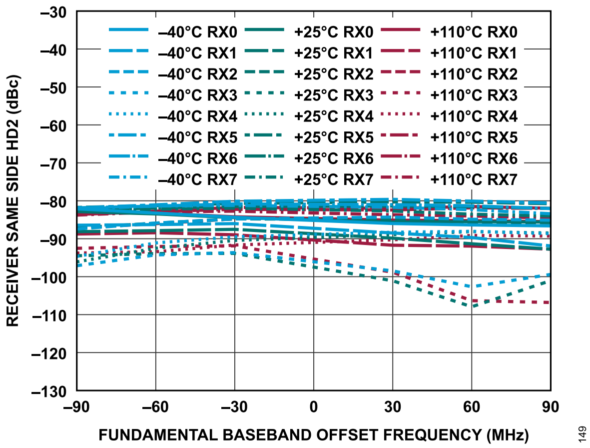

Figure 210. Receiver Same Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

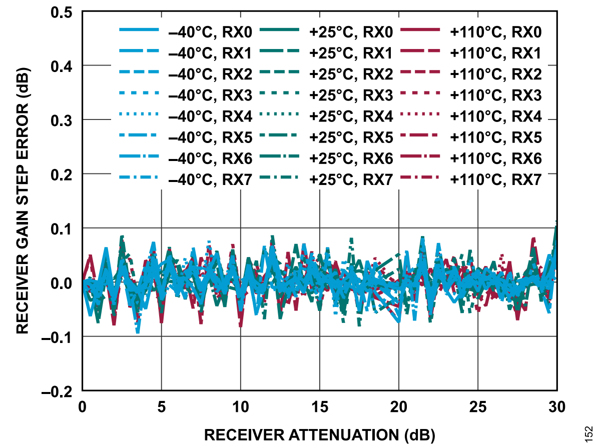

Figure 213. Receiver Gain Step Error vs. Attenuation, 30 MHz Offset, −1 dBFS Input Signal

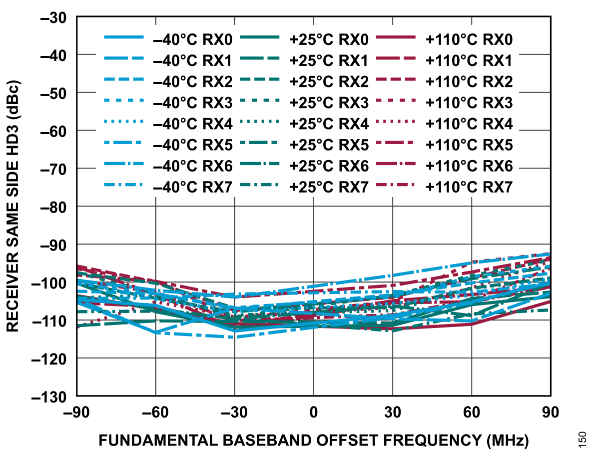

Figure 211. Receiver Same Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

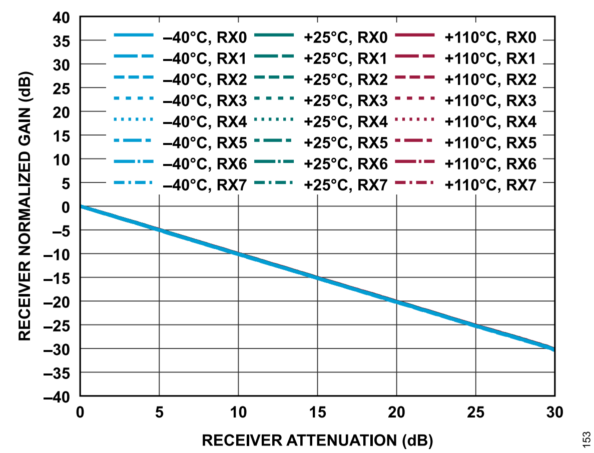

Figure 214. Receiver Normalized Gain vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

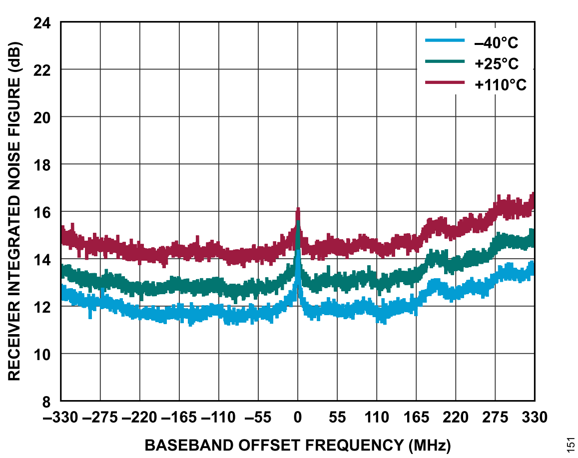

Figure 212. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 kHz Integration Steps, 983.04 MSPS Sample Rate

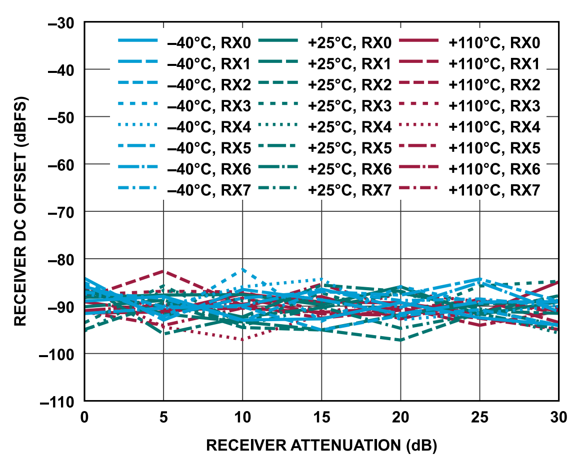

Figure 215. Receiver DC Offset vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

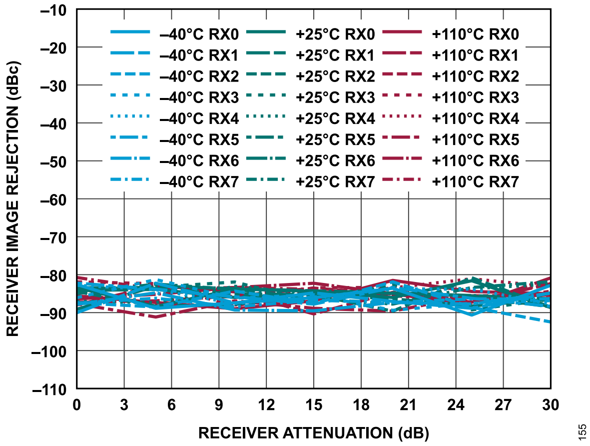

Figure 216. Receiver Image vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

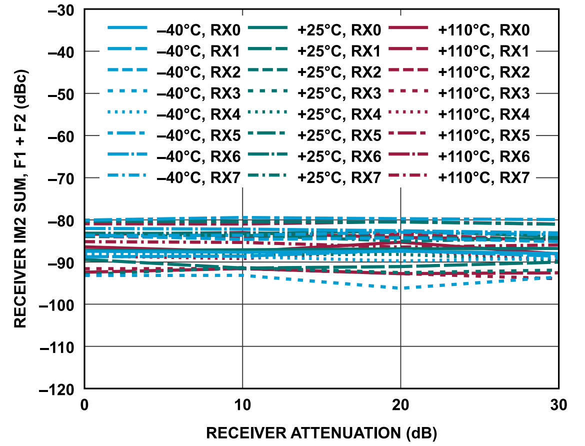

Figure 219. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

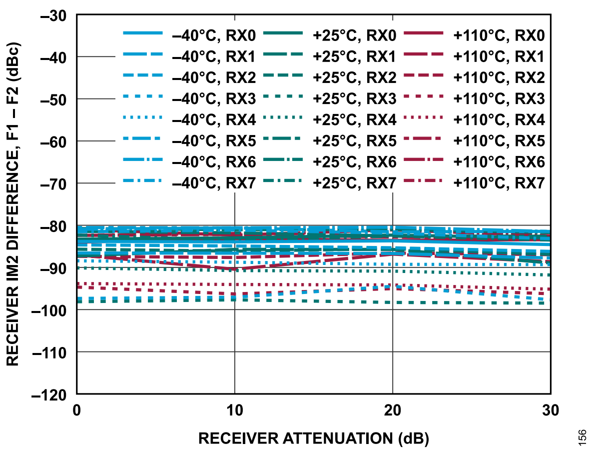

Figure 217. Receiver IM2, f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

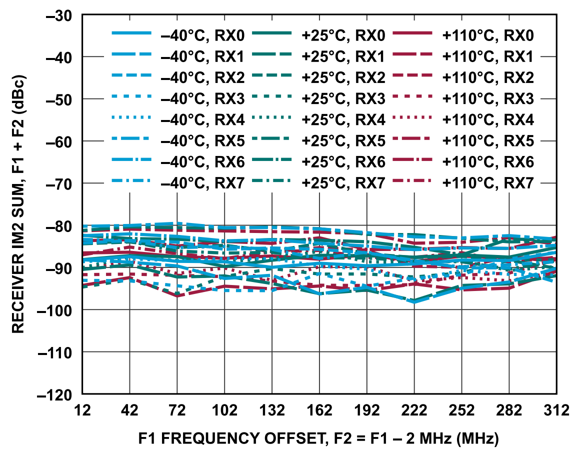

Figure 220. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 282 MHz Offset, f2 = 2 MHz Offset

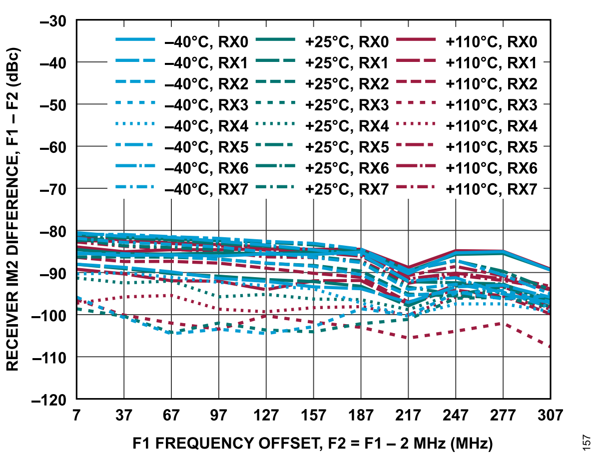

Figure 218. Receiver IM2, f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

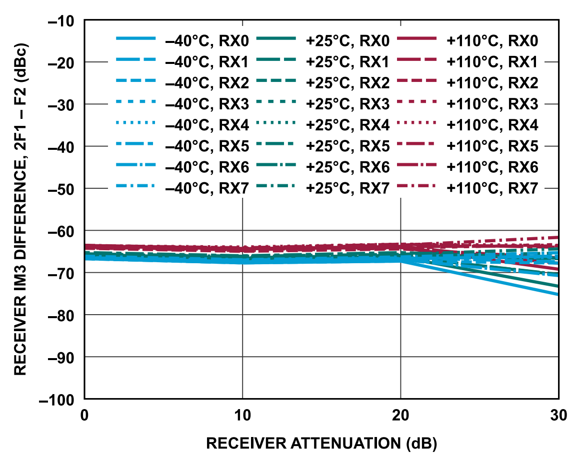

Figure 221. Receiver IM2, f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

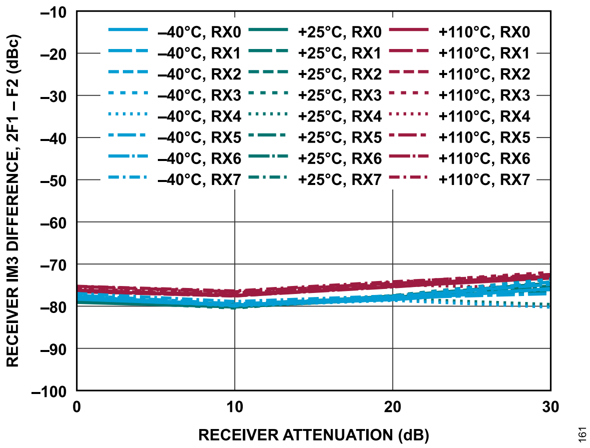

Figure 222. Receiver IM3, 2f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

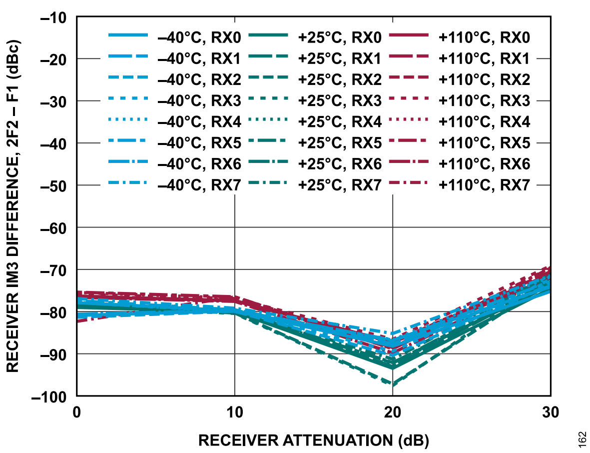

Figure 223. Receiver IM3, 2f2 − f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

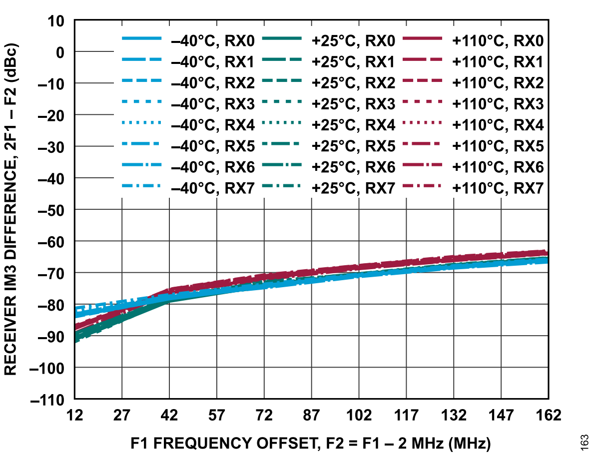

Figure 224. Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

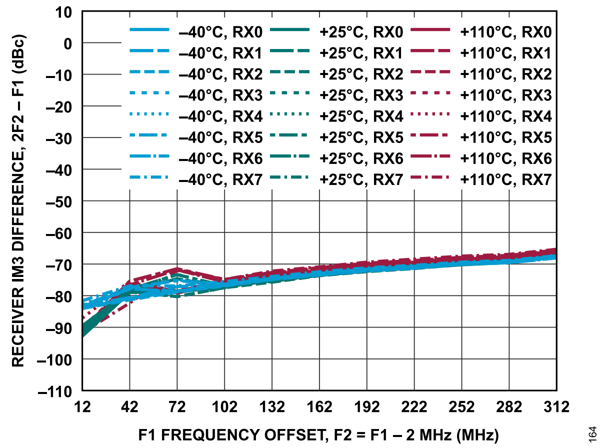

Figure 225. Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

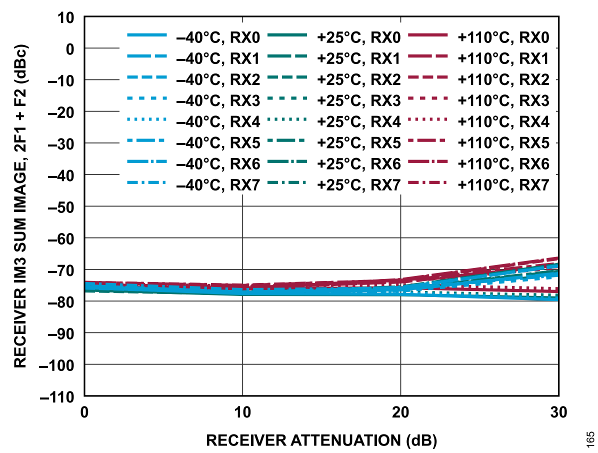

Figure 226. Receiver IM3, 2f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

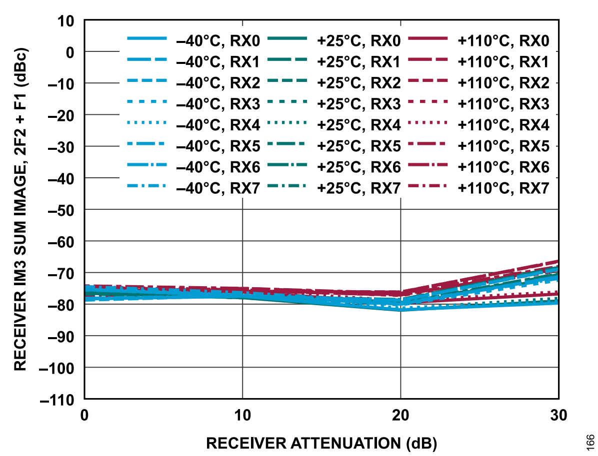

Figure 227. Receiver IM3, 2f2 + f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

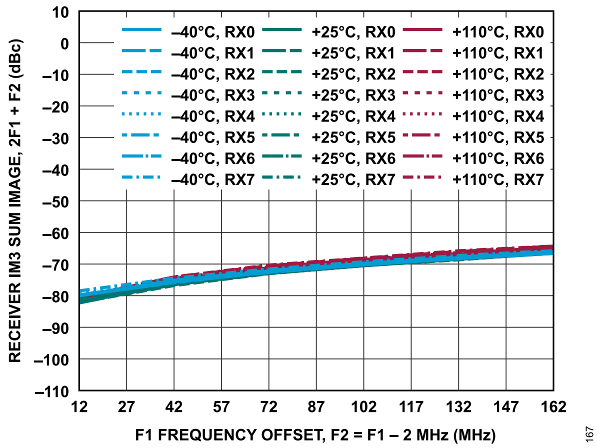

Figure 228. Receiver IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

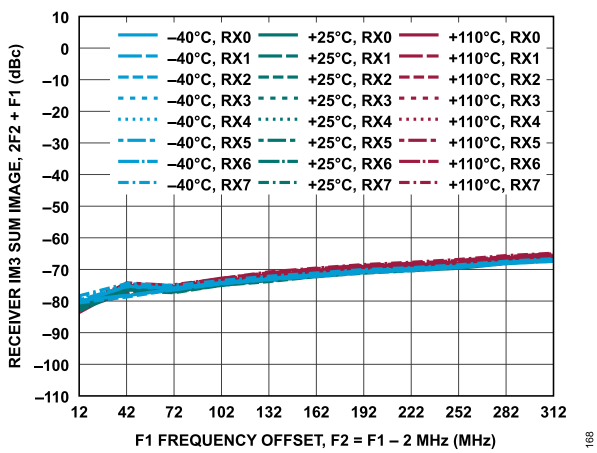

Figure 229. Receiver IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

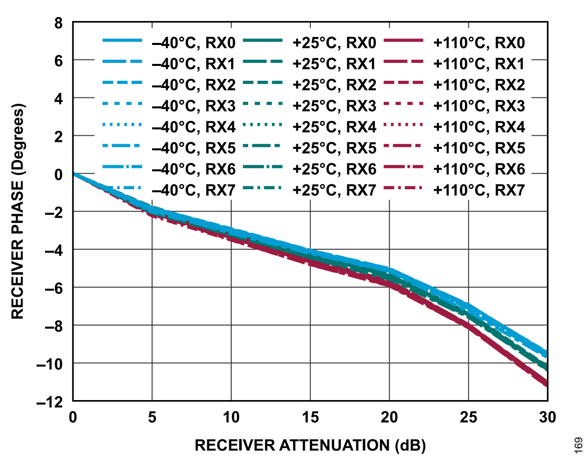

Figure 230. Receiver Phase vs. Receiver Attenuation

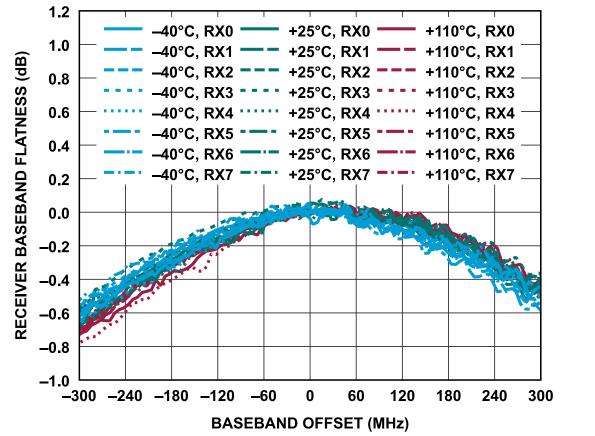

Figure 231. Receiver Baseband Flatness vs. Baseband Offset

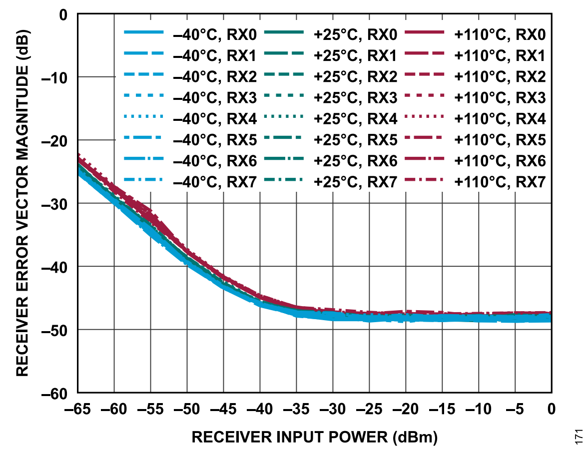

Figure 232. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Centered Around DC, TDD Mode, AGC Enabled

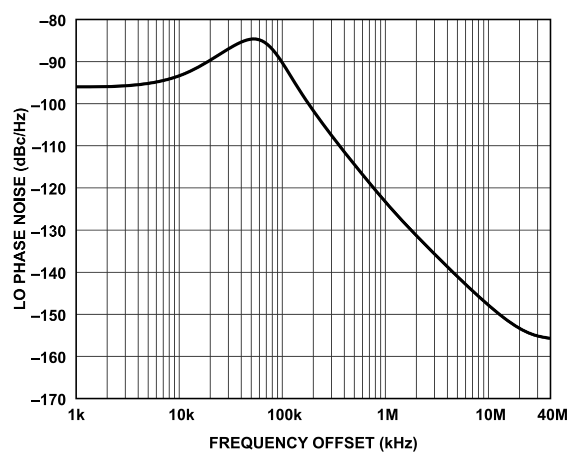

Figure 233. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 60 kHz, Phase Margin = 55°

TYPICAL PERFORMANCE CHARACTERISTICS

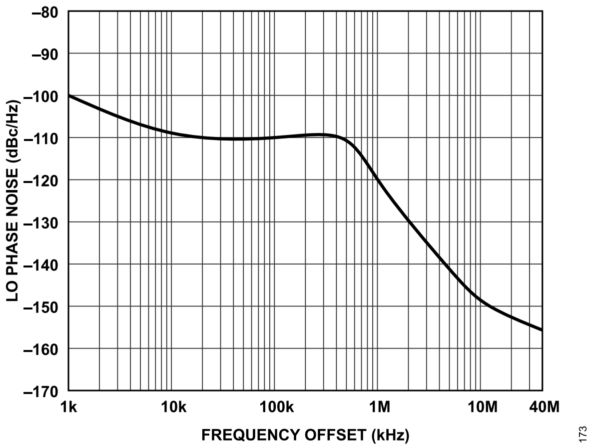

Figure 234. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 55º

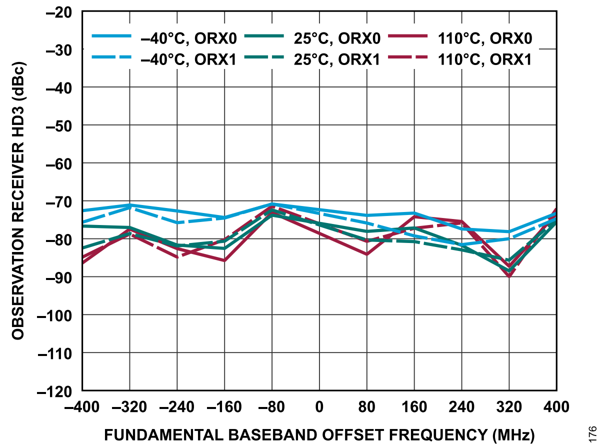

Figure 237. Observation Receiver HD3 vs. Baseband Offset Frequency, −10 dBFS Input Signal

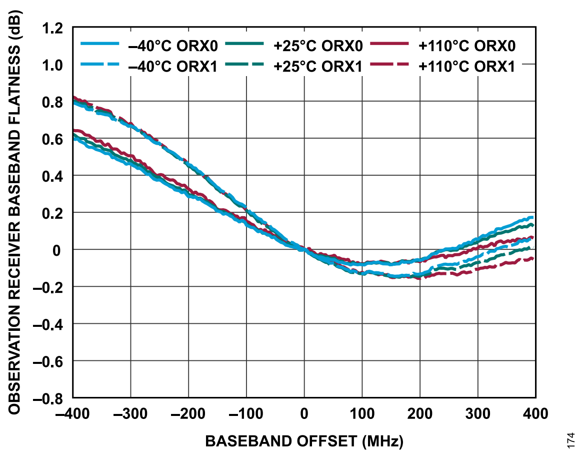

Figure 235. Observation Receiver Baseband Flatness vs. Baseband Offset

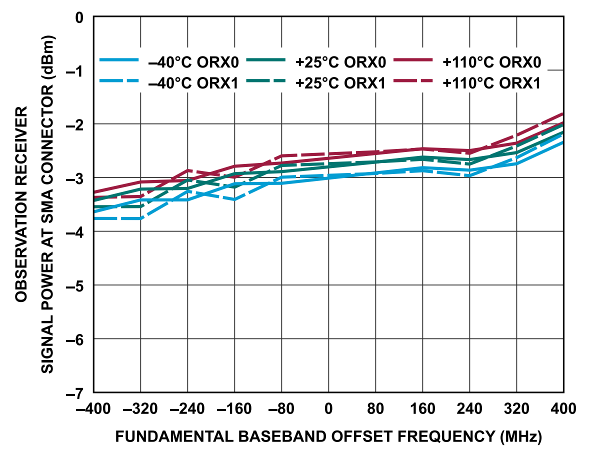

Figure 238. Observation Receiver Signal Power at SMA Connector vs. Baseband Frequency, −10 dBFS Input Signal (Match Is Not De−Embedded)

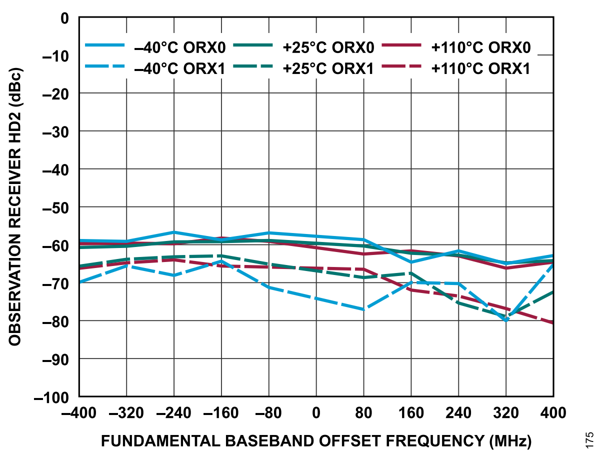

Figure 236. Observation Receiver HD2 vs. Baseband Offset Frequency, −10 dBFS Input Signal

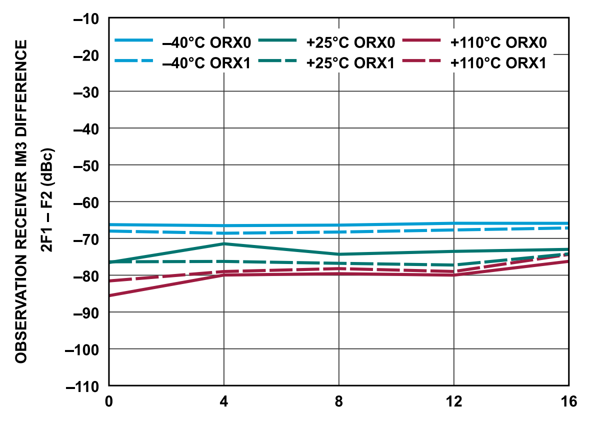

Figure 239. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3512 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

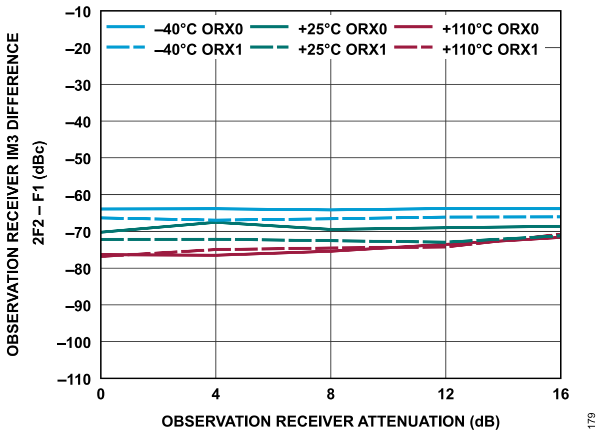

Figure 240. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3512 MHz

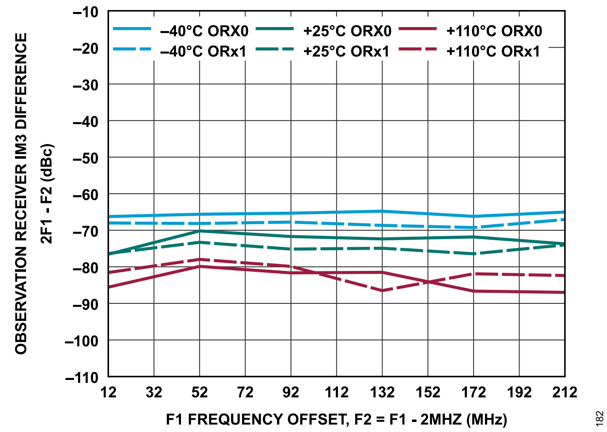

Figure 243. Observation Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 3502 MHz

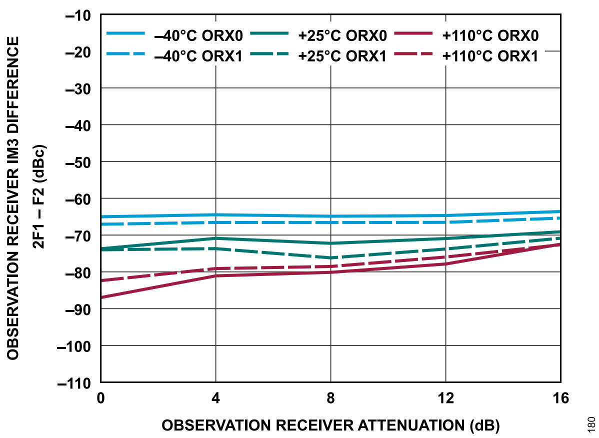

Figure 241. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3712 MHz

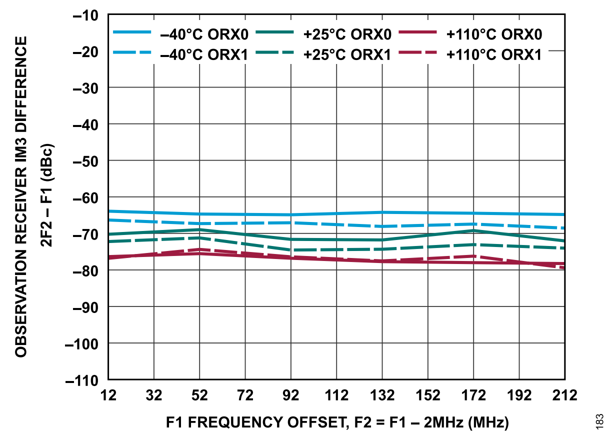

Figure 244. Observation Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 3502 MHz

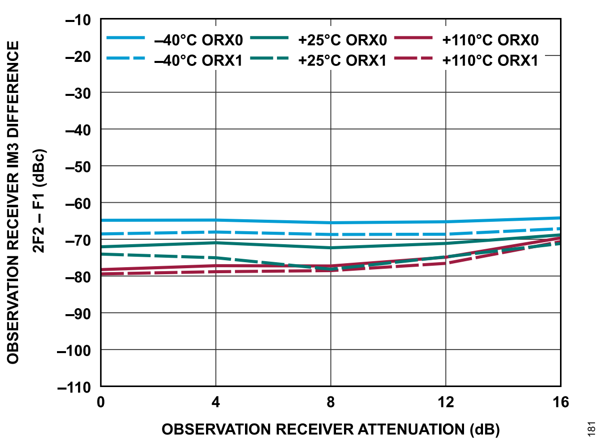

Figure 242. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3712 MHz

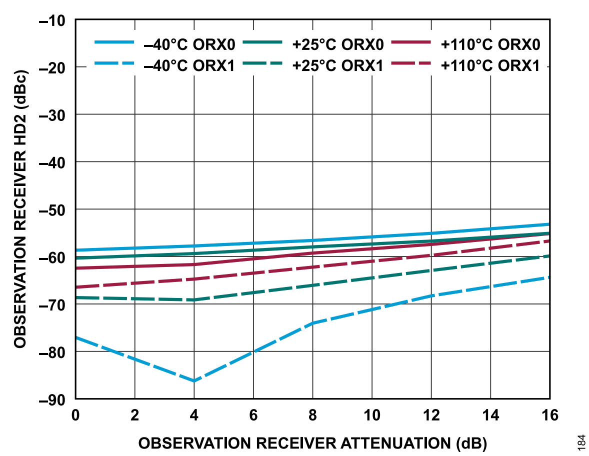

Figure 245. Observation Receiver HD2 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

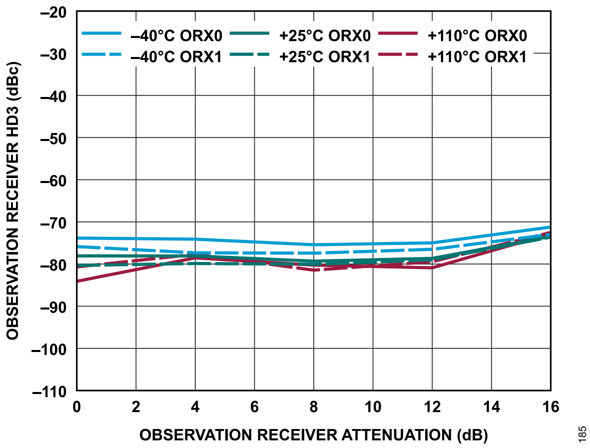

Figure 246. Observation Receiver HD3 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

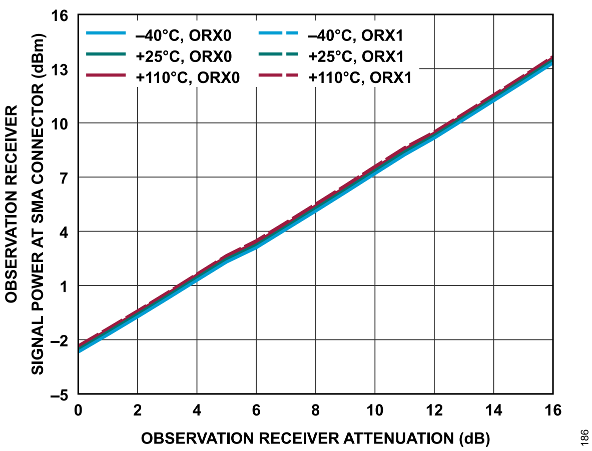

Figure 247. Observation Receiver Signal Power at SMA Connector vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

4500 MHZ BAND

The temperature settings refer to the die temperature. All LO frequencies set to 4500 MHz, unless otherwise noted. The observation receiver measurements are taken with 5898.24 MHz sampling frequency, unless otherwise noted.

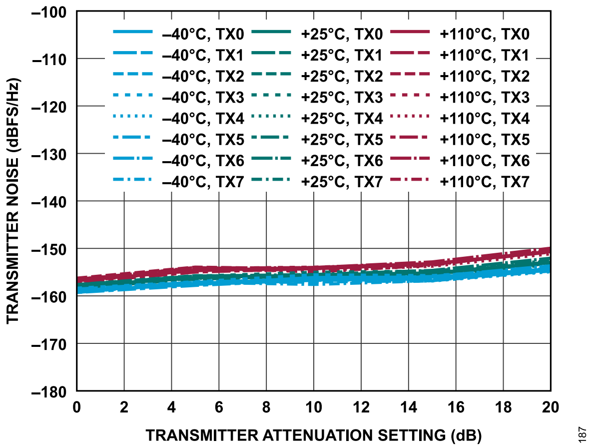

Figure 248. Transmitter Noise vs. Transmitter Attenuation, 150 MHz Offset

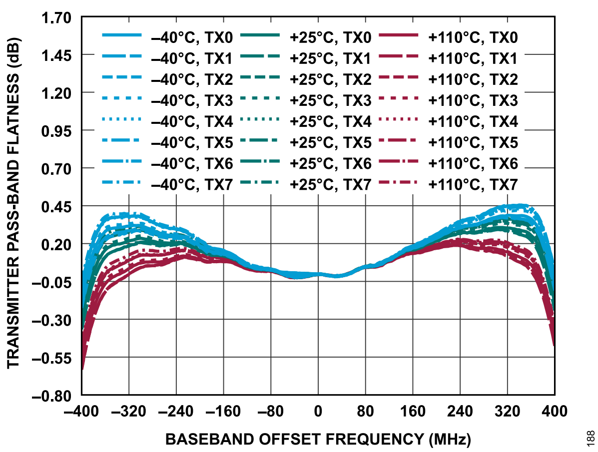

Figure 249. Transmitter Pass-Band Flatness vs. Baseband Offset Frequency

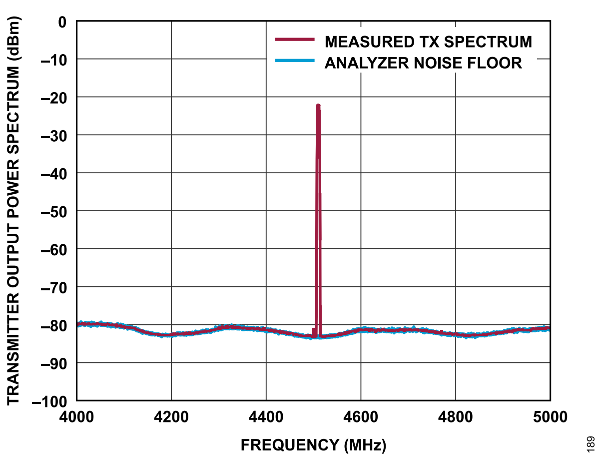

Figure 250. Transmitter Output Power Spectrum, Tx0, 5MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T_J = 25°C

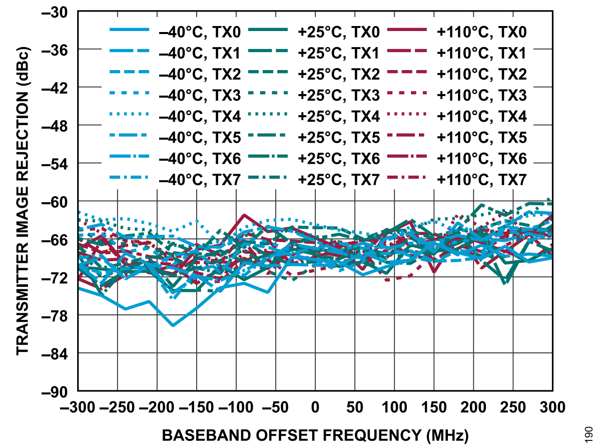

Figure 251. Transmitter Image Rejection vs. Baseband Offset Frequency, −6 dBFS Continuous Wave Signal

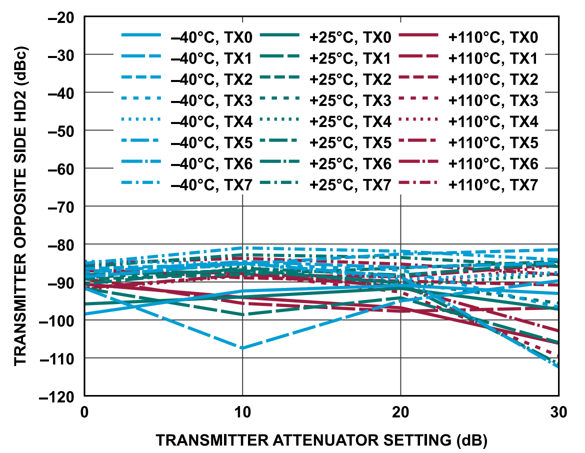

Figure 252. Transmitter Opposite Side Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

TYPICAL PERFORMANCE CHARACTERISTICS

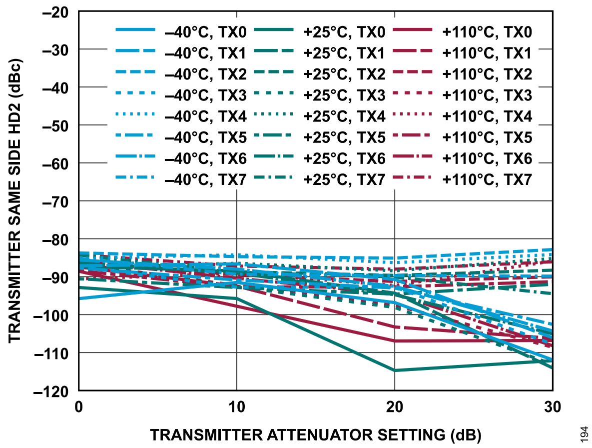

Figure 253. Transmitter Same Side HD2 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

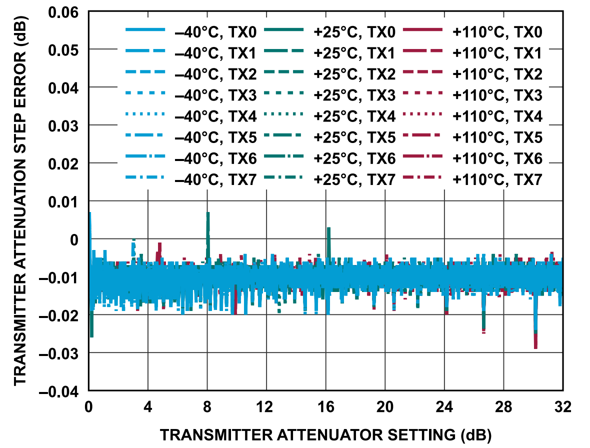

Figure 256. Transmitter Attenuation Step Error vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

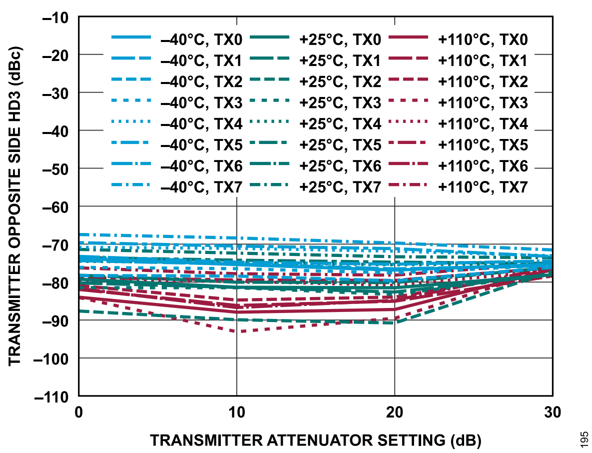

Figure 254. Transmitter Opposite Side Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

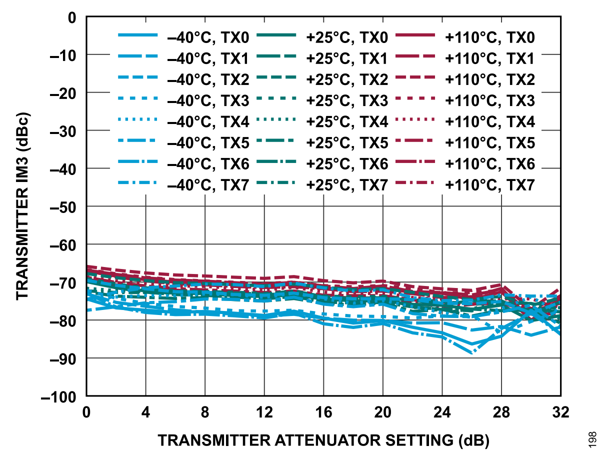

Figure 257. Transmitter IM3, 2f1 − f2 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

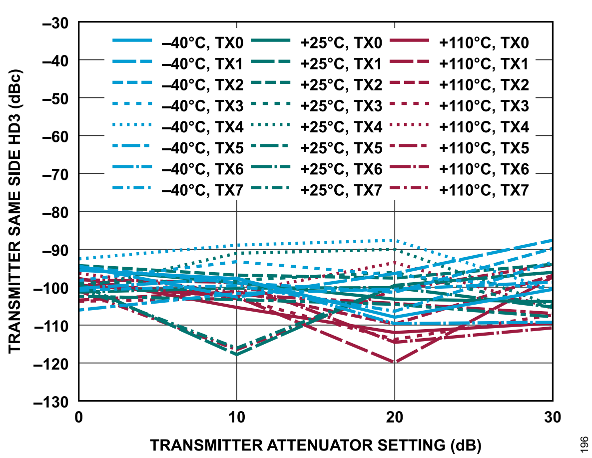

Figure 255. Transmitter Same Side HD3 vs. Transmitter Attenuation, 30 MHz Offset, −12 dBFS Continuous Wave Signal

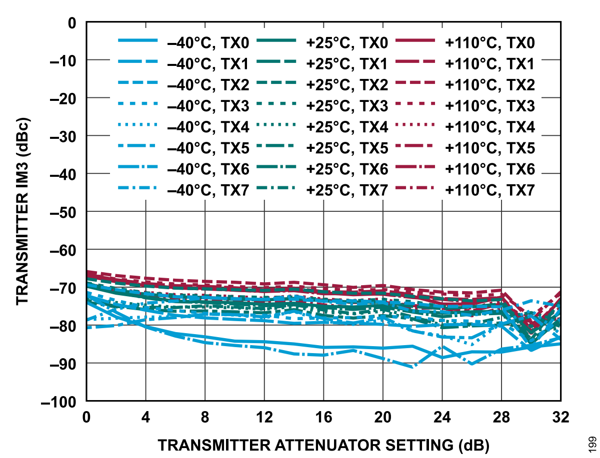

Figure 258. Transmitter IM3, 2f2 − f1 vs. Transmitter Attenuation, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 165 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

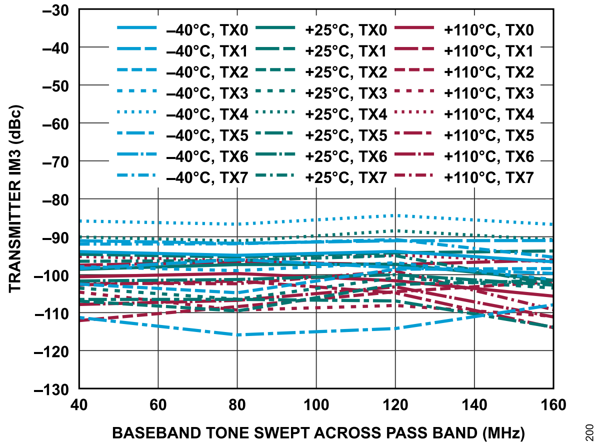

Figure 259. Transmitter IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

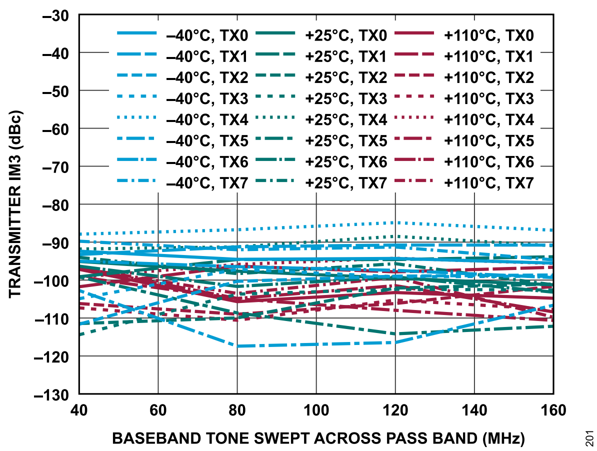

Figure 260. Transmitter IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

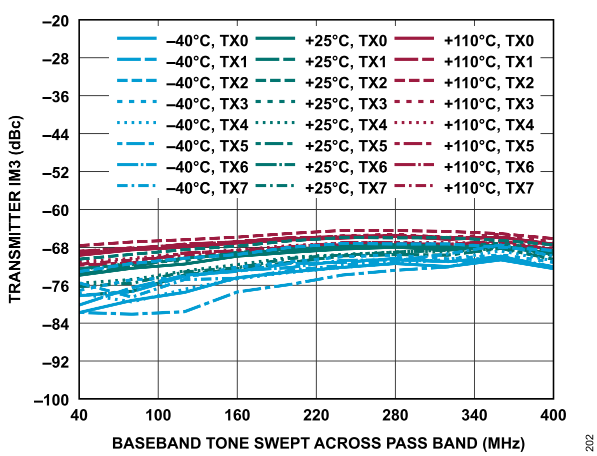

Figure 261. Transmitter IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

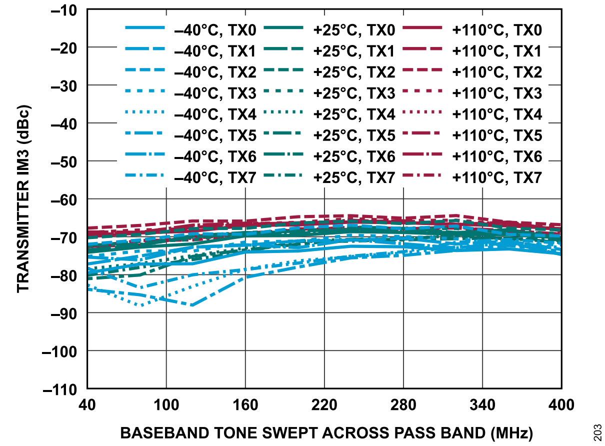

Figure 262. Transmitter IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = f1 + 5 MHz

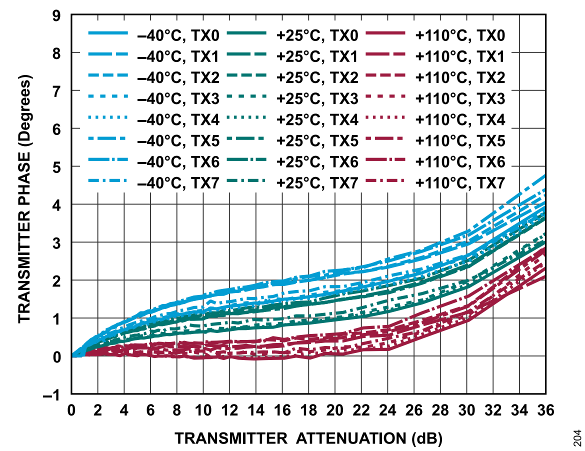

Figure 263. Transmitter Phase vs. Transmitter Attenuation

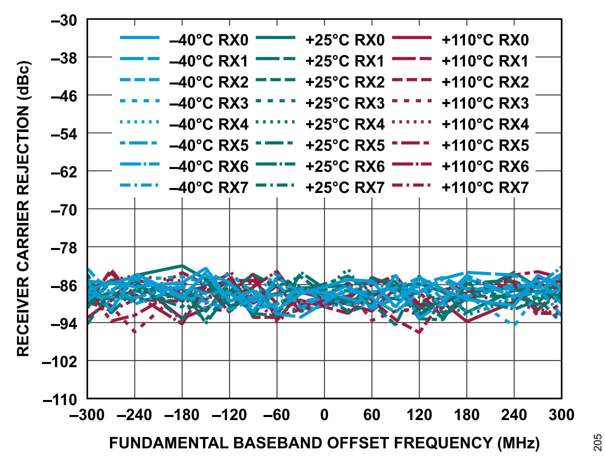

Figure 264. Receiver Carrier Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

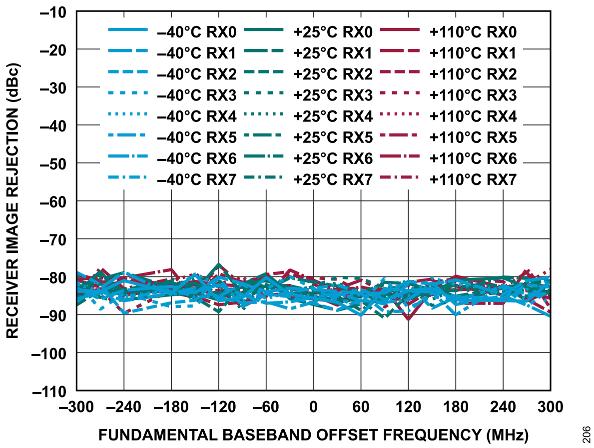

Figure 265. Receiver Image Rejection vs. Baseband Offset Frequency, −1 dBFS Input Signal

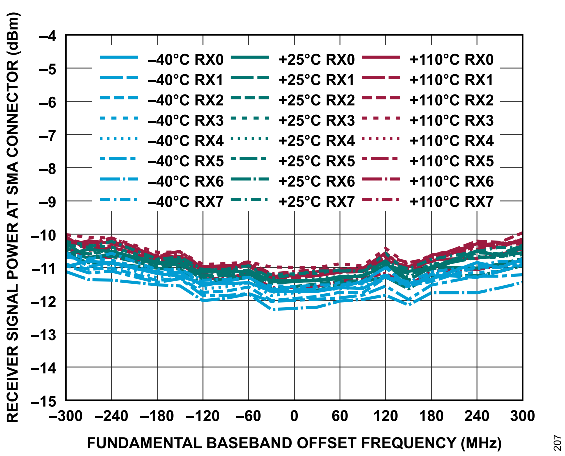

Figure 266. Receiver Signal Power at SMA Connector vs. Baseband Offset Frequency, −1 dBFS Input Signal (Match Is Not De−Embedded)

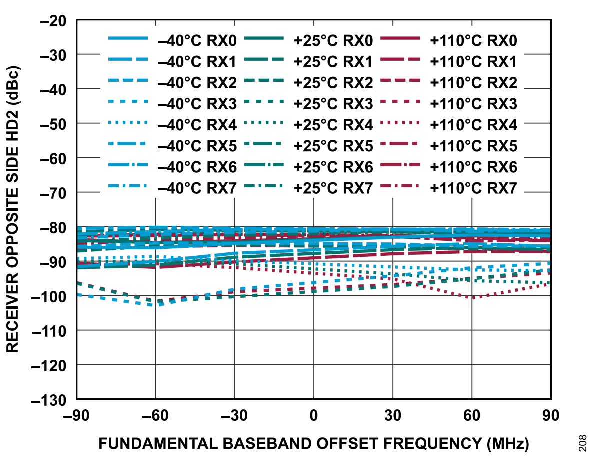

Figure 267. Receiver Opposite Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

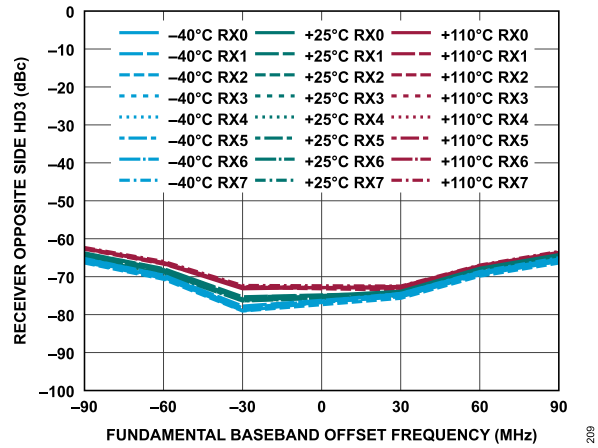

Figure 268. Receiver Opposite Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

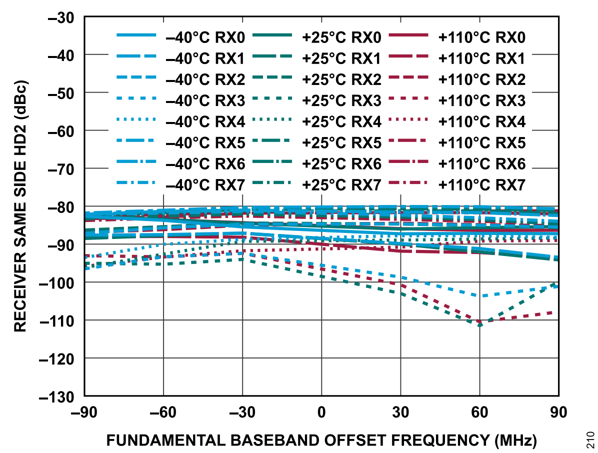

Figure 269. Receiver Same Side HD2 vs. Baseband Offset Frequency, −1 dBFS Input Signal

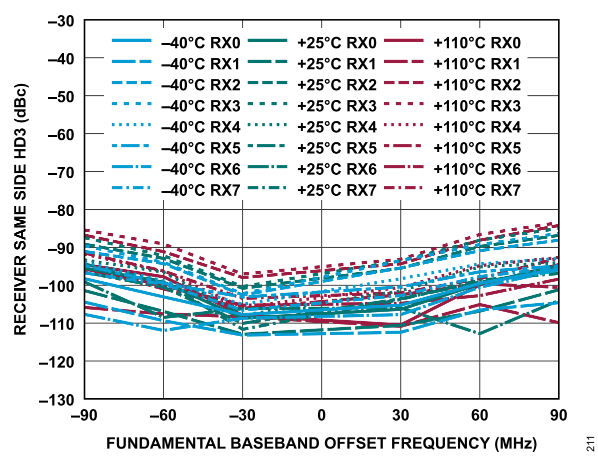

Figure 270. Receiver Same Side HD3 vs. Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

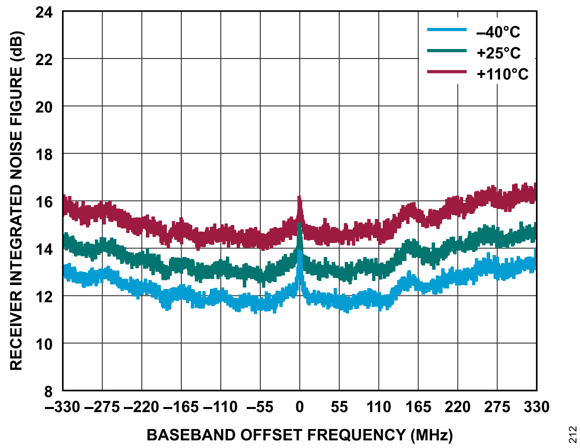

Figure 271. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 kHz Integration Steps, 983.04 MSPS Sample Rate

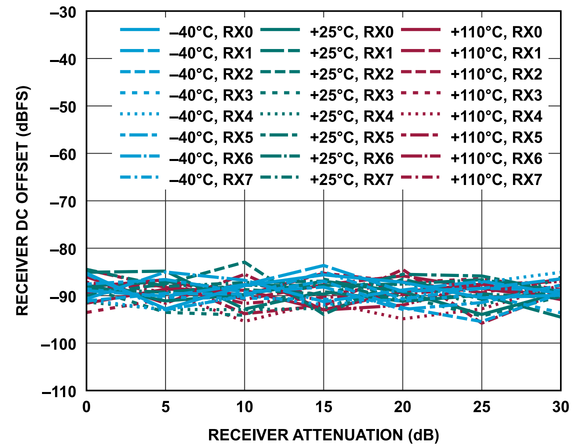

Figure 274. Receiver DC Offset vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

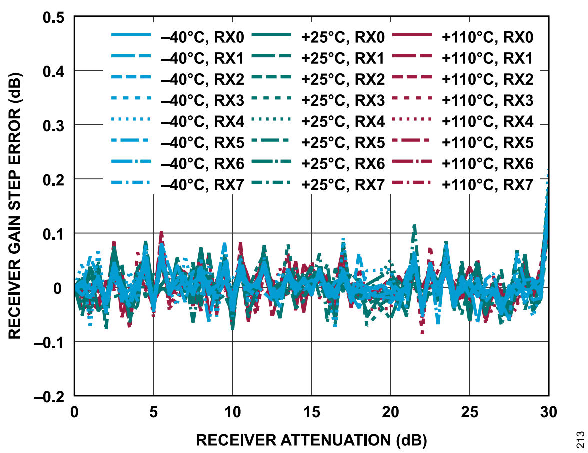

Figure 272. Receiver Gain Step Error vs. Attenuation, 30 MHz Offset, −1 dBFS Input Signal

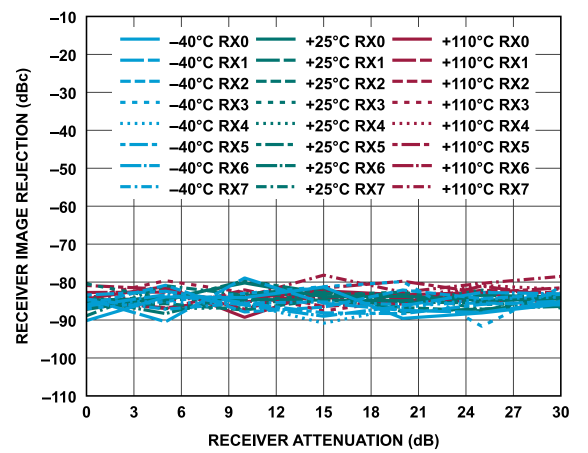

Figure 275. Receiver Image vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

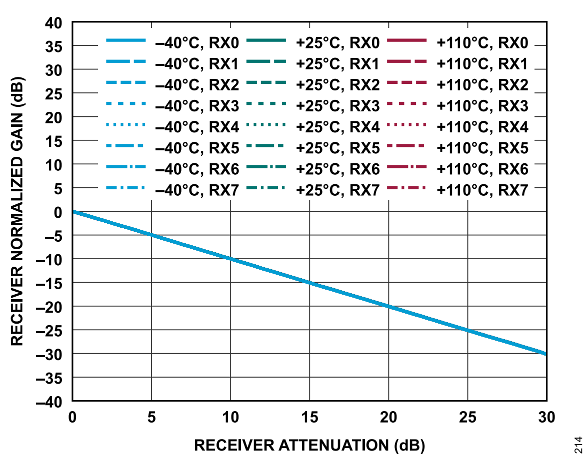

Figure 273. Receiver Normalized Gain vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

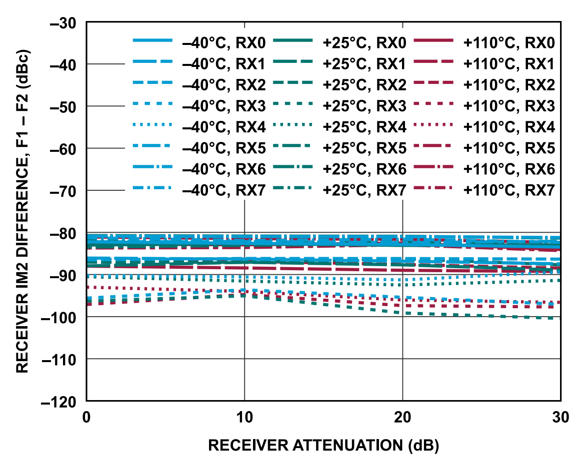

Figure 276. Receiver IM2, f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

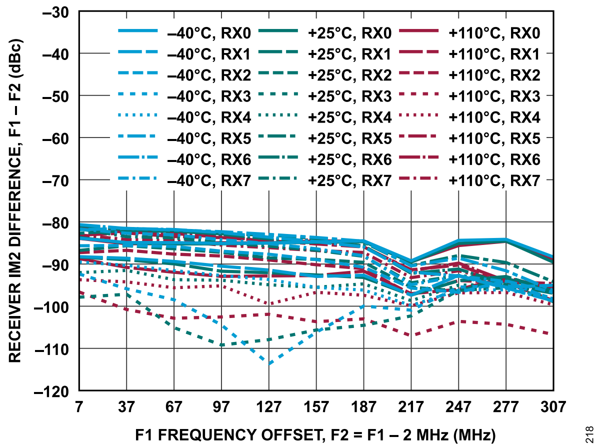

Figure 277. Receiver IM2, f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

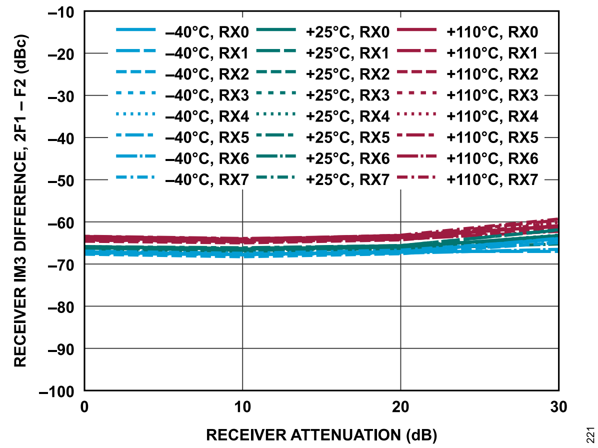

Figure 280. Receiver IM2, f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

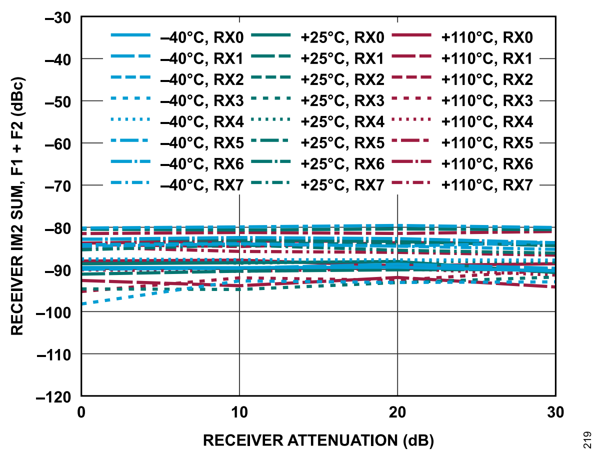

Figure 278. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

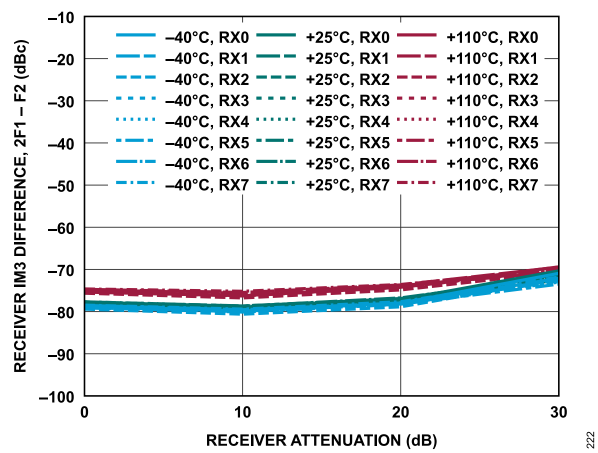

Figure 281. Receiver IM3, 2f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

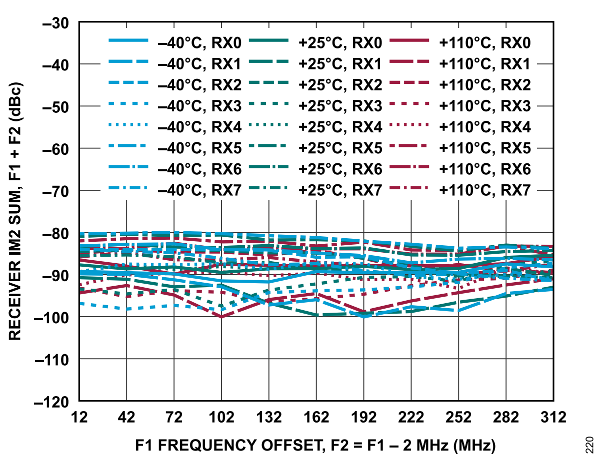

Figure 279. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 282 MHz Offset, f2 = 2 MHz Offset

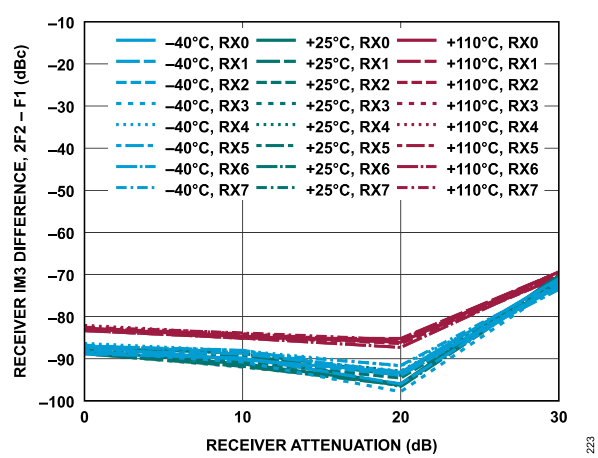

Figure 282. Receiver IM3, 2f2 − f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

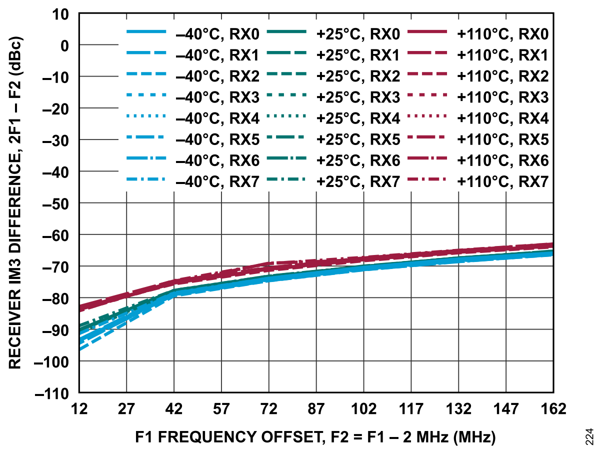

Figure 283. Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

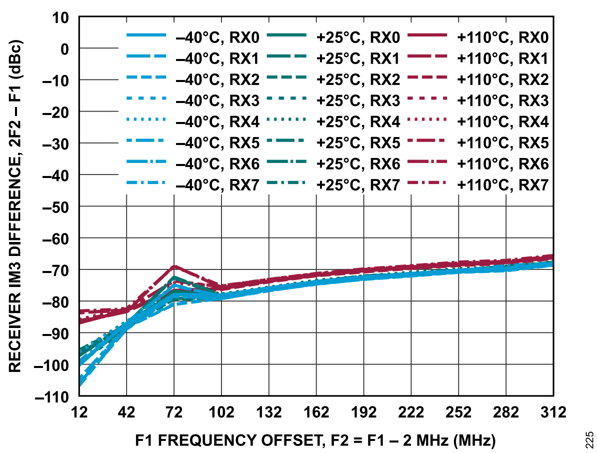

Figure 284. Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

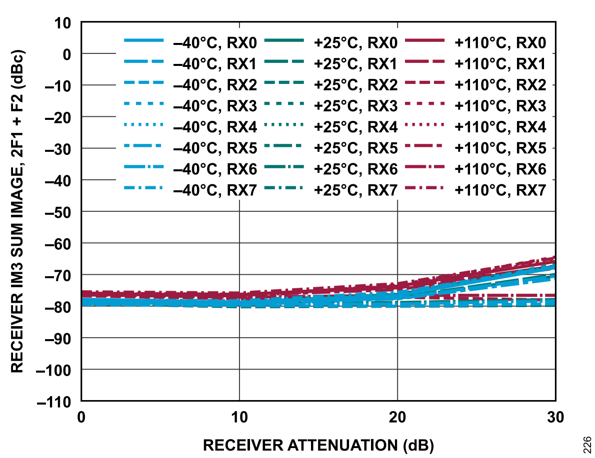

Figure 285. Receiver IM3, 2f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

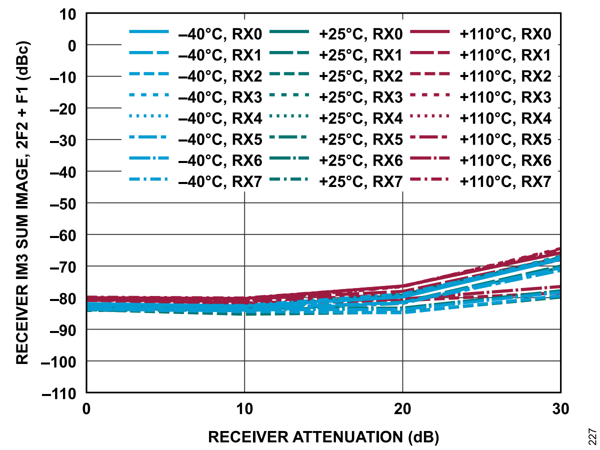

Figure 286. Receiver IM3, 2f2 + f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 42 MHz Offset, f2 = 2 MHz Offset

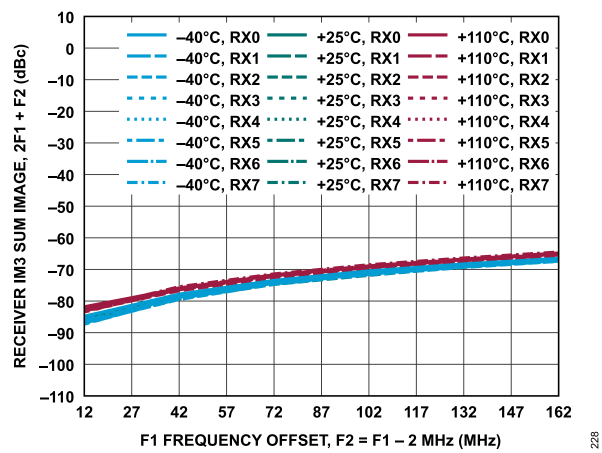

Figure 287. Receiver IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

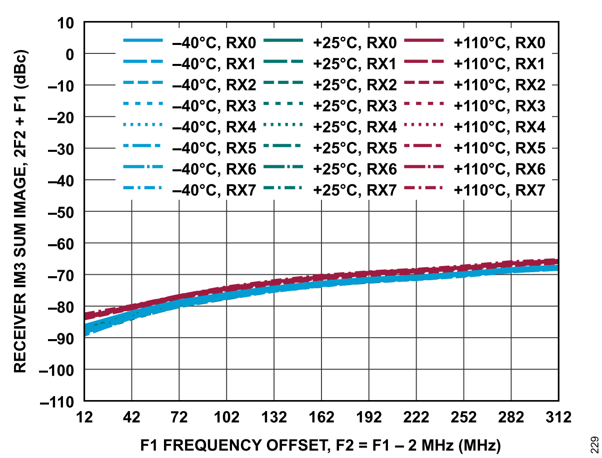

Figure 288. Receiver IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

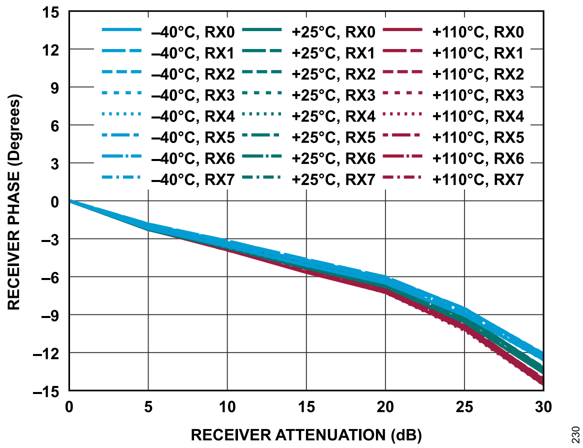

Figure 289. Receiver Phase vs. Receiver Attenuation

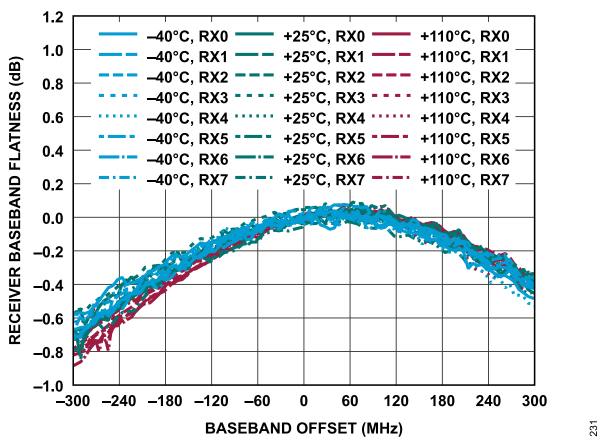

Figure 290. Receiver Baseband Flatness vs. Baseband Offset

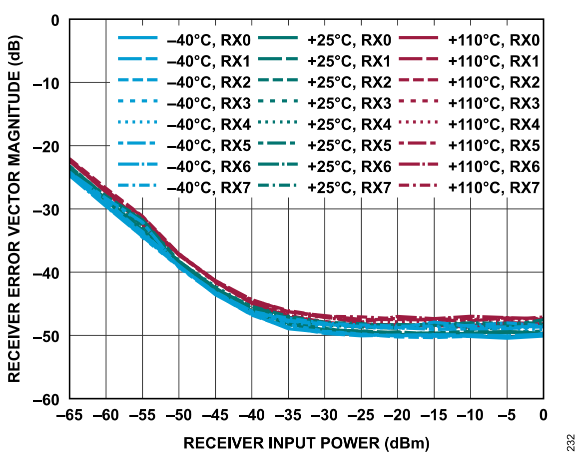

Figure 291. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Centered Around DC, TDD Mode, AGC Enabled

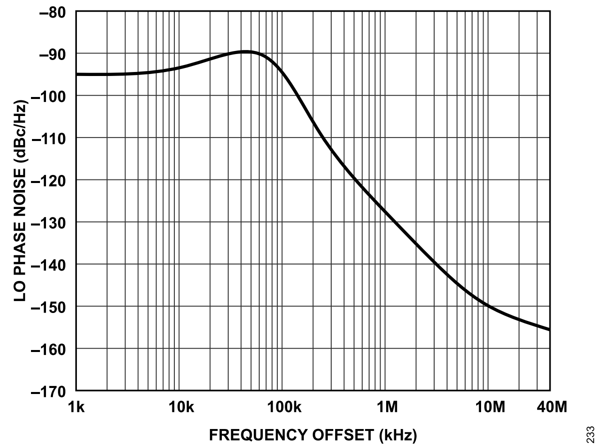

Figure 292. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 60 kHz, Phase Margin = 55°

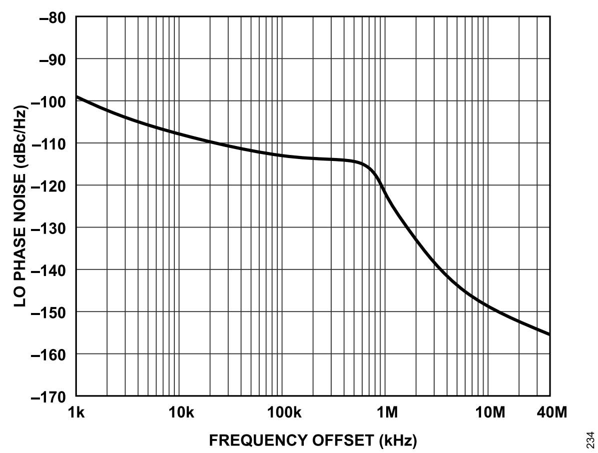

Figure 293. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 55°

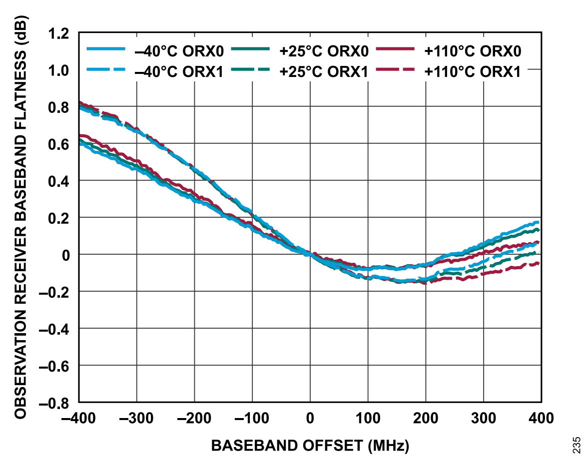

Figure 294. Observation Receiver Baseband Flatness vs. Baseband Offset Frequency, −10 dBFS input signal

TYPICAL PERFORMANCE CHARACTERISTICS

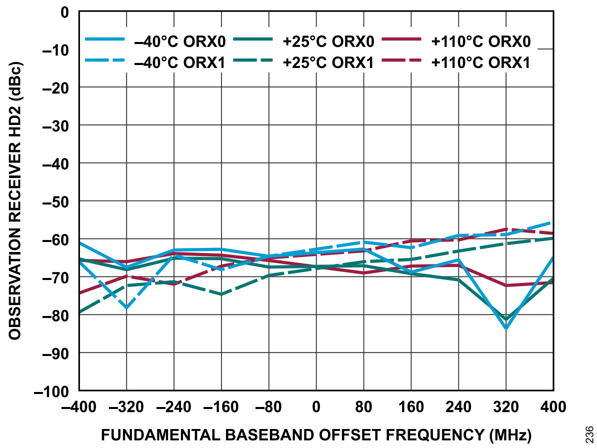

Figure 295. Observation Receiver HD2 vs. Baseband Offset Frequency, −10 dBFS Input Signal

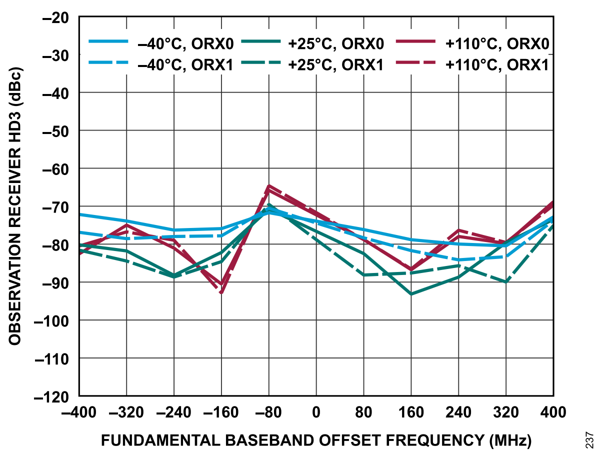

Figure 296. Observation Receiver HD3 vs. Baseband Offset Frequency, −10 dBFS Input Signal

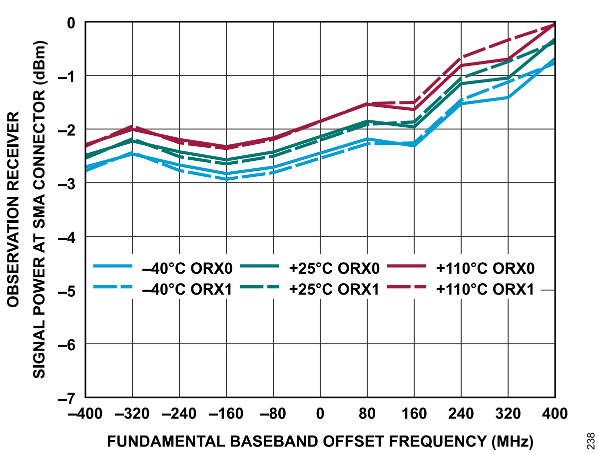

Figure 297. Observation Receiver Signal Power at SMA Connector vs. Baseband Frequency, −10 dBFS Input Signal (Match Is Not De−Embedded)

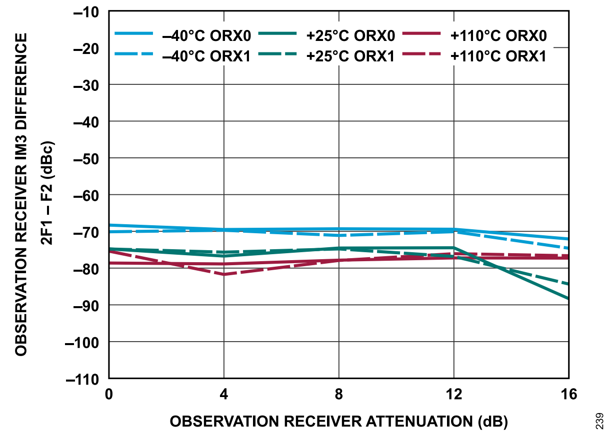

Figure 298. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3512 MHz

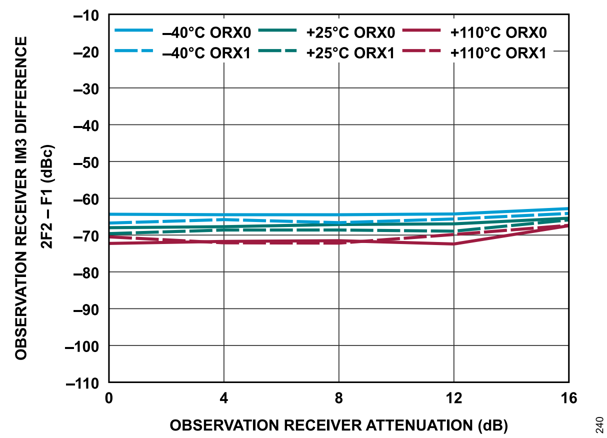

Figure 299. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3512 MHz

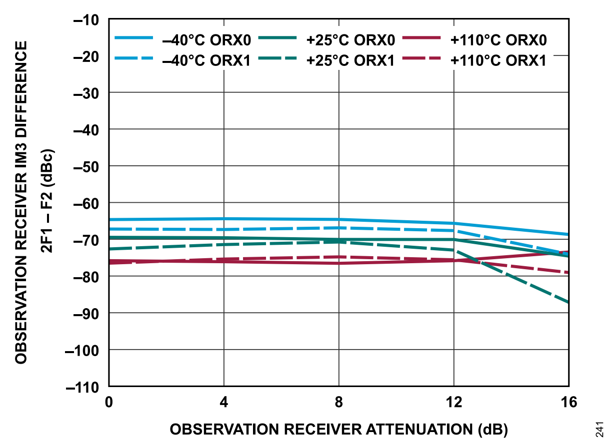

Figure 300. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3712 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

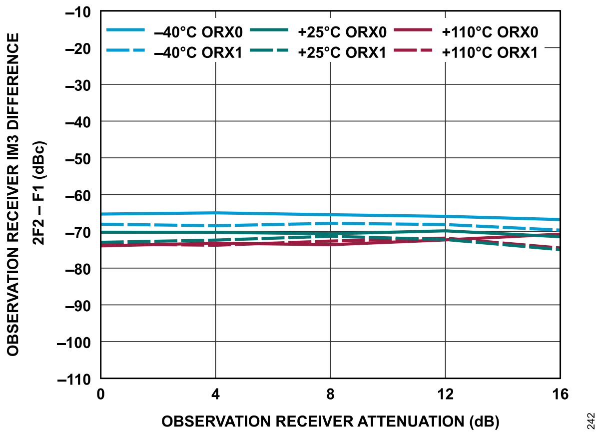

Figure 301. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3712 MHz

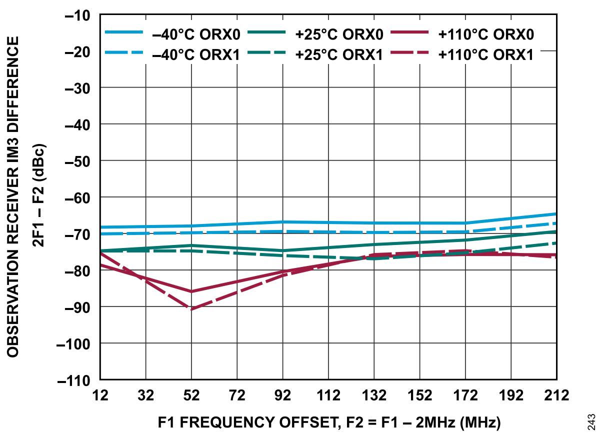

Figure 302. Observation Receiver IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 3502 MHz

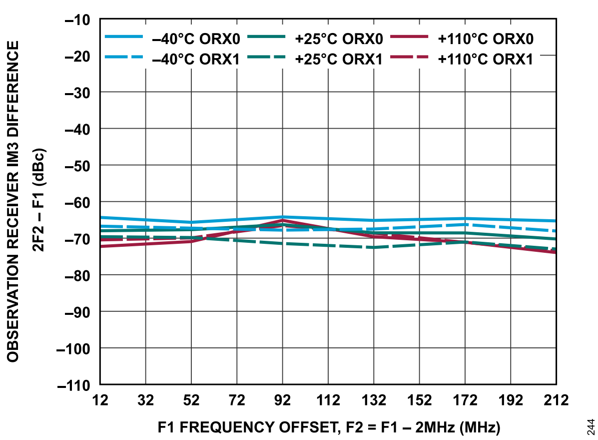

Figure 303. Observation Receiver IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −13 dBFS Signal Level per Tone, f2 = 3502 MHz

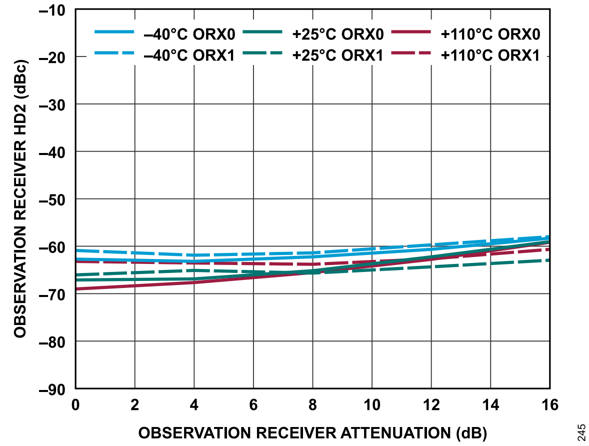

Figure 304. Observation Receiver HD2 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

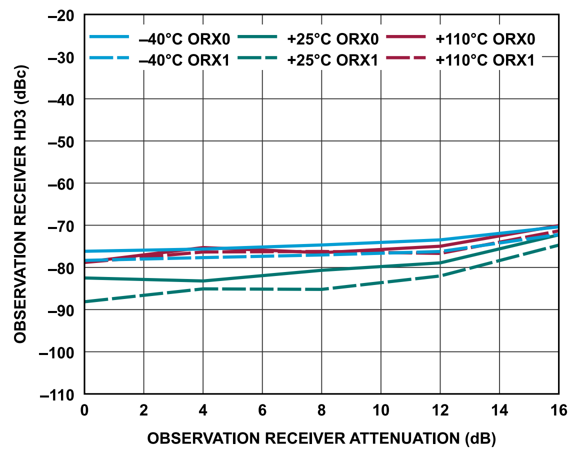

Figure 305. Observation Receiver HD3 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

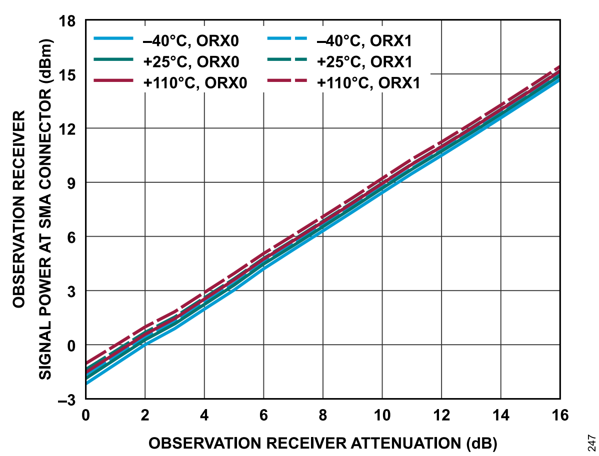

Figure 306. Observation Receiver Signal Power at SMA Connector vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

5600 MHZ BAND

The temperature settings refer to the die temperature. All LO frequencies set to 5600 MHz, unless otherwise noted. The observation receiver measurements are taken with 7863.42 MHz sampling frequency, unless otherwise noted.

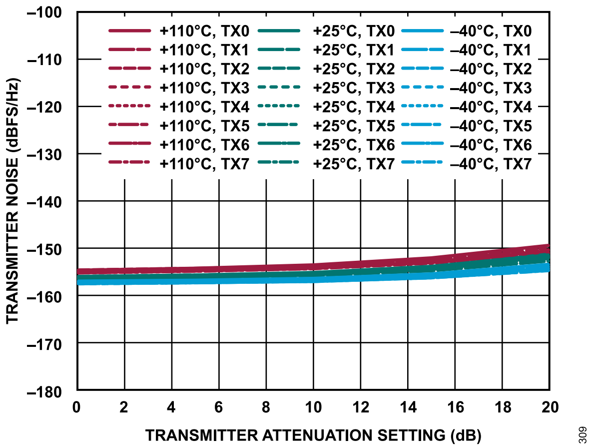

Figure 307. Transmitter Noise vs. Transmitter Attenuation Setting, 165 MHz Offset

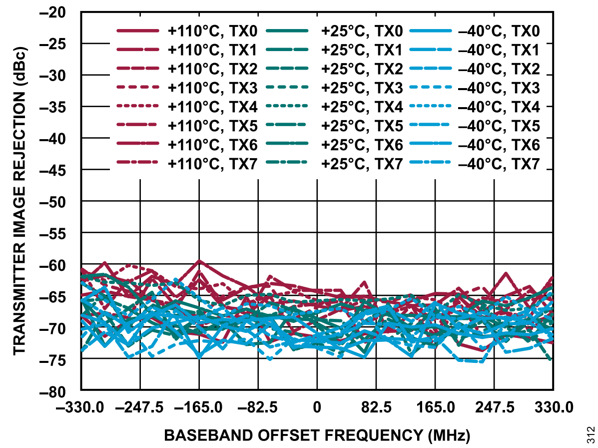

Figure 310. Transmitter Image Rejection vs. Baseband Offset Frequency, −6 dBFS Continuous Wave Signal

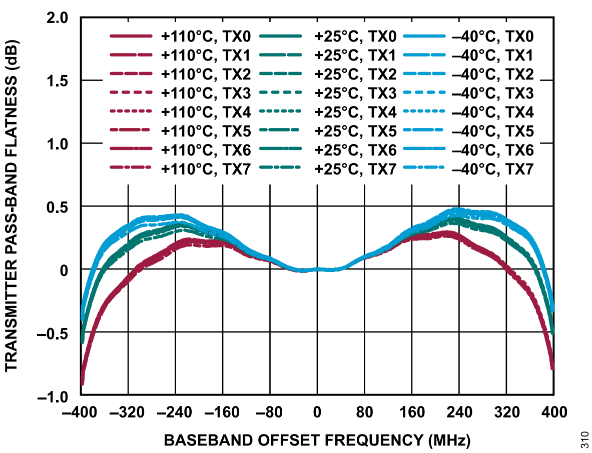

Figure 308. Transmitter Pass-Band Flatness vs. Baseband Offset Frequency

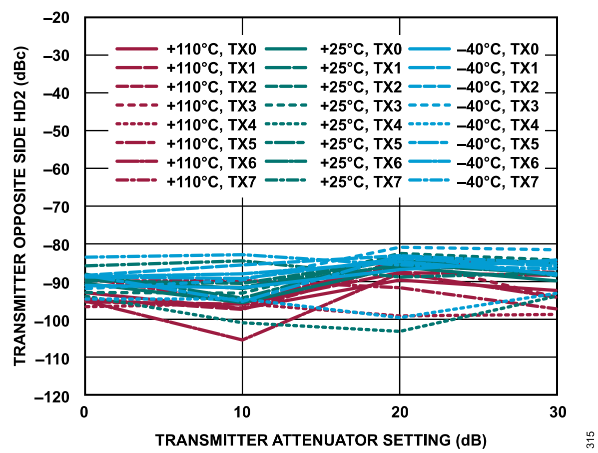

Figure 311. Transmitter Opposite Side HD2 vs. Transmitter Attenuator Setting, 165 MHz Offset, −12 dBFS Continuous Wave Signal

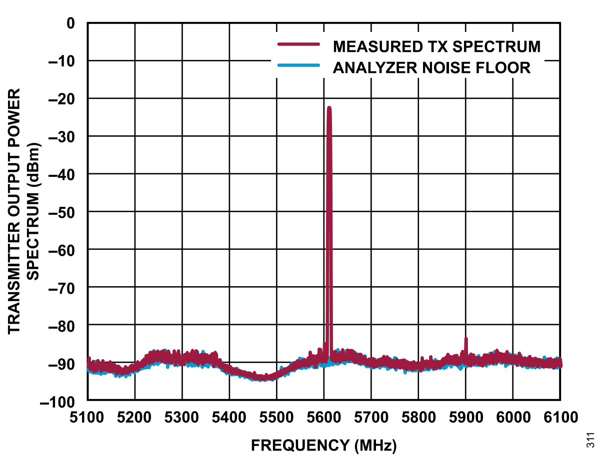

Figure 309. Transmitter Output Power Spectrum vs. Frequency, Tx0, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T_J = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

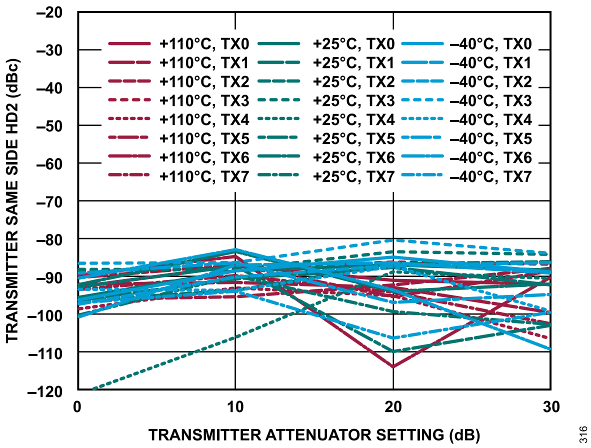

Figure 312. Transmitter Same Side HD2 vs. Transmitter Attenuator Setting, 165 MHz Offset, −12 dBFS Continuous Wave Signal

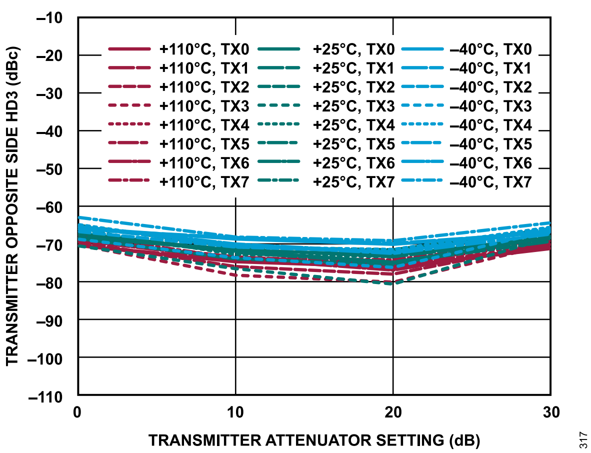

Figure 313. Transmitter Opposite Side HD3 vs. Transmitter Attenuator Setting, 110 MHz Offset, −12 dBFS Continuous Wave Signal

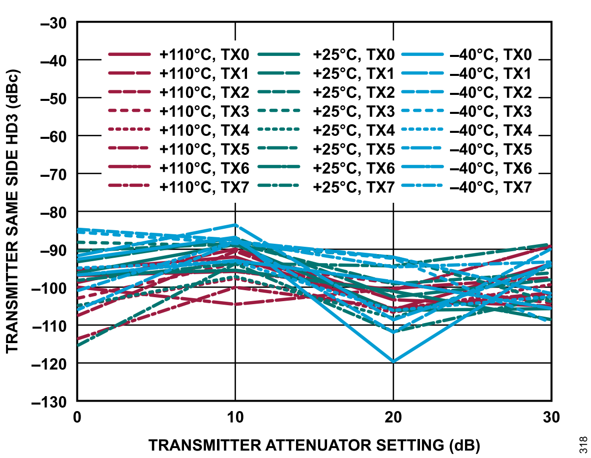

Figure 314. Transmitter Same Side HD3 vs. Transmitter Attenuator Setting, 110 MHz Offset, −12 dBFS Continuous Wave Signal

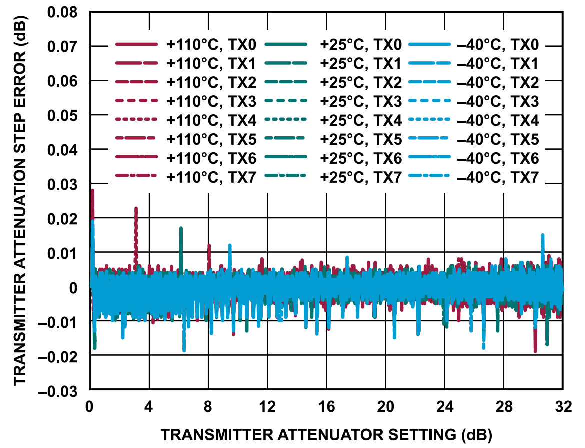

Figure 315. Transmitter Attenuation Step Error vs. Transmitter Attenuator Setting, 30 MHz Offset, −12 dBFS Continuous Wave Signal

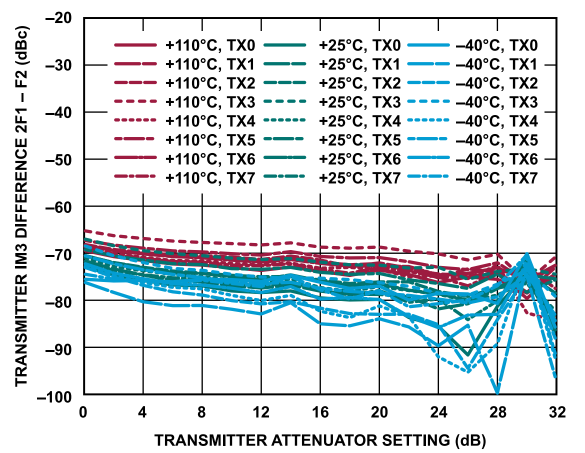

Figure 316. Transmitter IM3, 2f1 − f2 vs. Transmitter Attenuator Setting, −15 dBFS Signal Level per Tone, f1 = 160 MHz Offset, f2 = 2 MHz Offset

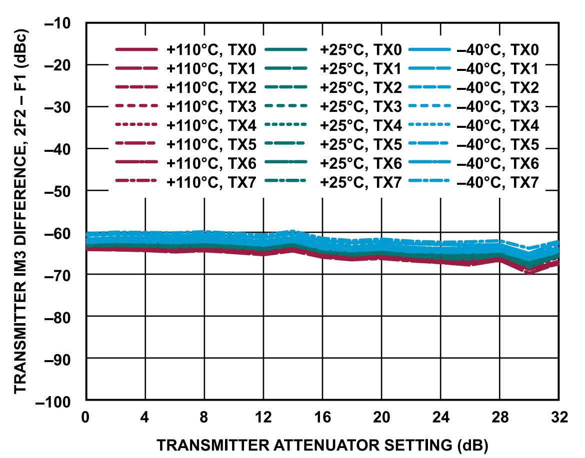

Figure 317. Transmitter IM3, 2f2 − f1 vs. Transmitter Attenuator Setting, −15 dBFS Signal Level per Tone, f1 = 320 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

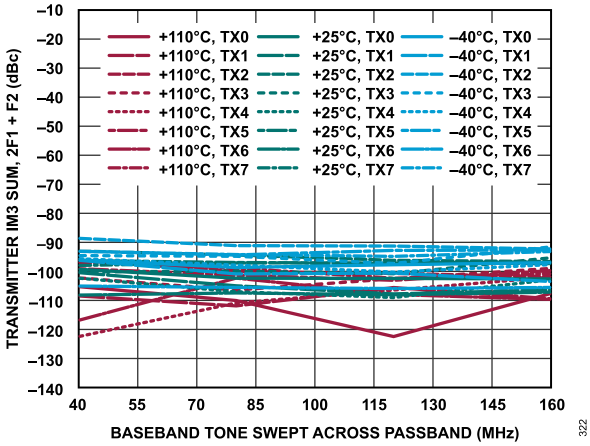

Figure 318. Transmitter IM3, 2f1 + f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = 5 MHz

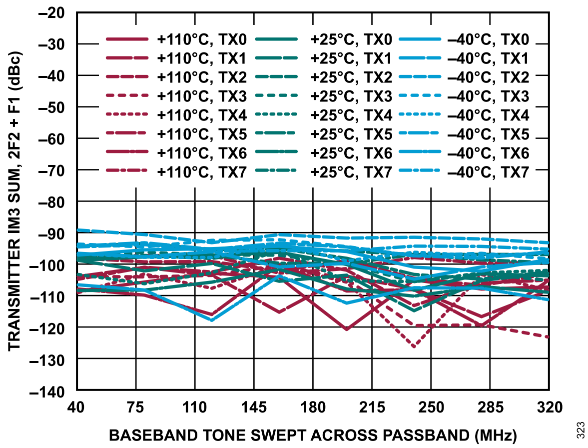

Figure 319. Transmitter IM3, 2f2 + f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = 5 MHz

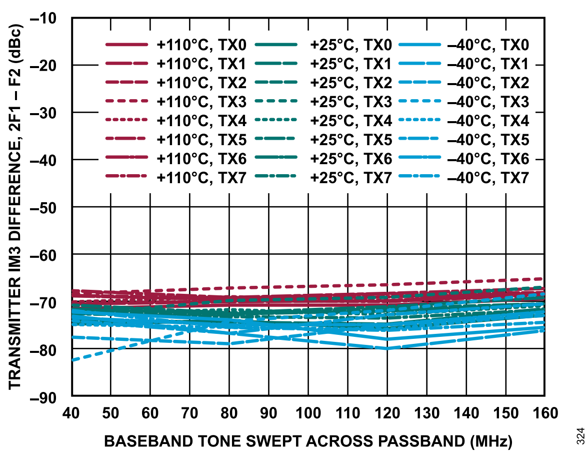

Figure 320. Transmitter IM3, 2f1 − f2 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = 5 MHz

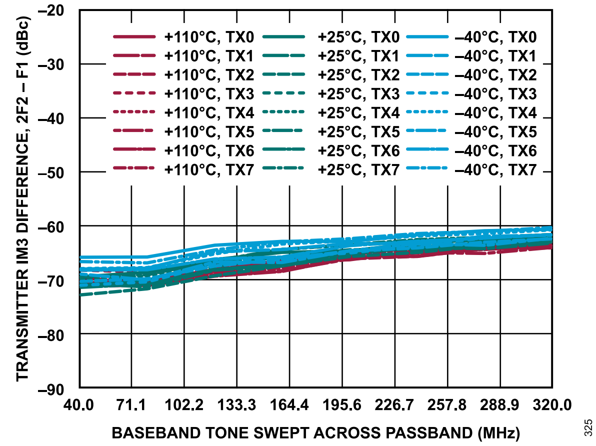

Figure 321. Transmitter IM3, 2f2 − f1 vs. Baseband Tone Swept Across Pass Band, −15 dBFS Signal Level per Tone, f2 = 5 MHz

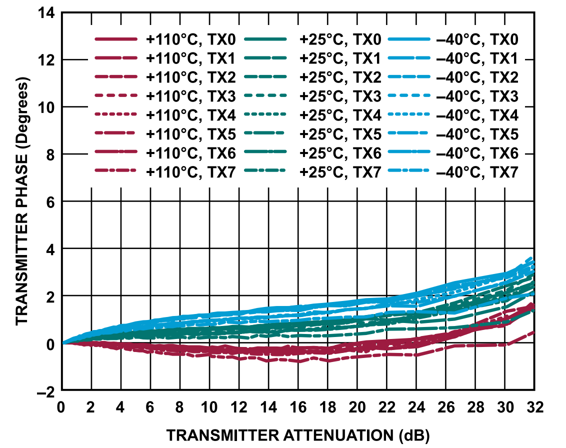

Figure 322. Transmitter Phase vs. Transmitter Attenuation

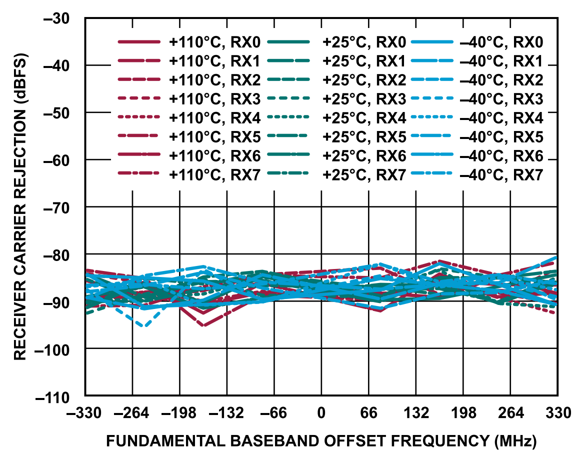

Figure 323. Receiver Carrier Rejection vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

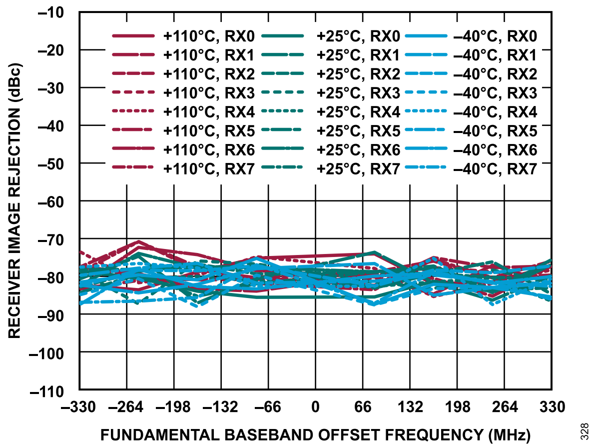

Figure 324. Receiver Image Rejection vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

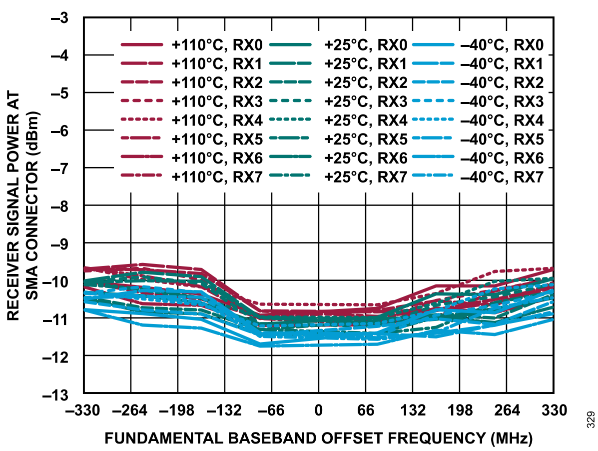

Figure 325. Receiver Signal Power at SMA Connector vs. Fundamental Baseband Offset Frequency, −1 dBFs Input Signal (Match Is Not De-Embedded)

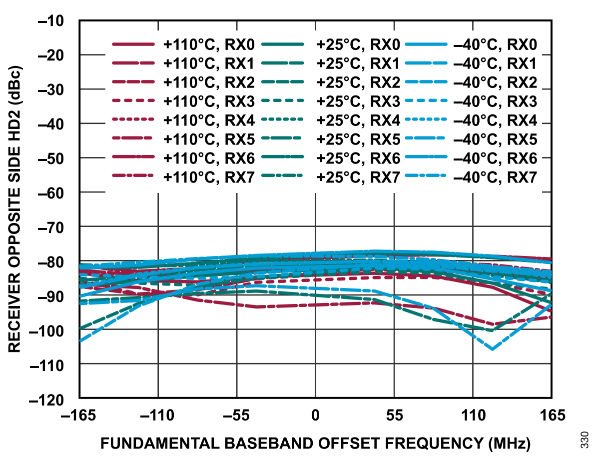

Figure 326. Receiver Opposite Side HD2 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

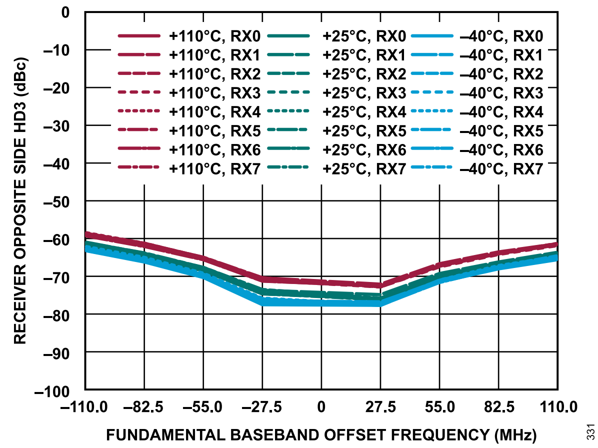

Figure 327. Receiver Opposite Side HD3 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

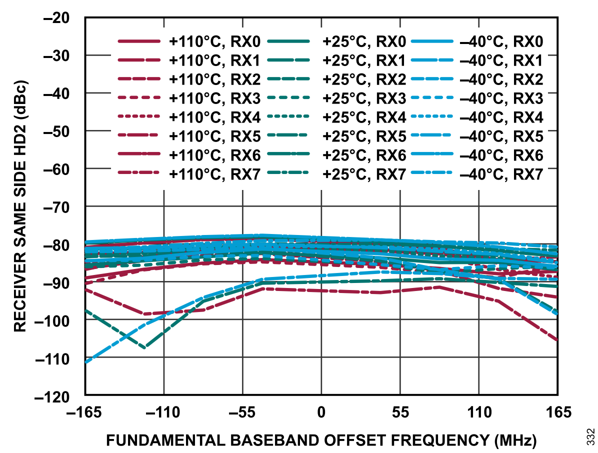

Figure 328. Receiver Same Side HD2 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

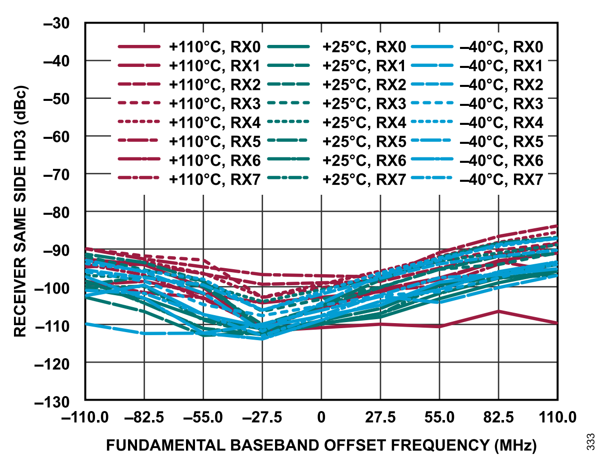

Figure 329. Receiver Same Side HD3 vs. Fundamental Baseband Offset Frequency, −1 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

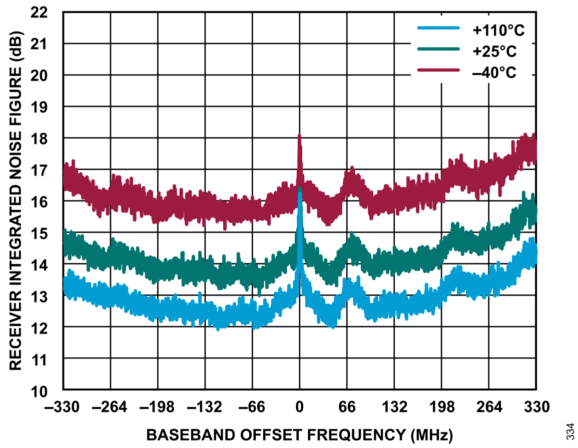

Figure 330. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 kHz Integration Steps, 983.04 MSPS Sample Rate

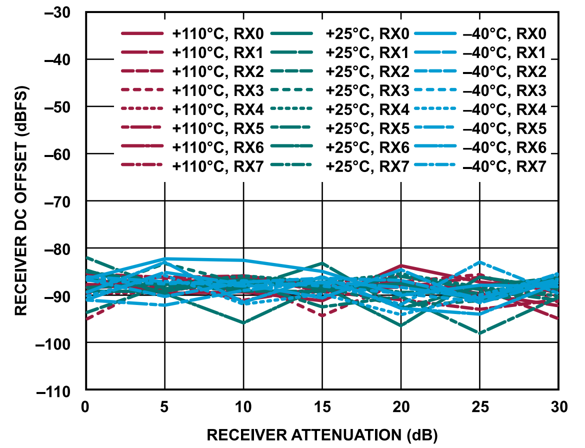

Figure 333. Receiver DC Offset vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

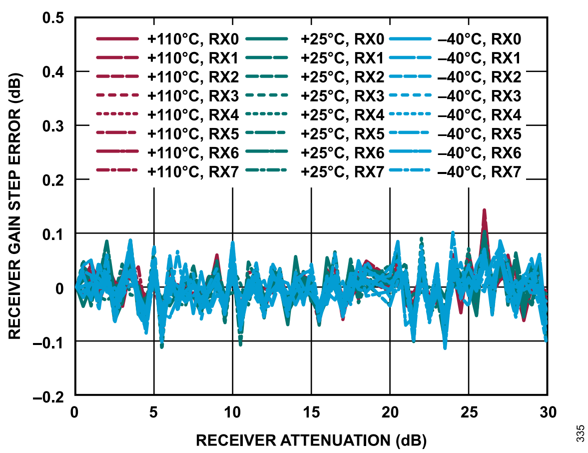

Figure 331. Receiver Gain Step Error vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

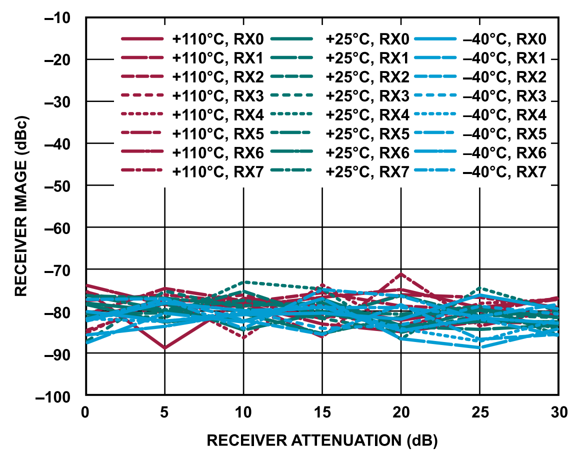

Figure 334. Receiver Image vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

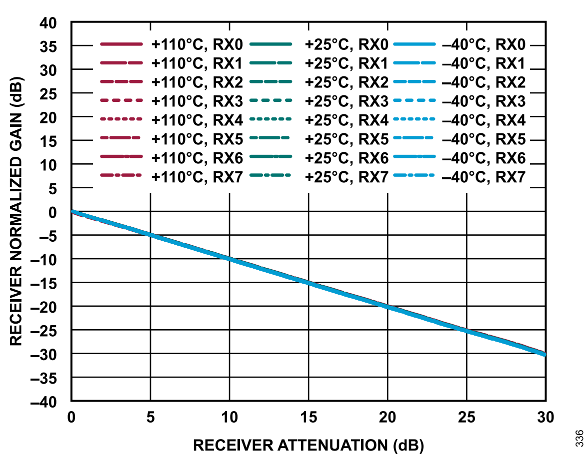

Figure 332. Receiver Normalized Gain vs. Receiver Attenuation, 30 MHz Offset, −1 dBFS Input Signal

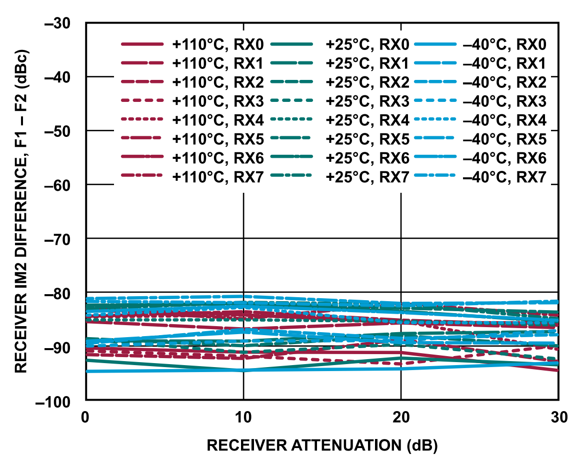

Figure 335. Receiver IM2, f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 328 MHz Offset, f2 = 2 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

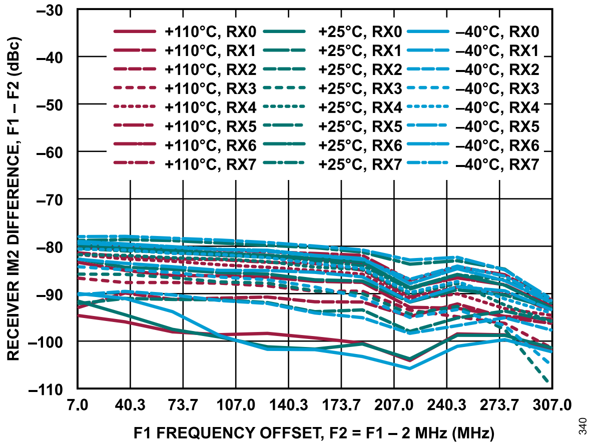

Figure 336. Receiver IM2, f1 − f2 vs. f1 Frequency Offset, f2 = f1 − 2 MHz, −7 dBFS Signal Level per Tone, f2 = f1 − 2 MHz

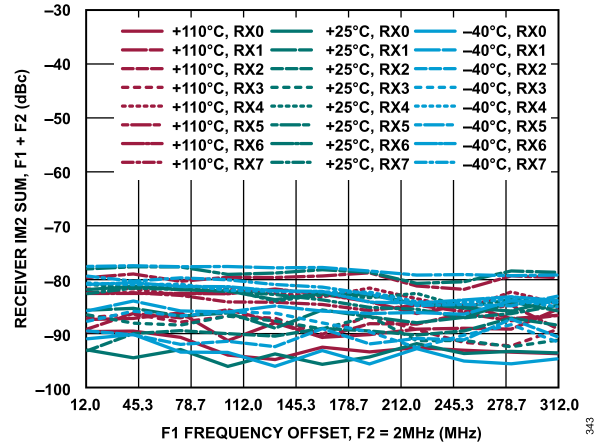

Figure 339. Receiver IM2, f1 + f2 vs. Frequency Offset, −7 dBFS Signal Level per Tone, f2 = 2 MHz

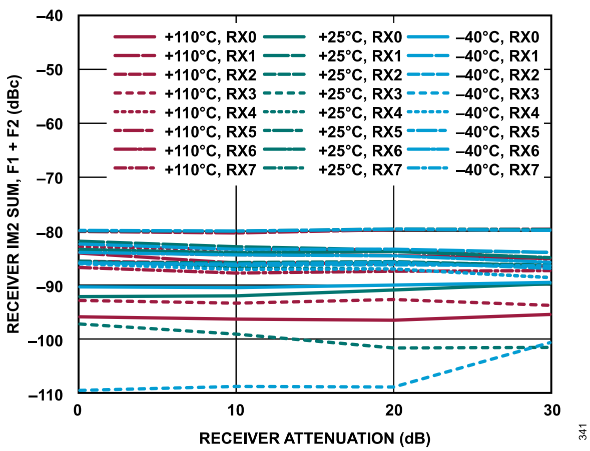

Figure 337. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 166 MHz Offset, f2 = 164 MHz Offset

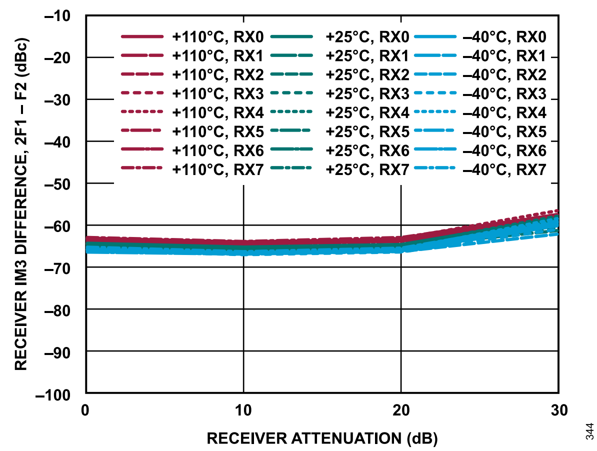

Figure 340. Receiver IM3, 2f1 − f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 166 MHz Offset, f2 = 2 MHz Offset

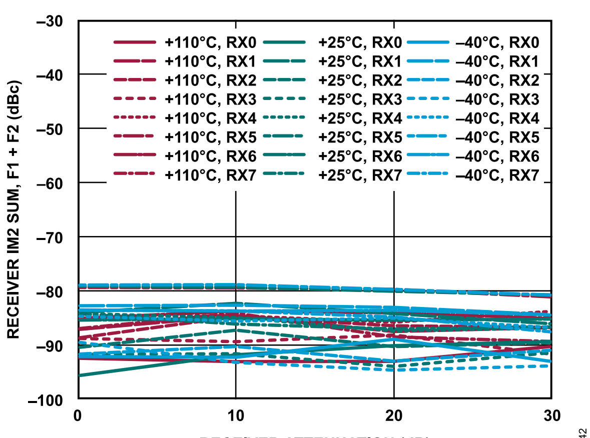

Figure 338. Receiver IM2, f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 328 MHz Offset, f2 = 2 MHz Offset

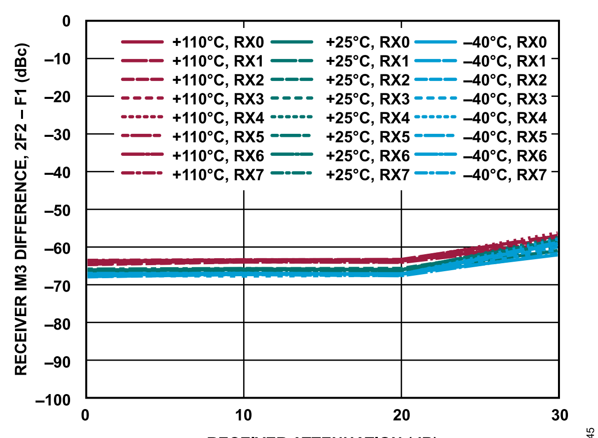

Figure 341. Receiver IM3, 2f2 − f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 326 MHz Offset, f2 = 328 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

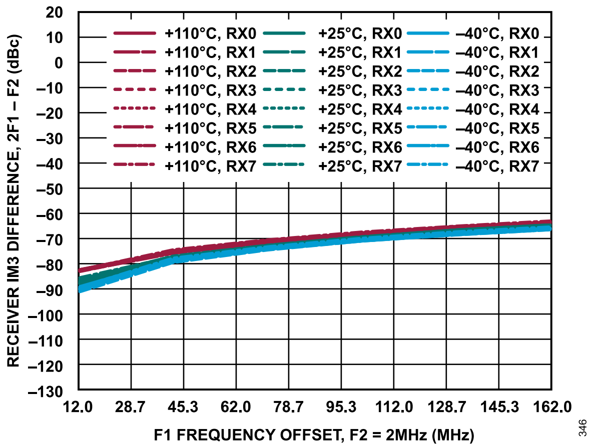

Figure 342. Receiver IM3, 2f1 − f2 vs. f1 Frequency Offset, f2 = 2 MHz, −7 dBFS Signal Level per Tone

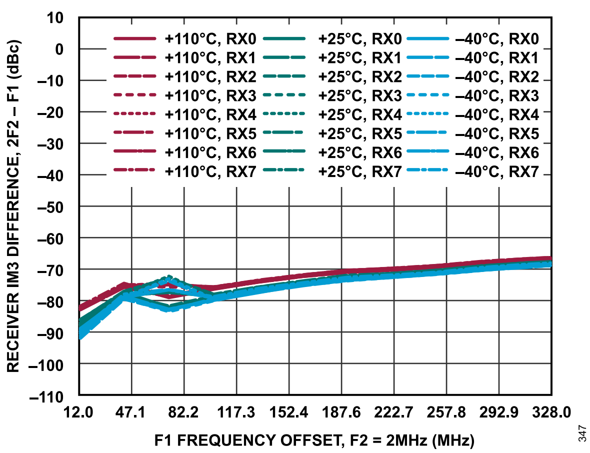

Figure 343. Receiver IM3, 2f2 − f1 vs. f1 Frequency Offset, f2 = 2 MHz, −7 dBFS Signal Level per Tone

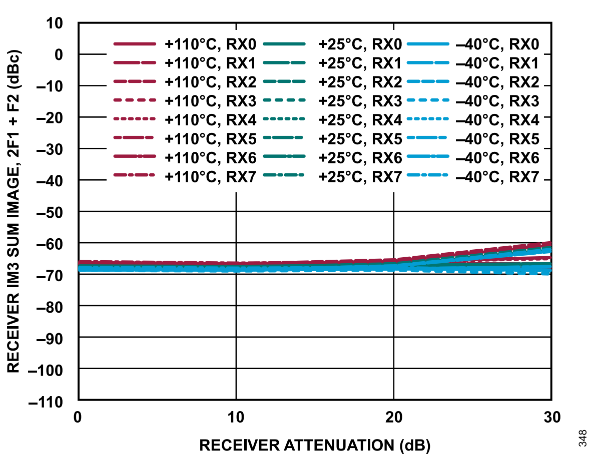

Figure 344. Receiver IM3, 2f1 + f2 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 162 MHz Offset, f2 = 2 MHz Offset

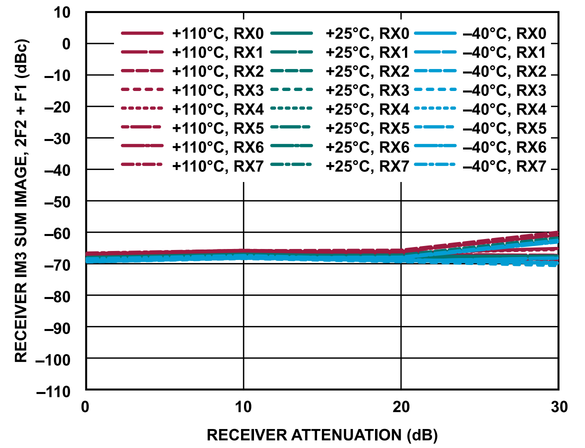

Figure 345. Receiver IM3, 2f2 + f1 vs. Receiver Attenuation, −7 dBFS Signal Level per Tone, f1 = 312 MHz Offset, f2 = 2 MHz Offset

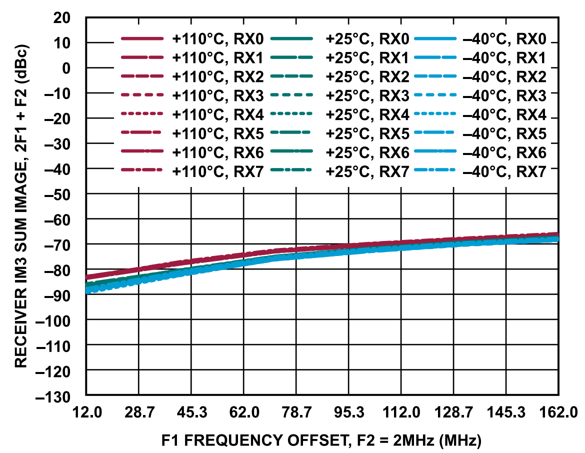

Figure 346. Receiver IM3, 2f1 + f2 vs. f1 Frequency Offset, f2 = 2 MHz, −7 dBFS Signal Level per Tone

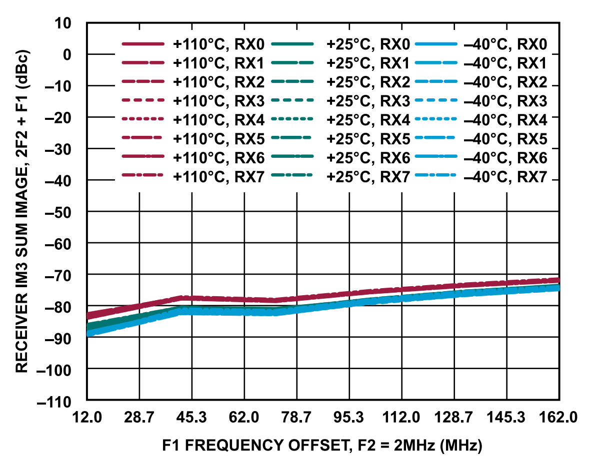

Figure 347. Receiver IM3, 2f2 + f1 vs. f1 Frequency Offset, f2 = 2 MHz, −7 dBFS Signal Level per Tone

TYPICAL PERFORMANCE CHARACTERISTICS

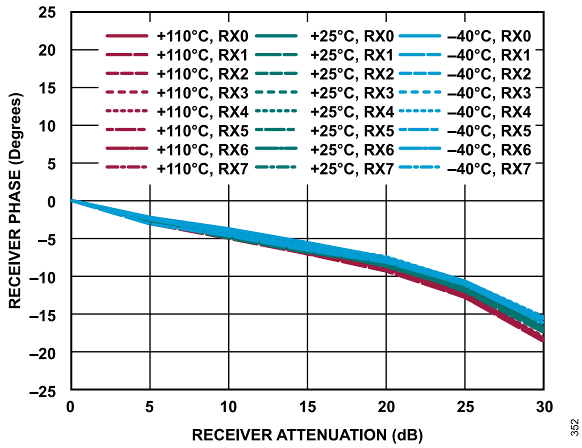

Figure 348. Receiver Phase vs. Receiver Attenuation

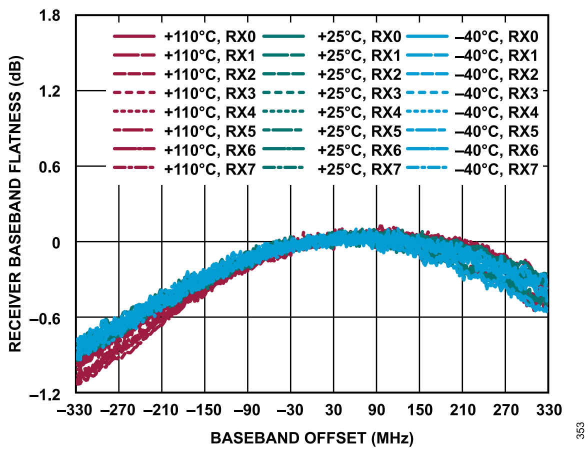

Figure 349. Receiver Baseband Flatness vs. Baseband Offset

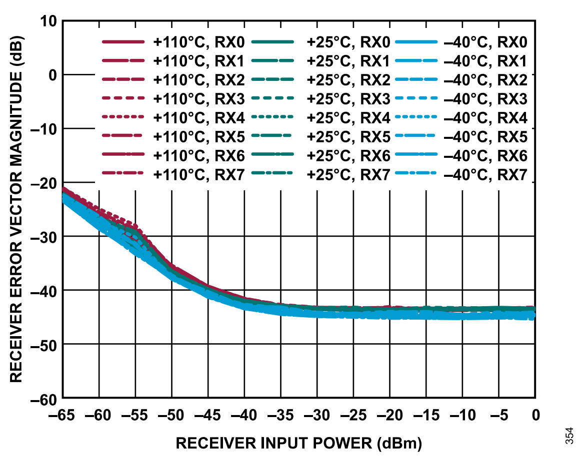

Figure 350. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Centered Around DC, TDD Mode, AGC Enabled

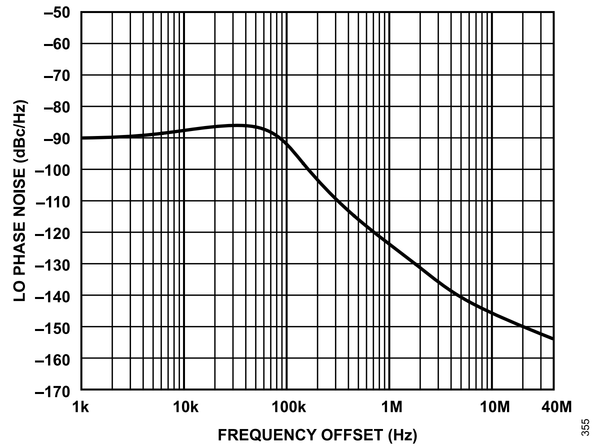

Figure 351. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 60 kHz, Phase Margin = 55°

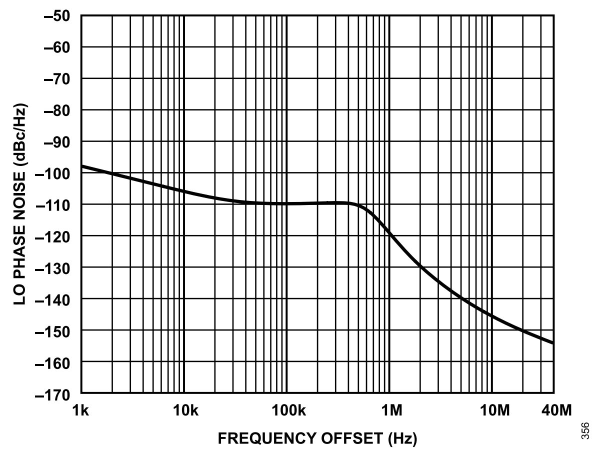

Figure 352. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 55°

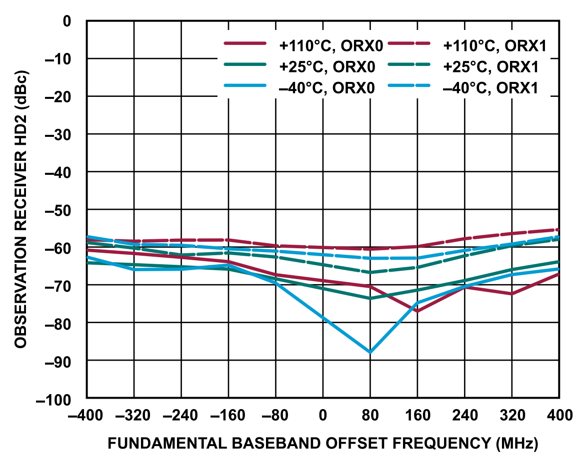

Figure 353. Observation Receiver HD2 vs. Fundamental Baseband Offset Frequency, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

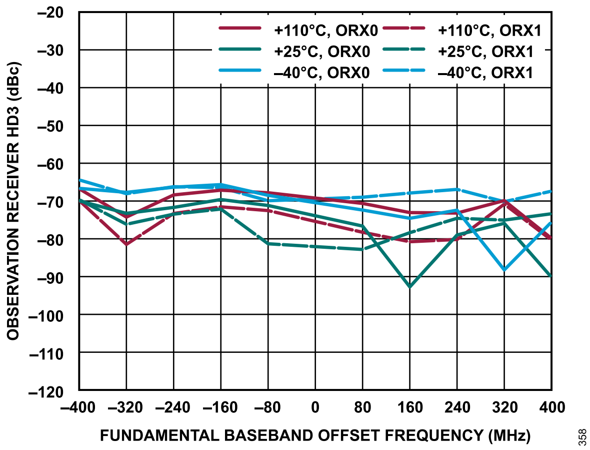

Figure 354. Observation Receiver HD3 vs. Fundamental Baseband Offset Frequency, −10 dBFS Input Signal

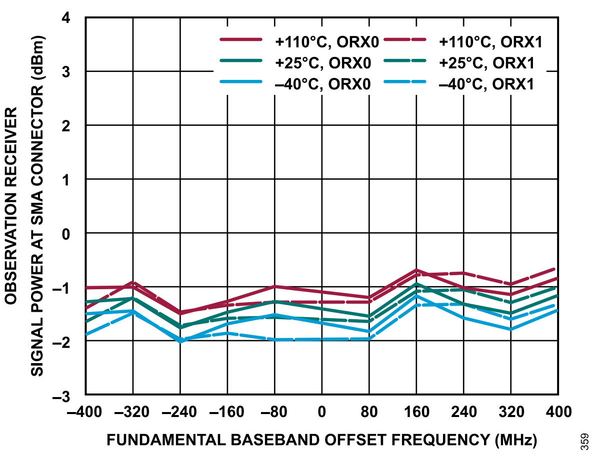

Figure 355. Observation Receiver Signal Power at SMA Connector vs. Fundamental Baseband Offset Frequency, −10 dBFS Input Signal (Match Is Not De-Embedded)

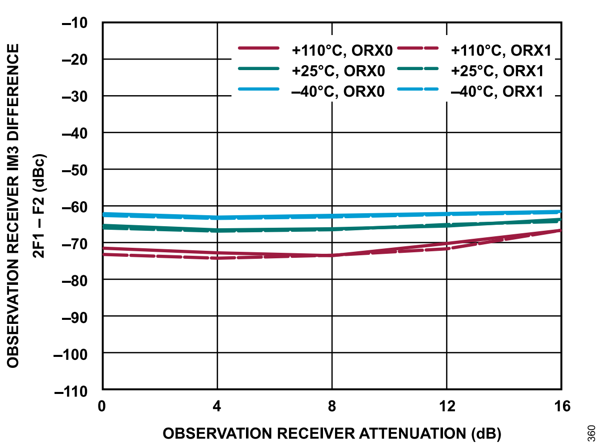

Figure 356. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 5602 MHz, f2 = 5612 MHz

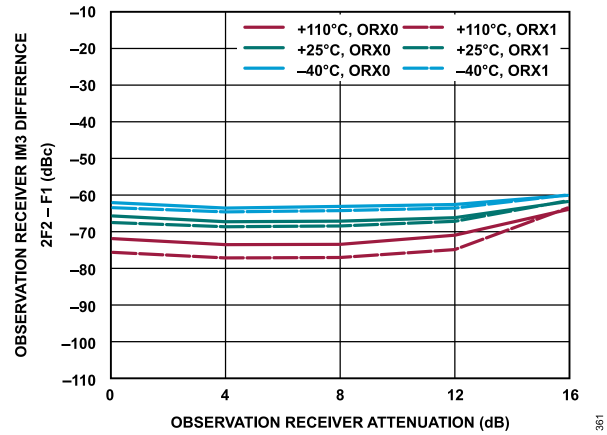

Figure 357. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 3502 MHz, f2 = 3512 MHz

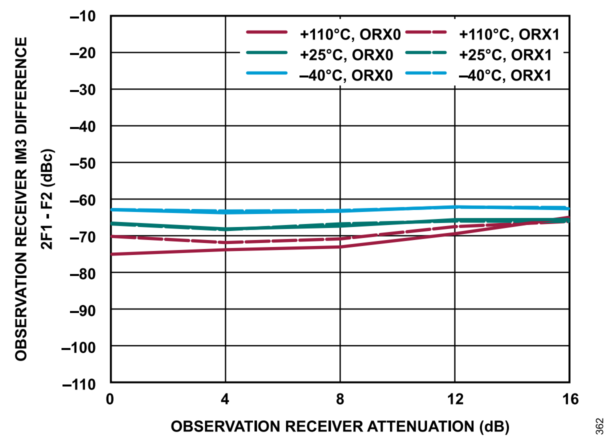

Figure 358. Observation Receiver IM3, 2f1 − f2 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 5602 MHz, f2 = 5812 MHz

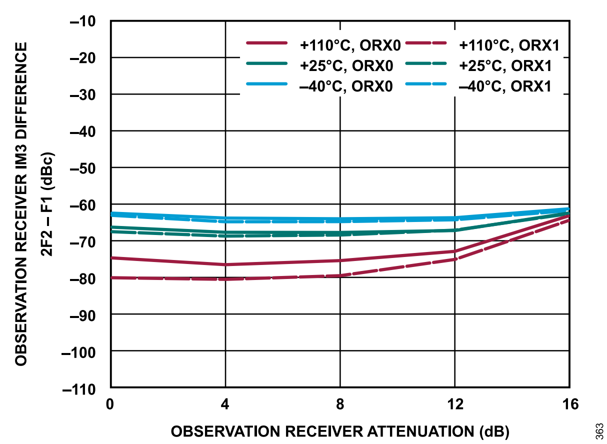

Figure 359. Observation Receiver IM3, 2f2 − f1 vs. Observation Receiver Attenuation, −13 dBFS Signal Level per Tone, f1 = 5602 MHz, f2 = 5812 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

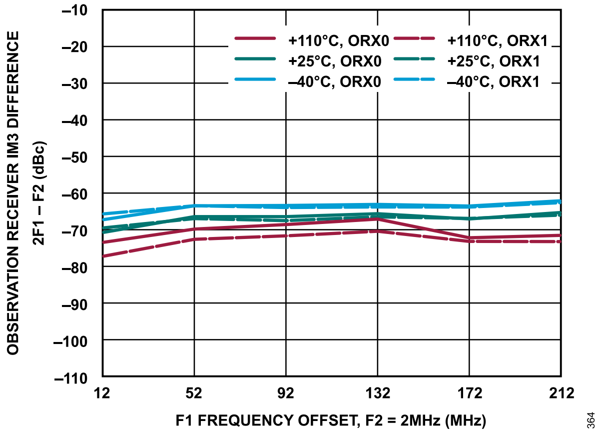

Figure 360. Observation Receiver IM3, 2f1 − f2 vs. f1 Frequency Offset, f2 = 2 MHz, −13 dBFS Signal Level per Tone

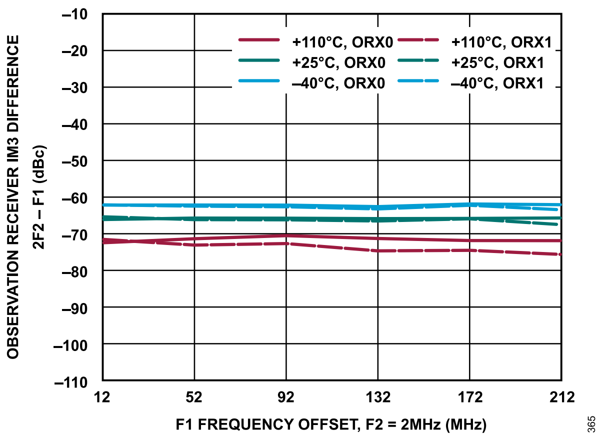

Figure 361. Observation Receiver IM3, 2f2 − f1 vs. f1 Frequency Offset, f2 = 2 MHz, −13 dBFS Signal Level per Tone

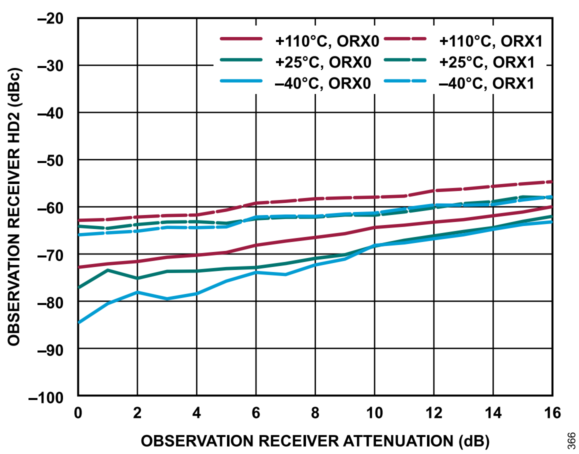

Figure 362. Observation Receiver HD2 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

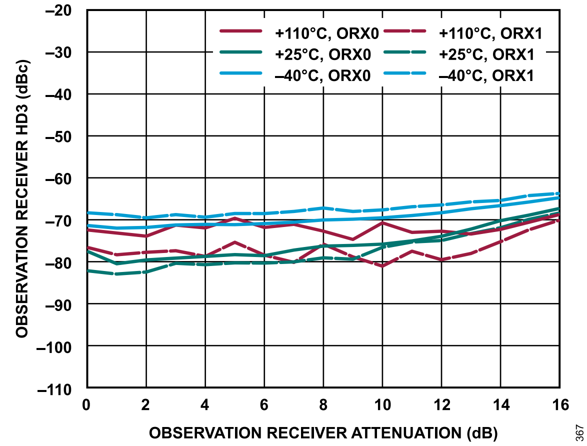

Figure 363. Observation Receiver HD3 vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

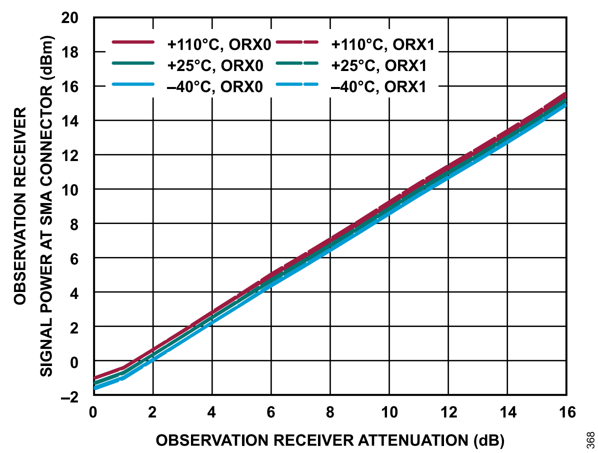

Figure 364. Observation Receiver Signal Power at SMA Connector vs. Observation Receiver Attenuation, 80 MHz Offset, −10 dBFS Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

ACROSS LO FREQUENCY

The temperature settings refer to the die temperature. The observation receiver measurements are taken with 5898.24 MHz sampling frequency for less than 5 GHz LO frequency and 7863.42 MHz sampling frequency for greater than 5 GHz LO frequency.

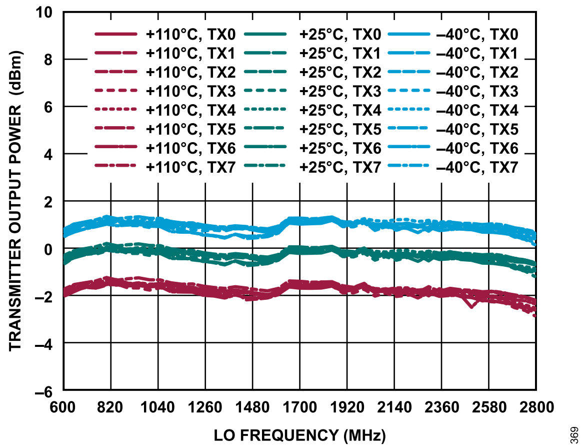

Figure 365. Transmitter Output Power vs. LO Frequency, Low Band Matching, 30 MHz Offset, 0 dB RF Attenuation, −6 dBFS Signal Level

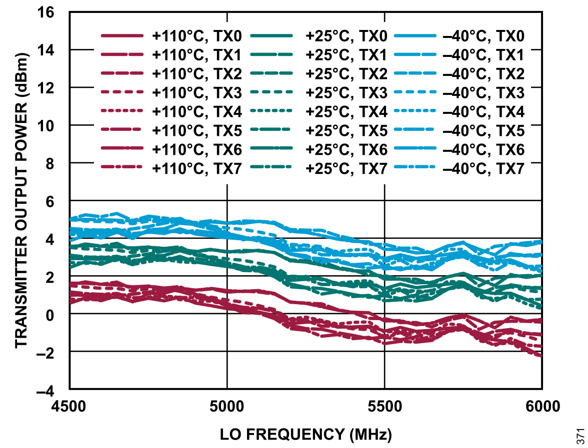

Figure 367. Transmitter Output Power vs. LO Frequency, High Band Matching, 30 MHz Offset, 0 dB RF Attenuation, −6 dBFS Signal Level

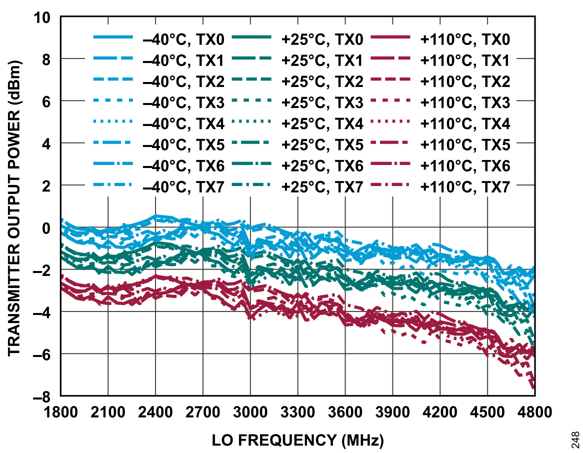

Figure 366. Transmitter Output Power vs. LO Frequency, Middle Band Matching, 30 MHz Offset, 0 dB RF Attenuation, −6 dBFS Signal Level

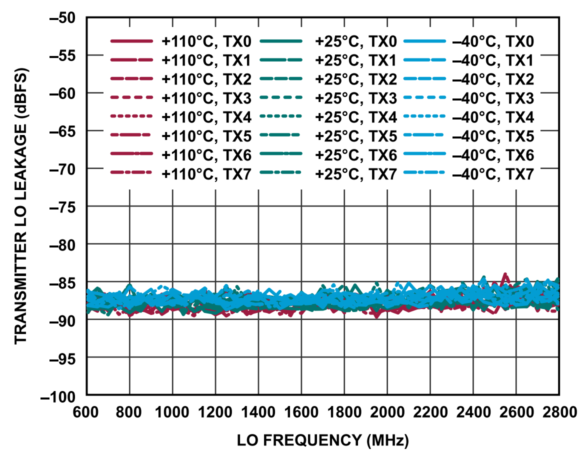

Figure 368. Transmitter LO Leakage vs. LO Frequency, Low Band Matching

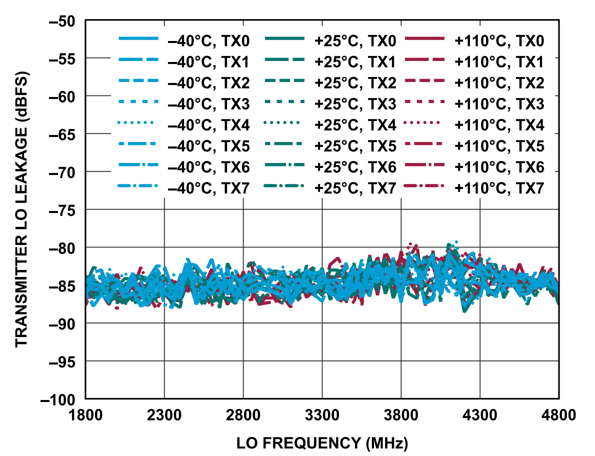

Figure 369. Transmitter LO Leakage vs. LO Frequency, Middle Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

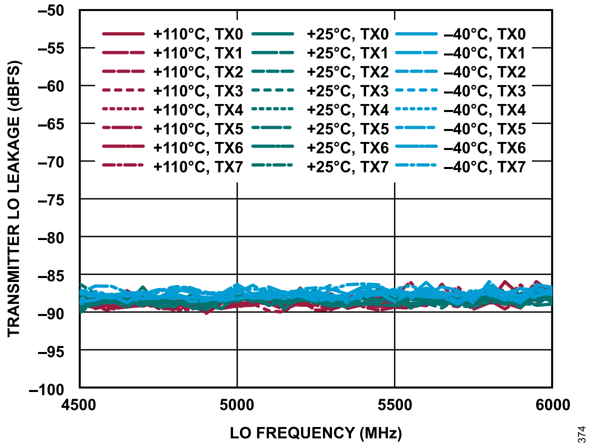

Figure 370. Transmitter LO Leakage vs. LO Frequency, High Band Matching

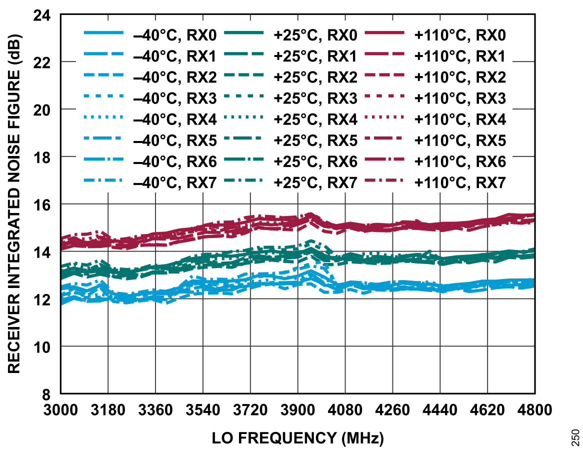

Figure 371. Receiver Integrated Noise Figure vs. LO Frequency, 600 MHz Integration Bandwidth

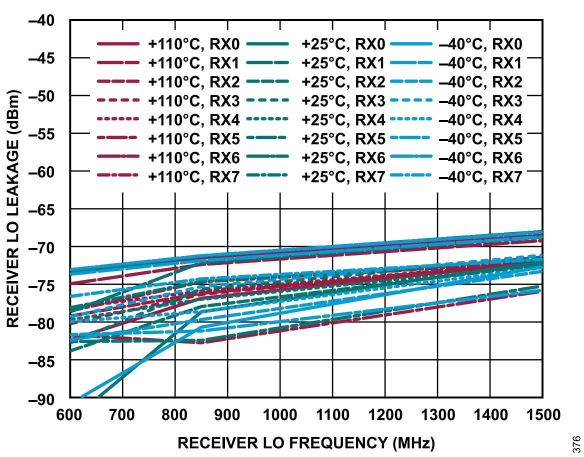

Figure 372. Receiver LO Leakage vs. Receiver LO Frequency, Maximum Receiver Gain, Low Band Matching

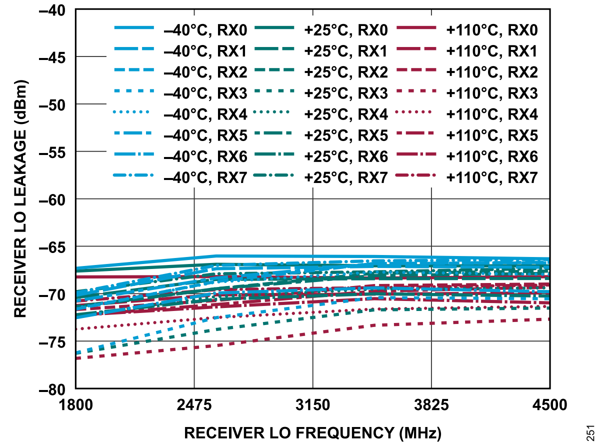

Figure 373. Receiver LO Leakage vs. Receiver LO Frequency, Maximum Receiver Gain, Middle Band Matching

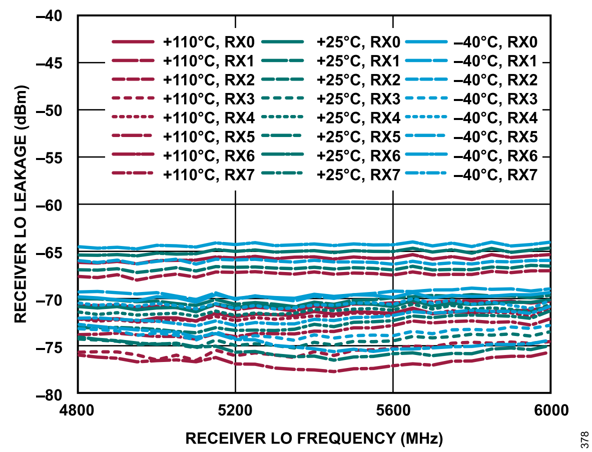

Figure 374. Receiver LO Leakage vs. Receiver LO Frequency, Maximum Receiver Gain, High Band Matching

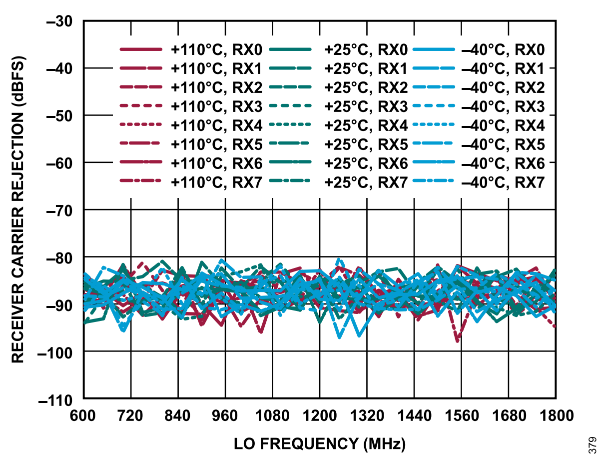

Figure 375. Receiver Carrier Rejection vs. LO Frequency, Low Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

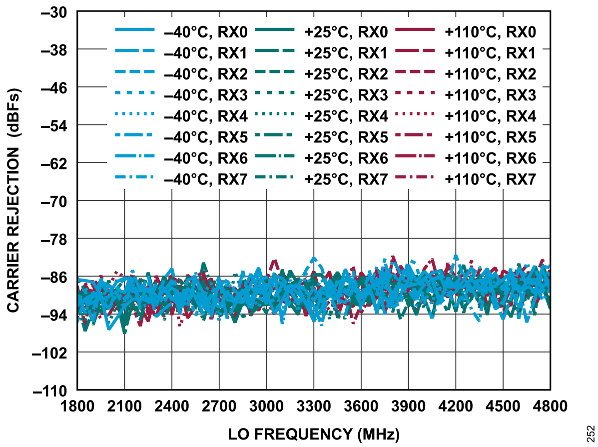

Figure 376. Carrier Rejection vs. LO Frequency, Middle Band Matching

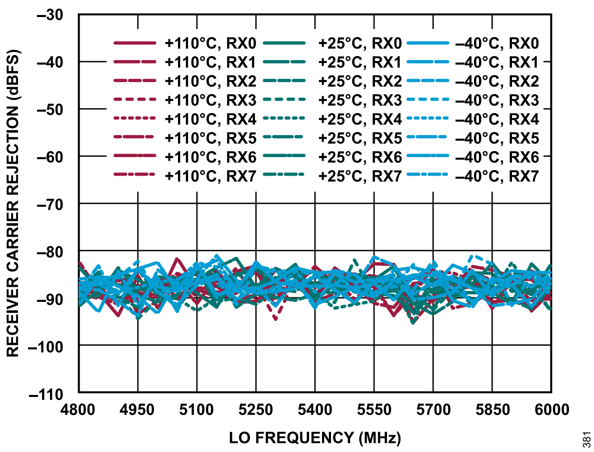

Figure 377. Receiver Carrier Rejection vs. LO Frequency, High Band Matching

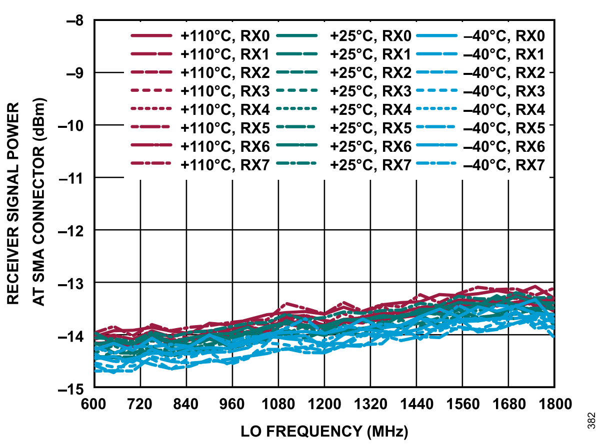

Figure 378. Receiver Signal Power at SMA Connector vs. LO Frequency, Low Band Matching

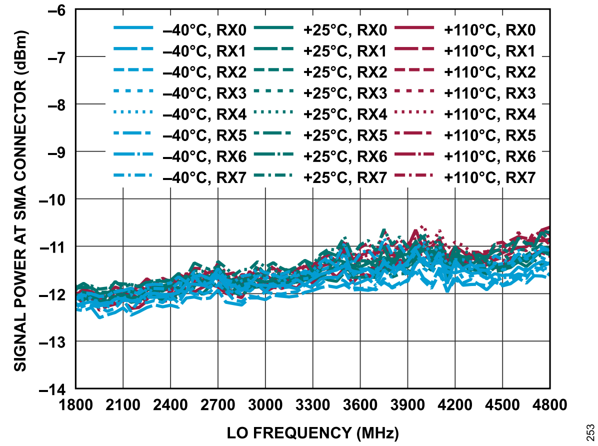

Figure 379. Receiver Signal Power at SMA Connector vs. LO Frequency, Middle Band Matching

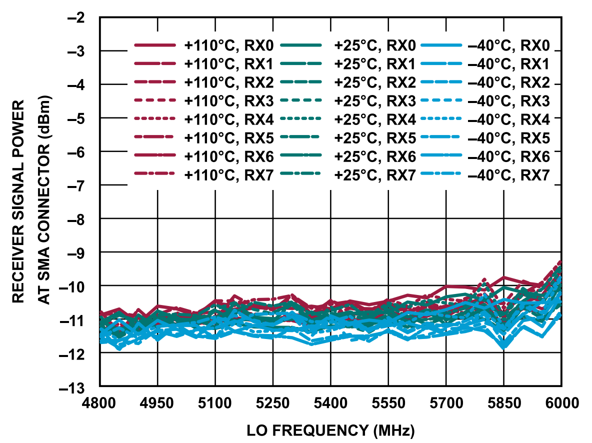

Figure 380. Receiver Signal Power at SMA Connector vs. LO Frequency, High Band Matching

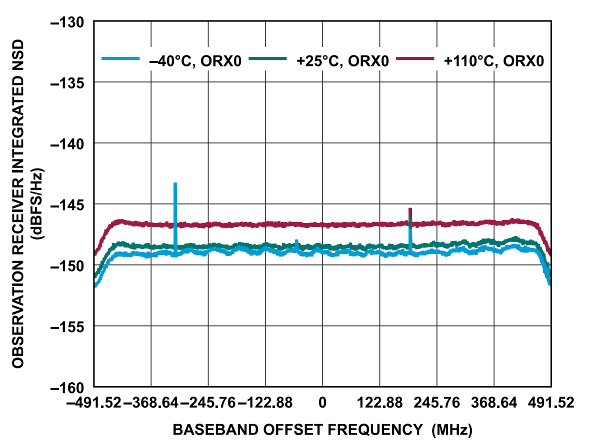

Figure 381. Observation Receiver Integrated NSD vs. LO Frequency, 1800 MHz, 5898.24 MSPS Sample Rate

TYPICAL PERFORMANCE CHARACTERISTICS

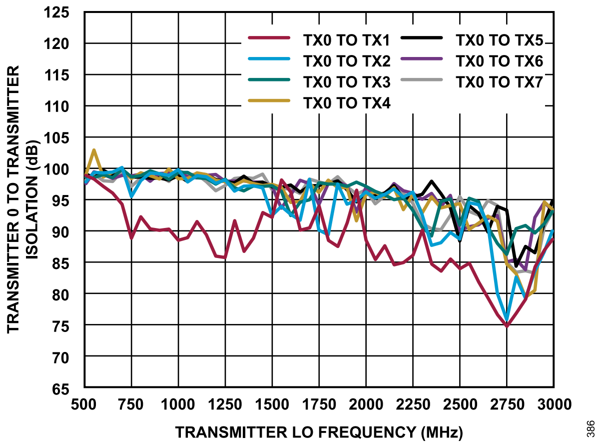

Figure 382. Transmitter 0 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

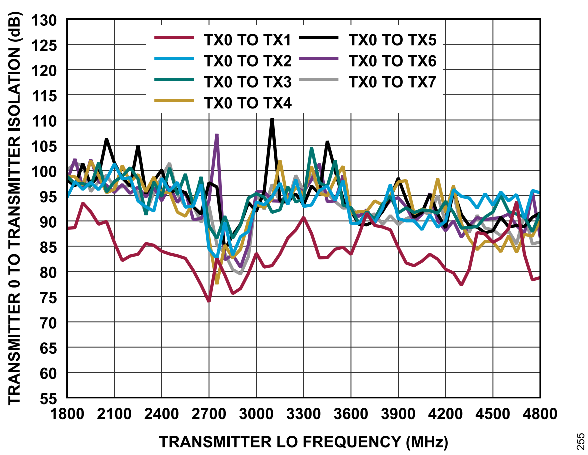

Figure 383. Transmitter 0 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

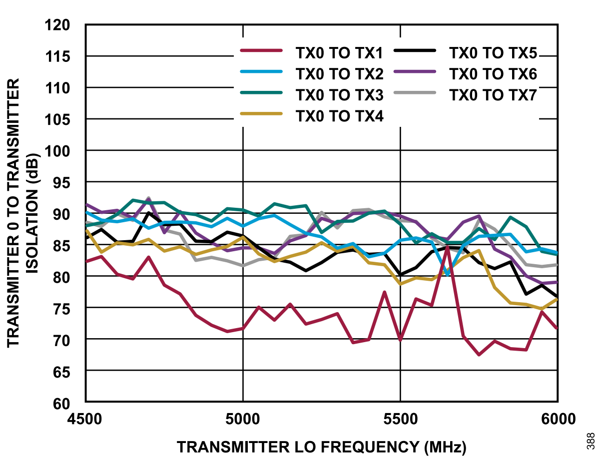

Figure 384. Transmitter 0 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

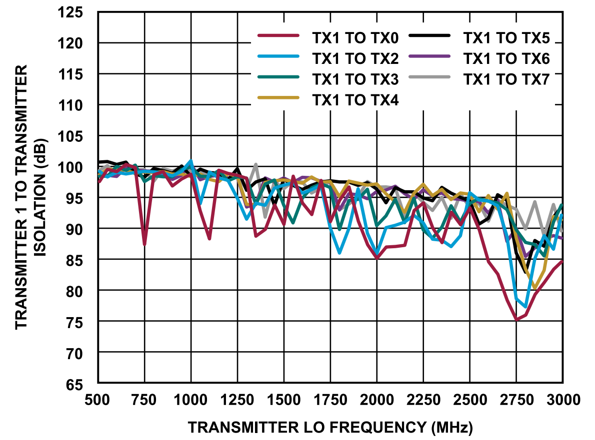

Figure 385. Transmitter 1 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

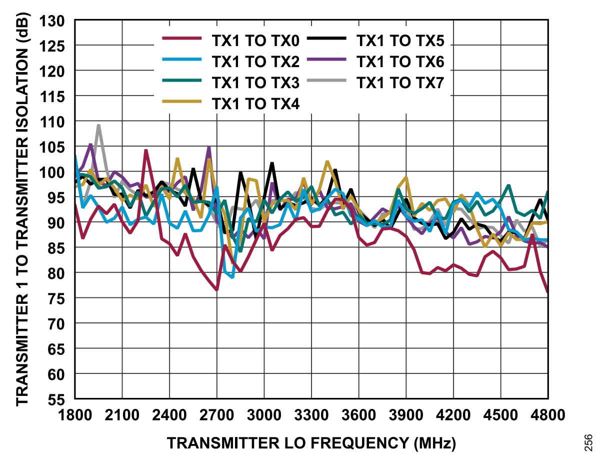

Figure 386. Transmitter 1 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

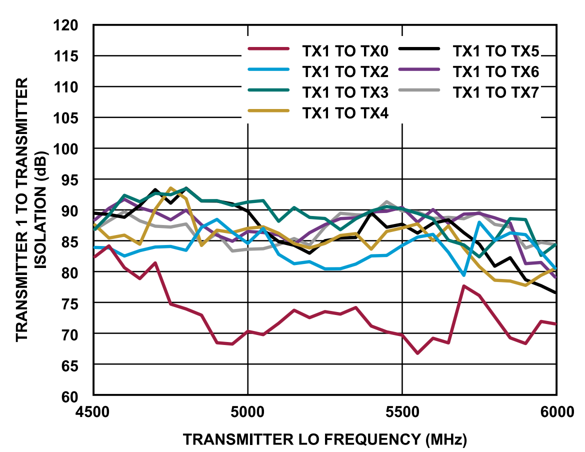

Figure 387. Transmitter 1 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

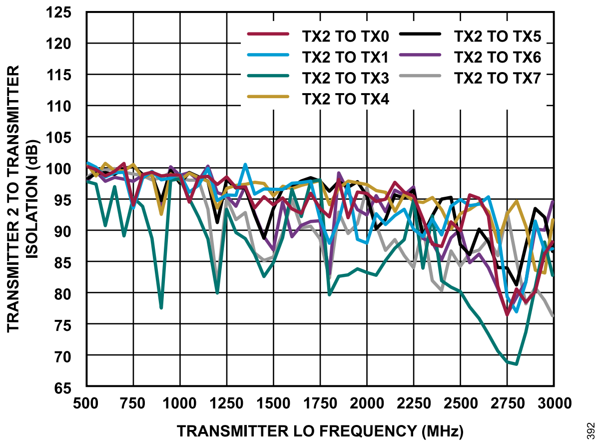

Figure 388. Transmitter 2 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

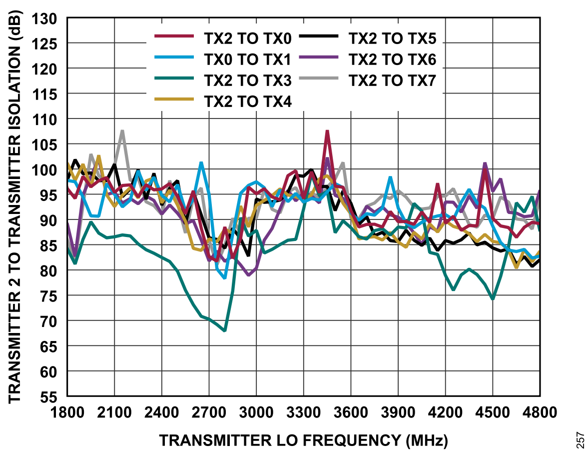

Figure 389. Transmitter 2 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

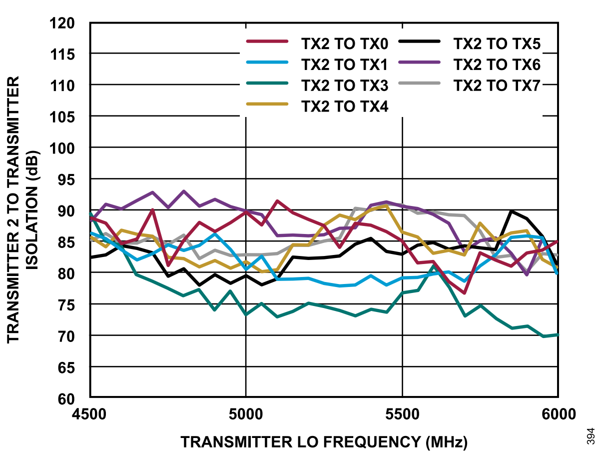

Figure 390. Transmitter 2 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

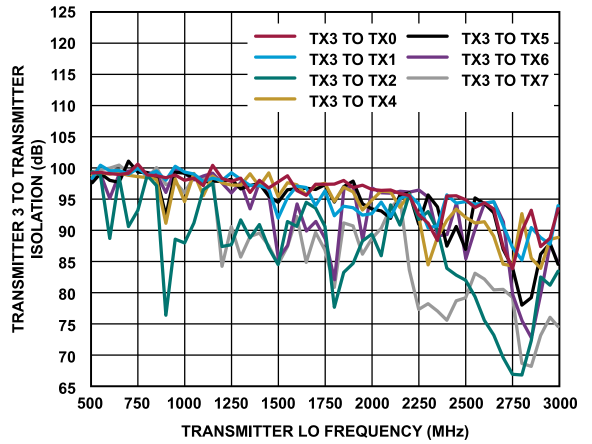

Figure 391. Transmitter 3 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

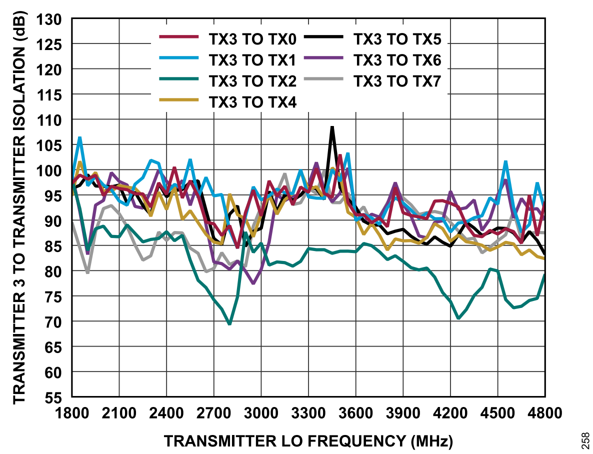

Figure 392. Transmitter 3 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

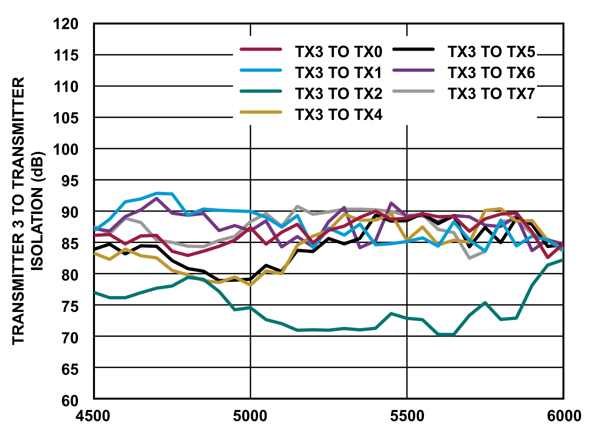

Figure 393. Transmitter 3 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

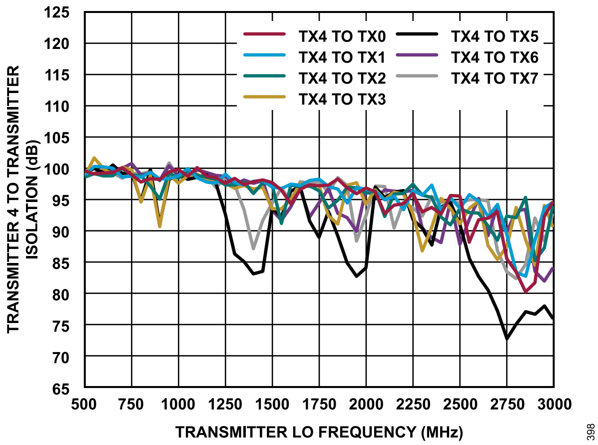

Figure 394. Transmitter 4 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

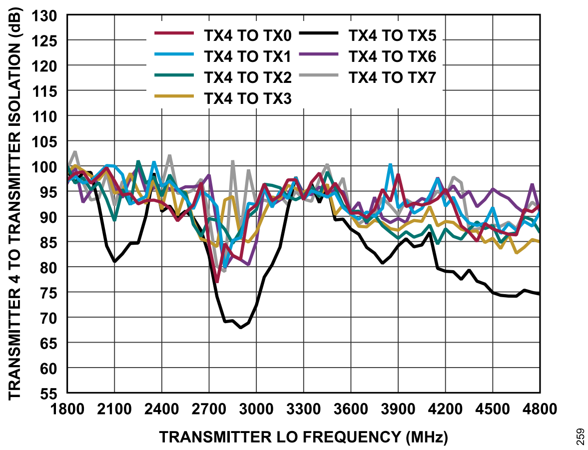

Figure 395. Transmitter 4 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

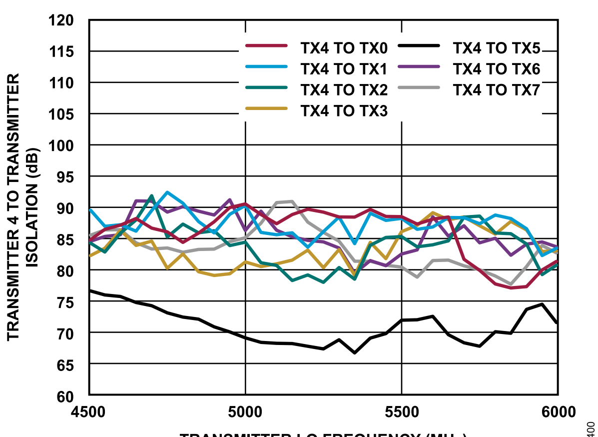

Figure 396. Transmitter 4 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

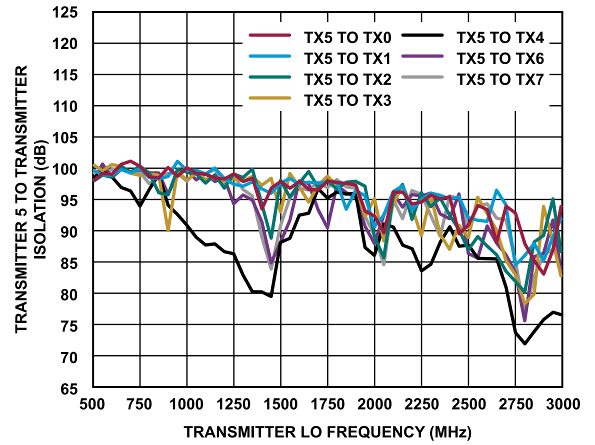

Figure 397. Transmitter 5 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

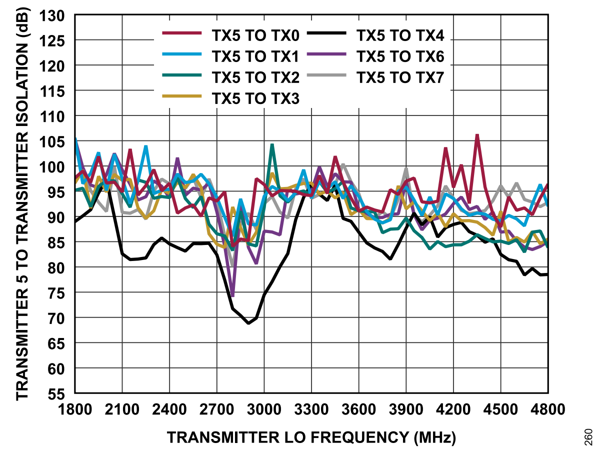

Figure 398. Transmitter 5 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

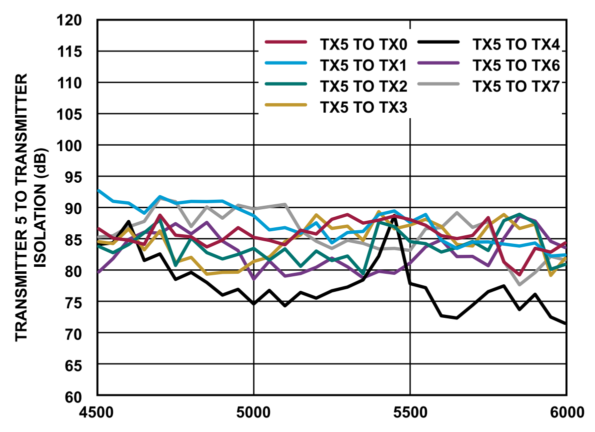

Figure 399. Transmitter 5 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

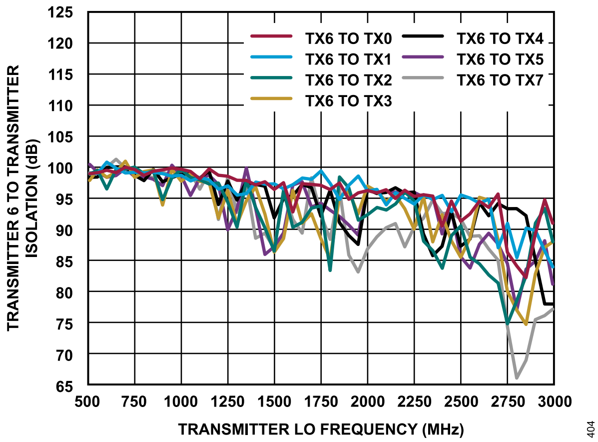

Figure 400. Transmitter 6 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

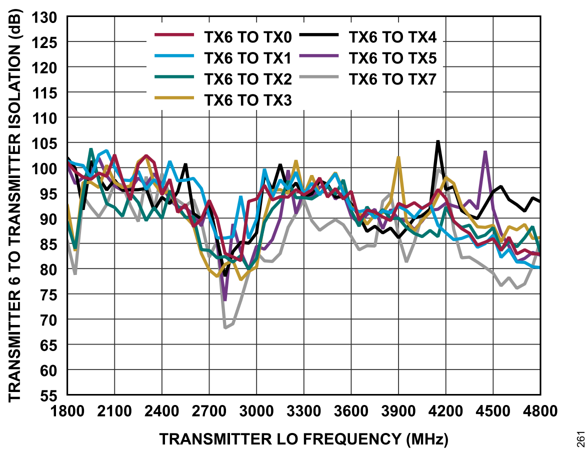

Figure 401. Transmitter 6 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

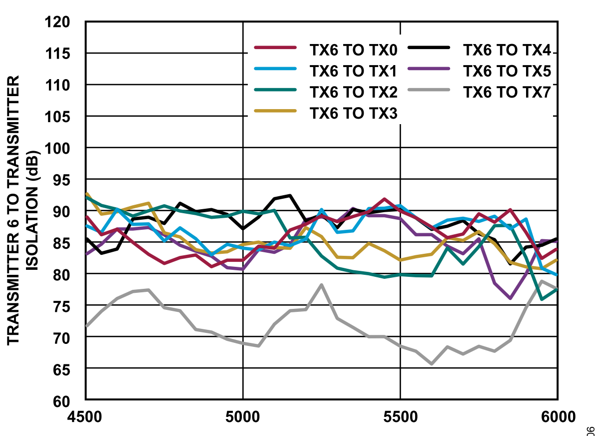

Figure 402. Transmitter 6 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

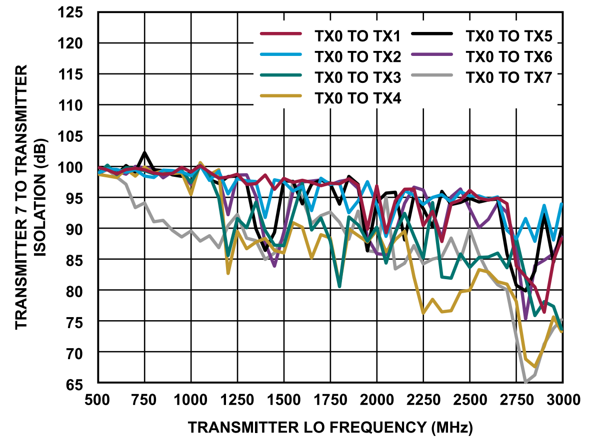

Figure 403. Transmitter 7 to Transmitter Isolation vs. Transmitter LO Frequency, Low Band Matching

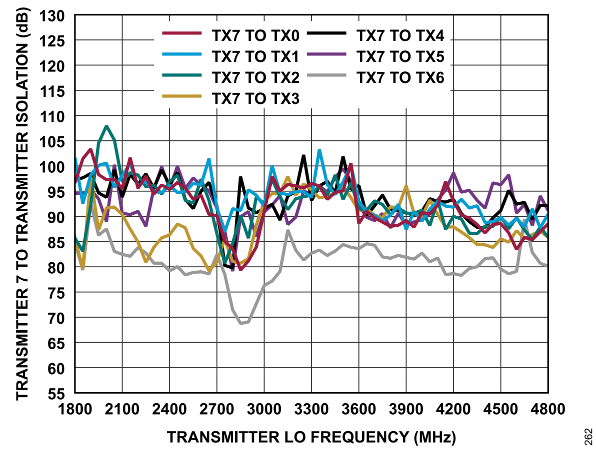

Figure 404. Transmitter 7 to Transmitter Isolation vs. Transmitter LO Frequency, Middle Band Matching

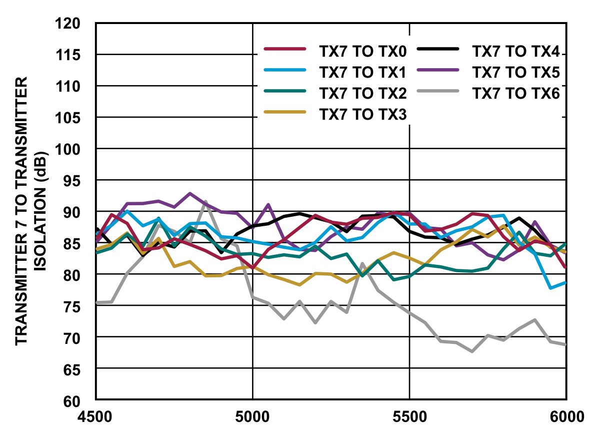

Figure 405. Transmitter 7 to Transmitter Isolation vs. Transmitter LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

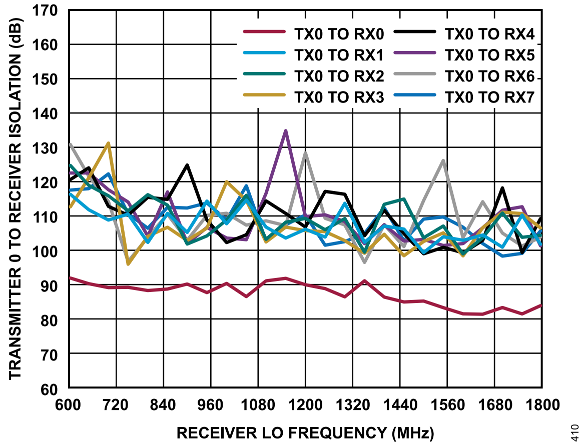

Figure 406. Transmitter 0 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

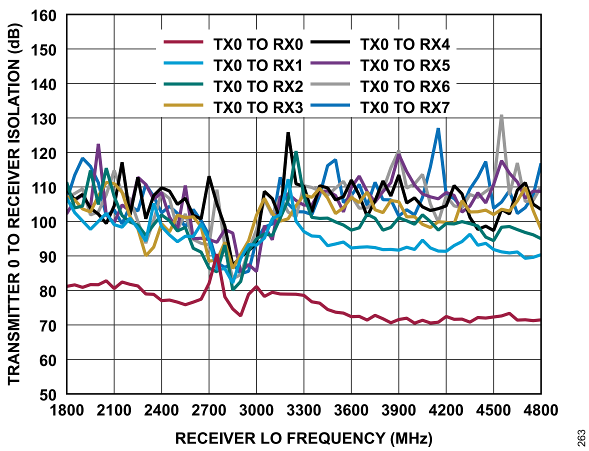

Figure 407. Transmitter 0 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

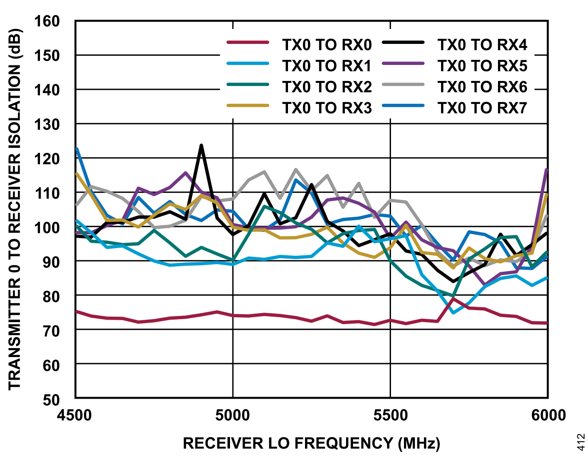

Figure 408. Transmitter 0 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

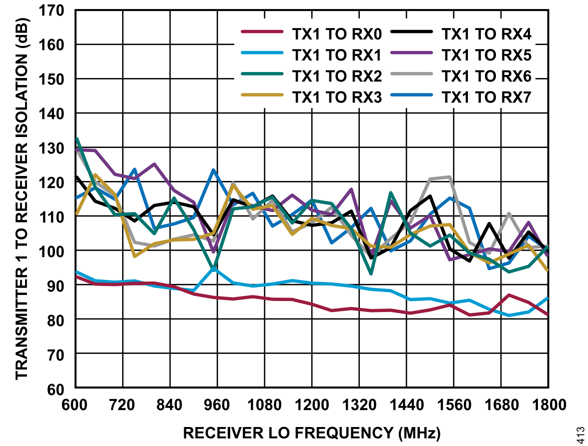

Figure 409. Transmitter 1 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

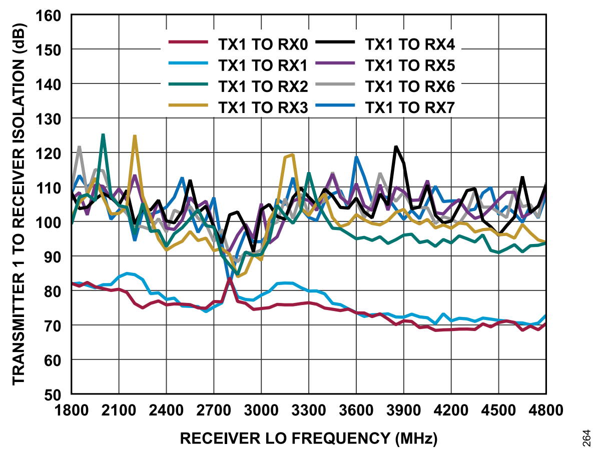

Figure 410. Transmitter 1 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

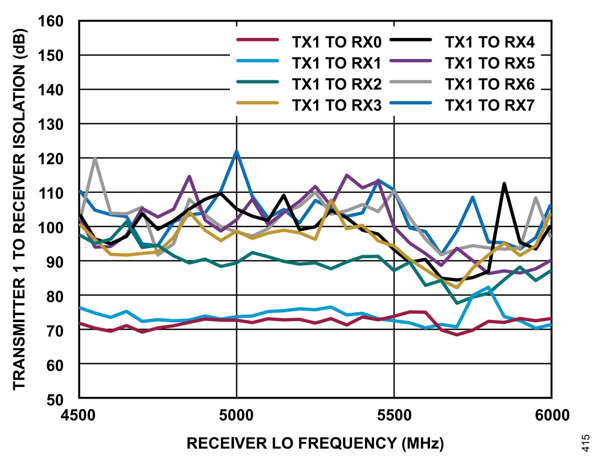

Figure 411. Transmitter 1 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

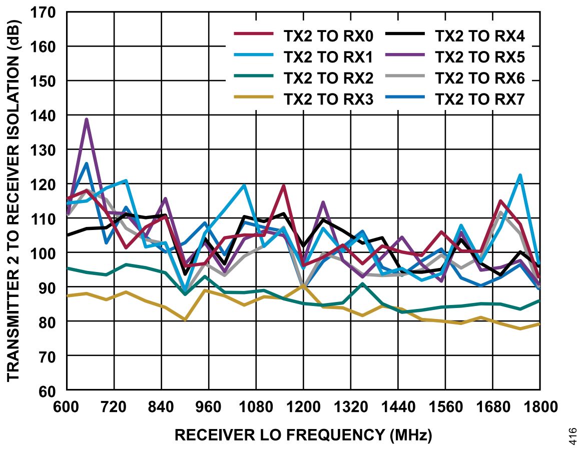

Figure 412. Transmitter 2 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

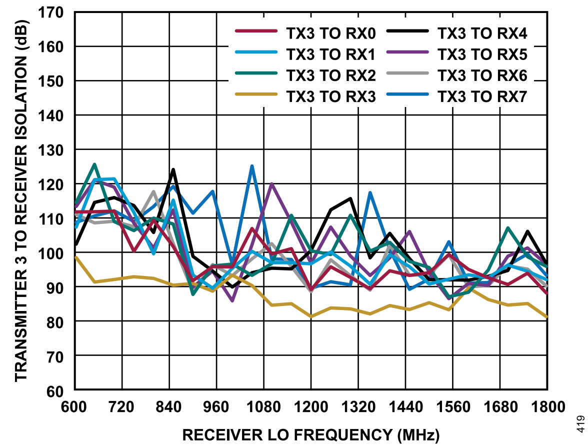

Figure 415. Transmitter 3 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

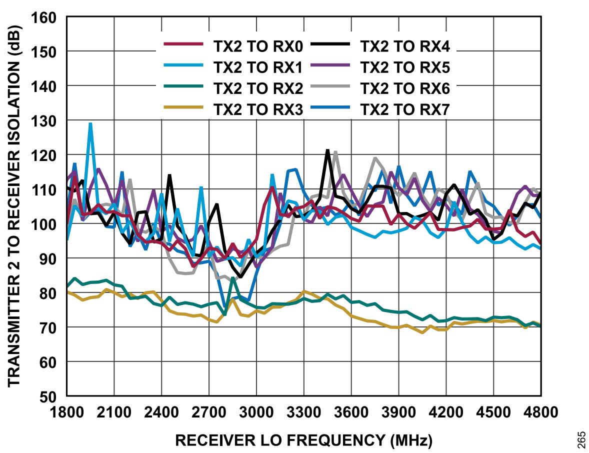

Figure 413. Transmitter 2 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

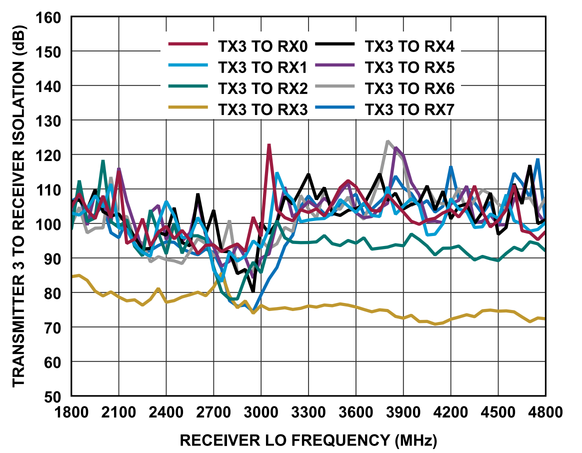

Figure 416. Transmitter 3 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

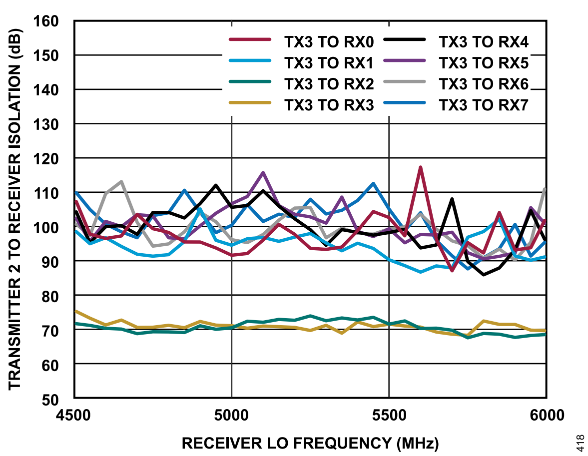

Figure 414. Transmitter 2 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

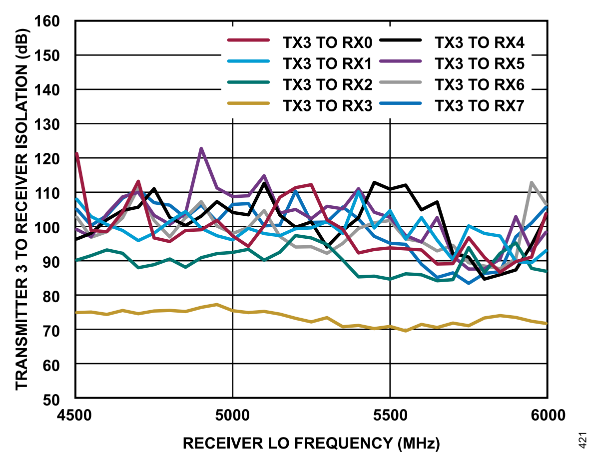

Figure 417. Transmitter 3 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

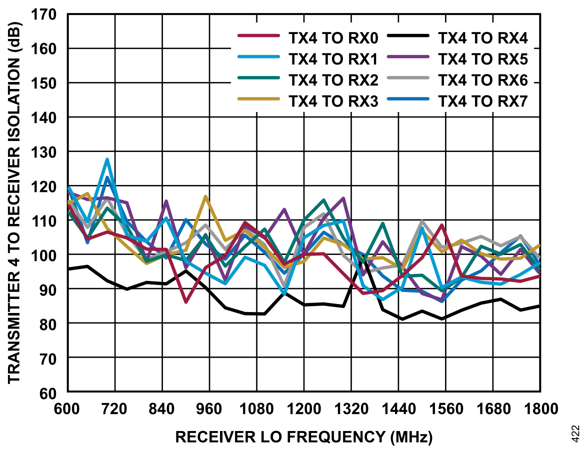

Figure 418. Transmitter 4 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

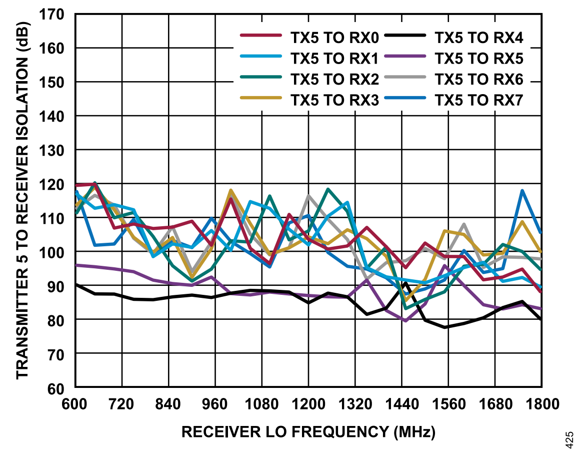

Figure 421. Transmitter 5 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

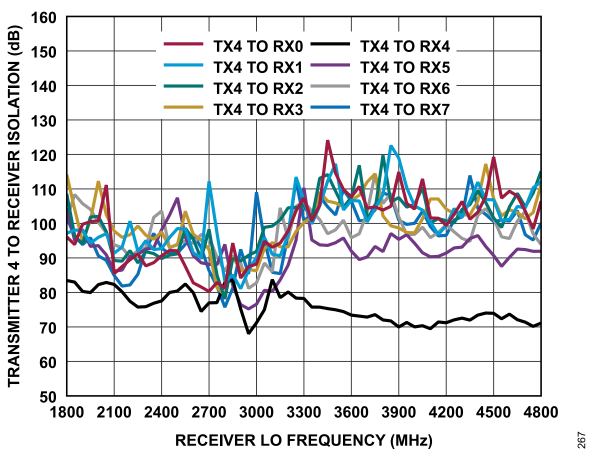

Figure 419. Transmitter 4 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

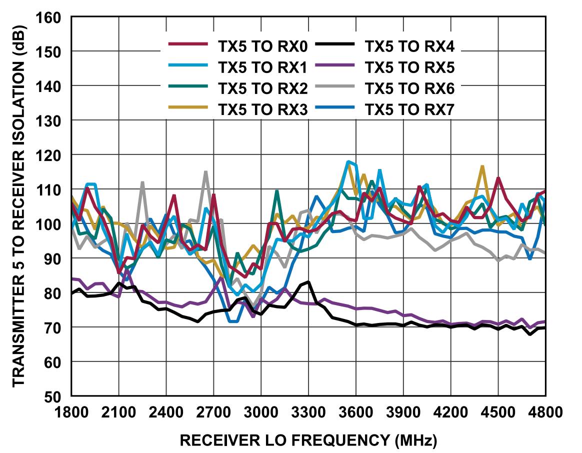

Figure 422. Transmitter 5 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

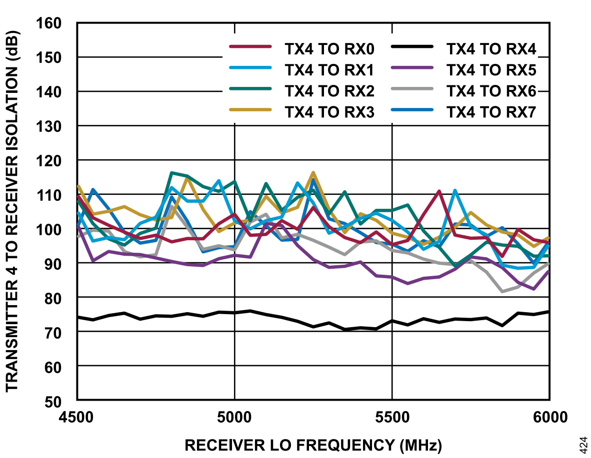

Figure 420. Transmitter 4 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

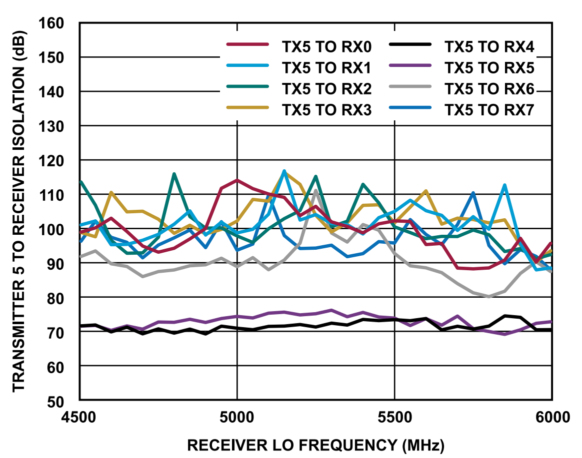

Figure 423. Transmitter 5 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

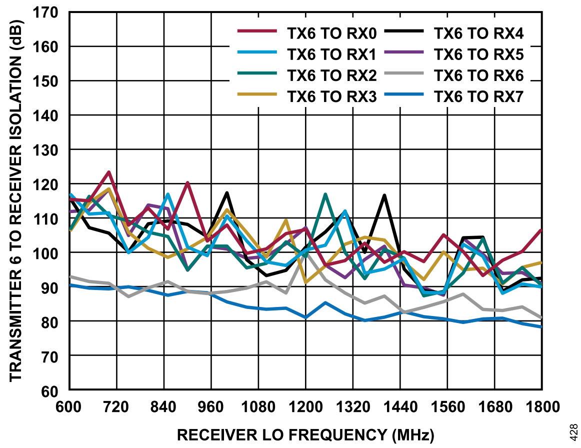

Figure 424. Transmitter 6 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

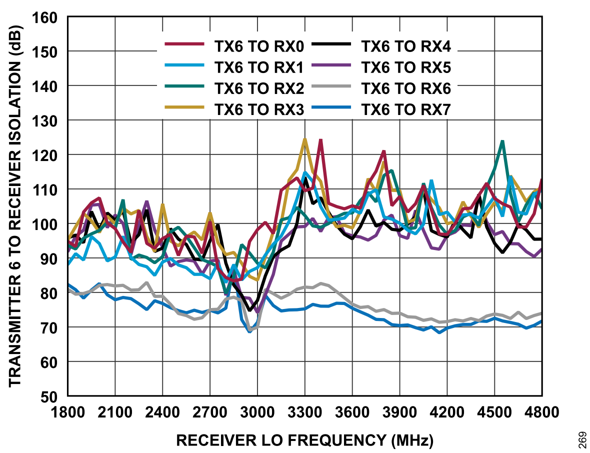

Figure 425. Transmitter 6 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

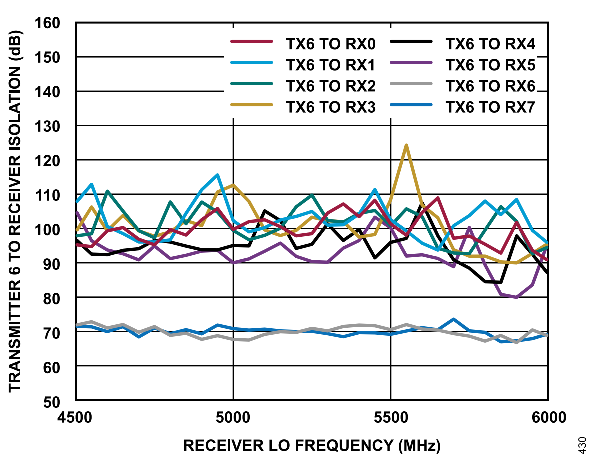

Figure 426. Transmitter 6 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

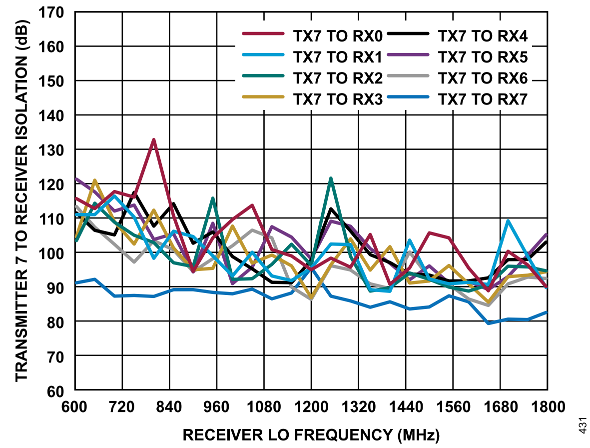

Figure 427. Transmitter 7 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

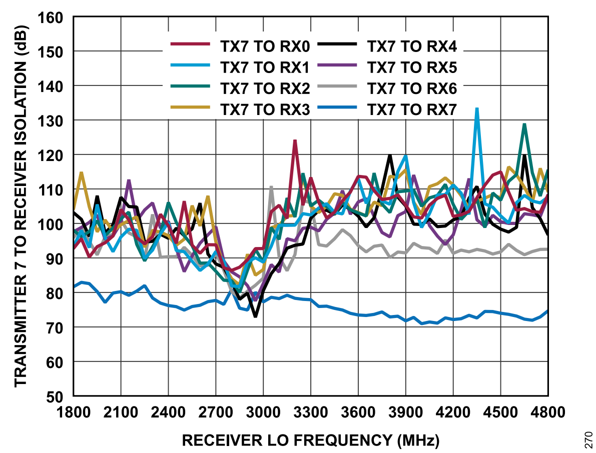

Figure 428. Transmitter 7 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

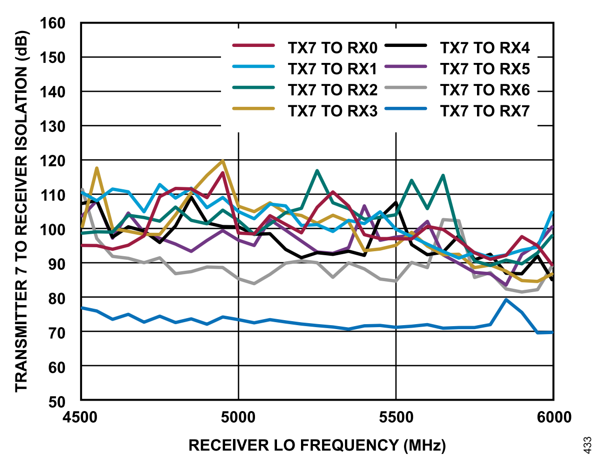

Figure 429. Transmitter 7 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

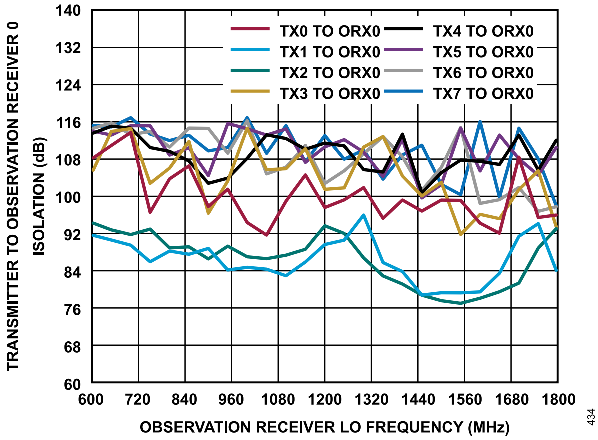

Figure 430. Transmitter to Observation Receiver 0 Isolation vs. Observation Receiver LO Frequency, Low Band Matching

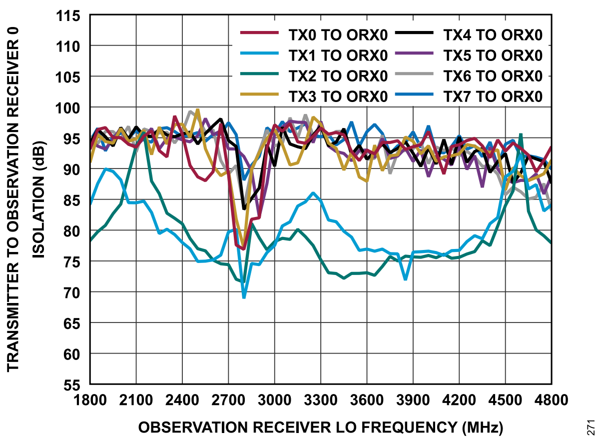

Figure 431. Transmitter to Observation Receiver 0 Isolation vs. Observation Receiver LO Frequency, Middle Band Matching

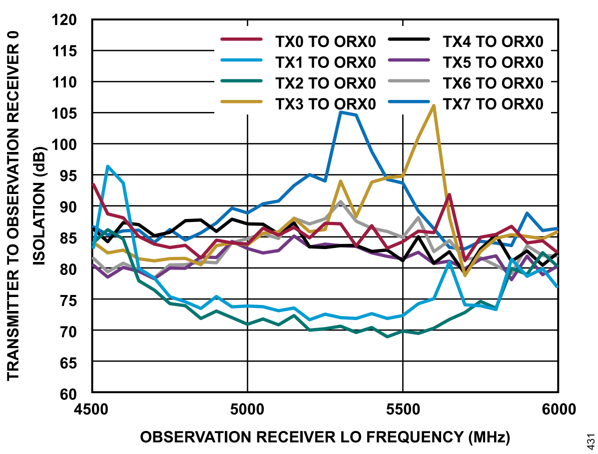

Figure 432. Transmitter to Observation Receiver 0 Isolation vs. Observation Receiver LO Frequency, High Band Matching

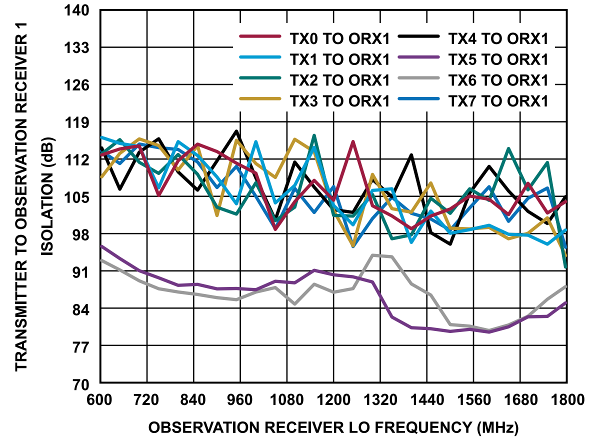

Figure 433. Transmitter to Observation Receiver 1 Isolation vs. Observation Receiver LO Frequency, Low Band Matching

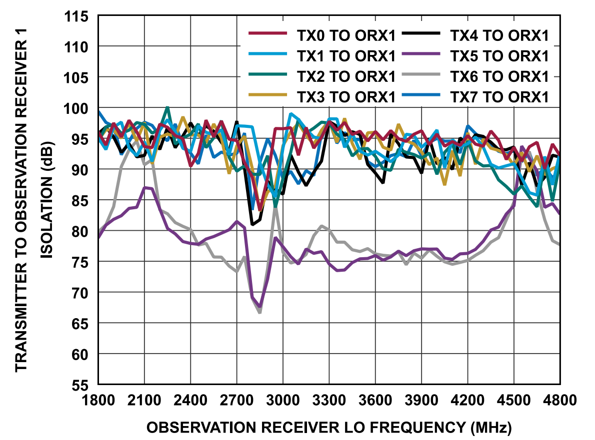

Figure 434. Transmitter to Observation Receiver 1 Isolation vs. Observation Receiver LO Frequency, Middle Band Matching

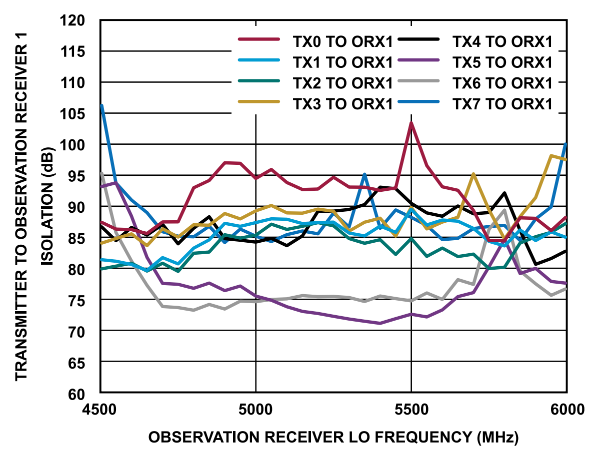

Figure 435. Transmitter to Observation Receiver 1 Isolation vs. Observation Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

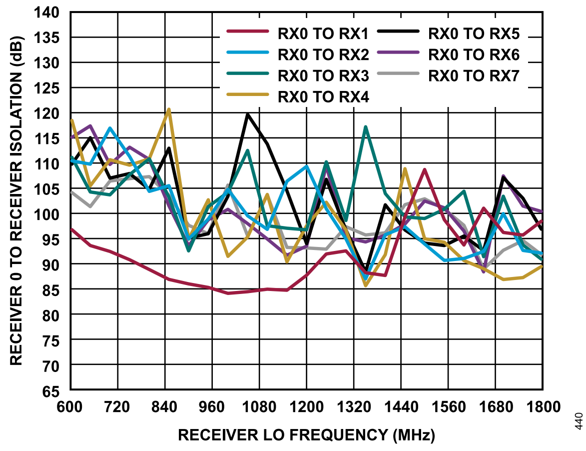

Figure 436. Receiver 0 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

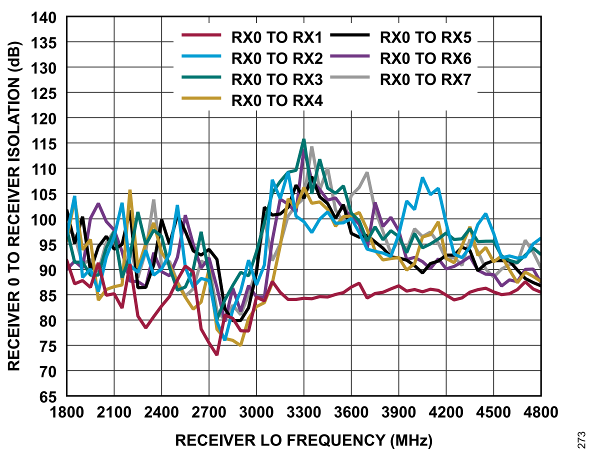

Figure 437. Receiver 0 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

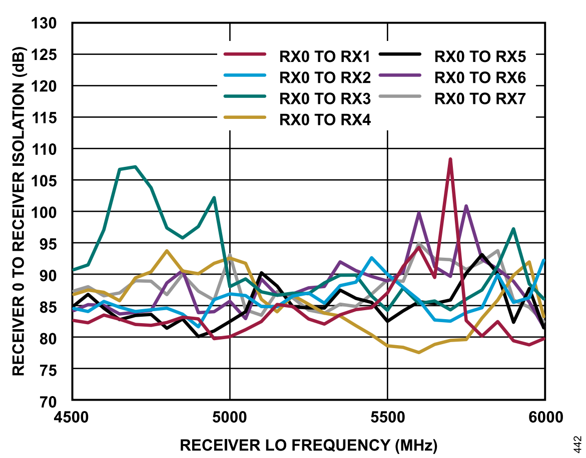

Figure 438. Receiver 0 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

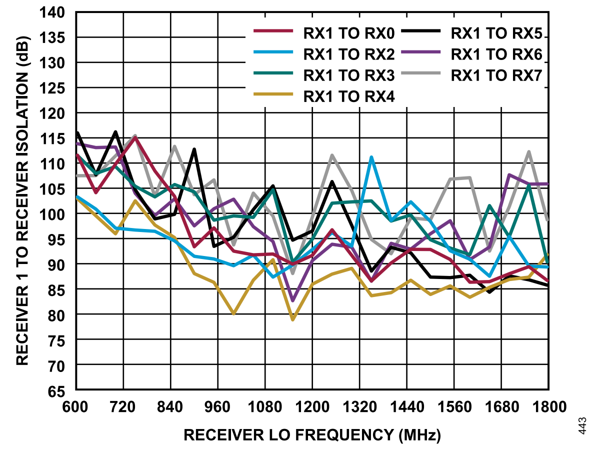

Figure 439. Receiver 1 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

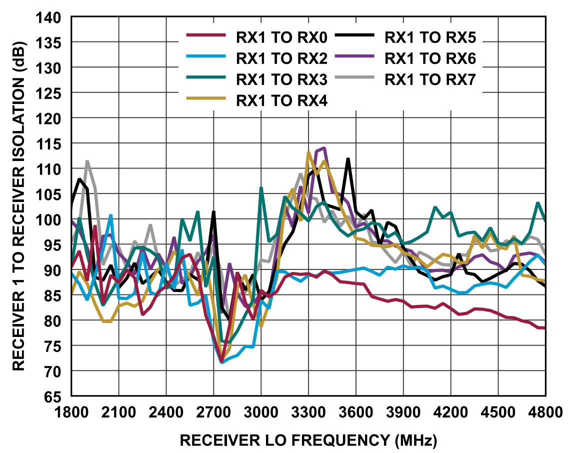

Figure 440. Receiver 1 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

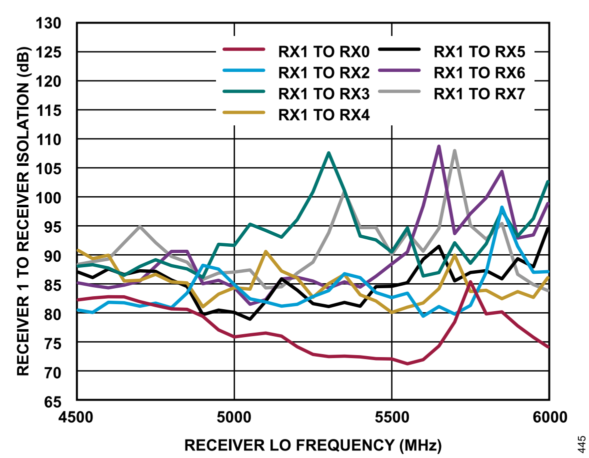

Figure 441. Receiver 1 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

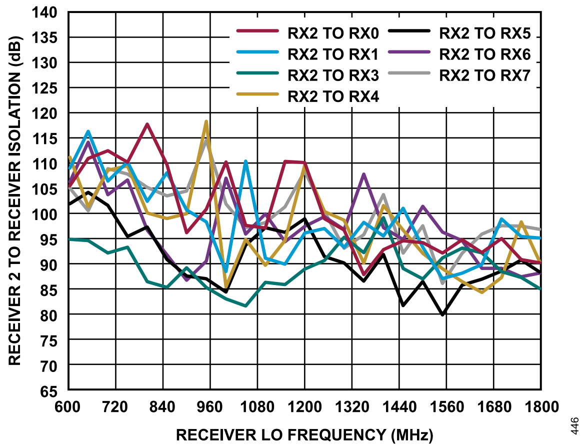

Figure 442. Receiver 2 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

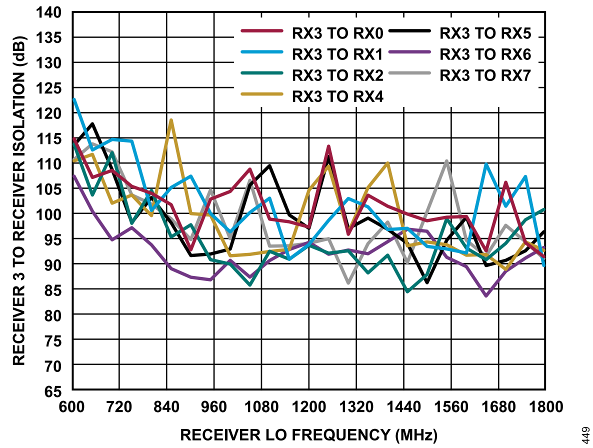

Figure 445. Receiver 3 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

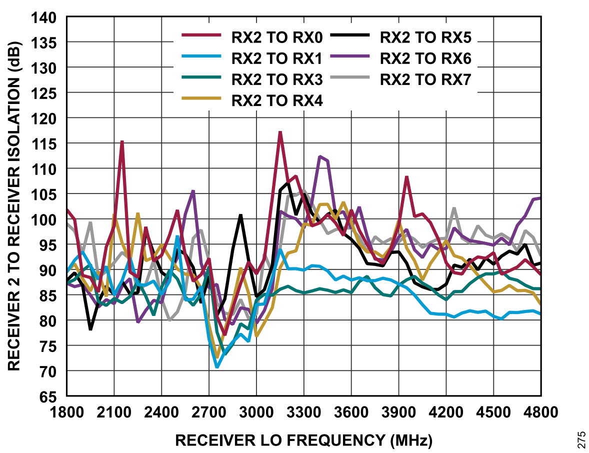

Figure 443. Receiver 2 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

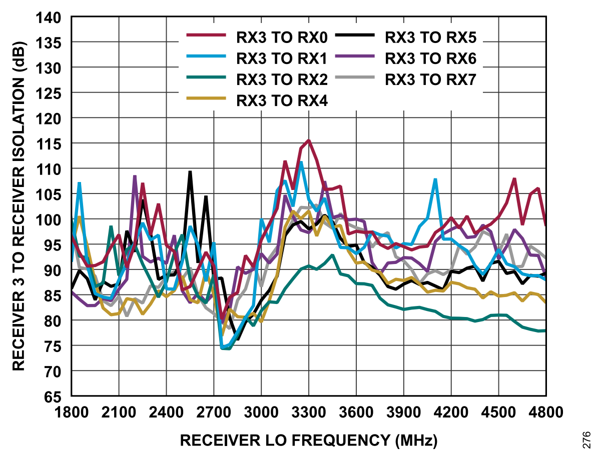

Figure 446. Receiver 3 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

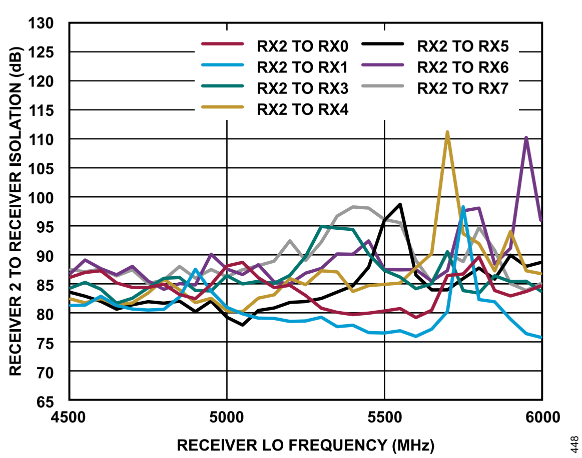

Figure 444. Receiver 2 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

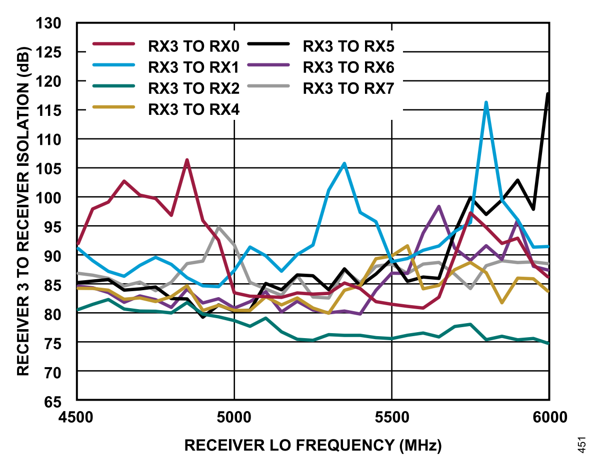

Figure 447. Receiver 3 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

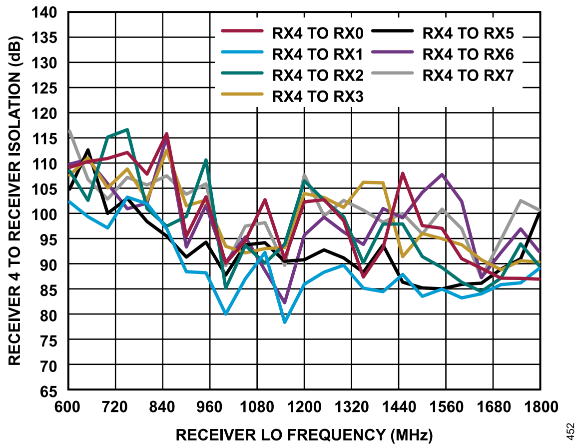

Figure 448. Receiver 4 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

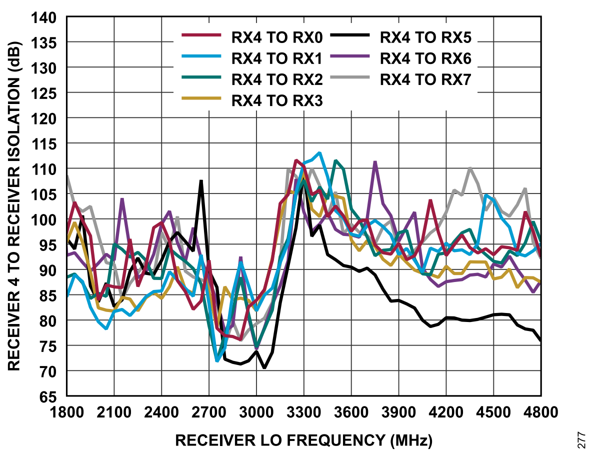

Figure 449. Receiver 4 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

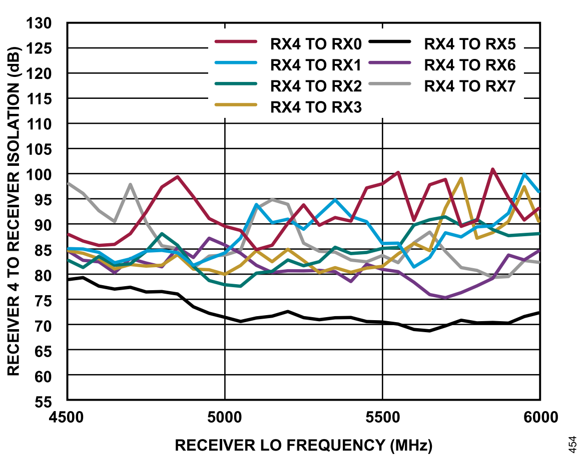

Figure 450. Receiver 4 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

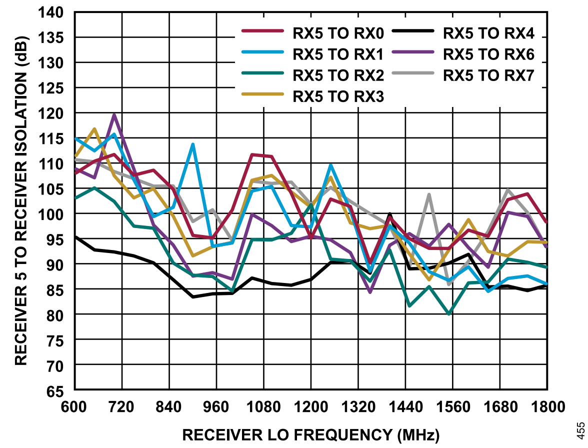

Figure 451. Receiver 5 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

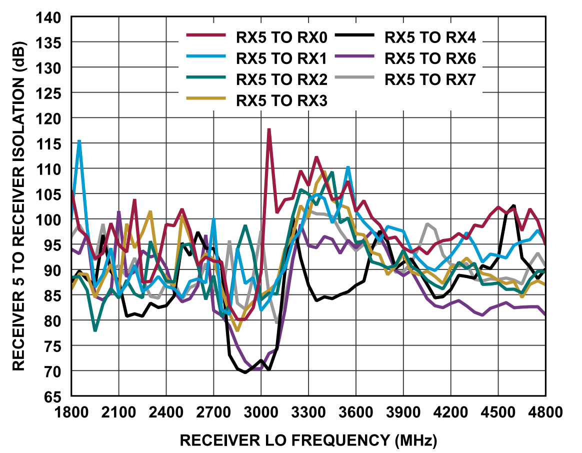

Figure 452. Receiver 5 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

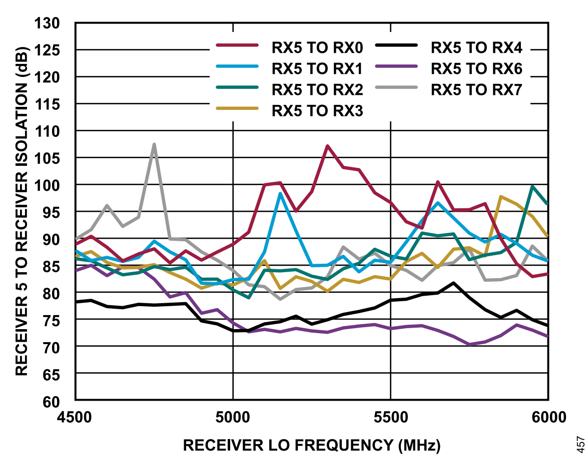

Figure 453. Receiver 5 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

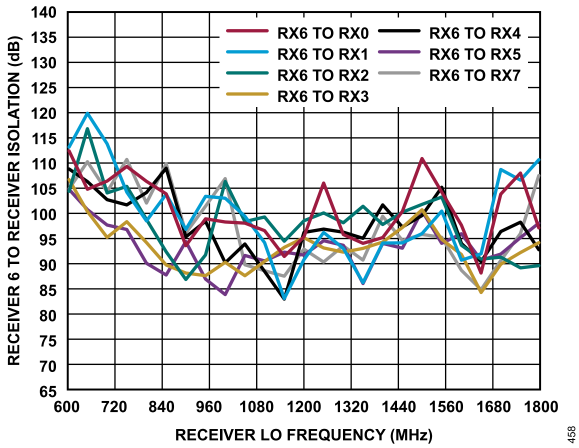

Figure 454. Receiver 6 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

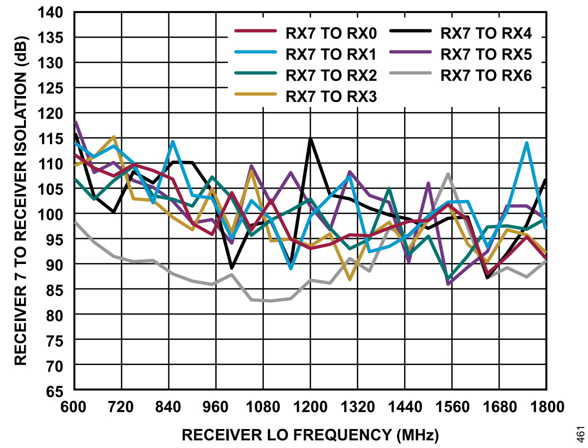

Figure 457. Receiver 7 to Receiver Isolation vs. Receiver LO Frequency, Low Band Matching

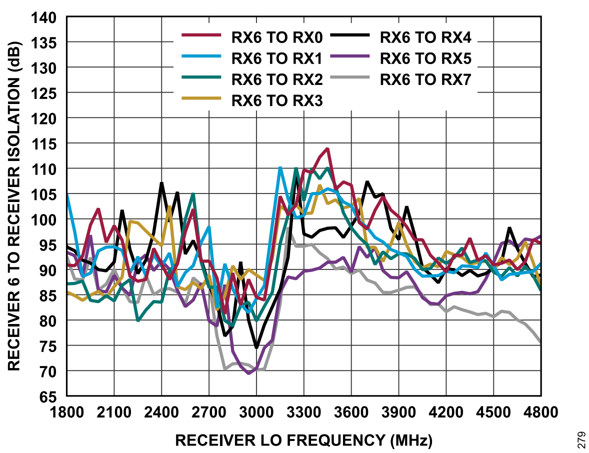

Figure 455. Receiver 6 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

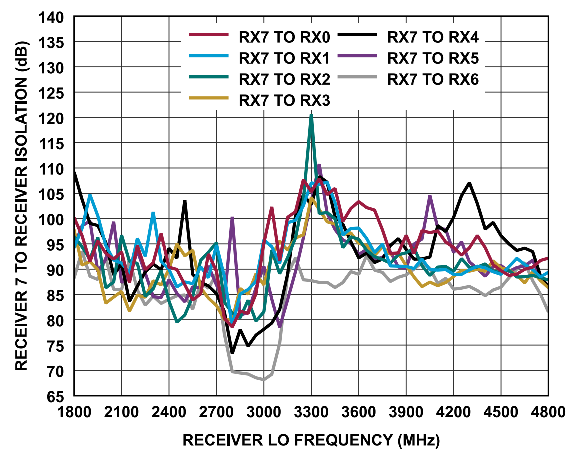

Figure 458. Receiver 7 to Receiver Isolation vs. Receiver LO Frequency, Middle Band Matching

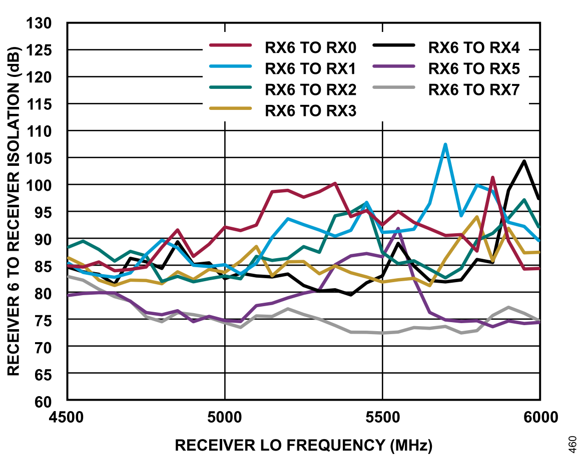

Figure 456. Receiver 6 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

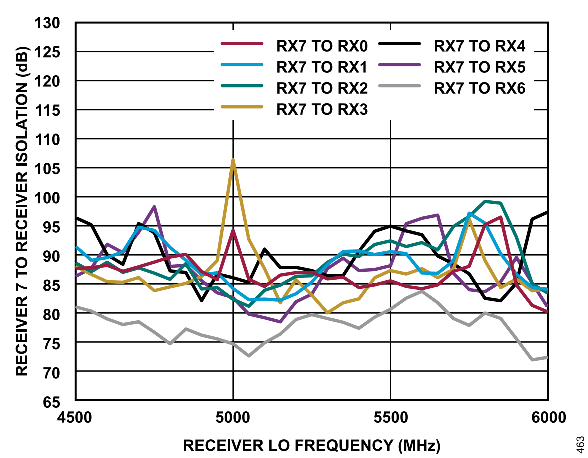

Figure 459. Receiver 7 to Receiver Isolation vs. Receiver LO Frequency, High Band Matching

TYPICAL PERFORMANCE CHARACTERISTICS

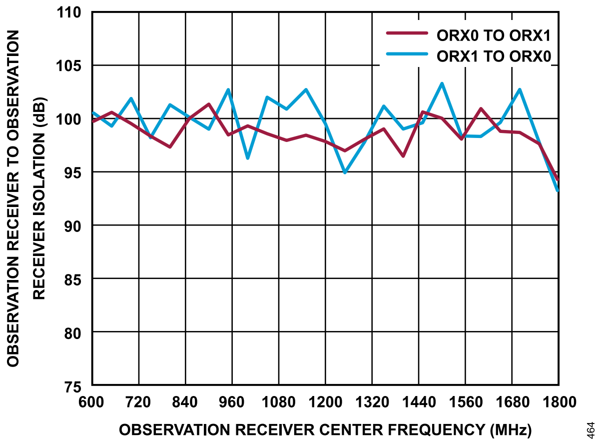

Figure 460. Observation Receiver to Observation Receiver Isolation vs. Observation Receiver Center Frequency, Low Band Matching

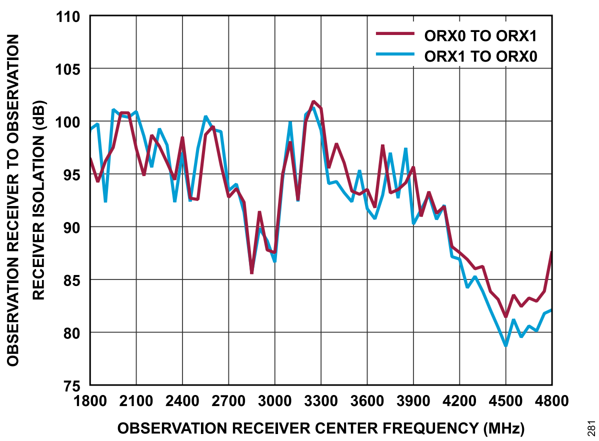

Figure 461. Observation Receiver to Observation Receiver Isolation vs. Observation Receiver Center Frequency, Middle Band Matching

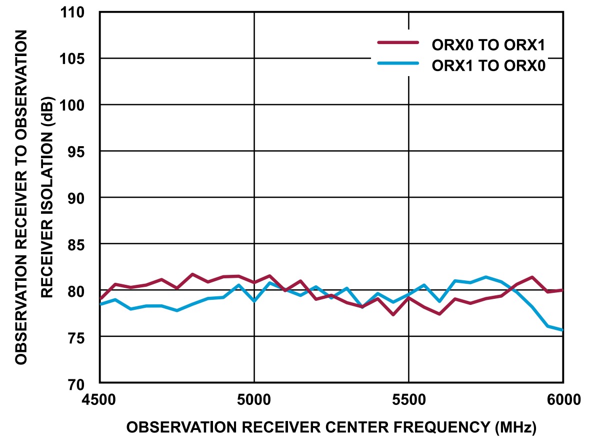

Figure 462. Observation Receiver to Observation Receiver Isolation vs. Observation Receiver Center Frequency, High Band Matching

THEORY OF OPERATION

GENERAL

The ADRV9042 is a highly integrated RF transceiver capable of configuration for a wide range of applications. The device integrates all the RF, mixed-signal, and digital blocks necessary to provide all transmitter, traffic receiver, and observation receiver functions in a single device. The programmability allows the device to be adapted for use in many 3G/4G/5G cellular standards in TDD modes.

One observation receiver channel monitors the transmitter outputs and provides tracking correction of DC offset, quadrature error, and transmitter LO leakage to maintain a high-performance level under varying temperatures and input signal conditions. The firmware supplied with the device implements all initialization and calibration with no user interaction. Additionally, the device includes test modes, which allow system designers to debug designs during prototyping and to optimize the radio configurations.

The ADRV9042 contains eight high-speeds serial interfaces (SERDES) links for the transmit chain and eight high-speeds links shared by the receiver and observation receiver chains.

TRANSMITTER

The ADRV9042 transmitter section consists of eight identical and independently controlled channels that provide all the digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the SERDES lanes pass through a digital processing block that includes a series of programmable half-band filters, interpolation stages, and FIR filters, including a programmable FIR filter with variable interpolation rates and up to 24 taps. The output of this digital chain is connected to the digital-to-analog converter (DAC). The DAC sample rate is adjustable for either 2949.12 MHz or 3932.16 MHz. The in-phase (I) and quadrature (Q) channels are identical in each transmitter signal chain.

After conversion to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the upconversion mixers. Each transmit chain provides a wide attenuation adjustment range with fine granularity to help the designers to optimize the signal-to-noise ratio (SNR).

RECEIVER

The ADRV9042 provides eight independent receiver channels. Each channel contains all the blocks necessary to receive RF signals and convert these signals to digital data usable by a baseband processor. Each channel contains a programmable attenuator stage, followed by matched I and Q mixers that downconvert received signals to baseband for digitization.

Two gain control options are available, as follows:

- Users can implement their own gain control algorithms using their baseband processor to manage manual gain control mode.
- Users can use the on-chip AGC system.

The performance is optimized by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receive signal path. Additionally, each channel contains independent receive signal power measurement capability, DC offset tracking, and all the circuitry necessary for self-calibration.

The receivers include analog-to-digital converters (ADCs) and adjustable sample rates that produce data streams from the received signals. The signals can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate. All receiver outputs are connected to the SERDES block, where the data is formatted and serialized for transmission to the baseband processor.

OBSERVATION RECEIVER

The ADRV9042 provides two independent observation receiver inputs. Unlike the receiver channels, the observation receiver channel path implements direct RF sampling. An RF ADC eliminates the need for a LO, which eliminates the spurious often seen with LO coupling. The channel also contains a programmable attenuator stage that provides 16 dB attenuation in the analog domain with roughly 1 dB step size.

REFERENCE CLOCK INPUT

The ADRV9042 requires a differential clock connected to the DEVCLKP and DEVCLKN pins. The frequency of the clock input must be between 61.44 MHz and 491.52 MHz and must have low phase noise because this signal generates the RF LO and internal sampling clocks.

SYNTHESIZERS

The ADRV9042 contains four fractional-N phase locked loops (PLLs) to generate the RF LO for the signal paths and all internal clock sources. This group of PLLs includes two RF PLLs for transmitting and receiving LO generation, a SERDES PLL, and a clock PLL. Each PLL is independently controlled, so no need for external components to set frequencies.

RF Synthesizers

The two RF synthesizers use a fractional-N PLL to generate the RF LO for multiple receiver and transmitter channels. The fractional-N PLL incorporates a four-core internal voltage-controlled oscillator (VCO) and loop filter, which are capable of generating low-phase noise signals with no external components required. The LOs on multiple devices can be phase synchronized to support active antenna systems and beamforming applications.

SERDES Synthesizers

The SERDES synthesizer uses a single core VCO fractional-N PLL to generate the required clock for the SERDES physical layer (PHY) to achieve the desired lane rate.

THEORY OF OPERATION

Clock Synthesizer

The ADRV9042 contains a single-core VCO fractional-N PLL synthesizer that generates all baseband-related clock signals and SERDES clocks. This fractional-N PLL is programmed based on the data rate and sample rate requirements of the system, which typically require the system to operate in integer mode.

External LO Inputs

The ADRV9042 provides two external LO inputs to allow an external synthesizer to be used with the device. These inputs must be 2× the desired LO frequency. One input is multiplexed with the RF1 PLL, and the other input is multiplexed with the RF2 PLL.

SPI

The ADRV9042 uses SPI to communicate with the baseband processor. This interface can be configured as a 4-wire interface with dedicated receive and transmit ports or as a 3-wire interface with a bidirectional data communications port. This bus allows the baseband processor to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first bit sets the bus direction of the bus transfer. The next 15 bits set the address where the data is written. The final eight bits are the data being transferred to the specific register address.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DIO pin, and the final eight bits are read from the ADRV9042, either on the SPI_DO pin in 4-wire mode or on the SPI_DIO pin in 3-wire mode.

GPIO_X PINS

The ADRV9042 provides 24 general-purpose input/output signals (GPIOs) referenced to VIF that can be configured for numerous functions. When configured as outputs, certain pins can provide real-time signal information to the baseband processor, which allows the baseband processor to determine the receiver performance. A pointer register selects what information is output to these pins.

The signals used for manual gain mode, calibration flags, state machine status, and various receiver parameters are among the outputs that can be monitored on the GPIO pins. Additionally, certain GPIO pins can be configured as inputs and used for various functions, such as setting the receiver gain in real time.

GPIO_ANA_X

The ADRV9042 contains 16 analog GPIOs ports that can be used to control other analog devices or receive control inputs referenced to the VDDA_1P8 supply.

JTAG BOUNDARY SCAN

The ADRV9042 provides support for a JTAG boundary scan. There are five dual function pins associated with the JTAG interface. These pins listed in Table 12 are used to access the on-chip test access port. To enable the JTAG functionality, set the GPIO_0 pin through the GPIO_2 pins according to Table 13. Pull the TEST_EN pin high to enable the JTAG mode.

Table 12. Dual Function Boundary Scan Test Pins

Mnemonic	JTAG Mnemonic	Description
GPIO_3	A	Test access port reset
GPIO_4	TDO	Test data output
GPIO_5	TDI	Test data input
GPIO_6	TMS	Test access port mode select
GPIO_7	TCK	Test clock

Table 13. JTAG Modes

TEST_EN Pin Level	GPIO[2:0]	Description
0	XXX[1]	No boundary scan
1	000	Boundary scan LVDS mode
1	011	Boundary scan CMOS mode

[1] X means any combination.

DTX

The ADRV9042 supports the DTx mode and discontinuous transmission (DTx) is a power saving feature. It works by monitoring the input data for continuous zeros in the data and ramps down the Tx path where a predefined number of zeros are detected. The DTx mode in ADRV9042 uses the TX slice processor to gate off the clocks from the TX data path and ramps down the TX VGA block to save power, while TX tracking calibrations such as TX QEC and TX LOL are paused. There are three modes supported by this DTX function on the ADRV9042, which are automatic mode, SPI-controlled mode, and PIN-controlled mode.

DIGITAL PREDISTORTION (DPD)

The ADRV9042 provides a fully integrated DPD system that linearizes the output of the transmitter power amplifier by altering the digital waveform to compensate for nonlinearities in the power amplifier response. Both the DPD actuator and coefficient calculation are integrated within the device. This system uses an observation receiver channel to monitor the output of the power amplifier and calculates the appropriate predistortion that must be inserted into the transmitter datapath to linearize the output. The integrated DPD capability allows the system to drive the power amplifier closer to saturation, which enables a higher efficiency power amplifier while maintaining linearity. The DPD can linearize a wide range of power amplifiers with output power ranging from 25 mW to 80 W. The DPD engine is highly configurable and can operate over a range of clock rates, which allows the DPD system to scale, so this system can support different carrier configurations within the transmitter bandwidth.

THEORY OF OPERATION

CREST FACTOR REDUCTION (CFR)

The ADRV9042 includes a low-power CFR feature that enables power amplifiers to operate more efficiently. When non-constant envelope modulation schemes are used, the signal can have a high PAR. The CFR algorithm reduces the PAR, which enables the power amplifier to operate more efficiently while minimizing the impact to signal quality parameters such as EVM and out of band emission levels. The system designers can configure the CFR algorithm to ensure that these performance parameters are within the system specification limits.

CARRIER DIGITAL UP CONVERSION (CDUC) AND CARRIER DIGITAL DOWN CONVERSION (CDDC)

The ADRV9042 incorporates CDUC and CDDC, which are used to filter and place individual component carriers within the band of interest. The CDDC feature with its eight parallel paths, processes each carrier individually before sending over the serial data interface.

APPLICATIONS INFORMATION

POWER SUPPLY SEQUENCE

The ADRV9042 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal sequence, the VDIG_0P8 supply must come up first. After the VDIG_0P8 source is enabled, the VANA_1P0 supplies must be enabled next, followed by the VANA_1P8 supplies. Note that the VIF_1P8 supply can be enabled at any time without affecting the other circuits in the device. In addition to this sequence, it is also recommended to toggle the RESETB signal after power has stabilized before initializing the device.

The power-down sequence recommendation is similar to power-up. All supplies must be disabled in reverse order (or all together) before VDIG_0P8 is disabled. If such a sequence is not possible, then all supplies must have their sources disabled simultaneously to ensure no back feeding to circuits that have been powered down.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
BP-736-2	BGA_ED	736-Ball Ball Grid Array, Thermally Enhanced

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRV9042BBPZ-8T1	−40°C to +110°C	736-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	Tray, 48	BP-736-2
ADRV9042BBPZRL-8T1	−40°C to +110°C	736-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	Reel, 300	BP-736-2

[1] Z = RoHS Compliant Part.

Updated: August 13, 2025

EVALUATION BOARDS

Model[1]	Description
ADRV904X-LB/PCBZ	Evaluation Board for Low Band (600 MHz to 2800 MHz) Operation
ADRV904X-MB/PCBZ	Evaluation Board for Middle Band (1800 MHz to 4800 MHz) Operation
ADRV904X-HB/PCBZ	Evaluation Board for High Band (4500 MHz to 6000 MHz) Operation
ADRV904X-UB/PCBZ	Evaluation Board for Ultra High Band (6000 MHz to 7500 MHz) Operation

[1] Z = RoHS Compliant Part.

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