Data Sheet

ADRF5703

Silicon Digital Attenuator, 0.25dB LSB, 7-Bit, 9kHz to 20GHz

FEATURES

- Frequency range: 9kHz to 20GHz
- Attenuation range: 31.75dB with 0.25dB step size
- Low insertion loss
  - 1dB typical up to 6GHz
  - 1.3dB typical up to 12GHz
  - 1.7dB typical up to 20GHz
- Attenuation accuracy: −(4% of the attenuation state) or +(0.1) typical up to 20GHz
- Step error: 0.20dB typical up to 20GHz
- High linearity
  - Input P0.1dB
    - Attenuation state < 16dB: 33dBm typical at ATTIN
    - Attenuation state ≥ 16dB: 31dBm typical at ATTIN
  - Input IP3: 55dBm typical at ATTIN
- High RF power handling
  - 27dBm average at ATTIN
  - 30dBm peak at ATTIN
  - 27dBm hot switching at ATTIN
- RF amplitude settling time (50% triggered control to 0.05dB of final RF output): 1µs typical
- Consistent return loss at all attenuation states
- Single-supply operation with derated power handling
- No low frequency spurs and no internal voltage generation
- Serial and parallel mode control, CMOS- and LVTTL-compatible
- 24-terminal, 4.0mm × 4.0mm, land grid array (LGA) package

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G millimeter wave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

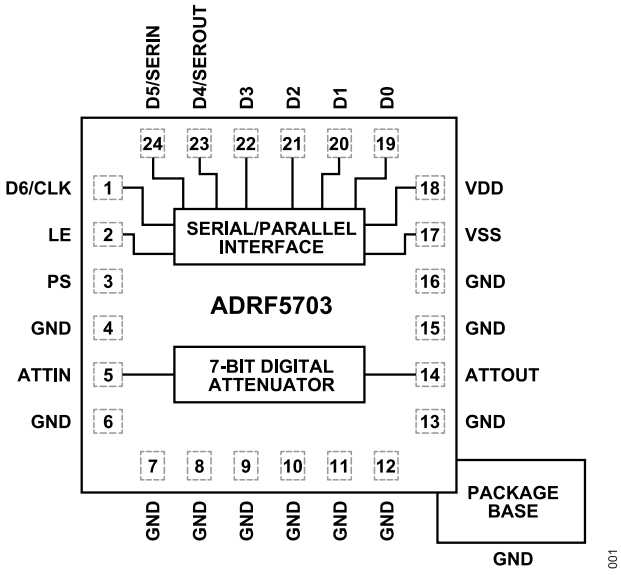

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5703 is a 7-bit digital attenuator with a 31.75dB attenuation range and 0.25dB step size manufactured in a silicon on insulator (SOI) process.

This device operates from 9kHz to 20GHz with an insertion loss better than 1.7dB and excellent attenuation accuracy. The ADRF5703 has RF input power handling capabilities of 27dBm average and 30dBm peak for all states from the ATTIN pin.

The ADRF5703 operates with a dual-supply voltage +3.3V and −3.3V. The device can also operate with a single-supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated, see Table 2.

The device features serial or parallel mode control and complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5703 comes in a 24-terminal, 4.0mm × 4.0mm, land grid array (LGA) package and can operate from −40°C to +105°C.

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REVISION HISTORY

9/2025—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3V, V_{SS} = −3.3V, control voltages (V_{CTRL}) = 0V or 3.3V, T_{CASE} = 25°C, and 50Ω system, unless otherwise noted. V_{CTRL} is the voltages of the digital control input pins.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		20000	MHz
INSERTION LOSS						
		9kHz to 6GHz		1		dB
		6GHz to 12GHz		1.3		dB
		12 GHz to 20GHz		1.7		dB
RETURN LOSS		ATTIN and ATTOUT, all attenuation states				
		9kHz to 6GHz		22		dB
		6GHz to 12GHz		21		dB
		12 GHz to 20GHz		21		dB
ATTENUATION						
Range		Between minimum and maximum attenuation states		31.75		dB
Step Size		Between any successive attenuation states		0.25		dB
Accuracy		Referenced to insertion loss				
		9kHz to 20GHz		−(4% of the attenuation state) or +(0.1)		dB
Step Error		Between any successive state				
		9kHz to 6GHz		0.04		dB
		6GHz to 12GHz		0.05		dB
		12 GHz to 20GHz		0.20		dB
RELATIVE PHASE		Maximum attenuation state referenced to insertion loss				
		6GHz		13		Degrees
		12GHz		27		Degrees
		20GHz		48		Degrees
SWITCHING CHARACTERISTICS		All attenuation states at input power (P_{IN}) = 10dBm, f = 1GHz				
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		0.4		µs
On Time and Off Time	t_{ON}, t_{OFF}	50% triggered control to 90% of RF output		0.6		µs
RF Amplitude Settling Time						
0.1dB		50% triggered control to 0.1dB of final RF output		0.9		µs
0.05dB		50% triggered control to 0.05dB of final RF output		1		µs
Overshoot		Worst-case transition		3.7		dB
Undershoot		Worst-case transition		2.4		dB
RF Phase Settling Time		f = 20GHz				
5°		50% triggered control to 5° of final RF output		0.5		µs
1°		50% triggered control to 1° of final RF output		0.6		µs
INPUT LINEARITY[1]		3MHz to 18GHz				
0.1dB Power Compression	P0.1dB					
Input at ATTIN		Attenuation state < 16dB		33		dBm
		Attenuation state ≥ 16dB		31		dBm
Input at ATTOUT		Attenuation state < 16dB		30		dBm
		Attenuation state ≥ 16dB		27		dBm

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Third-Order Intercept	IP3	Two-tone P_{IN} = 22dBm per tone, Δf = 1MHz, all attenuation states				dBm
Input at ATTIN				55		dBm
Input at ATTOUT				55		dBm
Second-Order Intercept	IP2	Two-tone P_{IN} = 22dBm per tone, Δf = 1MHz, all attenuation states		110		dBm
VIDEO FEEDTHROUGH[2]				2		mV p-p
DIGITAL CONTROL INPUTS		LE, PS, and D0 to D6				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}					
D0, D1, D2, and D3				30		µA
LE, PS, D4, D5, and D6				<1		µA
SUPPLY CURRENT						
Positive Supply Current	I_{DD}	V_{DD} = 3.3V		0.7		mA
Negative Supply Current	I_{SS}	V_{SS} = −3.3V		0.6		mA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Power Handling [3]		f = 3MHz to 18GHz, T_{CASE} = 85°C,[4] all attenuation states				
Input at ATTIN						
Average					27	dBm
Peak[5]					30	dBm
Hot Switching					27	dBm
Input at ATTOUT						
Average					24	dBm
Peak					27	dBm
Hot Switching					24	dBm
T_{CASE}			−40		+105	°C

1 For input linearity performance over frequency, see Figure 30 and Figure 31.

2 Video feedthrough is the peak transient measured at the RF ports in a 50Ω test setup without an RF signal present while switching the control voltage.

3 For RF power handling derating over the extended frequency range, see Figure 2.

4 For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specifications by 3dB.

5 Peak: ≤100ns pulse duration and 5% duty cycle.

SPECIFICATIONS

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3V, V_{SS} = 0V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and 50Ω system, unless otherwise noted. V_{CTRL} is the voltages of the digital control input pins.

The small signal and bias specifications are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		20000	MHz
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		1.7		µs
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		1.7		µs
0.1dB Settling Time		50% V_{CTRL} to 0.1dB of final RF_{OUT}		2		µs
0.05dB Settling Time		50% V_{CTRL} to 0.05dB of final RF_{OUT}		2.1		µs
INPUT LINEARITY		3MHz to 18GHz				
0.1dB Power Compression	P0.1dB			20		dBm
Third-Order Intercept	IP3	Two-tone P_{IN} = 22dBm per tone, Δf = 1 MHz		43		dBm
SUPPLY CURRENT						
Positive Supply Current	I_{DD}			0.55		mA
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling		f = 3MHz to 18GHz, T_{CASE} = 85°C				
Input at ATTIN						
Average					20	dBm
Peak					20	dBm
How Switching					20	dBm
Input at ATTOUT						
Average					20	dBm
Peak					20	dBm
Hot Switching					20	dBm
Case Temperature	T_{CASE}		−40		+105	°C

TIMING SPECIFICATIONS

See Figure 35, Figure 36, and Figure 37 for the timing diagrams.

Table 3. Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Serial period, see the Serial Mode Interface section	20			ns
t_{CS}	Control setup time, see the Serial Mode Interface section	3			ns
t_{CH}	Control hold time, see the Serial Mode Interface section	3			ns
t_{LN}	LE setup time, see the Serial Mode Interface section	3			ns
t_{LEW}	LE pulse width, see the Serial Mode Interface section and the Latched Parallel Mode section	5			ns
t_{LES}	LE pulse spacing, see the Serial Mode Interface section	150			ns
t_{CKN}	Serial clock hold time from LE, see the Serial Mode Interface section	3			ns
t_{PH}	Hold time, see the Latched Parallel Mode section	3			ns
t_{PS}	Setup time, the Latched Parallel Mode section	5			ns
t_{CO}	Clock to output (SEROUT) time, see the Serial Mode Interface section			20	ns

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3V to +3.6V
Negative Supply Voltage	−3.6V to +0.3V
Digital Control Inputs	
Voltage	−0.3V to V_{DD} +0.3V
Current	3mA
RF Power[1] (f = 3MHz to 20GHz, T_{CASE} = 85°C[2])	
Dual Supply (V_{DD} = 3.3V, V_{SS} = −3.3V)	
Input at ATTIN	
Average	27.5dBm
Peak	30.5dBm
Hot Switching	27.5dBm
Input at ATTOUT	
Average	24.5dBm
Peak	27.5dBm
Hot Switching	24.5dBm
Single Supply (V_{DD} = 3.3V, V_{SS} = 0V)	
Input at ATTIN	
Average	20.5dBm
Peak	20.5dBm
Hot Switching	20.5dBm
Input at ATTOUT	
Average	20.5dBm
Peak	20.5dBm
Hot Switching	20.5dBm
Unbiased (V_{DD} and V_{SS} = 0V, Input at ATTIN and ATTOUT)	27dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to 150°C
Reflow	260°C

[1] For RF power handling derating over the extended frequency range, see Figure 2.

[2] For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specifications by 3dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to carrier bottom) thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-24-20	100	°C/W

POWER DERATING CURVE

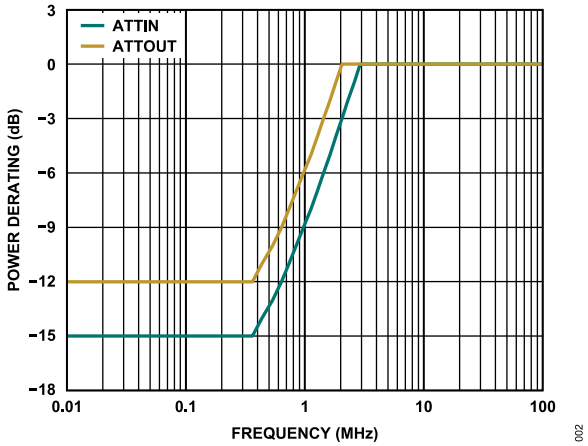

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5703

Table 6. ADRF5703, 24-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
ATTIN Pin and ATTOUT Pin	1500	1C
Supply and Control Pins	3000	2
CDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

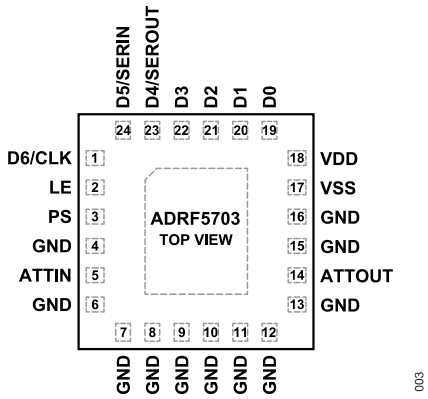

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D6/CLK	Parallel Control Input for 16dB Attenuator Bit. Serial Clock Input (CLK). See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
2	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
3	PS	Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information. See Figure 7 for the interface schematic.
4, 6 to 13, 15, 16	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
5	ATTIN	Attenuator Input. No DC blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
14	ATTOUT	Attenuator Output. No DC blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
17	VSS	Negative Supply Input. See Figure 9 for the interface schematic.
18	VDD	Positive Supply Input. See Figure 8 for the interface schematic.
19	D0	Parallel Control Input for 0.25dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
20	D1	Parallel Control Input for 0.5dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
21	D2	Parallel Control Input for 1.0dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
22	D3	Parallel Control Input for 2dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
23	D4/SEROUT	Parallel Control Input for 4dB Attenuator Bit. Serial Data Output (SEROUT). See the Theory of Operation section for more information. See Figure 6 for the interface schematic.
24	D5/SERIN	Parallel Control Input for 8dB Attenuator Bit. Serial Data Input (SERIN). See the Theory of Operation section for more information. See Figure 7 for the interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

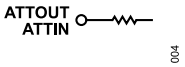

Figure 4. ATTIN and ATTOUT Interface Schematic

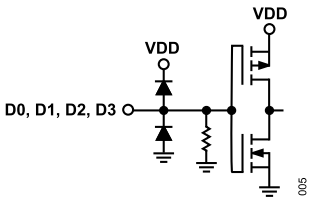

Figure 5. Digital Input Interface Schematic (D0, D1, D2, and D3)

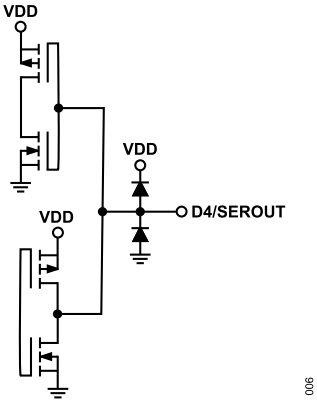

Figure 6. Digital Input Interface Schematic (D4/SEROUT)

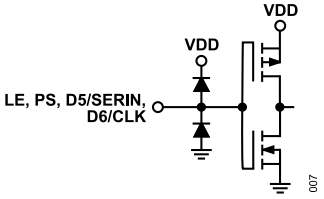

Figure 7. Digital Input Interface Schematic (LE, PS, D5/SERIN, D6/CLK)

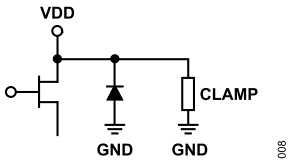

Figure 8. VDD Input Interface Schematic

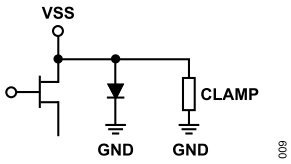

Figure 9. VSS Input Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

V_{DD} = +3.3V, V_{SS}= −3.3V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted.

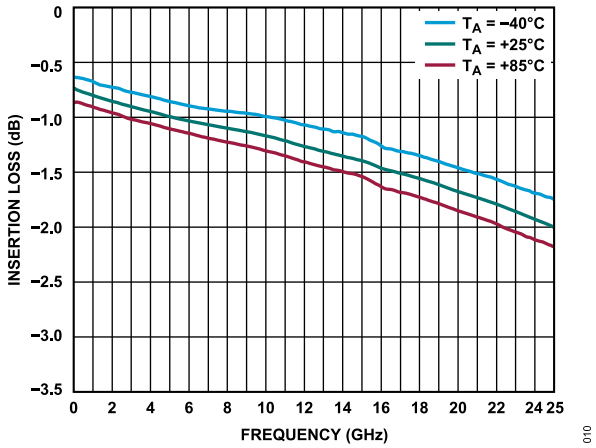

Figure 10. Insertion Loss vs. Frequency over Temperature

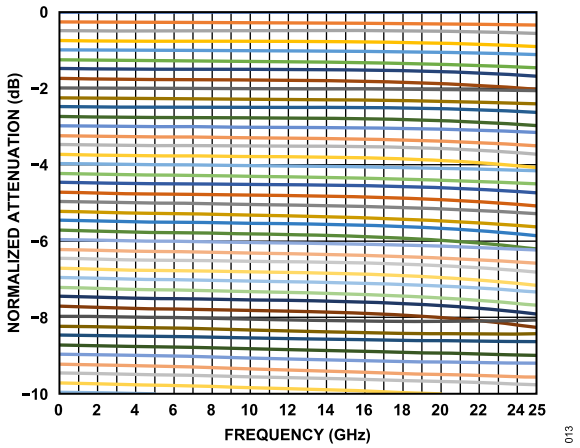

Figure 13. Normalized Attenuation vs. Frequency for Attenuation States up to −10dB

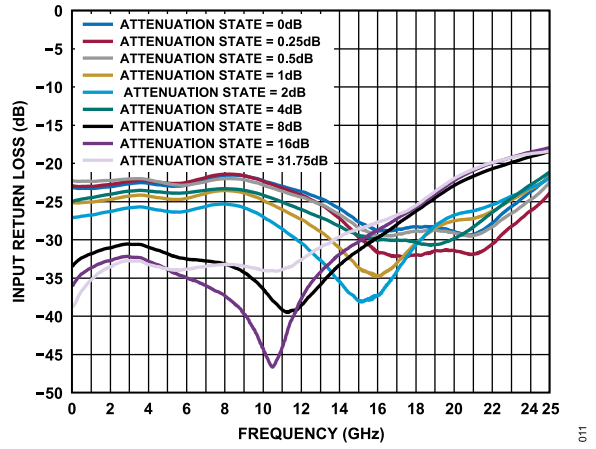

Figure 11. Input Return Loss vs. Frequency for Major Attenuation States

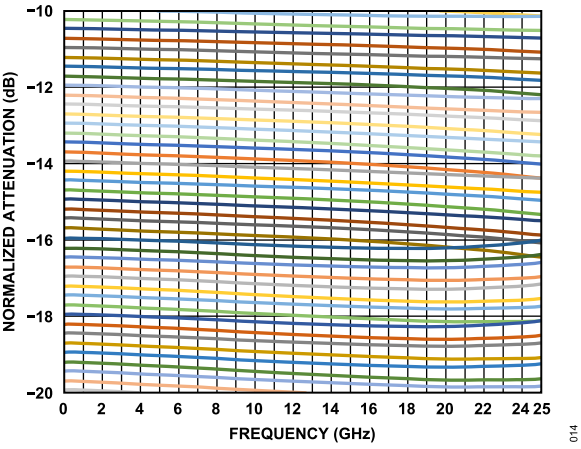

Figure 14. Normalized Attenuation vs. Frequency for Attenuation States from −10dB to −20dB

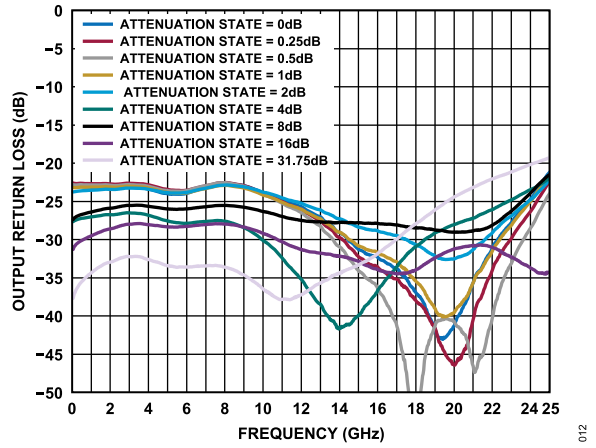

Figure 12. Output Return Loss vs. Frequency for Major Attenuation States

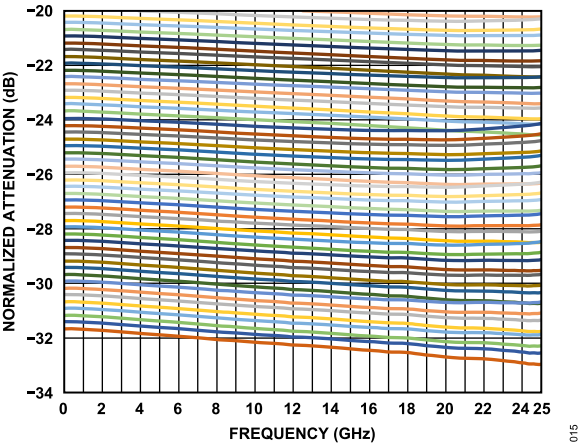

Figure 15. Normalized Attenuation vs. Frequency for Attenuation States from −20dB to −32dB

TYPICAL PERFORMANCE CHARACTERISTICS

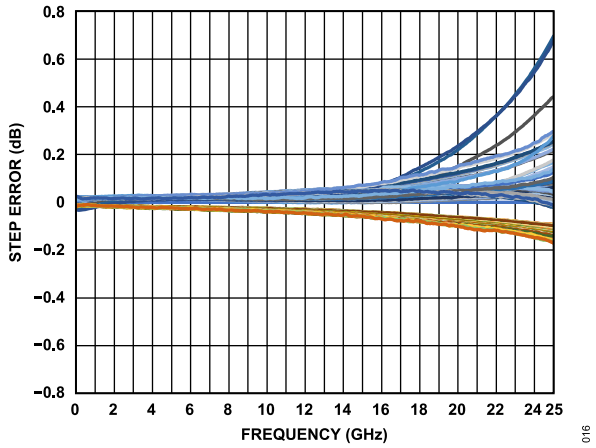

Figure 16. Step Error vs. Frequency at 25°C for 128 Attenuation States

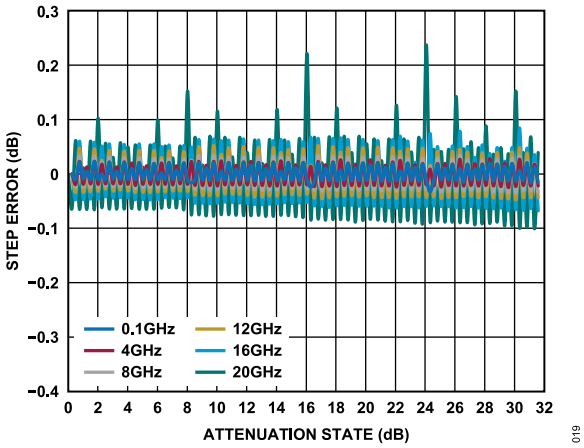

Figure 19. Step Error vs. Attenuation State at 25°C for Various Frequencies

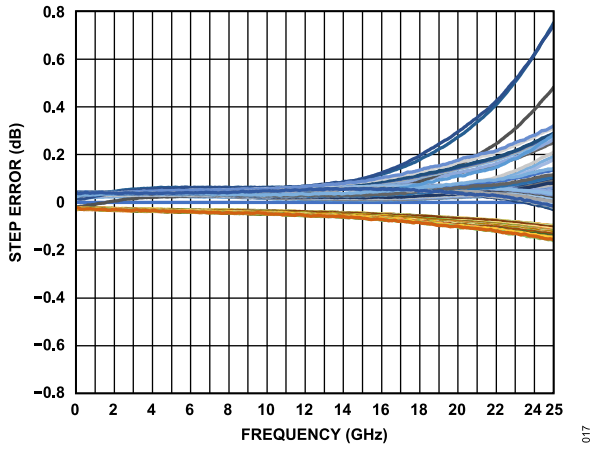

Figure 17. Step Error vs. Frequency at 85°C for 128 Attenuation States

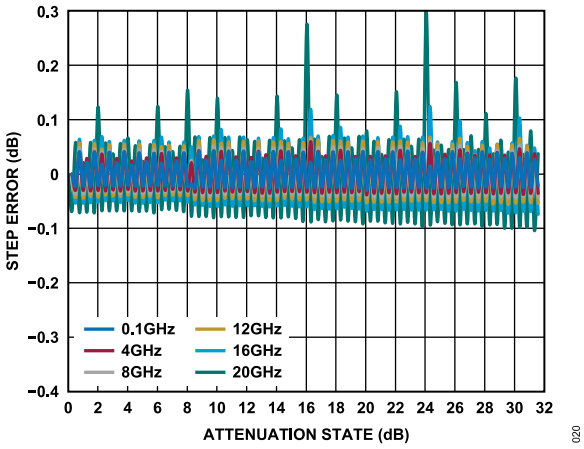

Figure 20. Step Error vs. Attenuation State at 85°C for Various Frequencies

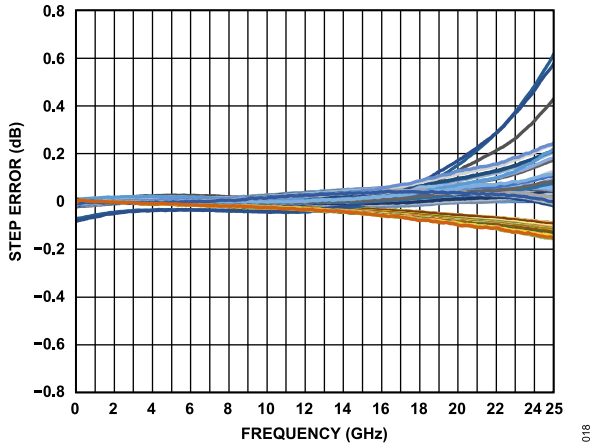

Figure 18. Step Error vs. Frequency at −40°C for 128 Attenuation States

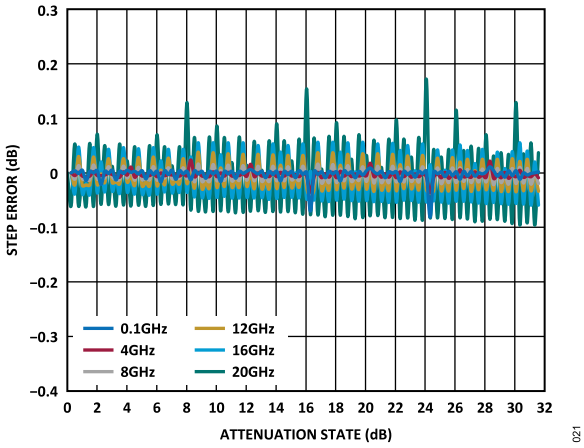

Figure 21. Step Error vs. Attenuation State at −40°C for Various Frequencies

TYPICAL PERFORMANCE CHARACTERISTICS

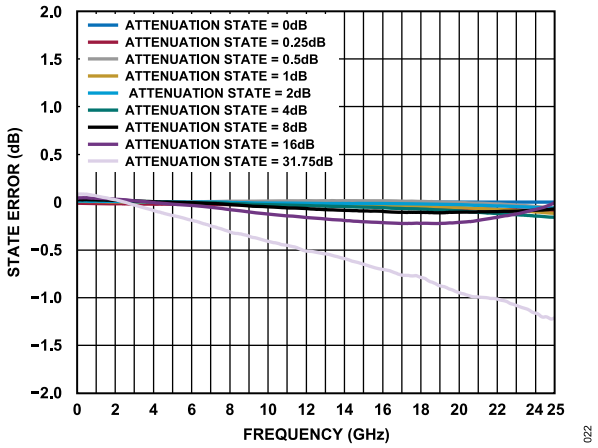

Figure 22. State Error vs. Frequency at 25°C for Major Attenuation States

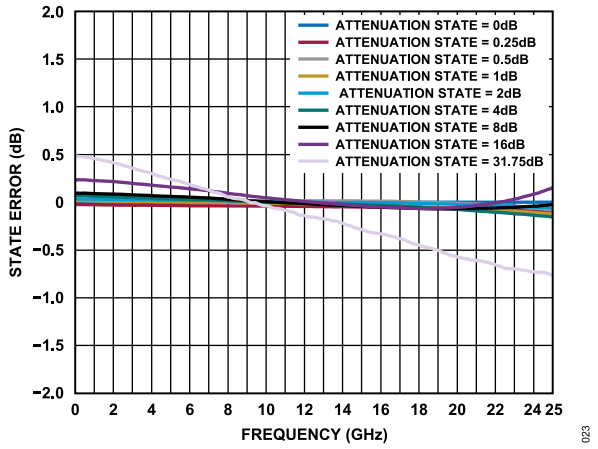

Figure 23. State Error vs. Frequency at 85°C for Major Attenuation States

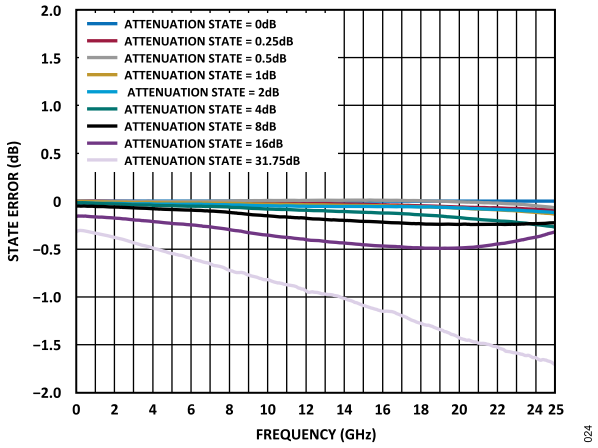

Figure 24. State Error vs. Frequency at −40°C for Major Attenuation States

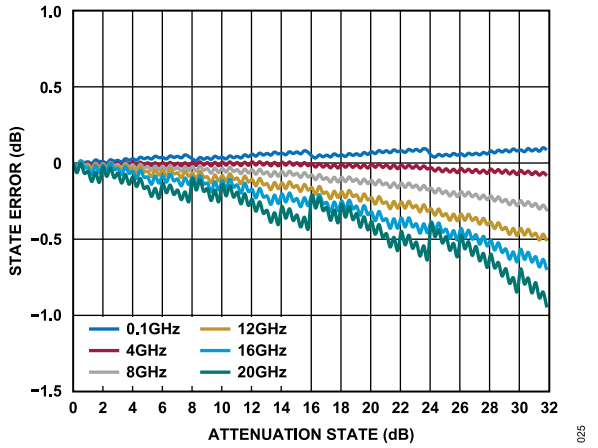

Figure 25. State Error vs. Attenuation State at 25°C for Various Frequencies

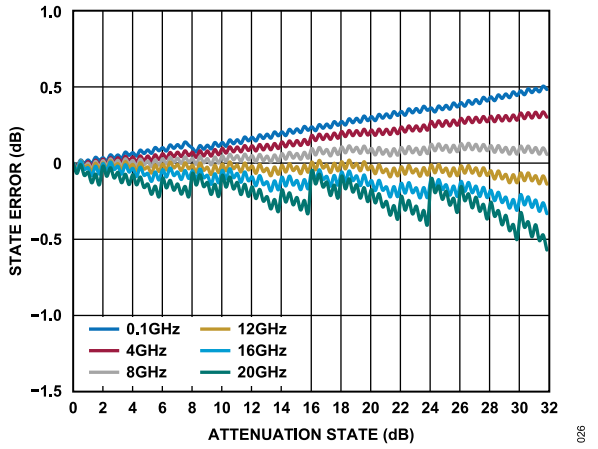

Figure 26. State Error vs. Attenuation State at 85°C for Various Frequencies

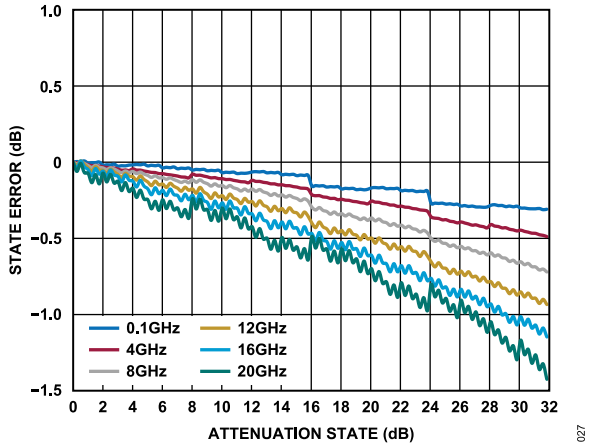

Figure 27. State Error vs. Attenuation State at −40°C for Various Frequencies

TYPICAL PERFORMANCE CHARACTERISTICS

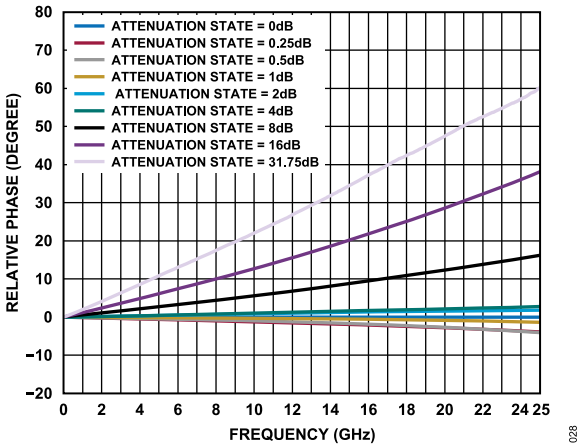

Figure 28. Relative Phase vs. Frequency for Major Attenuation States

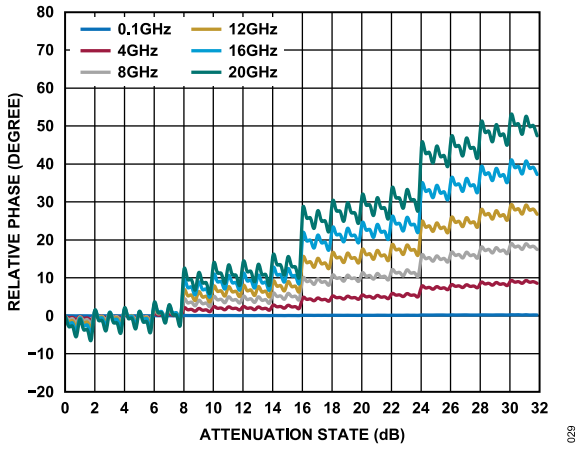

Figure 29. Relative Phase vs. Attenuation State for Various Frequencies

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = +3.3V, V_{SS}= −3.3V, V_{CTRL} = 0V or 3.3V, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted.

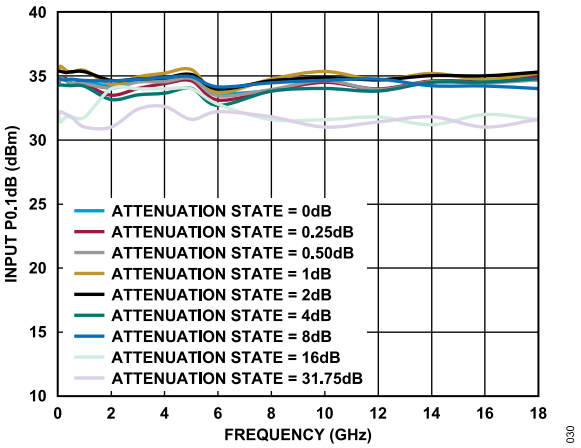

Figure 30. Input P0.1dB vs. Frequency for Major Attenuation States

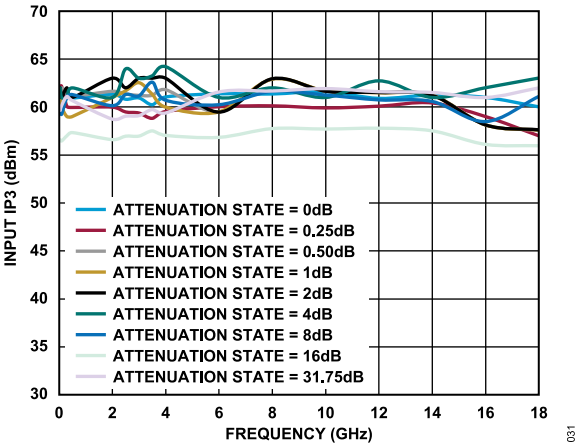

Figure 31. Input IP3 vs. Frequency for Major Attenuation States

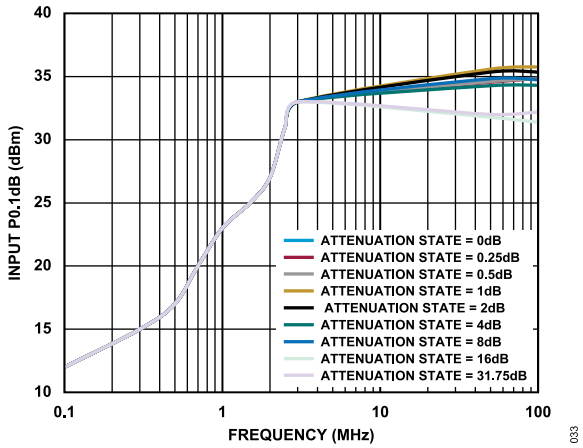

Figure 32. Input P0.1dB vs. Frequency for Major Attenuation States, Low Frequency Detail

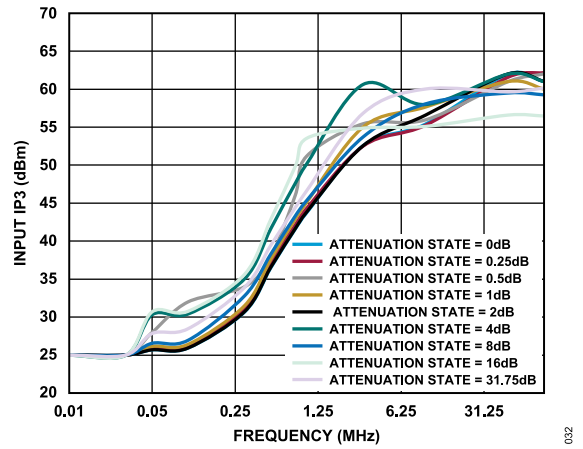

Figure 33. Input IP3 vs. Frequency for Major Attenuation States, Low Frequency Detail

THEORY OF OPERATION

The ADRF5703 incorporates a 7-bit fixed attenuator array that offers an attenuation range of 31.75dB in 0.25dB steps. An integrated driver provides serial or parallel mode control of the attenuator array.

The ADRF5703 has nine digital control inputs, D0 (LSB) to D6 (MSB), LE, and PS. To select the desired attenuation state in serial or parallel mode, refer to Table 8 and Table 9. For the timing diagrams, see Figure 35, Figure 36, and Figure 37.

POWER SUPPLY

The ADRF5703 requires a positive supply voltage applied to the VDD pin and a negative supply applied to the VSS pin. Bypassing capacitors are recommended on the supply line to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1kΩ resistor to limit the current flowing into the digital control input pins in such cases.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5703 has internal power-on reset circuitry that sets the attenuator to the maximum attenuation state (31.75dB) when VDD is applied.

SINGLE-SUPPLY OPERATION

The ADRF5703 can operate with a single positive supply voltage applied to the VDD pin and the VSS pin connected to ground. In single-supply operation, the switching characteristics, linearity, and power handling performance are derated, see Table 2 for additional information.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0V. No DC blocking is required at the RF ports when the RF line potential is equal to 0V.

The power handling is defined by the ATTIN port. Refer to the RF input power specifications in Table 1.

Table 8. Truth Table

Digital Control Input[1]							
D6	D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	Low	High	0.25
Low	Low	Low	Low	Low	High	Low	0.5
Low	Low	Low	Low	High	Low	Low	1.0
Low	Low	Low	High	Low	Low	Low	2.0
Low	Low	High	Low	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	High	31.75

[1] Any combination of the attenuation states within this table provides an attenuation equal to the sum of bits selected.

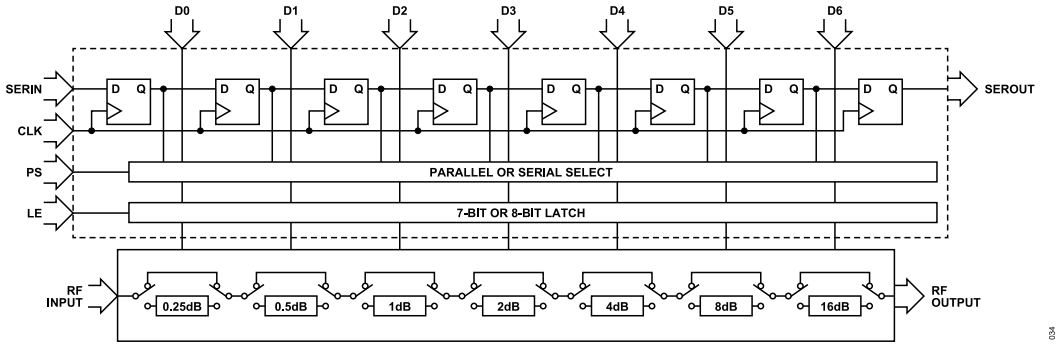

Figure 34. Simplified Circuit Diagram

THEORY OF OPERATION

SERIAL OR PARALLEL MODE SELECTION

The ADRF5703 can be controlled in either serial or parallel mode by setting the PS pin to high or low, respectively (see Table 9).

Table 9. Mode Selection

PS	Control Mode
Low	Parallel
High	Serial

SERIAL MODE INTERFACE

The ADRF5703 supports a 4-wire SPI: serial data input (SERIN), clock (CLK), serial data output (SEROUT), and latch enable (LE). The serial control interface is activated when PS pin is set to high.

The ADRF5703 attenuation states can be controlled using the 7-bit or 8-bit SERIN data. If an 8-bit word is used to control the state of the attenuator, the first two bits are don't care bit. It does not matter if these bits are held low or high, or if they are omitted altogether. Only Bits[D6:D0] set the state of the attenuator.

In serial mode, the SERIN data is clocked MSB first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new SERIN data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 35, Figure 36, the Timing Specifications section, and the RF Input and Output section for additional information.

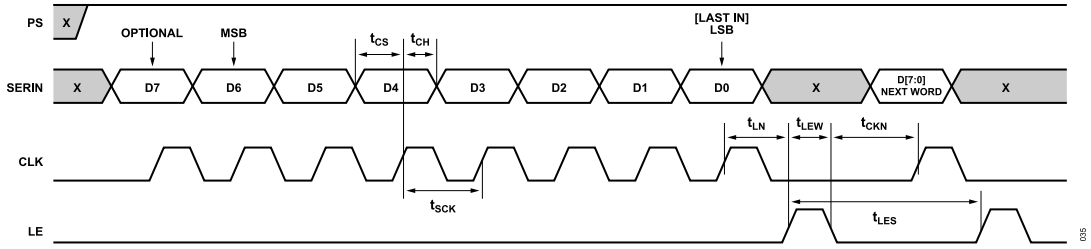

Figure 35. Serial Control Timing Diagram

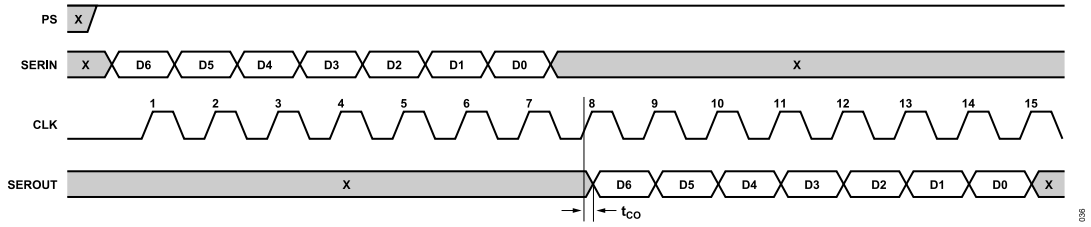

Figure 36. Serial Output Timing Diagram

THEORY OF OPERATION

PARALLEL MODE INTERFACE

The ADRF5703 has seven digital control inputs, D0 (LSB) to D6 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 8.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pin high. To change the attenuation state, use the control voltage inputs (D0 to D6) directly. Direct parallel mode is for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pin must be kept low when changing the control voltage inputs (D0 to D6) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 7-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 37 and Table 3 for additional information).

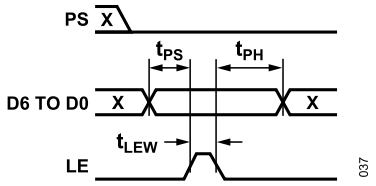

Figure 37. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

The ADRF5703 has two power supply pins (VDD and VSS) and nine control pins (PS, LE, D0 to D6). Figure 38 shows the external components and connections for the supply and control pins. The supply pins (VDD and VSS) are decoupled with 0.1µF multilayer ceramic capacitor. Place the decoupling capacitor as close as possible to the ADRF5703. The device pinout allows the placement of the decoupling capacitors close to the ADRF5703. No other external components are required for bias and operation, except DC blocking capacitors on the RF pins (ATTIN and ATTOUT) when the RF lines are biased at a voltage different than 0V. Refer to Pin Configuration and Function Descriptions section for additional information.

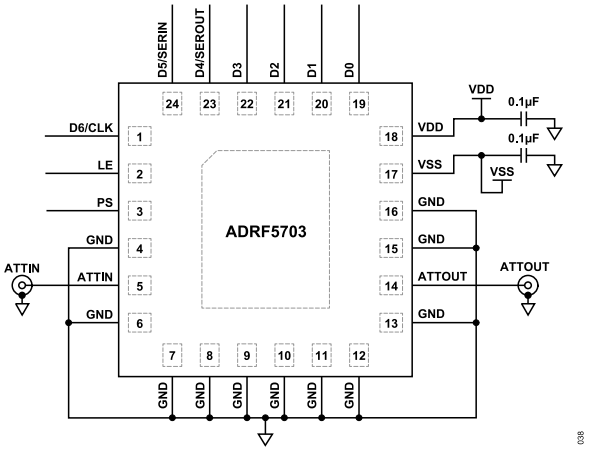

Figure 38. Simplified Application Circuit

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50Ω characteristic impedance on the PCB. Figure 39 shows the referenced CPWG RF trace design for an RF substrate with an 8mil thick Rogers RO4003 dielectric material. The RF trace with a 14mil width and a 7mil clearance is recommended for 1.5mil finished copper thickness.

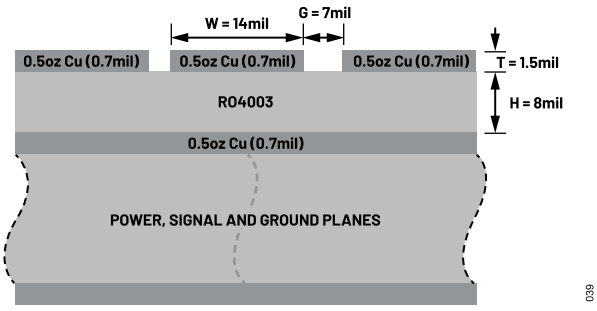

Figure 39. Example PCB Stackup

Figure 40 shows the routing of the RF traces, supply, and control signals from the ADRF5703. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

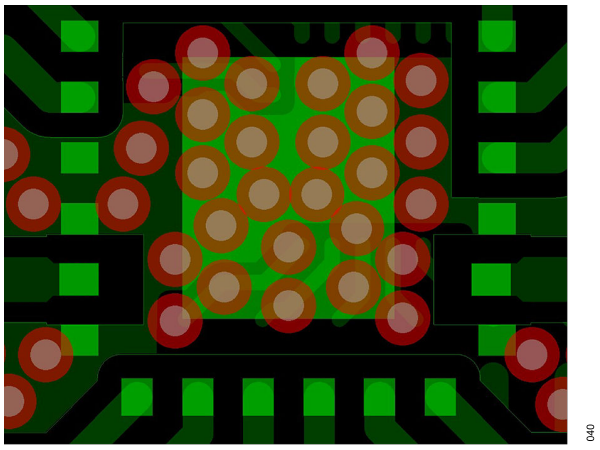

Figure 40. PCB Routings

Figure 41 shows the recommended layout from the ATTIN and ATTOUT pins of the ADRF5703 to the 50Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended to the device edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction and is divided into multiple openings for the paddle.

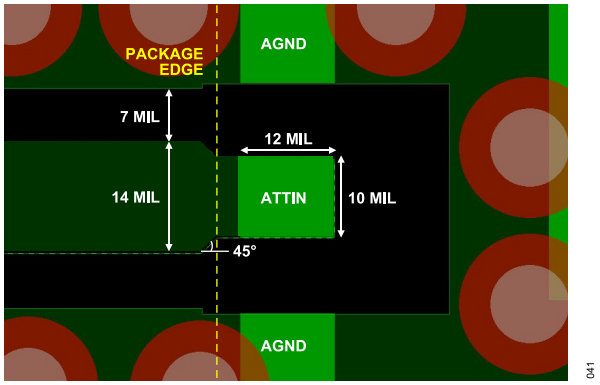

Figure 41. Recommended ATTIN Pin and ATTOUT Pin Transitions

For alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-24-20	LGA	24-Terminal Land Grid Array Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Quantity	Package Option
ADRF5703BCCZN	−40°C to +105°C	24-Terminal Land Grid Array [LGA]	Tape, 500	CC-24-20
ADRF5703BCCZN-R7	−40°C to +105°C	24-Terminal Land Grid Array [LGA]	Reel, 500	CC-24-20

[1] Z = RoHS-Compliant Part.