

FEATURES

Integrated dual-channel RF front end

- 2-stage LNA and high power SPDT switch
- On-chip bias and matching
- Single-supply operation

Gain

- High gain mode: 33 dB typical at 4.6 GHz
- Low gain mode: 18 dB typical at 4.6 GHz

Low noise figure

- High gain mode: 1.6 dB typical at 4.6 GHz
- Low gain mode: 1.6 dB typical at 4.6 GHz

High channel to channel isolation

- Between RxOUT-ChA and RxOUT-ChB: 45 dB typical
- Between TERM-ChA and TERM-ChB: 53 dB typical

Low insertion loss: 0.50 dB typical at 4.6 GHz

High power handling at $T_{CASE} = 105^{\circ}C$

Full lifetime

- LTE average power (9 dB PAR): 40 dBm
- Single event (<10 sec operation)
- LTE average power (9 dB PAR): 43 dBm

High OIP3: 31 dBm typical

Power-down mode and low gain mode for LNA

Low supply current

- High gain mode: 86 mA typical at 5 V
- Low gain mode: 36 mA typical at 5 V
- Power-down mode: 12 mA typical at 5 V

Positive logic control

40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

Wireless infrastructure

TDD massive multiple input and multiple output (MIMO) and active antenna systems

TDD-based communication systems

GENERAL DESCRIPTION

The ADRF5547 is a dual-channel, integrated RF, front end multichip module designed for time division duplexing (TDD) applications that operates from 3.7 GHz to 5.3 GHz. The ADRF5547 is configured in dual channels with a cascading two-stage low noise amplifier (LNA) and a high power silicon, single-pole, double-throw (SPDT) switch.

In high gain mode, the cascaded, two-stage LNA and switch offer a low noise figure of 1.6 dB and high gain of 33 dB at 4.6 GHz with an output third order intercept point (OIP3) of 31 dBm (typical).

FUNCTIONAL BLOCK DIAGRAM

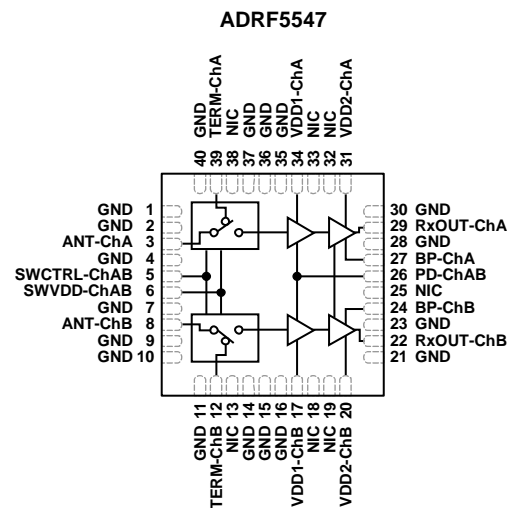


Figure 1.

20750-001

In low gain mode, one stage of the two-stage LNAs is in bypass, providing 18 dB gain at lower current of 36 mA. In power-down mode, the LNAs are turned off and the device draws 12 mA.

In transmit operation, when RF inputs are connected to a termination pin (TERM-ChA or TERM-ChB), the switch provides a low insertion loss of 0.50 dB and handles long term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 40 dBm for full lifetime operation and 43 dBm for single event (<10 sec) LNA protection operation.

The device comes in an RoHS compliant, compact, 40-lead, 6 mm × 6 mm LFCSP.

Rev. A

Document Feedback

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REVISION HISTORY

6/2020—Rev. 0 to Rev. A

| | |
|--|----|
| Changes to Theory of Operation Section..... | 13 |
| Changes to Applications Information Section and Figure 28..... | 14 |

10/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, and SWVDD-ChAB = 5 V, SWCTRL-ChAB = 0 V or SWVDD-ChAB, BP-ChA = VDD1-ChA or 0 V, BP-ChB = VDD1-ChB or 0 V, PD-ChAB = 0 V or VDD1-ChA, and $T_{CASE} = 25^{\circ}C$ on a 50 Ω system, unless otherwise noted.

Table 1

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|------|------|----------|-------------|
| FREQUENCY RANGE | | 3.7 | | 5.3 | GHz |
| GAIN ¹ | Receive operation at 4.6 GHz | | | | |
| High Gain Mode | | | 33 | | dB |
| Low Gain Mode | | | 18 | | dB |
| GAIN FLATNESS ¹ | Receive operation in any 100 MHz bandwidth | | | | |
| High Gain Mode | | | 0.6 | | dB |
| Low Gain Mode | | | 0.2 | | dB |
| NOISE FIGURE ¹ | Receive operation at 4.6 GHz | | | | |
| High Gain Mode | | | 1.6 | | dB |
| Low Gain Mode | | | 1.6 | | dB |
| OUTPUT THIRD ORDER INTERCEPT POINT (OIP3) ¹ | Receive operation, two-tone output power = 8 dBm per tone at 1 MHz tone spacing | | | | |
| High Gain Mode | | | 31 | | dBm |
| Low Gain Mode | | | 22 | | dBm |
| OUTPUT 1 dB COMPRESSION (OP1dB) | | | | | |
| High Gain Mode | | | 18 | | dBm |
| Low Gain Mode | | | 6 | | dBm |
| INSERTION LOSS ¹ | Transmit operation at 4.6 GHz | | 0.50 | | dB |
| CHANNEL TO CHANNEL ISOLATION ¹ | At 4.6 GHz | | | | |
| Between RxOUT-ChA and RxOUT-ChB | Receive operation | | 45 | | dB |
| Between TERM-ChA and TERM-ChB | Transmit operation | | 53 | | dB |
| SWITCH ISOLATION ¹ | Transmit operation, PD-ChAB = 0 V | | 20 | | dB |
| SWITCHING CHARACTERISTICS (T_{ON} , T_{OFF}) | 50% control voltage to 90%, 10% of RxOUT-ChA or RxOUT-ChB in receive operation | | 860 | | ns |
| | 50% control voltage to 90%, 10% of TERM-ChA or TERM-ChB in transmit operation | | 800 | | ns |
| RF INPUT POWER AT ANT-CHA, ANT-CHB ¹ | Receive operation, LTE average (9 dB PAR) | | | 15 | dBm |
| RECOMMENDED OPERATING CONDITIONS | | | | | |
| Bias Voltage Range | VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, SWVDD-ChAB | 4.75 | 5 | 5.25 | V |
| Control Voltage Range ² | SWCTRL-ChAB, BP-ChA, BP-ChB, PD-ChAB | 0 | | V_{DD} | V |
| RF Input Power at ANT-ChA, ANT-ChB | SWCTRL-ChAB = 5 V, BP-ChA = BP-ChB = 0 V, PD-ChAB = 5 V, $T_{CASE} = 105^{\circ}C$ Continuous wave | | | 40 | dBm |
| | 9 dB PAR LTE full lifetime average | | | 40 | dBm |
| | 9 dB PAR LTE single event (<10 sec) average | | | 43 | dBm |
| Case Temperature Range (T_{CASE}) ³ | | -40 | | +105 | $^{\circ}C$ |
| Junction Temperature at Maximum T_{CASE} ^{1,3} | Receive operation | | | 132 | $^{\circ}C$ |
| | Transmit operation | | | 134 | $^{\circ}C$ |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------|--|-----|--------|----------|------|
| DIGITAL INPUTS | | | | | |
| SWCTRL-ChAB, PD-ChAB | | | | | |
| Low (V_{IL}) | | 0 | | 0.7 | V |
| High (V_{IH}) ² | | 1.4 | | V_{DD} | V |
| BP-ChA, BP-ChB | | | | | |
| Low (V_{IL}) | | 0 | | 0.3 | V |
| High (V_{IH}) ² | | 1.0 | | V_{DD} | V |
| SUPPLY CURRENT (I_{DD}) | VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB = 5 V per channel | | | | |
| High Gain Mode | | | 86 | | mA |
| Low Gain Mode | | | 36 | | mA |
| Power-Down Mode | | | 12 | | mA |
| Transmit Current (Switch) | SWVDD-ChAB = 5 V | | 4.3 | | mA |
| DIGITAL INPUT CURRENTS | SWCTRL-ChAB, PD-ChAB, BP-ChA, BP-ChB = 5 V per channel | | | | |
| SWCTRL-ChAB | | | 0.0004 | | mA |
| PD-ChAB | | | 0.2 | | mA |
| BP-ChA, BP-ChB | | | 0.4 | | mA |

¹ See Table 5 and Table 6.

² V_{DD} (shown in the maximum column) is the voltage of the SWVDD-ChAB, VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB pins.

³ Measured at the exposed pad (EPAD).

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--|------------------------------|
| Positive Supply Voltage VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB | 7 V |
| SWVDD-ChAB | 5.4 V |
| Digital Control Input Voltage SWCTRL-ChAB | -0.3 V to $V_{DD}^1 + 0.3$ V |
| BP-ChA, BP-ChB, PD-ChAB | -0.3 V to $V_{DD}^1 + 0.3$ V |
| RF Input Power (LTE Peak) | |
| Transmit | 53 dBm |
| Receive | 25 dBm |
| Temperature | |
| Storage | -65°C to +150°C |
| Reflow (Moisture Sensitivity Level (MSL) 3 Rating) | 260°C |
| Electrostatic Discharge (ESD) Sensitivity | |
| Human Body Model (HBM) | 1 kV, Class 1C |
| Charge Device Model (CDM) | 1.25 kV |

¹ V_{DD} is the voltage of the VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

| Package Type | θ_{JC} | Unit |
|-----------------------------|---------------|------|
| CP-40-15 | | |
| High Gain and Low Gain Mode | 30 | °C/W |
| Power-Down Mode | 8.7 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

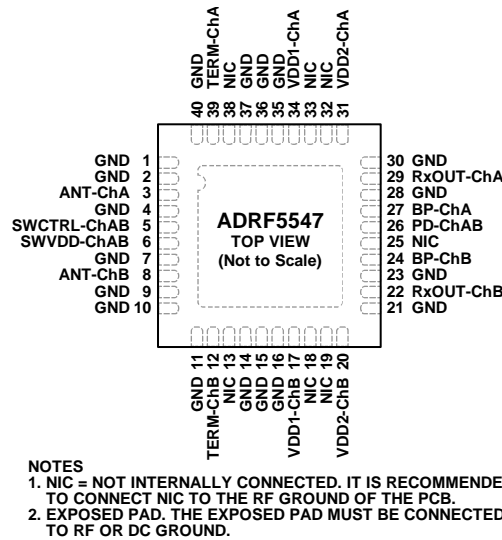


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---|-------------|---|
| 1, 2, 4, 7, 9 to 11, 14 to 16, 21, 23, 28, 30, 35 to 37, 40 | GND | Ground. See Figure 3 for the interface schematic. |
| 3 | ANT-ChA | RF Input to Channel A. |
| 5 | SWCTRL-ChAB | Control Voltage for Switches on Channel A and Channel B. See Figure 7 for the interface schematic. |
| 6 | SWVDD-ChAB | Supply Voltage for Switches on Channel A and Channel B. See Figure 7 for the interface schematic. |
| 8 | ANT-ChB | RF Input to Channel B. |
| 12 | TERM-ChB | Termination Output. This pin is the transmitter path for Channel B. |
| 13, 18, 19, 25, 32, 33, 38 | NIC | Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB. |
| 17 | VDD1-ChB | Supply Voltage for Stage 1 LNA on Channel B. See Figure 5 for the interface schematic. |
| 20 | VDD2-ChB | Supply Voltage for Stage 2 LNA on Channel B. See Figure 5 for the interface schematic. |
| 22 | RxOUT-ChB | RF Output. This pin is the receiver path for Channel B. See Figure 4 for the interface schematic. |
| 24 | BP-ChB | Bypass Second Stage LNA of Channel B. See Figure 6 for the interface schematic. |
| 26 | PD-ChAB | Power-Down All Stages of LNA for Channel A and Channel B. See Figure 6 for the Interface schematic. |
| 27 | BP-ChA | Bypass Second Stage LNA of Channel A. See Figure 6 for the interface schematic. |
| 29 | RxOUT-ChA | RF Output. This pin is the receiver path for Channel A. See Figure 4 for the interface schematic. |
| 31 | VDD2-ChA | Supply Voltage for Stage 2 LNA on Channel A. See Figure 5 for the interface schematic. |
| 34 | VDD1-ChA | Supply Voltage for Stage 1 LNA on Channel A. See Figure 5 for the interface schematic. |
| 39 | TERM-ChA | Termination Output. This pin is the transmitter path for Channel A. |
| | EPAD | Exposed Pad. The exposed pad must be connected to RF or dc ground. |

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

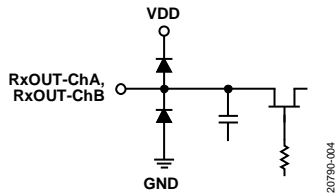


Figure 4. RxOUT-ChA and RxOUT-ChB Interface Schematic

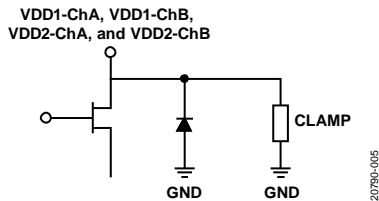


Figure 5. VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB Interface Schematic

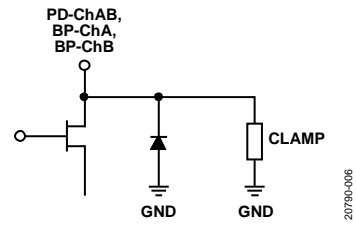


Figure 6. PD-ChAB, BP-ChA, and BP-ChB Interface Schematic

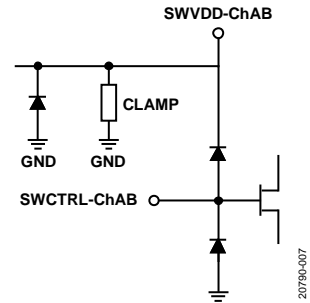


Figure 7. SWCTRL-ChAB, SWVDD-ChAB Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION, HIGH GAIN MODE

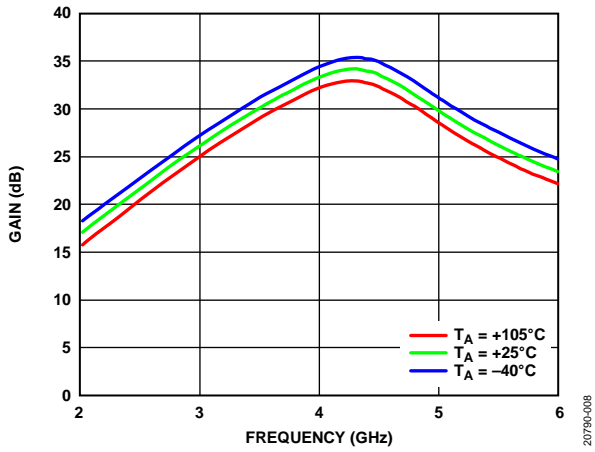


Figure 8. Gain vs. Frequency at Various Temperatures

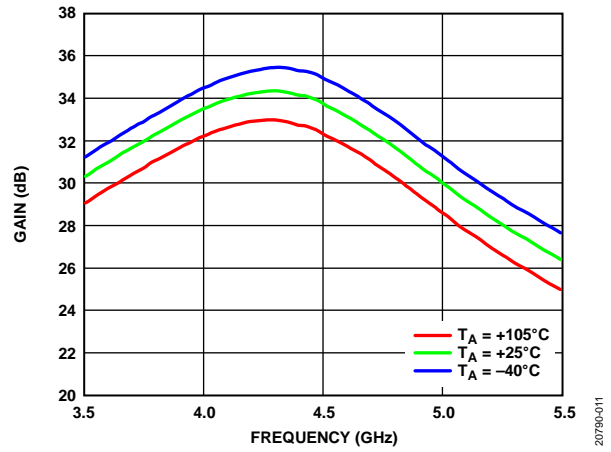


Figure 11. Gain vs. Frequency at Various Temperatures, 3.5 GHz to 5.5 GHz

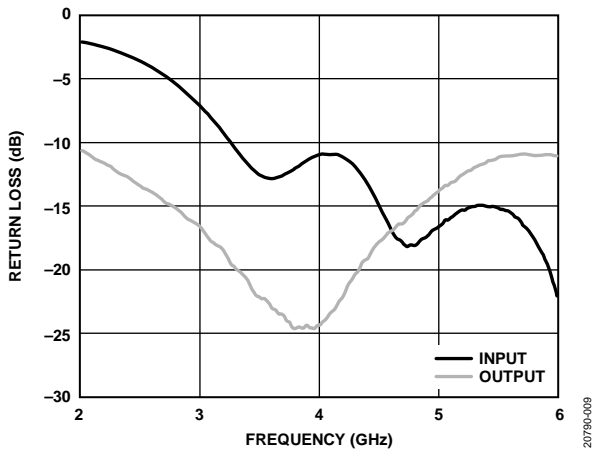


Figure 9. Return Loss vs. Frequency

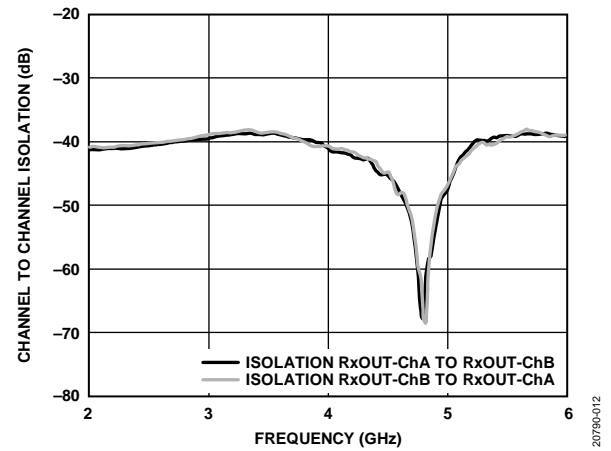


Figure 12. Channel to Channel Isolation vs. Frequency

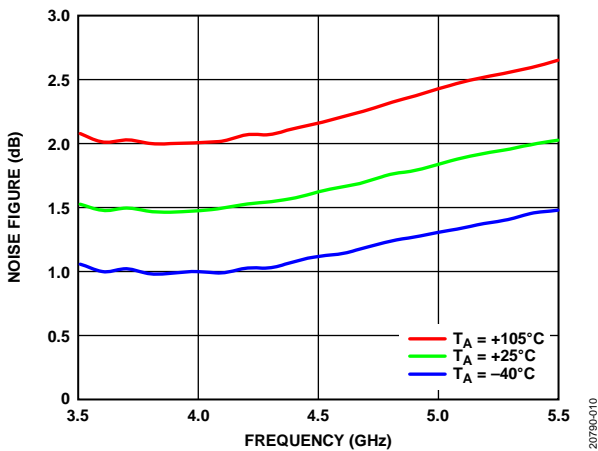


Figure 10. Noise Figure vs. Frequency for Various Temperatures

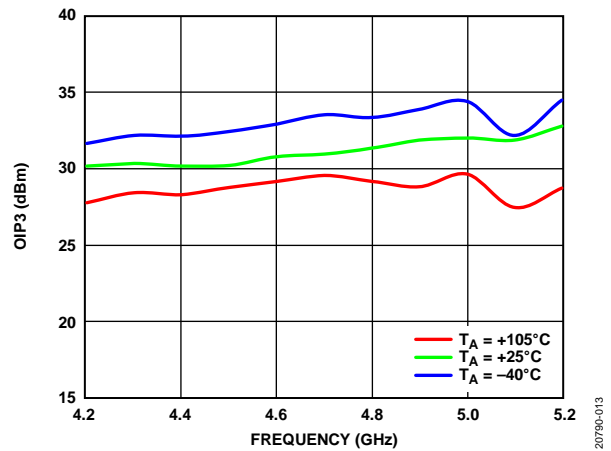


Figure 13. OIP3 vs. Frequency for Various Temperatures, 8 dBm Output Tone Power

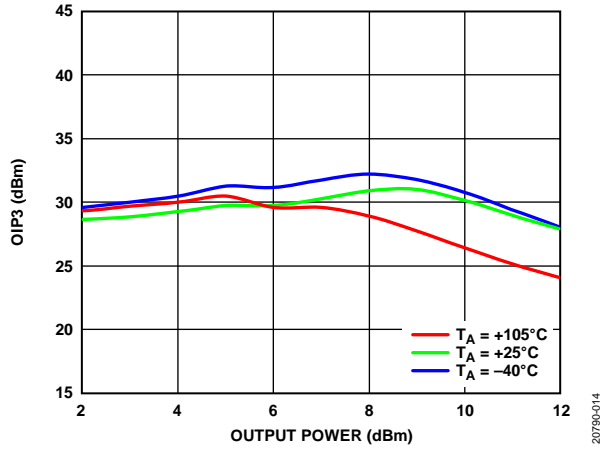


Figure 14. OIP3 vs. Output Power for Various Temperatures, 4.6 GHz

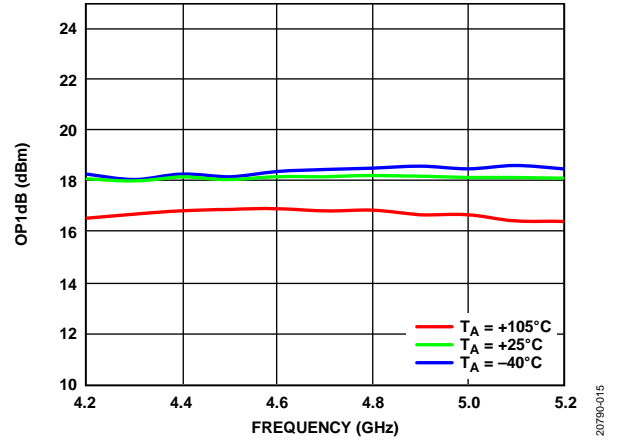


Figure 15. OP1dB vs. Frequency at Various Temperatures

RECEIVE OPERATION, LOW GAIN MODE

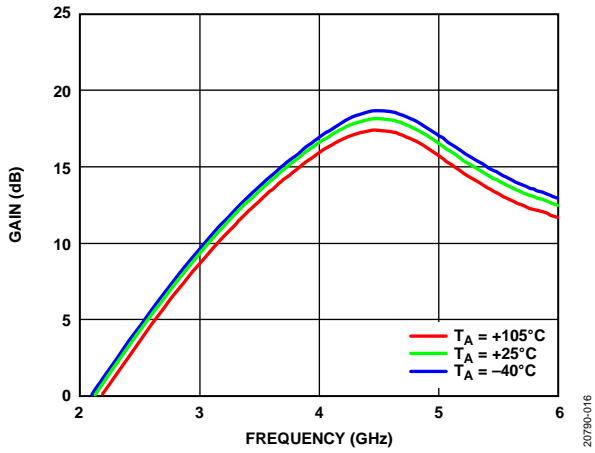


Figure 16. Gain vs. Frequency at Various Temperatures

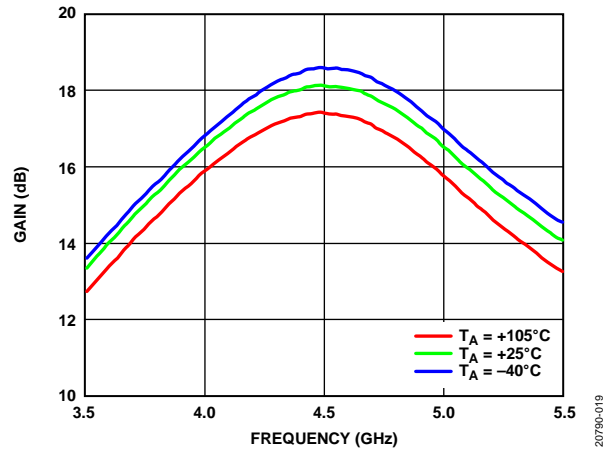


Figure 19. Gain vs. Frequency at Various Temperatures, 3.5 GHz to 5.5 GHz

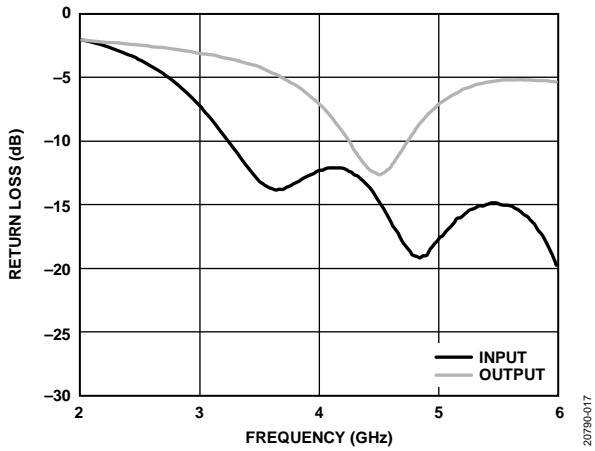


Figure 17. Return Loss vs. Frequency

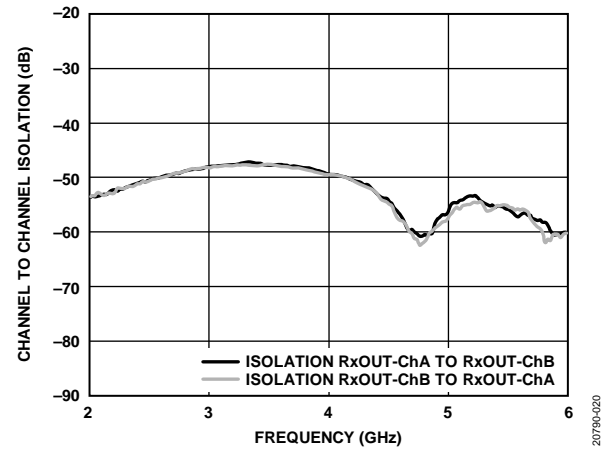


Figure 20. Channel to Channel Isolation vs. Frequency

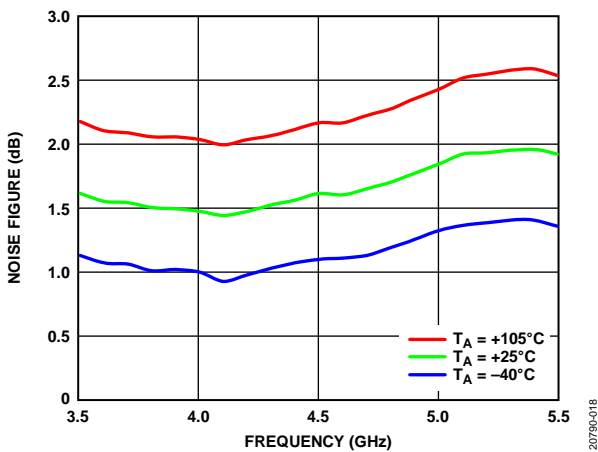


Figure 18. Noise Figure vs. Frequency at Various Temperatures

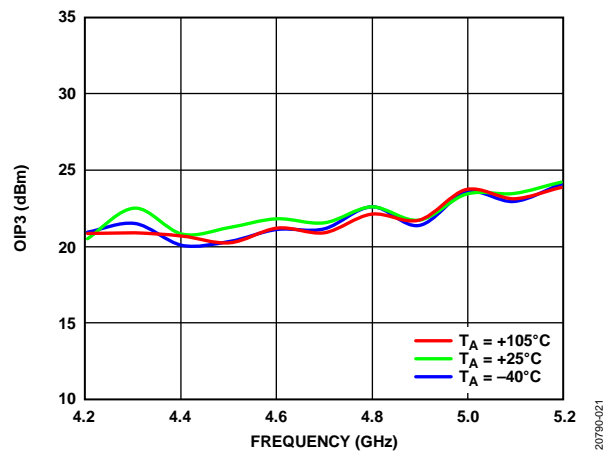


Figure 21. OIP3 vs. Frequency at Various Temperatures, -8 dBm Output Tone Power

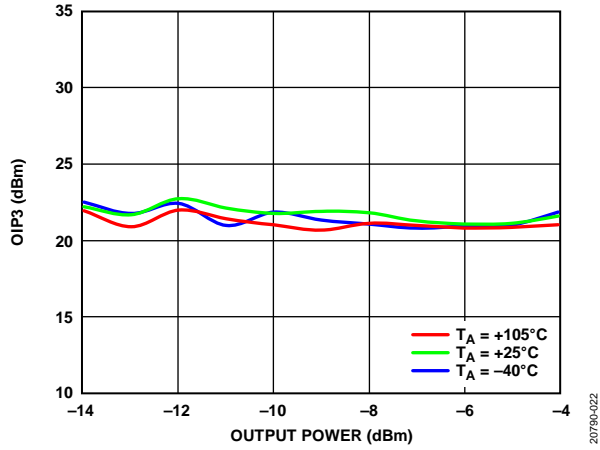


Figure 22. OIP3 vs. Output Power for Various Temperatures, 4.6 GHz

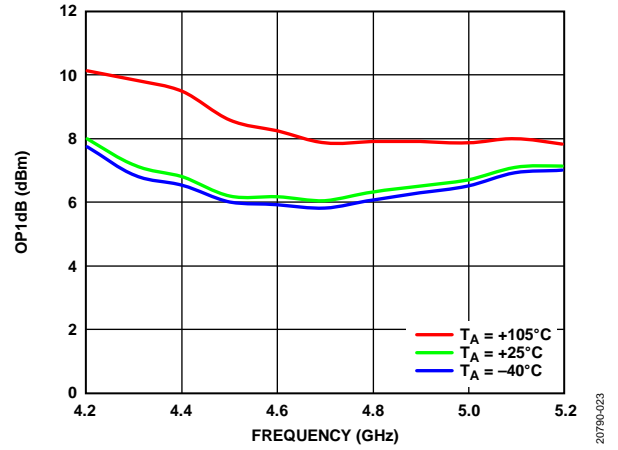


Figure 23. OP1dB vs. Frequency at Various Temperatures

TRANSMIT OPERATION

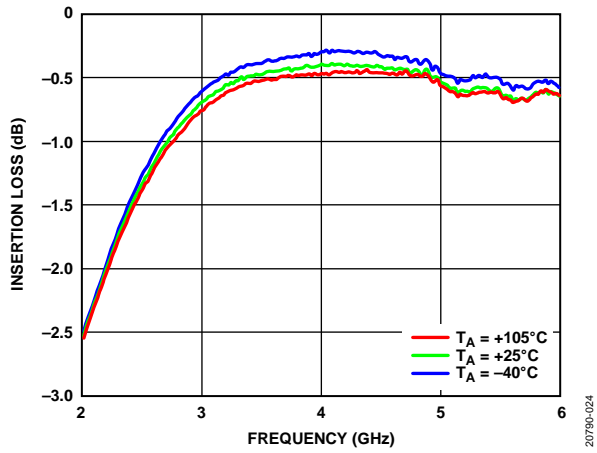


Figure 24. Insertion Loss vs. Frequency at Various Temperatures

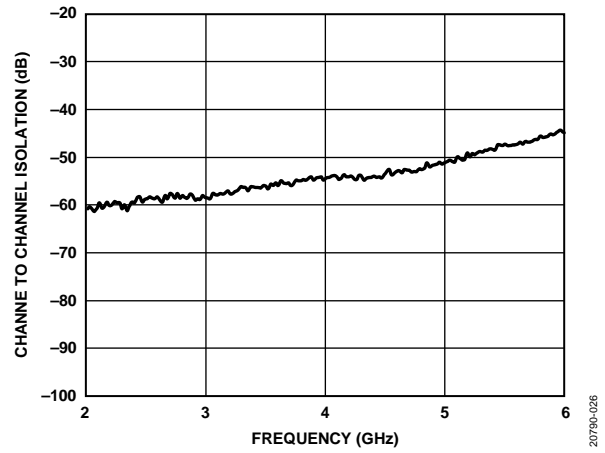


Figure 26. Channel to Channel Isolation vs. Frequency

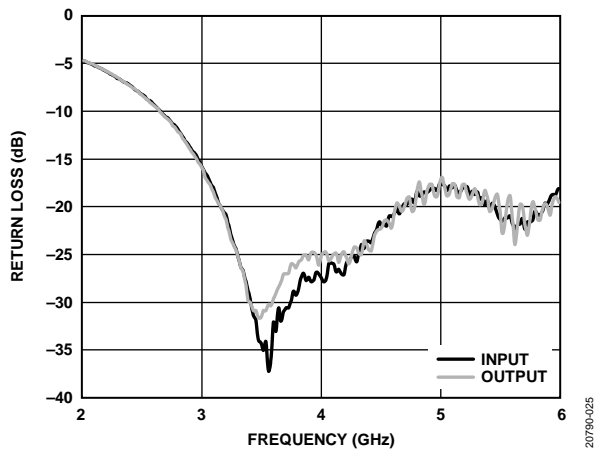


Figure 25. Return Loss vs. Frequency

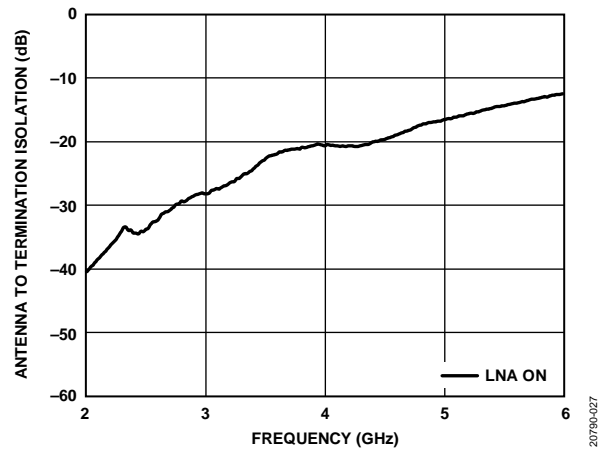


Figure 27. Antenna to Termination Isolation vs. Frequency

THEORY OF OPERATION

The ADRF5547 requires a positive supply voltage applied to VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB. Use bypassing capacitors on the supply lines to filter noise and use 300 Ω series resistors on the BP-Chx and PD-ChAB digital control pins for glitch and overcurrent protection.

SIGNAL PATH SELECT

When SWCTRL-ChAB is set to high, the ADRF5547 supports transmit operations. During this operation, when applying an RF input to ANT-ChA and ANT-ChB, the signal paths connect from ANT-ChA to TERM-ChA and from ANT-ChB to TERM-ChB.

When SWCTRL-ChAB is set to low, the ADRF5547 supports receive operations. During this operation, applying an RF input at ANT-ChA and ANT-ChB connects ANT-ChA to RxOUT-ChA and ANT-ChB to RxOUT-ChB.

Receive Operation

The ADRF5547 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table 6.

When PD-ChAB is set to low, the LNA powers up and the user can select high gain mode or low gain mode. To select high gain mode, set BP-ChA or BP-ChB to low. To select low gain mode, set BP-ChA or BP-ChB to high.

When PD-ChAB is set to high, the ADRF5547 enters power-down mode. To select power-down high isolation mode, set BP-ChA or BP-ChB to low. To select power-down low isolation mode, set BP-ChA or BP-ChB to high.

BIASING SEQUENCE

To power up the ADRF5547, perform the following steps:

1. Connect GND to ground.
2. Power up VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB.
3. Power up SWCTRL-ChAB.
4. Power up PD-ChAB.
5. Power up BP-ChA and BP-ChB.
6. Apply an RF input signal to ANT-ChA and ANT-ChB.

To power down the ADRF5547, perform these steps in the reverse order.

Table 5. Truth Table: Signal Path

| SWCTRL-ChAB | Signal Path Select | |
|-------------|---------------------------------|-------------------|
| | Transmit Operation ¹ | Receive Operation |
| Low | Off | On |
| High | On | Off |

¹ See the signal path descriptions in Table 6.

Table 6. Truth Table: Operation

| Operation | PD-ChAB | BP-ChA, BP-ChB | Signal Path |
|--------------------------------|---------|----------------|--|
| Receive Operation | | | ANT-ChA to RxOUT-ChA, ANT-ChB to RxOUT-ChB |
| High Gain Mode | Low | Low | |
| Low Gain Mode | Low | High | |
| Power-Down High Isolation Mode | High | Low | |
| Power-Down Low Isolation Mode | High | High | |

APPLICATIONS INFORMATION

To generate the evaluation PCB used in the application circuit shown in Figure 28, use proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and the backside ground slug must connect directly to the ground plane. Use 300 Ω series resistors

on the BP-Chx and PD-ChAB digital control pins for glitch and overcurrent protection.

See the [ADRF5547-EVALZ](#) user guide for additional information on the evaluation board.

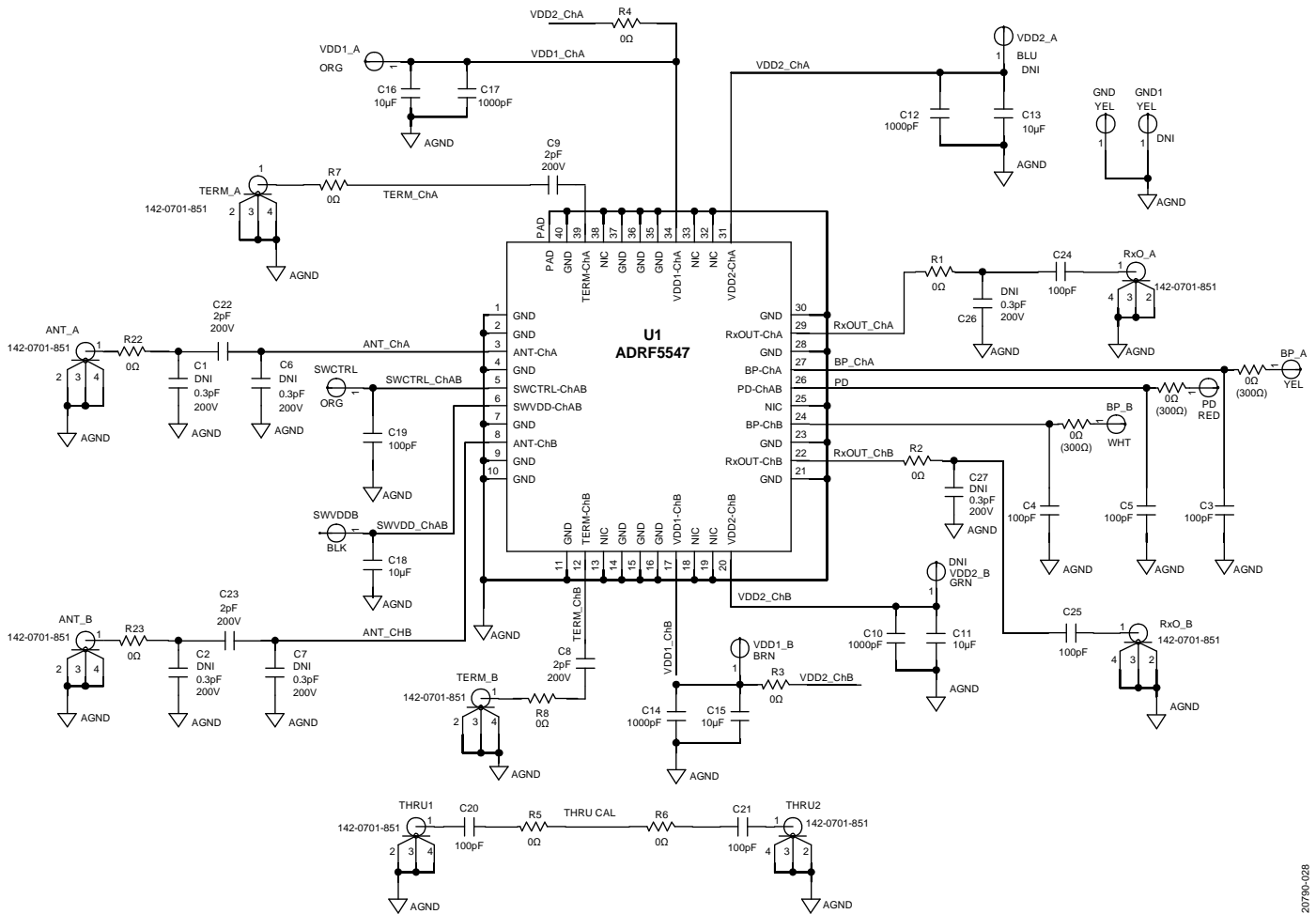
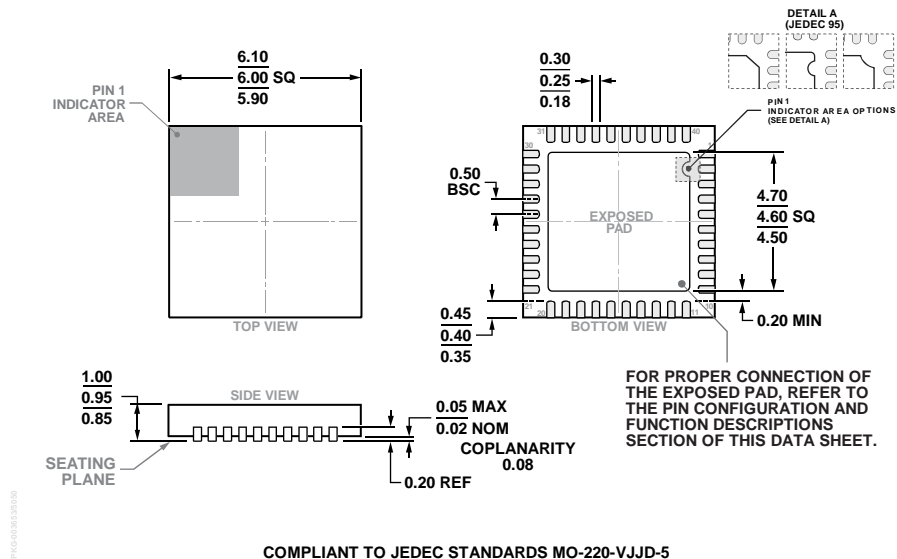


Figure 28. Application Circuit

20750-028

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 29. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADRF5547BCPZN | -40°C to +105°C | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-15 |
| ADRF5547BCPZN-R7 | -40°C to +105°C | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-15 |
| ADRF5547BCPZN-RL | -40°C to +105°C | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-15 |
| ADRF5547-EVALZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.