

Die on Carrier, Silicon Digital Attenuator, 2 dB LSB, 5-Bit, 100 MHz to 22 GHz

FEATURES

- ▶ Wideband frequency range: 100 MHz to 22 GHz
- ▶ Attenuation range: 46 dB with 2 dB steps
- ▶ Low insertion loss
 - ▶ 1.5 dB typical up to 10 GHz
 - ▶ 1.9 dB typical up to 20 GHz
- ▶ High attenuation accuracy
 - ▶ $+(0.1 + 0.5\% \text{ of attenuation state})$ typical up to 10 GHz
 - ▶ $-(0.1 + 1.5\% \text{ of attenuation state})$ typical up to 10 GHz
 - ▶ $+(0.1 + 0.5\% \text{ of attenuation state})$ typical up to 20 GHz
 - ▶ $-(0.1 + 4.0\% \text{ of attenuation state})$ typical up to 20 GHz
- ▶ Low step error
 - ▶ ± 0.2 dB typical up to 10 GHz
 - ▶ ± 0.3 dB typical up to 20 GHz
- ▶ High input linearity
 - ▶ P0.1dB: >27 dBm typical at all attenuation states
 - ▶ P1dB: >30 dBm typical at all attenuation states
 - ▶ IP3: >47 dBm typical at all attenuation states
- ▶ High RF power handling
 - ▶ 24 dBm steady state average
 - ▶ 30 dBm steady state peak
- ▶ Consistent return loss at all attenuation states
- ▶ Tight distribution in relative phase
- ▶ No low frequency spurious signals
- ▶ Parallel mode control, CMOS/LVTTL compatible
- ▶ RF amplitude settling time (0.1 dB of final RF output): 130 ns
- ▶ 18-pad, 3.196 mm × 1.841 mm, die on carrier [CHIP]

APPLICATIONS

- ▶ Industrial scanners
- ▶ Test and instrumentation
- ▶ Cellular infrastructure: 5G millimeterwave
- ▶ Military radios, radars, electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

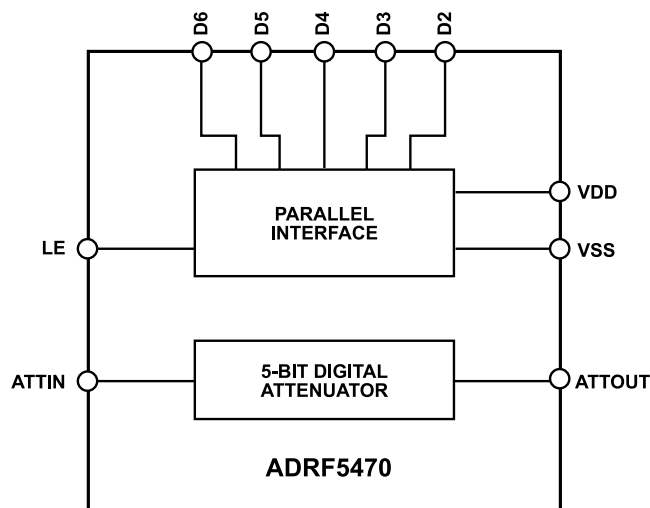


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5470 is a 5-bit digital attenuator with a 46 dB attenuation range in 2 dB steps manufactured in a silicon process attached on a gallium arsenide (GaAs) carrier substrate. The substrate incorporates the bond pads for chip and wire assembly, and the bottom of the device is metalized and connected to ground.

This device operates from 100 MHz to 22 GHz with better than 1.9 dB of insertion loss and high attenuation accuracy. The ADRF5470 supports bidirectional operation and has a RF input power handling capability of 24 dBm average and 30 dBm peak for all attenuation states.

The ADRF5470 requires a dual-supply voltage of +3.3 V and -3.3 V. The device features parallel mode control and complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5470 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated (see Table 2).

The ADRF5470 is designed to match a characteristic impedance of 50 Ω .

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REVISION HISTORY**3/2025—Revision 0: Initial Version**

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$V_{DD} = +3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , $T_{DIE} = 25^\circ\text{C}$, and a $50\ \Omega$ system, unless otherwise noted. V_{CTRL} refers to the control voltages on the LE, D2, D3, D4, D5, and D6 pads.

S-parameters are measured with microstrip launchers and 3 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are de-embedded. See the [Applications Information](#) section for assembly details.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		22,000	MHz
INSERTION LOSS	100 MHz to 10 GHz		1.5		dB
	10 GHz to 20 GHz		1.9		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	100 MHz to 10 GHz		20		dB
	10 GHz to 20 GHz		20		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		46		dB
Step Size	Between any successive attenuation states		2		dB
Accuracy	Referenced to insertion loss				
	100 MHz to 10 GHz		+(0.1 + 0.5% of state)		dB
			-(0.1 + 1.5% of state)		dB
	10 GHz to 20 GHz		+(0.1 + 0.5% of state)		dB
			-(0.1 + 4.0% of state)		dB
Step Error	Between any successive state				
	100 MHz to 10 GHz		± 0.2		dB
	10 GHz to 20 GHz		± 0.3		dB
RELATIVE PHASE	Referenced to insertion loss				
	100 MHz to 10 GHz		35		Degrees
	10 GHz to 20 GHz		70		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power (P_{IN}) = 10 dBm				
Rise Time and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output (RF_{OUT})		10		ns
On Time and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF_{OUT}		50		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered control to 0.1 dB of final RF_{OUT}		130		ns
0.05 dB	50% triggered control to 0.05 dB of final RF_{OUT}		150		ns
Overshoot			1		dB
Undershoot			0.75		dB
RF Phase Settling Time	Frequency = 20 GHz				
5°	50% triggered control to 5° of final RF output		60		ns
1°	50% triggered control to 1° of final RF output		80		ns
INPUT LINEARITY ¹	100 MHz to 20 GHz, all attenuation states				
0.1 dB Power Compression (P0.1dB)			>27		dBm
1 dB Power Compression (P1dB)			>30		dBm
Third-Order Intercept (IP3)	Two-tone $P_{IN} = 15\text{ dBm}$ per tone, $\Delta f = 1\text{ MHz}$		>47		dBm
DIGITAL CONTROL INPUTS	LE, D2, D3, D4, D5, and D6				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Current					
Low (I_{INL})			-33		μA
High (I_{INH})			<1		μA
SUPPLY CURRENT					
Positive Supply Current (I_{DD})					
Bias Low	LE, D2, D3, D4, D5, and D6 = 0 V		350		μA
Bias High	LE, D2, D3, D4, D5, and D6 = 3.3 V		150		μA
Negative Supply Current (I_{SS})			-520		μA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
Positive (V_{DD})		3.15		3.45	V
Negative (V_{SS})		-3.45		-3.15	V
Digital Control Voltage		0		V_{DD}	V
RF Power Handling ^{2, 3}	Frequency = 100 MHz to 20 GHz, $T_{DIE} = 85^{\circ}\text{C}$, all attenuation states				
Input at ATTIN or ATTOUT	Steady state, average			24	dBm
	Steady state, peak			30	dBm
	Hot switching, average			24	dBm
	Hot switching, peak			27	dBm
Die Temperature (T_{DIE}) ⁴		-40		+105	$^{\circ}\text{C}$

¹ For input linearity performance over wide frequency range, see [Figure 21](#) and [Figure 22](#).

² For power derating over frequency, see [Figure 2](#) and [Figure 3](#). Applicable for all ATTIN and ATTOUT power specifications.

³ For 105 $^{\circ}\text{C}$ operation, the average power handling degrades from the $T_{DIE} = 85^{\circ}\text{C}$ specifications by 3 dB.

⁴ T_{DIE} refers to the bottom of the die on carrier.

SPECIFICATIONS

SINGLE-SUPPLY OPERATION

$V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{CTRL} = 0\text{ V}$ or $V_{DD}\text{ V}$, $T_{DIE} = 25^{\circ}\text{C}$, and a $50\ \Omega$ system, unless otherwise noted.

Table 2. Single-Supply Operational Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		100		22,000	MHz
SWITCHING CHARACTERISTICS					
t_{RISE} and t_{FALL}	10% to 90% of RF_{OUT}		95		ns
t_{ON} and t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		125		ns
RF Amplitude Settling Time					
0.1 dB	50% V_{CTRL} to 0.1 dB of final RF_{OUT}		160		ns
0.05 dB	50% V_{CTRL} to 0.05 dB of final RF_{OUT}		165		ns
RF Phase Settling Time	Frequency = 20 GHz				
5°	50% triggered control to 5° of final RF_{OUT}		70		ns
1°	50% triggered control to 1° of final RF_{OUT}		150		ns
INPUT LINEARITY	Frequency = 100 MHz to 20 GHz				
0.1 dB Power Compression			17		dBm
Input Third-Order Intercept	Two-tone input power = 5 dBm each tone, $\Delta f = 1\text{ MHz}$		42		dBm
RECOMMENDED OPERATING CONDITONS					
RF Power Handling ^{1, 2}	Frequency = 100 MHz to 20 GHz, $T_{DIE} = 85^{\circ}\text{C}$, all attenuation states				
Input at ATTIN or ATTOUT	Steady state, average			15	dBm
	Steady state, peak			15	dBm
	Hot switching, average			15	dBm
	Hot switching, peak			15	dBm

¹ For power derating over frequency, see [Figure 2](#) and [Figure 3](#). Applicable for all ATTIN and ATTOUT power specifications.

² For 105°C operation, the average power handling degrades from the $T_{DIE} = 85^{\circ}\text{C}$ specification by 3 dB.

TIMING SPECIFICATIONS

See [Figure 24](#) for the timing diagram.

Table 3. Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{LEW}	LE pulse width, see Figure 24	10			ns
t_{PH}	Hold time, see Figure 24			10	ns
t_{PS}	Setup time, see Figure 24	2			ns

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	-0.3 V to +3.6 V
V_{SS}	-3.6 V to +0.3 V
Digital Control Inputs	
Voltage	-0.3 V to $V_{DD} + 0.3$ V
Current	3 mA
RF Input Power ¹ , Dual Supply ($V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, Frequency = 100 MHz to 20 GHz, $T_{DIE} = 85^{\circ}\text{C}^2$)	
Steady State, Average	25 dBm
Steady State, Peak	31 dBm
Hot Switching, Average	25 dBm
Hot Switching, Peak	28 dBm
RF Input Power ¹ , Single Supply ($V_{DD} = 3.3$ V, $V_{SS} = 0$ V, Frequency = 100 MHz to 20 GHz, $T_{DIE} = 85^{\circ}\text{C}^2$)	
Steady State, Average	16 dBm
Steady State, Peak	16 dBm
Hot Switching, Average	16 dBm
Hot Switching, Peak	16 dBm
RF Power Under Unbiased Condition (V_{DD} and $V_{SS} = 0$ V)	
Input at ATTIN or ATTOUT	11 dBm
Temperature	
Junction (T_J)	135°C
Storage	-55°C to +150°C
Processing	170°C
Continuous Power Dissipation (P_{DISS})	0.25W

¹ For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

² For 105°C operation, the average power handling degrades from the $T_{DIE} = 85^{\circ}\text{C}$ specifications by 3 dB.

Stresses at or above those listed under absolute maximum ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

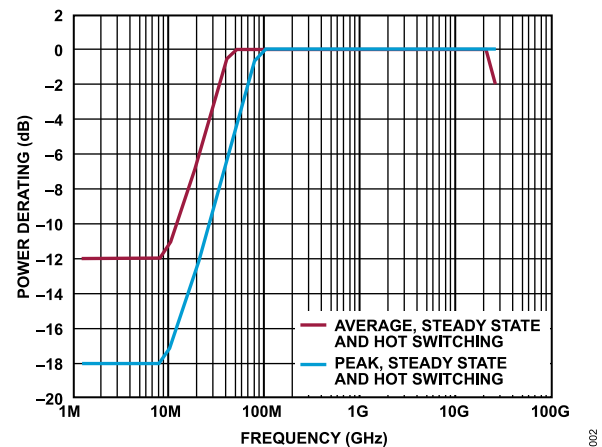
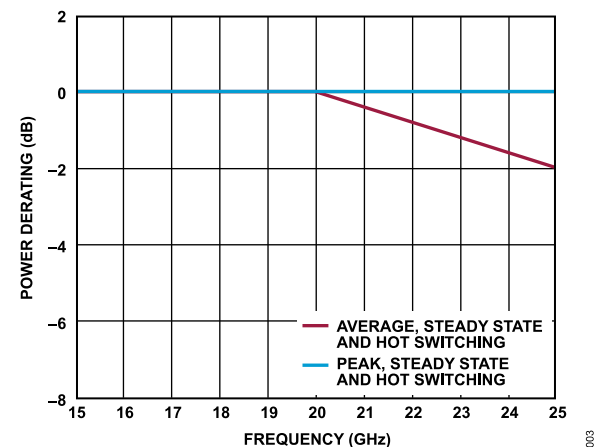
Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to carrier bottom) thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
C-18-2	200	°C/W

POWER DERATING CURVES

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{DIE} = 85^{\circ}\text{C}$ Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{DIE} = 85^{\circ}\text{C}$

ABSOLUTE MAXIMUM RATINGS**ELECTROSTATIC DISCHARGE (ESD) RATINGS**

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADRF5470

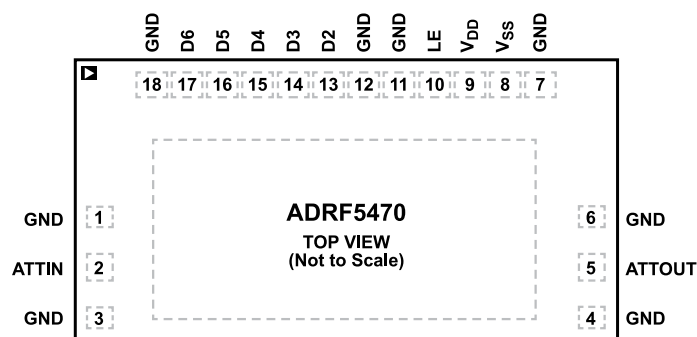
Table 6. ADRF5470, 18-Pad Die on Carrier [CHIP]

ESD Model	Withstand Threshold (V)
HBM	
ATTIN and ATTOUT Pads	±1000
Supply and Control Pads	±2000

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. THE CARRIER BOTTOM IS GOLD METALIZED AND MUST BE DIRECTLY ATTACHED TO THE GROUND PLANE USING CONDUCTIVE EPOXY.

004

Figure 4. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 7, 11, 12, 18	GND	Grounds. Bonding of these GND pads are optional. See the Applications Information section.
2	ATTIN	Attenuator Input. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 6 for the interface schematic.
5	ATTOUT	Attenuator Output. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 6 for the interface schematic.
8	V _{SS}	Negative Supply Input. See Figure 8 for the interface schematic.
9	V _{DD}	Positive Supply Input. See Figure 7 for the interface schematic.
10	LE	Latch Enable Input. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
13	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
14	D3	Parallel Control Input for 4 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
15	D4	Parallel Control Input for 8 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
16	D5	Parallel Control Input for the First 16 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
17	D6	Parallel Control Input for the Second 16 dB Attenuator Bit. See the Theory of Operation section for more information. See Figure 5 for the interface schematic.
	Carrier Bottom	The carrier bottom is gold metalized and must be directly attached to the ground plane using conductive epoxy.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

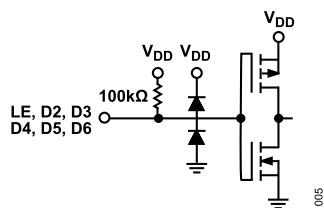


Figure 5. Digital Input Interface Schematic (LE, D2, D3, D4, D5 and D6)

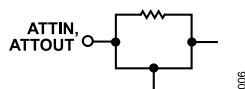


Figure 6. ATTIN and ATTOUT Interface Schematic

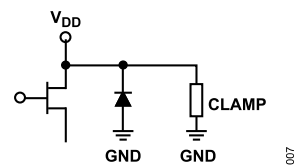


Figure 7. VDD Interface Schematic

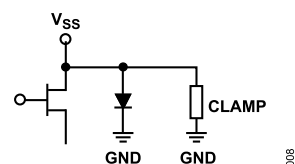


Figure 8. VSS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , $T_{DIE} = 25^\circ\text{C}$, and a $50\ \Omega$ system, unless otherwise noted.

S-parameters are measured with microstrip launchers and 3 mil width ribbon bonds using ground-signal-ground (GSG) probes. The launchers are deembedded. See the [Applications Information](#) section for assembly details.

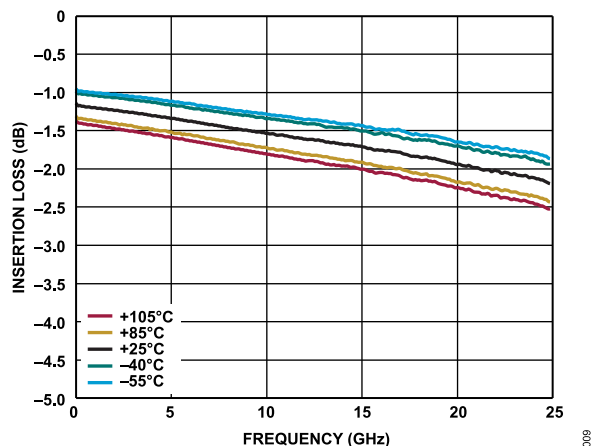


Figure 9. Insertion Loss vs. Frequency over Temperature

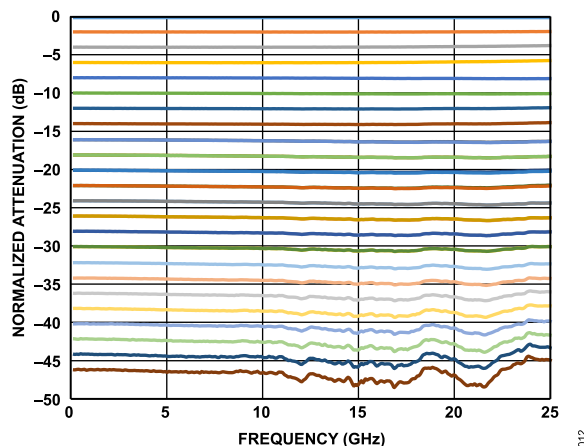


Figure 11. Normalized Attenuation vs. Frequency for All States

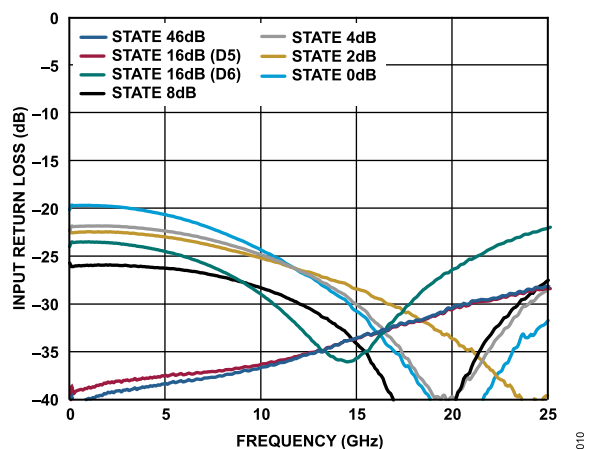


Figure 10. Input Return Loss vs. Frequency (Major States Only)

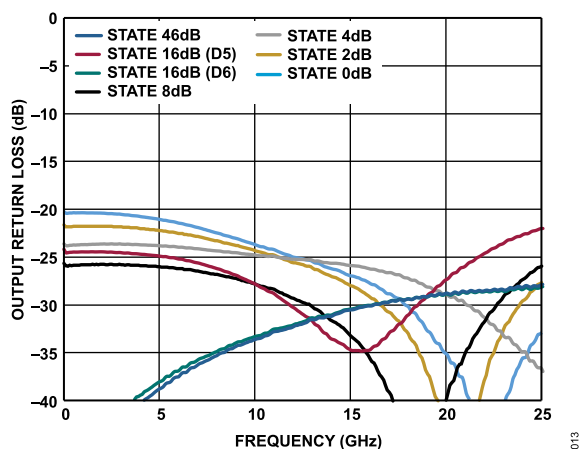


Figure 12. Output Return Loss vs. Frequency (Major States Only)

TYPICAL PERFORMANCE CHARACTERISTICS

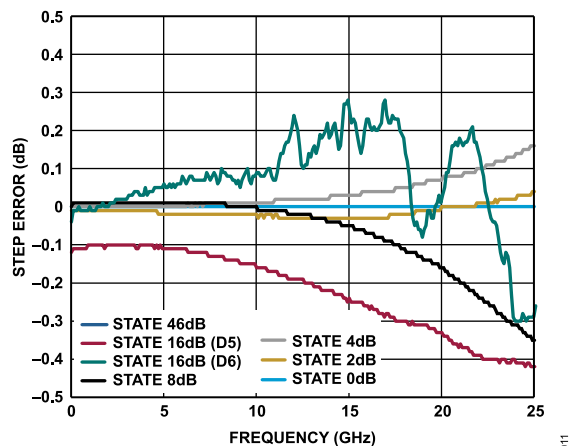


Figure 13. Step Error vs. Frequency

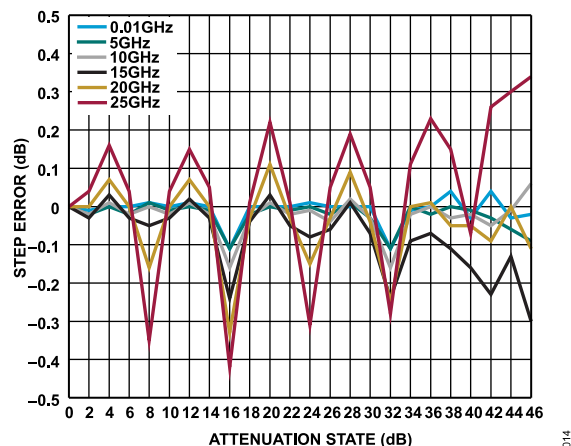


Figure 16. Step Error vs. Attenuation State over Frequency

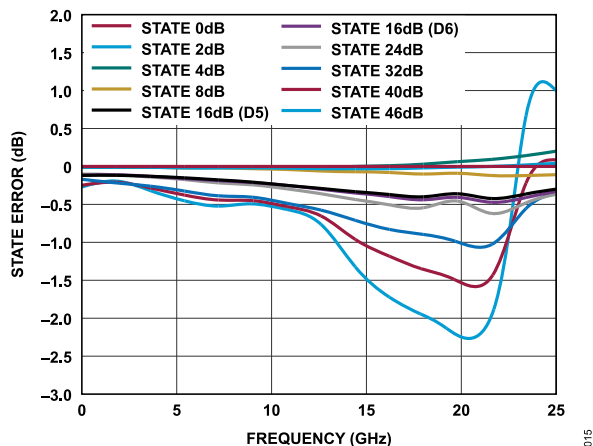


Figure 14. State Error vs. Frequency

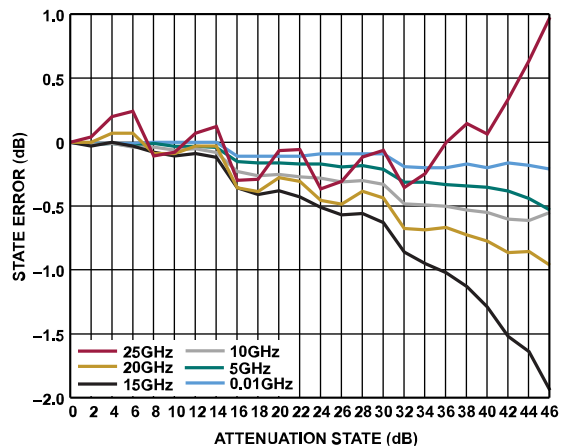


Figure 17. State Error vs. Attenuation State over Frequency

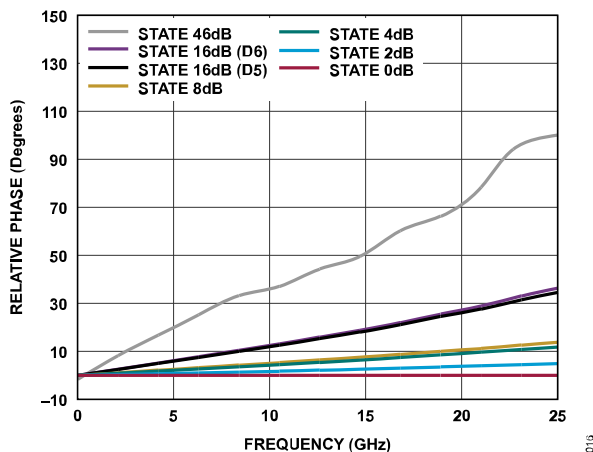


Figure 15. Relative Phase vs. Frequency

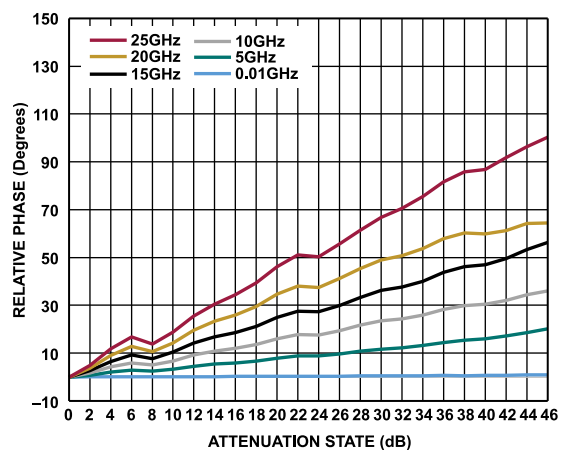


Figure 18. Relative Phase vs. Attenuation State over Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , $T_{DIE} = 25^{\circ}\text{C}$, and a $50\ \Omega$ system, unless otherwise noted.

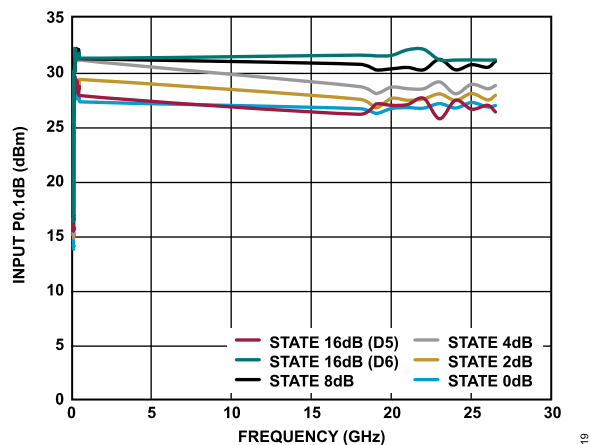


Figure 19. Input P0.1dB vs. Frequency

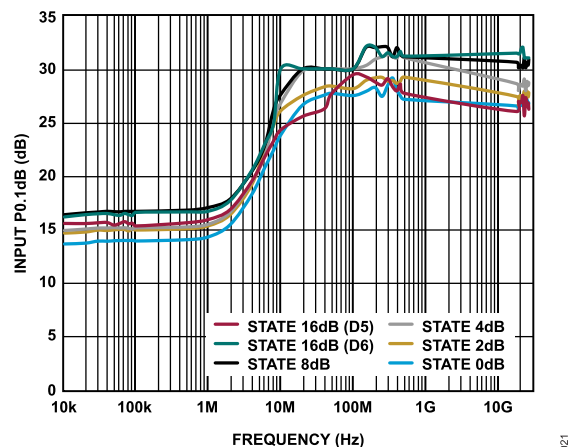


Figure 21. Input P0.1dB vs. Frequency, Low Frequency Detail

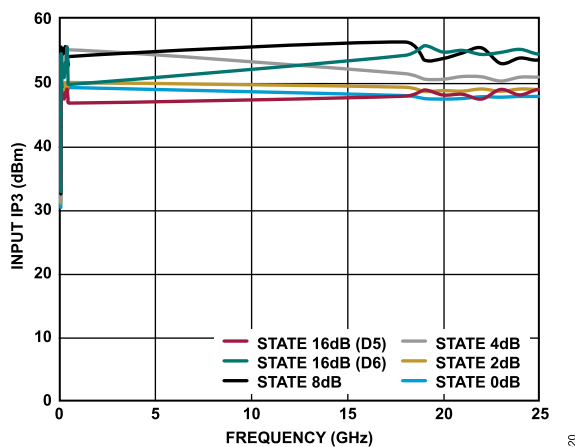


Figure 20. Input IP3 vs. Frequency

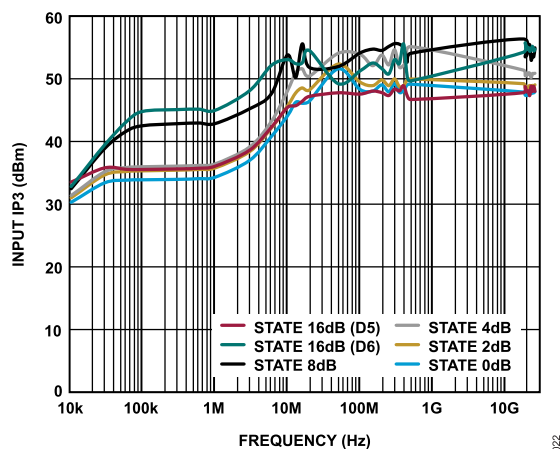


Figure 22. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5470 incorporates a 5-bit fixed attenuator array that offers an attenuation range of 46 dB in 2 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5470 has five digital control inputs, D2 (LSB) to D6 (MSB), to select the desired attenuation state in parallel mode, as shown in Figure 23. Internally, there are two 16 dB stages, and these stages can be controlled by the D5 and D6 pads.

POWER SUPPLY

The ADRF5470 requires a positive supply voltage applied to the V_{DD} pad and a negative supply voltage applied to the V_{SS} pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp-up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 k Ω resistor to limit the current flowing into the control pad.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Table 8. Truth Table

Digital Control Input ¹					Attenuation State (dB)
D6 ²	D5 ²	D4	D3	D2	
Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	High	2
Low	Low	Low	High	Low	4
Low	Low	High	Low	Low	8
Low	High	Low	Low	Low	16 (D5)
High	Low	Low	Low	Low	16 (D6)
High	High	High	High	High	46

¹ Any combination of the V_{CTRL} input states provides an attenuation equal to the sum of the bits selected.

² D5 and D6 both correspond to the 16 dB state. D5 has slightly better state accuracy at higher frequencies.

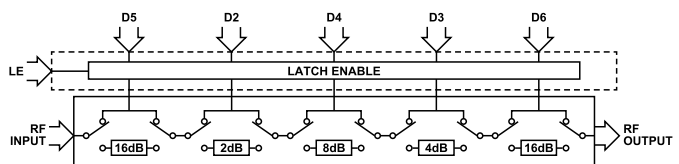


Figure 23. Simplified Circuit Diagram

Power-Up State

The ADRF5470 has an internal pull-up resistor (see Figure 5). The internal pull-up resistor sets the attenuator to the maximum attenuation state (46 dB) when the V_{DD} and V_{SS} voltages are applied if D2 to D6 are left floating.

Single-Supply Operation

The ADRF5470 can operate with a single positive supply voltage applied to the V_{DD} pad and the V_{SS} pad connected to ground. However, some performance difference can occur in the switching characteristics and large signal (see the Single-Supply Operation section within the Specifications section for further information).

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0 V. No DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω . Therefore, external matching components are not required.

The ADRF5470 supports bidirectional operation with equal power handling capability. Refer to the RF input power specifications in Table 1.

THEORY OF OPERATION

PARALLEL MODE INTERFACE

The ADRF5470 has five digital control inputs, D2 (LSB) to D6 (MSB), to select the desired attenuation state in parallel mode, as shown in [Table 8](#).

There are two modes of parallel operation: direct and latched.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pad high. To change the attenuation state, use the control voltage inputs (D2 to D6) directly. Direct parallel mode is for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pad must be kept low when changing the control voltage inputs (D2 to D6) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 5-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see [Figure 24](#) and the [Timing Specifications](#) section for additional information).

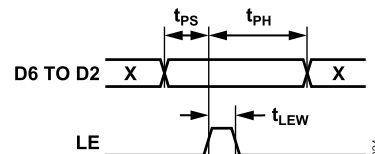


Figure 24. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

DIE ASSEMBLY

An assembly diagram of the ADRF5470 is shown in Figure 25.

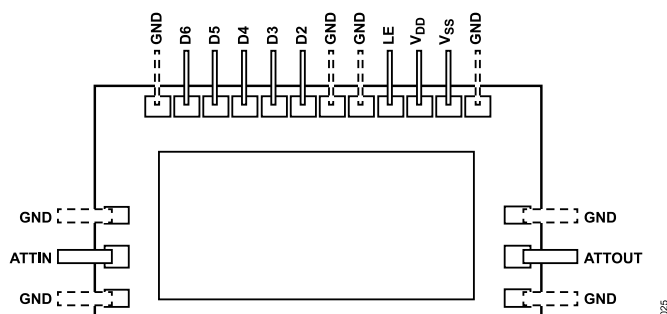


Figure 25. Die Assembly Diagram

The ADRF5470 is designed to have the optimum RF input and output impedance match with 3 mil $\times$ 0.5 mil gold ribbon wire and 3 mil loop height typical. The bonding diagrams are shown in Figure 26 and Figure 27. Alternatively, using multiple wire bonds with equivalent inductance yields similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad because the device is designed to match internally to the recommended ribbon bond. A spacing of 3 mils from the RF transmission line to the device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The DC pads are large enough to accommodate ribbon bonds, if preferred.

All bonds must be thermosonically bonded at a nominal stage temperature of 150°C, and a minimum amount of ultrasonic energy must be applied to achieve reliable bonds.

The device is metalized on the backside, and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

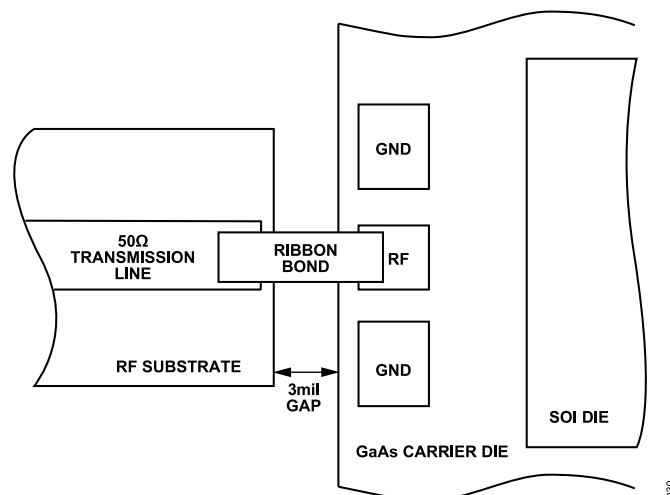


Figure 26. Bonding Diagram Top View

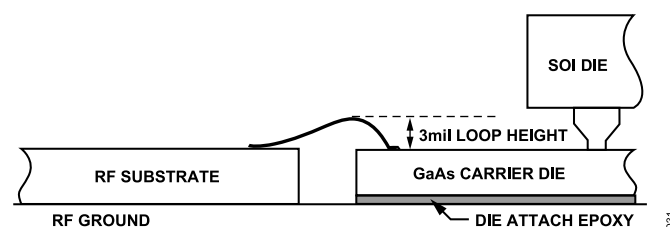


Figure 27. Bonding Diagram Side View

HANDLING, MOUNTING, AND EPOXY DIE ATTACH

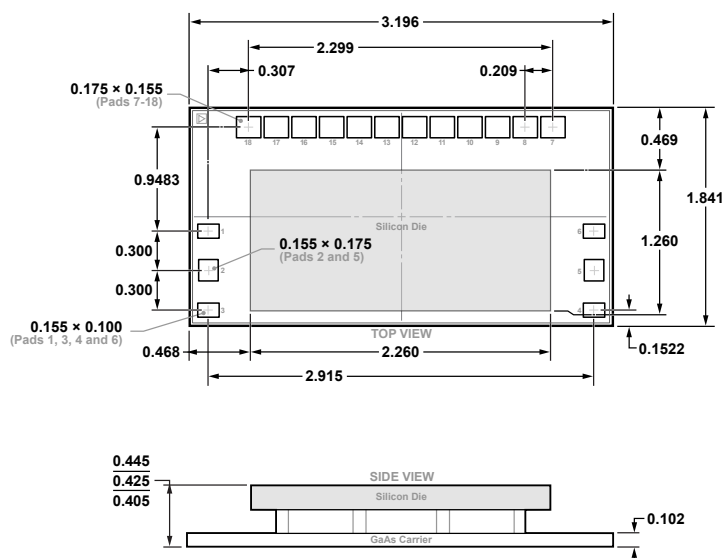
Keep devices in ESD protective sealed bags for shipment and store all bare die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs devices. However, for die on carrier devices, the use of a vacuum tool is recommended to avoid any damage on the device substrate. Handle these devices in a clean environment.

To attach the die with epoxy, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Set epoxy cure temperatures per the recommendations of the manufacturer and the maximum ratings of the device to minimize accumulated mechanical stress after assembly.

Because both dies are attached with solder joints, users must follow best practices for the thermomechanical design of their module assemblies. The temperature expansion coefficient of the substrate material must match the thermal expansion coefficient of the GaAs and silicon (Si) die. Do not allow warpage or other mechanical deformation on the substrate. Set the die attach process and the epoxy cure temperatures to lower the accumulated stress after assembly.

OUTLINE DIMENSIONS



**Figure 28. 18-Pad Die on Carrier [CHIP]
(C-18-2)**
Dimensions Shown in Millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5470BCZ	-40°C to +105°C	18-Pad Die on Carrier [CHIP]	Waffle Pack, 50	C-18-2
ADRF5470BCZ-GP	-40°C to +105°C	18-Pad Die on Carrier [CHIP]	Gel Pack, 50	C-18-2
ADRF5470BCZ-SX	-40°C to +105°C	18-Pad Die on Carrier [CHIP]	Waffle Pack, 2	C-18-2

¹ Z = RoHS Compliant Part.