# High Power T/R Switch with Limiter, 8 GHz to 12 GHz

## FEATURES

- High Power T/R Switch with Integrated Power Limiter on Rx
- Frequency range: 8 GHz to 12 GHz
- Reflective 50Ω design
- Low insertion loss:
  - Tx Path: 0.9 dB at 10 GHz
  - Rx Path: 1.3 dB at 10 GHz
- High Isolation
- High power handling ($T_{CASE}$=85°C)
  - Tx Input: Pulsed 40dBm, 100µs pulse width at 7% Duty Cycle
  - ANT Input: Pulsed 40dBm, 100µs pulse width at 7% Duty Cycle
- Limiter Output on Rx: 18 dBm leakage (TBC)
- High Linearity
  - Input P0.1dB at Tx: 40dBm
- Fast Switching and Recovery time
- Dual supply, no low frequency spurious
- Positive Control Interface: CMOS/LVTTL-compatible
- 20-lead, 3 mm × 3 mm LGA package
- Pin compatible with ADRF5144

## APPLICATIONS

- Electronic warfare
- Military radios, radars, and electronic counter measures
- GaN and PIN diode replacement

## FUNCTIONAL BLOCK DIAGRAM

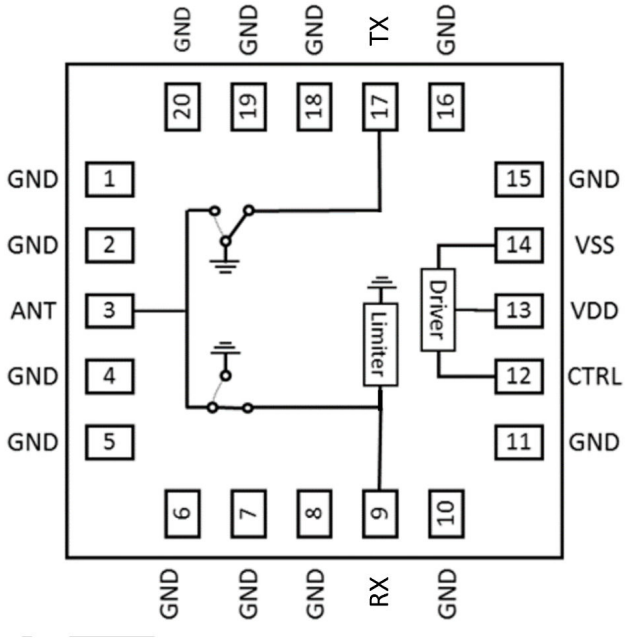


*Figure 1. Functional Diagram*

## GENERAL DESCRIPTION

The ADRF5141 is a reflective, single pole double-throw (SPDT) switch manufactured in the silicon process. It is used in transmit-receive (T/R) applications with an integrated power limiter at the receive side.

The ADRF5141 operates from 8 GHz to 12 GHz. The RX arm with the integrated power limiter has a limiting capability of 18 dBm output power (TBC) with a low insertion loss of 1.3 dB at 10GHz while the TX arm has an insertion loss of 0.9 dB at 10GHz.

The ADRF5141 draws a low current of 13 µA on the positive supply of +3.3 V and 360 µA on negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls. The ADRF5141 requires no additional driver circuitry, making it an ideal alternative to GaN and PIN diode-based switches.

The ADRF5141 comes in a 20-lead, 3.0 mm × 3.0 mm, RoHS-compliant, land grid array (LGA) package and can operate from −40°C to +85°C.

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## SPECIFICATIONS

$V_{DD}$ = 3.3 V, $V_{SS}$ = −3.3 V, $V_{CTL}$ = 0 V or 3.3 V, $T_{CASE}$ = 25°C, 50 Ω system, unless otherwise noted.

***Table 1.***

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | f | | 6 | | 12 | GHz |
| INSERTION LOSS | | | | | | |
| TX – ANT | | 8 GHz to 11 GHz | | 0.9 | | dB |
| | | 6 GHz to 12 GHz | | 1.1 | | dB |
| RX – ANT | | 8 GHz to 11 GHz | | 1.4 | | dB |
| | | 6 GHz to 12 GHz | | 1.7 | | dB |
| ISOLATION | | 6 GHz to 12 GHz | | | | |
| RX – ANT | | TX selected | | 55 | | dB |
| TX – RX | | TX selected | | 55 | | dB |
| TX – ANT | | RX selected | | 21 | | dB |
| RETURN LOSS | | | | | | |
| ANT | | 8 GHz to 11 GHz | | 13 | | dB |
| | | 6 GHz to 12 GHz | | 10 | | dB |
| TX | | 8 GHz to 11 GHz | | 16 | | dB |
| | | 6 GHz to 12 GHz | | 13 | | dB |
| RX | | 8 GHz to 11 GHz | | 19 | | dB |
| | | 6 GHz to 12 GHz | | 11 | | dB |
| SWITCHING CHARACTERISTICS | | | | | | |
| Rise and Fall Time | $t_{RISE}$, $t_{FALL}$ | 10% to 90% of RF output | | 15 | | ns |
| On and Off Time | $t_{ON}$, $t_{OFF}$ | 50% $V_{CTL}$ to 90% of RF output | | 50 | | ns |
| Settling Time | | | | | | |
| 0.1 dB | | 50% $V_{CTL}$ to 0.1 dB of final RF output | | 65 | | ns |
| LIMITER | | Pulsed 40dBm, 100µs pulse width at 15% Duty Cycle | | | | |
| Response Time | | f = 10 GHz | | <10 | | ns |
| Recovery Time | | f = 10 GHz | | <10 | | ns |
| RX Output Leakage Power | $P_{LIM}$ | | | 18(TBC) | | dBm |
| INPUT LINEARITY | | 8 GHz to 12 GHz | | | | |
| Tx Arm | | | | | | |
| 1dB Compression | P1dB | | | 42 | | dBm |
| 0.1dB Compression | P0.1dB | | | 40 | | dBm |
| Third-Order Intercept | IP3 | Two-tone input power = 20 dBm each tone, Δf = 1 MHz | | 55 | | dBm |
| Rx Arm | | | | | | |
| 1dB Compression | P1dB | | | 15 | | dBm |
| 0.1dB Compression | P0.1dB | | | 13 | | dBm |
| Third-Order Intercept | IP3 | Two-tone input power = 2 dBm each tone, Δf = 1 MHz | | 40 | | dBm |
| DIGITAL CONTROL INPUTS | | CTRL pin | | | | |
| Voltage | | | | | | |
| Low | $V_{INL}$ | | 0 | | 0.8 | V |
| High | $V_{INH}$ | | 1.2 | | 3.3 | V |
| Current | | | | | | |
| Low | $I_{INL}$ | | | <1 | | µA |
| High | $I_{INH}$ | | | <1 | | µA |
| SUPPLY CURRENT | | VDD, VSS pins | | | | |
| Positive Supply Current | $I_{DD}$ | | | 13 | | µA |

## SPECIFICATIONS

*Table 1.*

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Negative Supply Current | $I_{SS}$ | | | 360 | | µA |
| RECOMMENDED OPERATING CONDITONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | $V_{DD}$ | | 3.15 | | 3.45 | V |
| Negative | $V_{SS}$ | | −3.15 | | −3.45 | V |
| Digital Control Voltage | $V_{CTL}$ | | 0 | | $V_{DD}$ | V |
| RF Input Power[1] | $P_{IN}$ | f = 8 GHz to 12 GHz, $T_{CASE}$ = 85°C | | | | |
| At TX | | | | | | |
| CW | | | | | 36 | dBm |
| Pulsed[2] | | 7% duty cycle, 100us pulse width | | | 40 | dBm |
| Peak | | 2% duty cycle, 100ns pulse width | | | 43 | dBm |
| At ANT | | | | | | |
| CW | | | | | 33 | dBm |
| Pulsed[3] | | 7% duty cycle, 100us pulse width | | | 40 | dBm |
| Peak | | 2% duty cycle, 100ns pulse width | | | 40 | dBm |
| Case Temperature | $T_{CASE}$ | | −40 | | +105 | °C |

[1] For 105°C operation, the power handling degrades from the $T_{CASE}$ = 85°C specifications by 3 dB.

[2] For different pulsed conditions, please contact applications support.

[3] For different pulsed conditions, please contact applications support.

## ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

*Table 2.*

| Parameter | Rating |
|---|---|
| Positive Supply Voltage | -0.3 V to +3.6 V |
| Negative Supply Voltage | −3.6 V to +0.3 V |
| Digital Control Input | |
| Voltage | −0.3 V to $V_{DD}$ + 0.3 V |
| Current | 3mA |
| RF Input Power (f = 8 GHz to 12 GHz, $T_{CASE}$ = 85°C) | |
| At TX | |
| CW | 37 dBm |
| Peak | 41 dBm |
| Pulsed | 44 dBm |
| At ANT | |
| CW | 34 dBm |
| Peak | 41 dBm |
| Pulsed | 41 dBm |
| Temperature | |
| Junction, $T_J$ | 135°C |
| Storage | −65°C to +150°C |
| Reflow | 260°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case bottom (channel to package bottom) thermal resistance.

*Table 3. Thermal Resistance*

| Package Type | $\theta_{JC}$[1] | Unit |
|---|---|---|
| CC-20-9 | | |
| TX path | 45 | °C/W |
| RX path | 28.6 | °C/W |

[1] $\theta_{JC}$ was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 105°C.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

### ESD Ratings for the ADRF5141

*Table 4. ADRF5141, 20-Terminal LGA*

| Human Body Model (HBM) | Withstand Threshold (V) | Class |
|---|---|---|
| All Pins | 2k | 2 |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

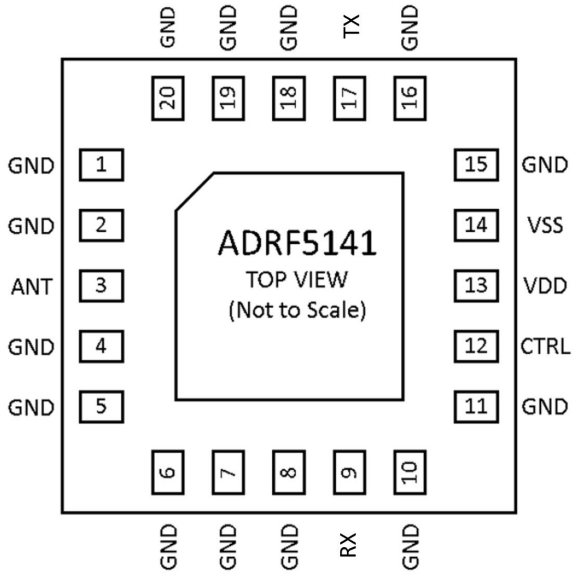


*Figure 2. Pin Configuration (Top View)*

*Table 5. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1,2,4,5,6,7,8,10, 11,15,16,18,19,20 | GND | Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB). |
| 3 | ANT | Antenna Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. |
| 9 | RX | Receiver Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. |
| 12 | CTRL | Control Input. |
| 13 | VDD | Positive Supply Voltage Pin. |
| 14 | VSS | Negative Supply Voltage Pin. |
| 17 | TX | Transmitter Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF/dc ground of the printed circuit board (PCB). |

## INTERFACE SCHEMATICS

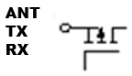


*Figure 3. RF Pin Interface Schematic*

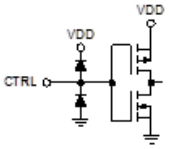


*Figure 4. Digital Pin Interface Schematic*

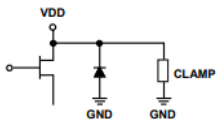


*Figure 5. VDD Pin Interface Schematic*

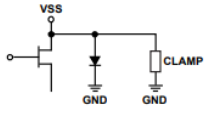


*Figure 6. VSS Pin Interface Schematic*

## TYPICAL PERFORMANCE CHARACTERISTICS

### INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD}$ = 3.3 V, $V_{SS}$ = -3.3V, $V_{CTL}$ = 0 V or $V_{DD}$ V, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted. Measured on the ADRF5141-EVALZ. See the Applications Information section for details on the evaluation board.

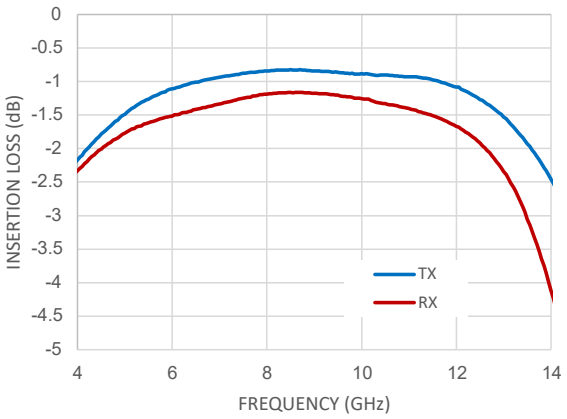


*Figure 7. Insertion Loss vs. Frequency at Room Temperature for TX and RX*

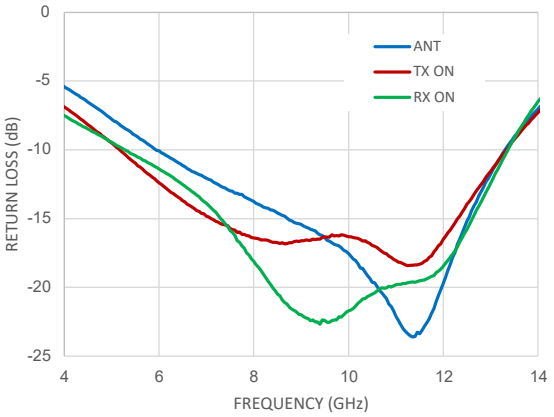


*Figure 8. Return Loss vs. Frequency*

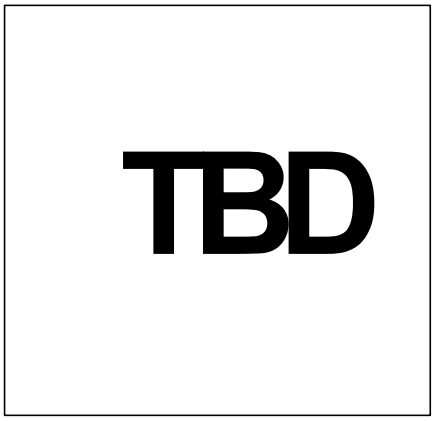


*Figure 9. Insertion Loss vs. Frequency over Temperature*

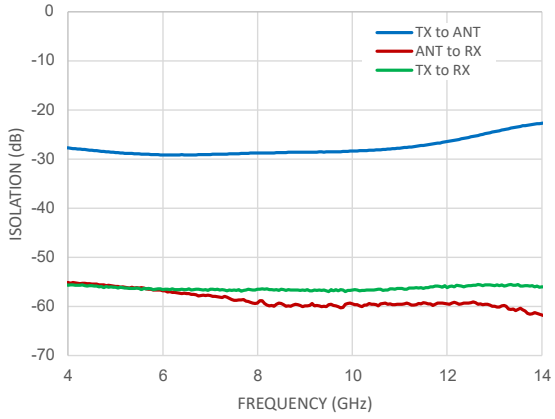


*Figure 10. Isolation vs. Frequency*

## TYPICAL PERFORMANCE CHARACTERISTICS

### INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD}$ = 3.3 V, $V_{SS}$ = -3.3 V, $V_{CTRL}$ = 0 V or $V_{DD}$ V, and $T_{CASE}$ = 25°C in a 50 Ω system, unless otherwise noted. All of the large signal performance parameters are measured on the ADRF5141-EVALZ.

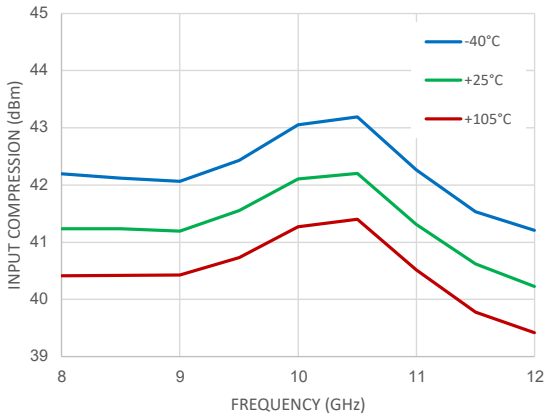


*Figure 11. Input 0.1dB Power Compression vs. Frequency over Temperature for TX*

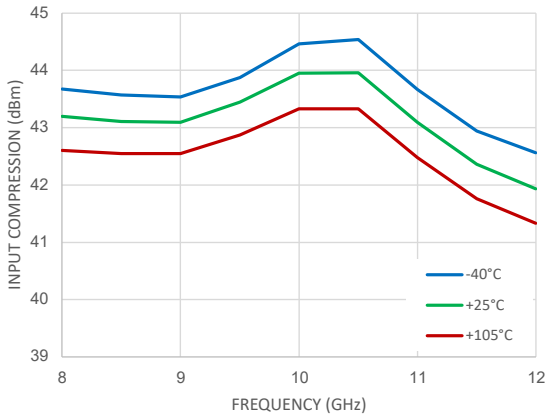


*Figure 14. Input 1dB Power Compression vs. Frequency over Temperature for TX*

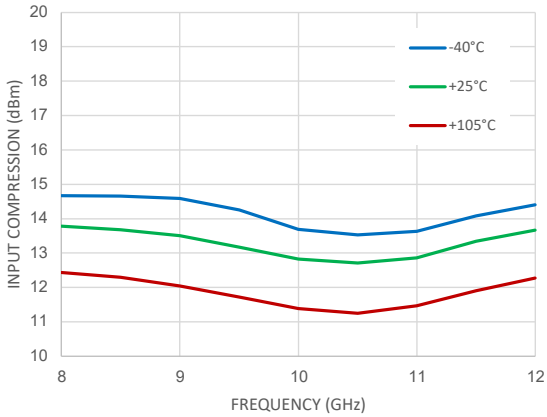


*Figure 12. Input 0.1dB Power Compression vs. Frequency over Temperature for RX*

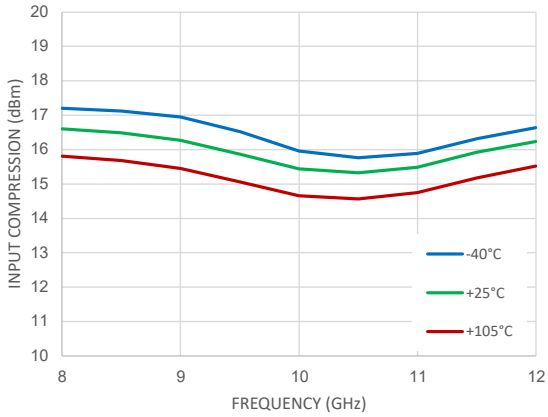


*Figure 15. Input 1dB Power Compression vs. Frequency over Temperature for RX*

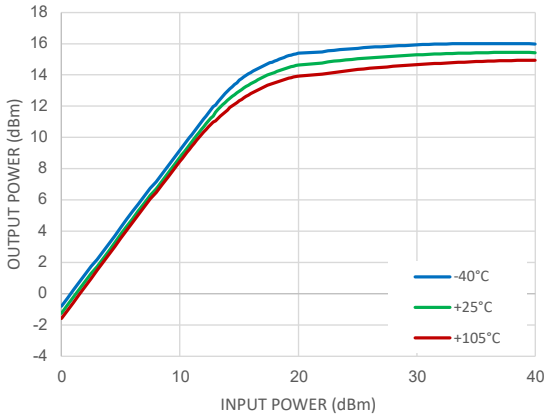


*Figure 13. Pin vs. Pout over Temperature at 10 GHz for RX*

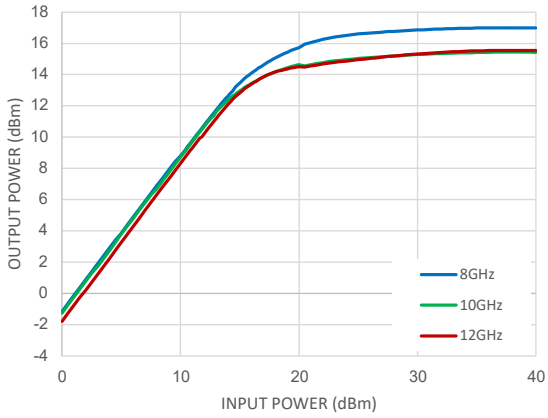


*Figure 16. Pin vs. Pout over Frequency at Room Temperature for RX*

## TYPICAL PERFORMANCE CHARACTERISTICS

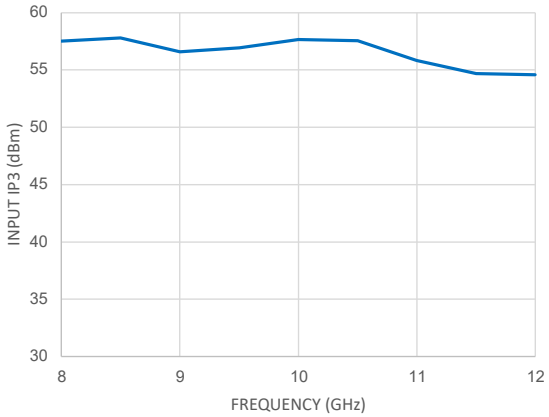


*Figure 17. Input IP3 vs. Frequency for TX*

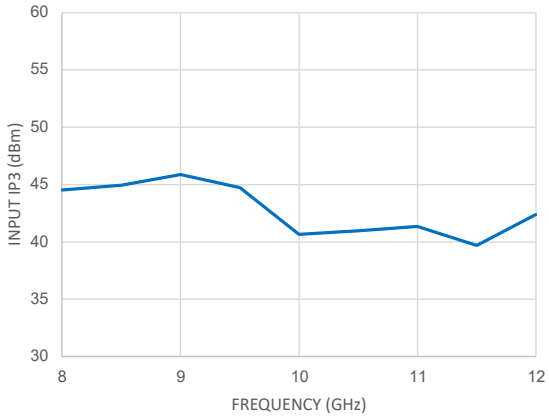


*Figure 18. Input IP3 vs. Frequency for RX*

## THEORY OF OPERATION

The ADRF5141 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features a single control input pin, CTRL that controls the state of RF paths, determining which RF port is in insertion loss state and which RF port is in isolation state (see Table 4).

### POWER SUPPLY

The ADRF5141 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect ground.
2. Power up $V_{DD}$ and $V_{SS}$. Power up $V_{SS}$ after $V_{DD}$ to avoid current transients on $V_{DD}$ during ramp-up.
3. Power up the digital control inputs. Power the digital control inputs before the $V_{DD}$ supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

### RF INPUT AND OUTPUT

All RF ports (ANT, RX, TX) are dc-coupled to 0V. When the RF line DC potential is at 0V, no dc blocking is required at the RF ports.

The RF ports are internally matched to 50Ω, hence, no external matching networks are required.

**Table 6. Control Voltage Truth Table**

*Table 6.*

| Digital Control Input | RF Paths | |
|---|---|---|
| **CTRL** | **TX to ANT** | **ANT to RX** |
| Low | Insertion loss (on) | Isolation (off) |
| High | Isolation (off) | Insertion loss (on) |

The antenna path can be switched to the receiver or transmitter arms having different insertion losses. When one arm is in conduction mode, the other arm is in isolation mode which is provided by a high insertion loss. The isolated port becomes a short reflective in this state.

## APPLICATION INFORMATION

### EVALUATION BOARD

The ADRF5141-EVALZ can withstand high power levels and temperatures at which the device operates.

The ADRF5141-EVALZ evaluation board is constructed with eight metal layers and dielectrics between each layer, as shown in Figure 19. Each metal layer has a 1 oz (1.3 mil) copper thickness, and the external layers are plated to 1.5 mil.

The top dielectric material is 8 mil Rogers RO4003C, which exhibits a low thermal coefficient, offering control over thermal rise of the board. The overall board thickness is around 62 mil.

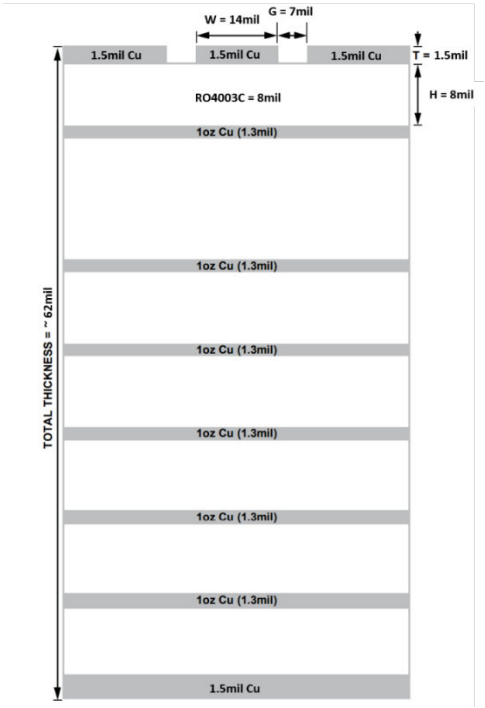


*Figure 19. A DRF5141-EVALZ Evaluation Board Cross Sectional View*

The top copper layer has all RF and DC traces. The other seven layers provide sufficient ground and help handle the thermal rise on the ADRF5141-EVALZ. RF transmission lines on the board are of a coplanar wave guide design with a width of 14 mil and ground spacing of 7 mil, making the characteristic impedance to be 50 Ω. The RF transmission lines are tapered at RF pin transition as shown in Figure 20. For optimal RF and thermal grounding, arrange as many plated through vias as possible around the transmission lines and under the exposed pad of the package.

The RF input and output ports (ANT, TX, and RX) are connected through 50 Ω transmission lines to the 2.92 mm launchers. These high frequency RF launchers are connected by contact and are not soldered to the board. The thru calibration line can calibrate out the board loss effects from the ADRF5141-EVALZ evaluation board measurements to determine the device performance at the pins of the IC.

To ensure maximum heat dissipation and to reduce thermal rise on the board, some application considerations are essential. The evaluation board must be attached to a metal support plate at the bottom of the board. The ADRF5141-EVALZ comes with this support plate attachment. Attach this evaluation board with its support plate to a heat sink using thermal grease during all high power operations.

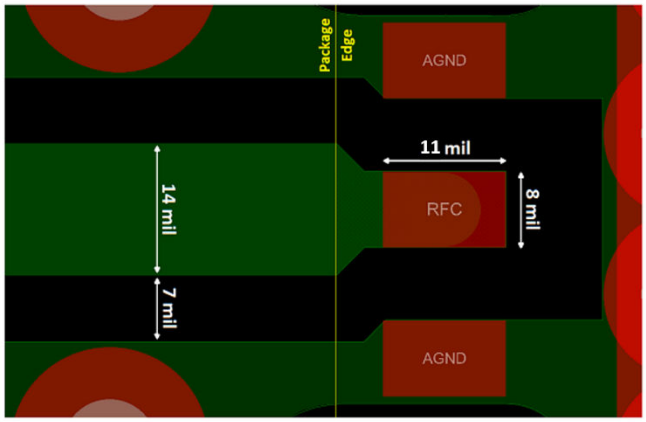


*Figure 20. RF Trasmission Lines*

### TYPICAL APPLICATION CIRCUIT

Two power supply ports are connected to the $V_{DD}$ and $V_{SS}$ test points, and the ground reference is connected to the GND test point. On the supply traces, $V_{DD}$ and $V_{SS}$, 100 pF, 10nF and 100nF bypassing capacitors are highly recommended.

One control port is connected to the CTRL test points. There are provisions for the resistor capacitor (RC) filter to eliminate dc-coupled noise, if needed by the application. The ADRF5141-EVALZ evaluation board schematic is shown in Figure 21.

The power limiter at the RX arm kicks in and limits the input power from ANT at the RX Output Leakage Power level (see Table 1). A typical configuration of ADRF5141 would be to connect an antenna at the ANT pin, a power amplifier (PA) at the TX pin and a low noise amplifier (LNA) to the RX pin. The integrated power limiter at the receiver arm provides a protection to the low noise amplifier input connected to the RX pin (see Figure 22).

## APPLICATION INFORMATION

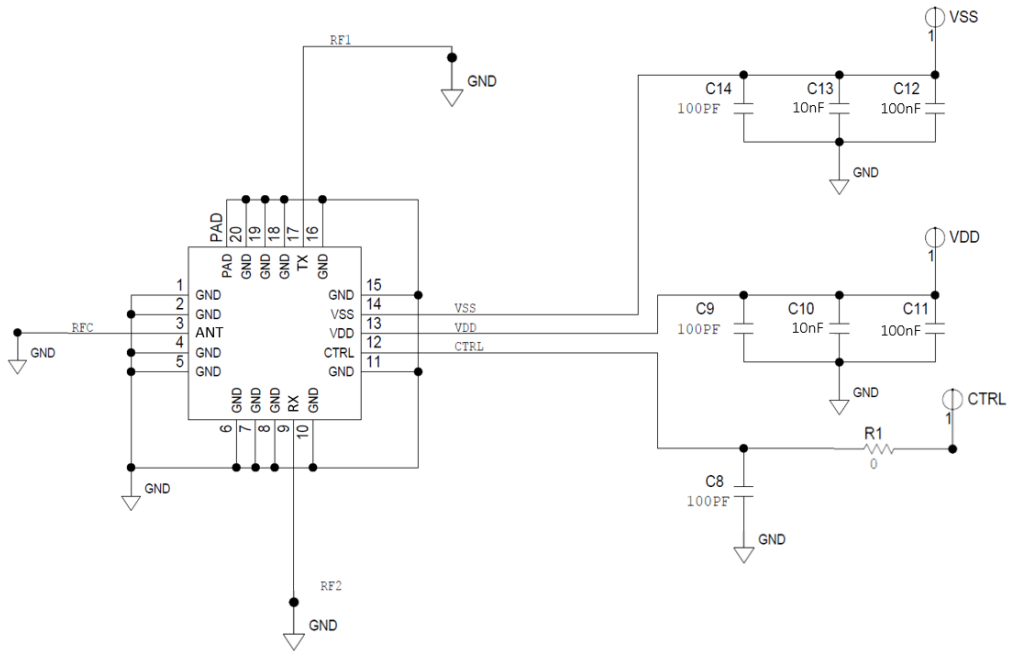


*Figure 21. Simplified Application Circuit*

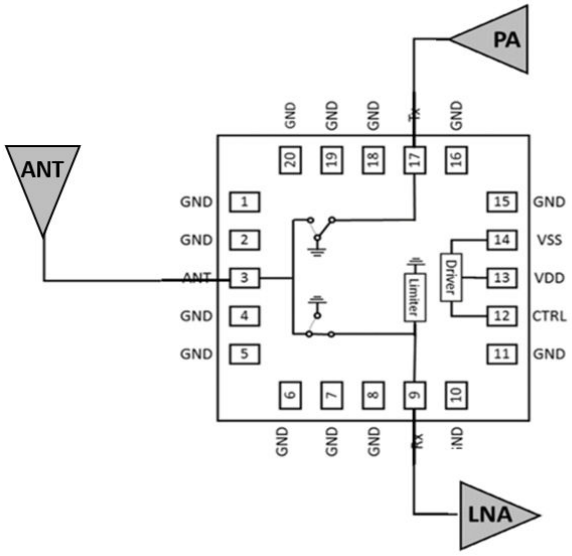


*Figure 22. Typical power amplifier, low noise amplifier, antenna configuration with ADRF5141 T/R switch*

## OUTLINE DIMENSIONS

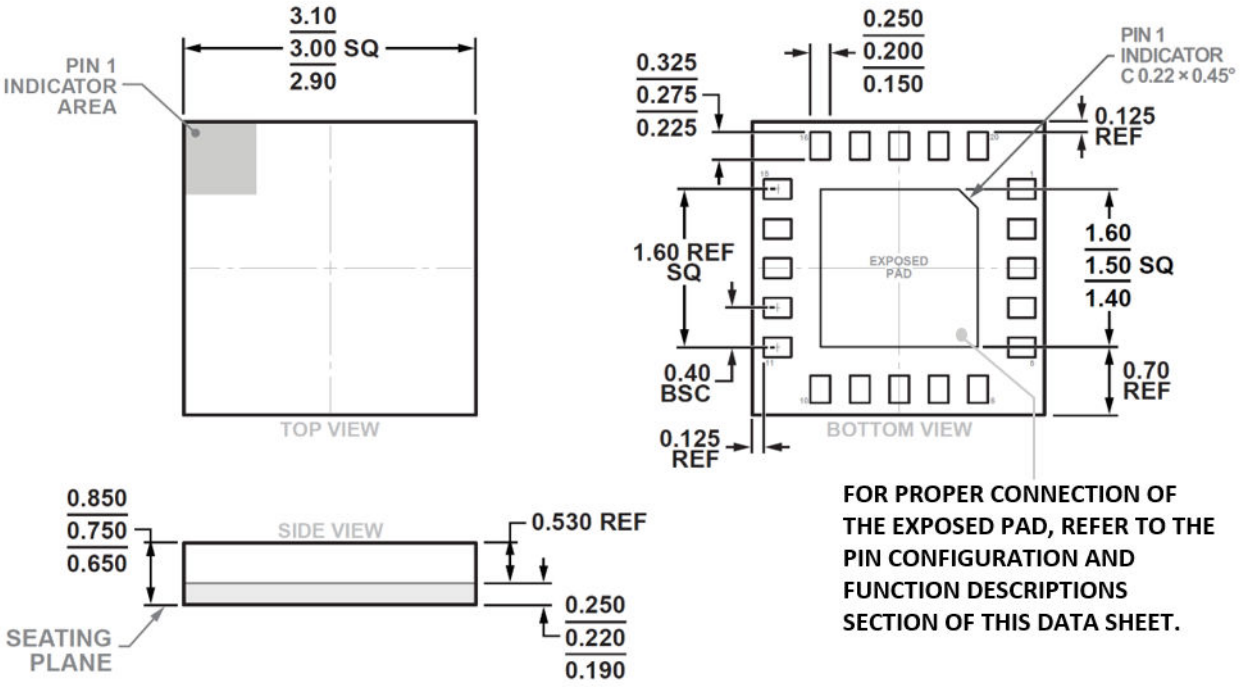


*Figure 23. Terminal Land Grid Array [LGA]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CC-20-9)*
*Dimensions shown in millimeters*