Nonreflective RF Path Selector SP3T with Bypass, 100MHz to 20GHz

FEATURES

- Wideband frequency range: 100MHz to 20GHz
- Nonreflective design with on-chip 50Ω terminations
- Low insertion loss
  - 0.7dB typical to 12GHz (external path)
  - 0.95dB typical to 20GHz (external path)
  - 1.15dB typical to 12GHz (through path)
  - 1.3dB typical to 20GHz (through path)
- High isolation
  - 50dB typical to 12GHz
  - 42dB typical to 20GHz
- High input linearity
  - P0.1dB: >33dBm typical
  - Input IP3: >58dBm typical
- High RF input power
  - 30dBm external paths
  - 18dBm terminated path
  - 30dBm hot switching
- ESD ratings
  - HBM: ±1.25kV for all pins
  - CDM: ±500V for all pins
- On time and off time (50% V_1 or V_2 to 10% to 90% of RF_{OUT}): 60ns
- 0.1dB RF settling time (50% V_1 or V_2 to 0.1dB of final RF_{OUT}): 110ns
- No low frequency spurs
- 30-terminal, 4mm × 3mm, LGA packaging

APPLICATIONS

- Test instrumentation
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

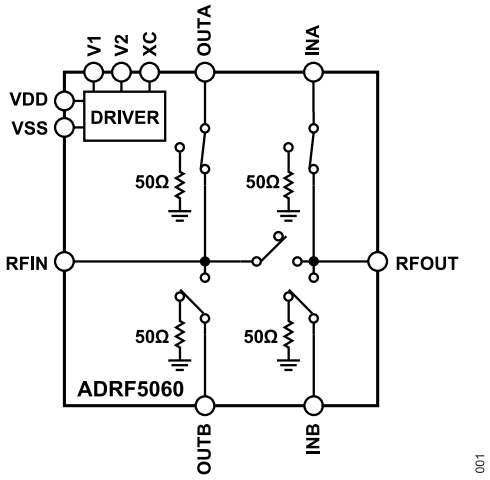

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5060 is a bidirectional, nonreflective RF path selector, SP3T with bypass manufactured in a silicon on insulator (SOI) process.

The ADRF5060 operates from 100MHz to 20GHz with an insertion loss of lower than 1.3dB on through path and isolation of higher than 42dB. The ADRF5060 has an RF input power handling capability of 33dBm external paths, 18dBm terminated path, and 30dBm hot switching at the RFIN or RFOUT port.

The ADRF5060 requires a dual-supply voltage of +3.3V and −3.3V. The device can also operate with a single positive supply voltage (VDD) pin applied while the negative supply pin (VSS) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated, see Figure 2.

The ADRF5060 employs complimentary metal-oxide semiconductor (CMOS)-/low-voltage, transistor to transistor logic (LVTTL) logic-compatible controls.

The ADRF5060 has three digital input pins (V1, V2, and XC) to control the digital switch states, including an all-off state and an additional control for cross port selection. See the Theory of Operation section for additional information.

The ADRF5060 comes in a 4 mm × 3 mm, LGA package.

TABLE OF CONTENTS

REVISION HISTORY

5/2025—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3V, VSS = −3.3V, V1 = 0 V or 3.3 V, V2 = 0V or 3.3V, T_A = 25°C, and it is a 50Ω system, unless otherwise noted. External Path A refers to the RFIN to OUTA and INA to RFOUT connected configuration, and External Path B refers to the RFIN to OUTB and INB to RFOUT connected configuration.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS						
External Path A or External Path B Selected		OUTA or OUTB to RFIN, and INA or INB to RFOUT				
		0.1GHz to 8GHz		0.65		dB
		8GHz to12 GHz		0.7		dB
		12GHz to 20GHz		0.95		dB
Through Path		RFIN to RFOUT				
		0.1GHz to 8GHz		1		dB
		8GHz to 12GHz		1.15		dB
		12GHz to 20GHz		1.3		dB
RETURN LOSS						
External Path A or External Path B Selected						
RFIN and RFOUT		0.1GHz to 12GHz		>20		dB
		12GHz to 20GHz		>18		dB
INA and INB and OUTA and OUTB (On)		0.1GHz to 20GHz		>20		dB
INA and INB and OUTA and OUTB (Off)		0.1GHz to 8GHz		>20		dB
		8GHz to 12GHz		15		dB
		12GHz to 20GHz		15		dB
Through Path						
RFIN to RFOUT		0.1GHz to 20GHz		>20		dB
ISOLATION						
External Path A or External Path B Selected (Adjacent RF Channels)		INA or INB to OUTA or OUTB				
		0.1GHz to 8GHz		55		dB
		8GHz to 12GHz		50		dB
		12GHz to 20GHz		42		dB
External Path A or External Path B Selected (Nonadjacent RF Channels)		OUTA or OUTB to RFIN, or INA or INB to RFOUT				
		0.1GHz to 8GHz		70		dB
		8GHz to 12GHz		65		dB
		12GHz to 20GHz		55		dB
Through Path		RFIN to OUTA and OUTB, or RFOUT to INA and INB				
		0.1GHz to 8GHz		60		dB
		8GHz to 12GHz		58		dB
		12GHz to 20GHz		51		dB
SWITCHING						
Rise and Fall Time	(t_{RISE}, t_{FALL})	90% to 10% of RF output (RF_{OUT})		20		ns
On Time and Off Time	(t_{ON}, t_{OFF})	50% control voltage (V_1 or V_2) to 10% to 90% of RF_{OUT}		60		ns
0.1dB RF Settling Time	$t_{SETTLING}$	50% V_1 or V_2 to 0.1dB of final RF_{OUT}		110		ns

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT LINEARITY						
0.1dB Power Compression	P0.1dB	f = 0.1GHz to 20GHz				
External Path A or External Path B Selected				>33		dBm
Through Path				>33		dBm
Third-Order Intercept	IP3	Two-tone input power (P_{IN}) = 15dBm continuous wave per tone, f = 0.1GHz to 20GHz, Δf = 1MHz				
External Path A or External Path B Selected				58		dBm
Through Path				57		dBm
SUPPLY CURRENT						
Positive	I_{DD}			160		µA
Negative	I_{SS}			500		µA
DIGITAL CONTROL INPUTS						
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.45	V
Current						
Low	I_{INL}	V1 and V2 pins		<1		µA
		XC pin		<1		µA
High	I_{INH}	V1 and V2 pins		<1		µA
		XC pin		33		µA
RECOMMENDED OPERATING CONDITIONS						
Positive Supply Voltage	V_{DD}		3.15		3.45	V
Negative Supply Voltage	V_{SS}		−3.45		−3.15	V
Digital Control Input Voltage	V_1 and V_2		0		V_{DD}	V
RF Input Power		f = 0.1GHz to 20GHz, T_{CASE} = 85°C, life time				
External Path A or External Path B Selected		RF signal is applied to RFIN or selected external RF path				
Average					30	dBm
Peak					33	dBm
Through Path		RF signal is applied to RFIN or RFOUT ports				
Average					30	dBm
Peak					33	dBm
Terminated Path		RF signal is applied to unselected (off) external RF paths				
Average					18	dBm
Hot Switching						
For RFIN and OUT		RF signal is applied to RFIN or RFOUT while switching			30	dBm
For INA, INB, OUTA, and OUTB		RF signal is applied to external RF path while switching			18	dBm
T_{CASE}			–40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	–0.3V to +3.6V
Negative	–3.6V to +0.3V
Digital Control Inputs[1]	
Voltage	–0.3V to V_{DD} + 0.3V
Current	3mA
RF Input Power (f[2] = 0.1GHz to 20GHz, T_{CASE} = 85°C[3])	
External Path A or External Path B Selected	
Average	31dBm
Peak[4]	33.5dBm
Through	
Average	31dBm
Peak	33.5dBm
Terminated	
Average	18.5dBm
Peak	21.5dBm
Hot Switching	31dBm
RF Power Under Unbiased Condition (V_{DD} = 0V, V_{SS} = 0V)	24dBm
Temperature	
Junction	135°C
Storage	–65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3dB.

4 Peak has ≤100ns pulse duration and 5% duty cycle.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-30-7		
Through Path	144	°C/W
Terminated Path	800	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 105°C.

POWER DERATING CURVE

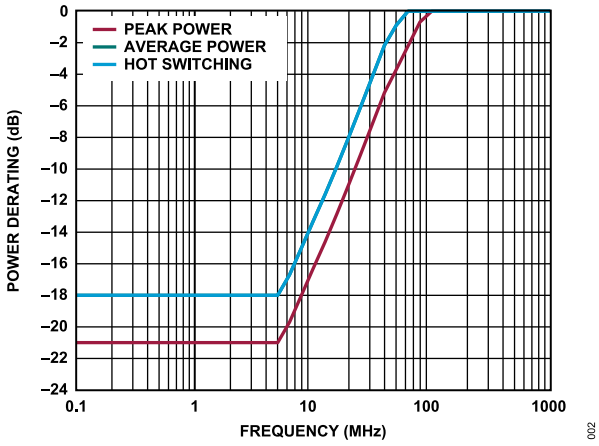

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5060

Table 4. ADRF5060, 30-Terminal LGA

ESD Model	Withstand Threshold	Class
HBM	±1.25kV for all pins	1C
CDM	±500V for all pins	C1

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

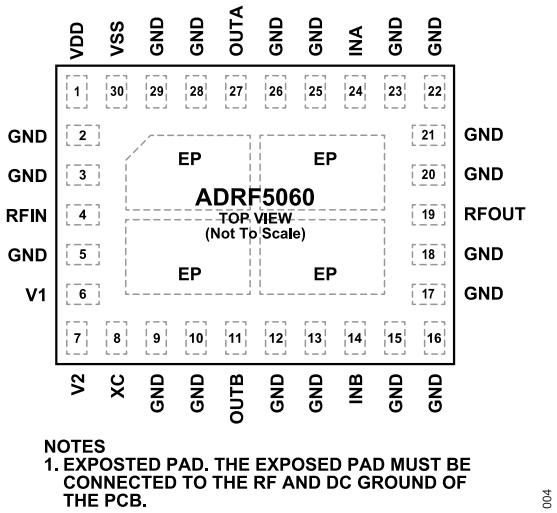

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Positive Supply Voltage. See Figure 6 for the interface schematic.
2, 3, 5, 9, 10, 12, 13, 15, 16, 17, 18, 20, 21, 22, 23, 25, 26, 28, 29	GND	Grounds.
4	RFIN	RF Input. The RFIN pin is DC-coupled to 0V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
6	V1	Digital Control Input 1. See Figure 5 for the interface schematic.
7	V2	Digital Control Input 2. See Figure 5 for the interface schematic.
8	XC	Digital Control Input for Cross Port Selection. See Figure 8 for the interface schematic and the Theory of Operation section for further details.
11	OUTB	Output Path for External Path B. The OUTB pin is DC-coupled to 0V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
14	INB	Input Path for External Path B. The INB pin is DC-coupled to 0V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 VDC. See Figure 4 for the interface schematic.
19	RFOUT	RF Output. The RFOUT pin is DC-coupled to 0V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 VDC. See Figure 4 for the interface schematic.
24	INA	Input Path for External Path A. The INA pin is DC-coupled to 0V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 VDC. See Figure 4 for the interface schematic.
27	OUTA	Output Path for External Path A. The OUTA pin is DC-coupled to 0V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
30	VSS	Negative Supply Voltage. See Figure 7 for the interface schematic.
	EP	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

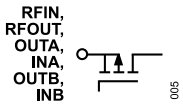

Figure 4. RFIN, RFOUT, OUTA, INA, OUTB, and INB Interface Schematic

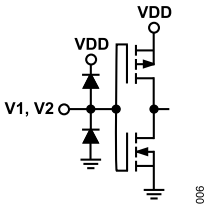

Figure 5. V1 and V2 Control Interface Schematic

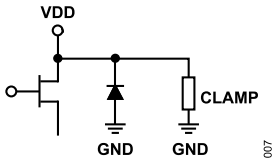

Figure 6. VDD Interface Schematic

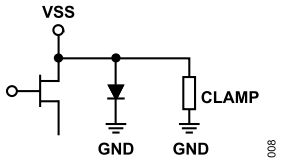

Figure 7. VSS Interface Schematic

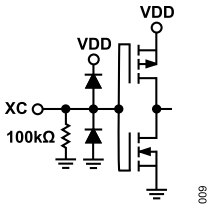

Figure 8. XC Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3V, VSS = −3.3V, V1, V2, and XC = 0V or 3.3V, and T_{CASE} = 25°C on a 50Ω system, unless otherwise noted.

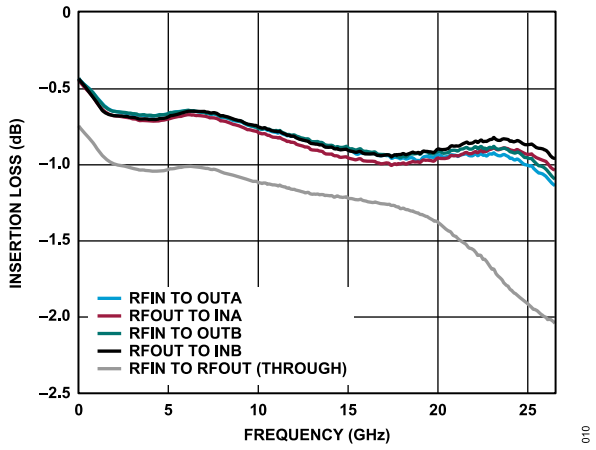

Figure 9. Insertion Loss vs. Frequency

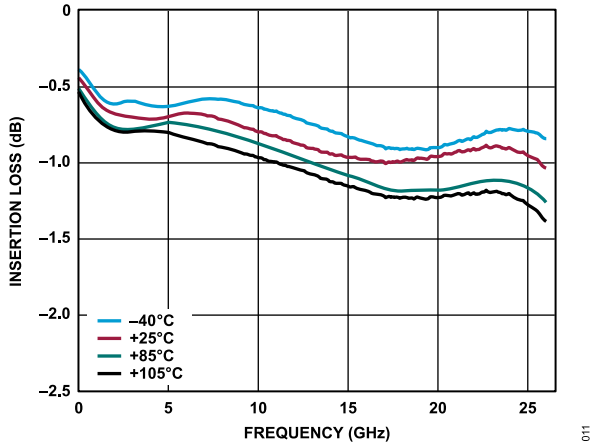

Figure 10. Insertion Loss for External Path A over Temperature vs. Frequency

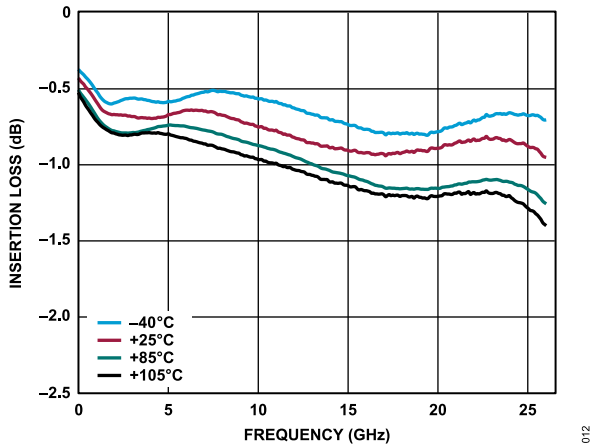

Figure 11. Insertion Loss for External Path B over Temperature vs. Frequency

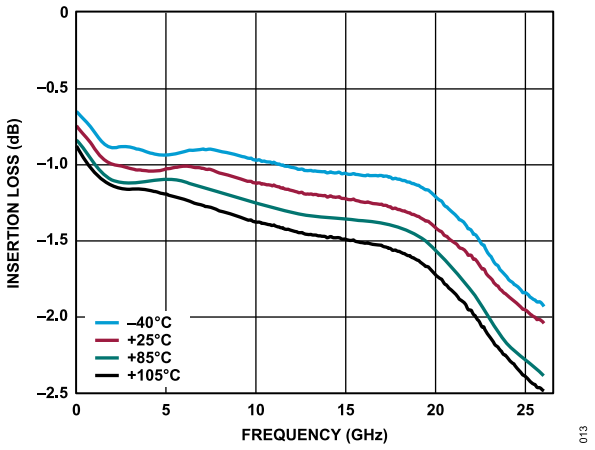

Figure 12. Insertion Loss of Through Path over Temperature vs. Frequency

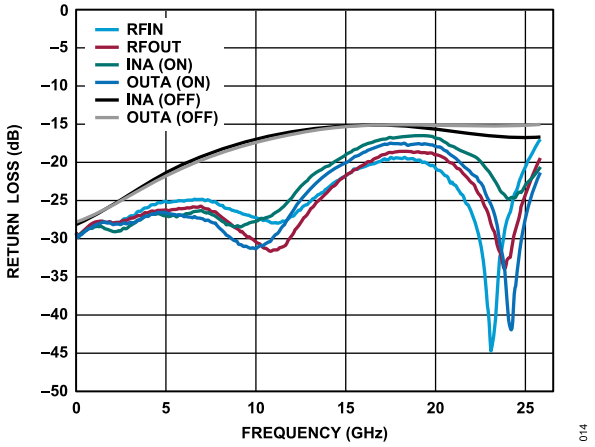

Figure 13. Return Loss for External Path A vs. Frequency

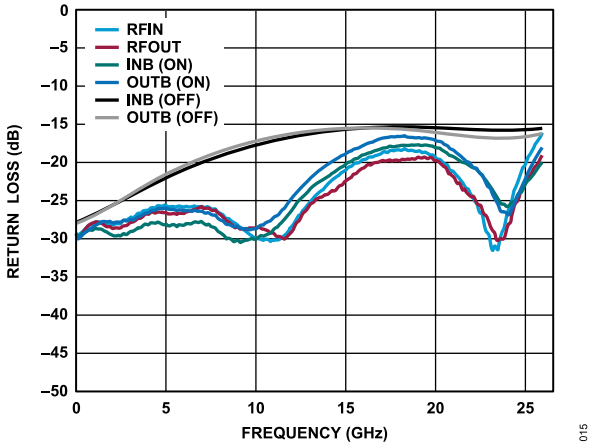

Figure 14. Return Loss for External Path B vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

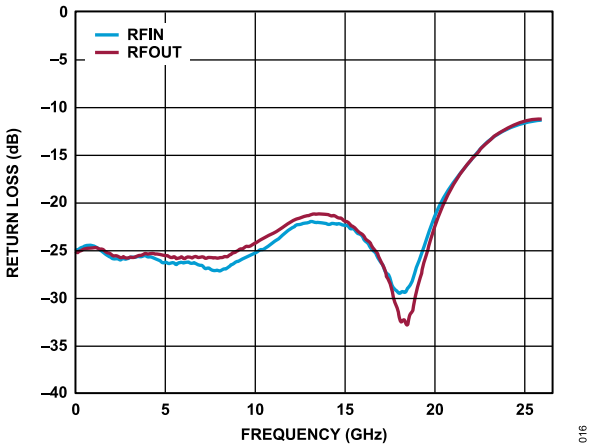

Figure 15. Return Loss for Through Path vs. Frequency

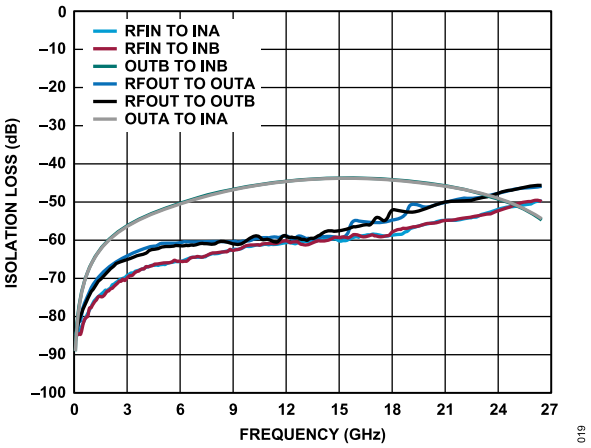

Figure 18. Isolation vs. Frequency, Through Path Selected

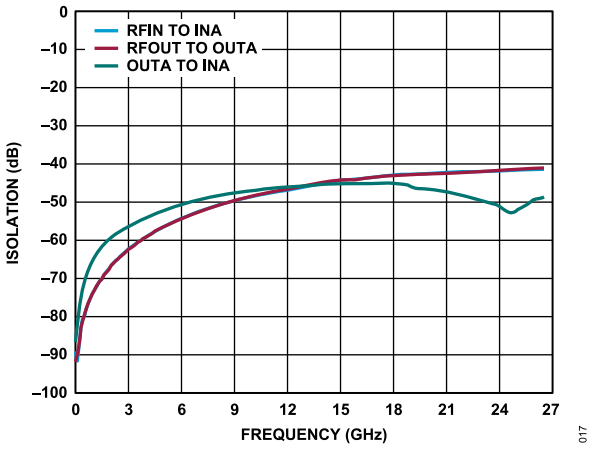

Figure 16. Isolation vs. Frequency, External Path A Selected

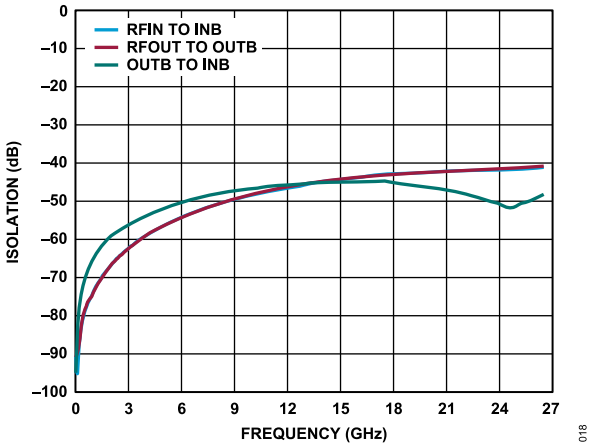

Figure 17. Isolation vs. Frequency, External Path B Selected

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3V, VSS = −3.3V, V1, V2, and XC = 0V or 3.3V, and T_{CASE} = 25°C on a 50Ω system, unless otherwise noted.

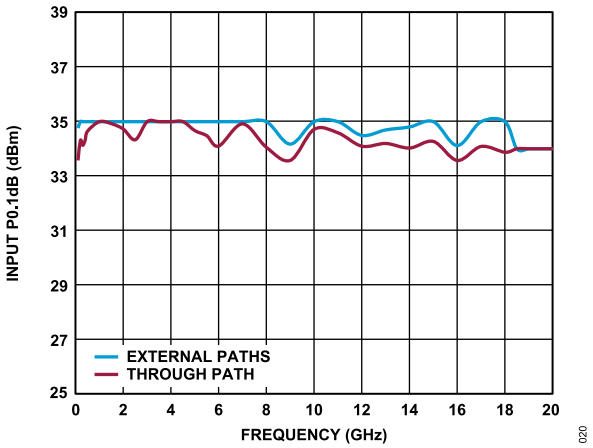

Figure 19. Input P0.1dB vs. Frequency

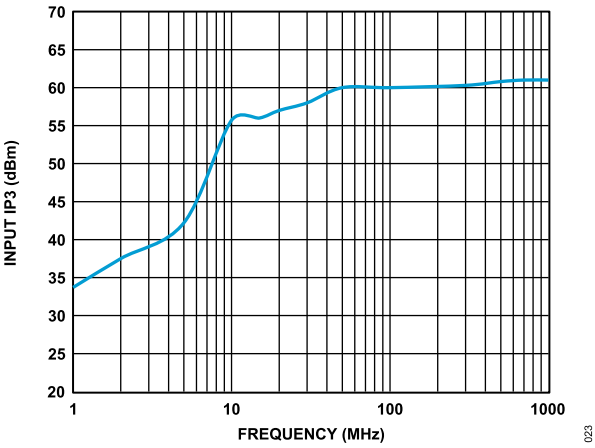

Figure 22. Input IP3 vs. Frequency, Low Frequency Detail

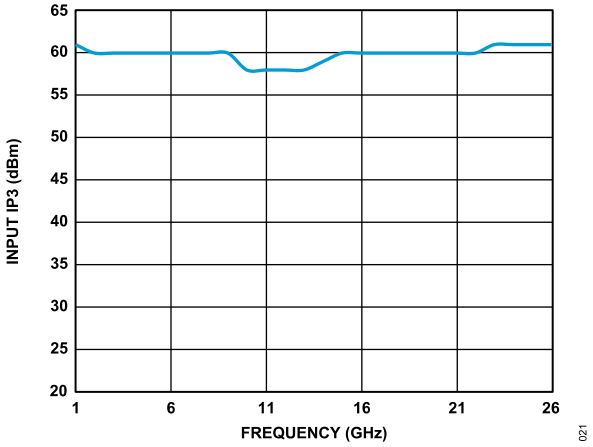

Figure 20. Input IP3 vs. Frequency

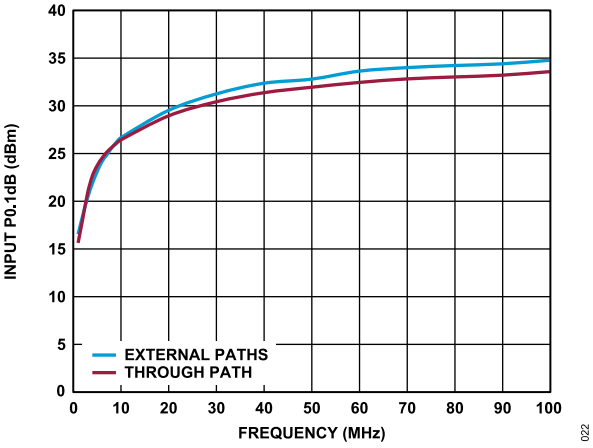

Figure 21. Input P0.1dB vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5060 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified CMOS-/LVTTL-compatible control interface. The driver features digital control input pins (XC, V1, and V2) that control the state of the external paths.

RF INPUT AND OUTPUT

All of the RF ports are DC-coupled to 0V, and no DC blocking capacitor is required at the RF ports if the RF line potential is equal to 0V.

The RF ports are internally matched to 50Ω; therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF path and the RFIN or RFOUT port. The through path conducts RF signal between the RFIN to RFOUT pins. The isolation path provides high loss between the insertion loss path and the unselected RF port that is terminated to an internal 50Ω resistor. The XC pin is used for the selection cross connections between External Path A or External Path B (see Table 6).

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFIN or RFOUT ports or the External A or External B paths.

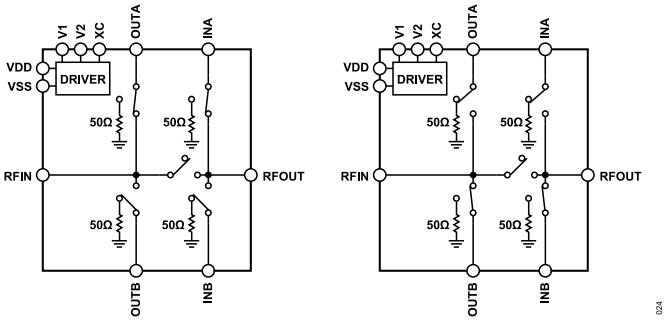

Figure 23. External Path A (Left) and External Path B (Right) Configuration

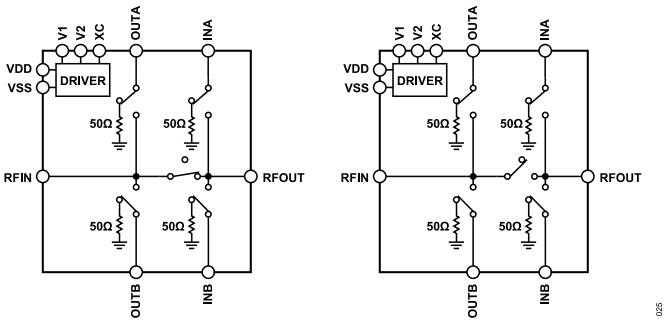

Figure 24. Through (Left) and All Off (Right) Configuration

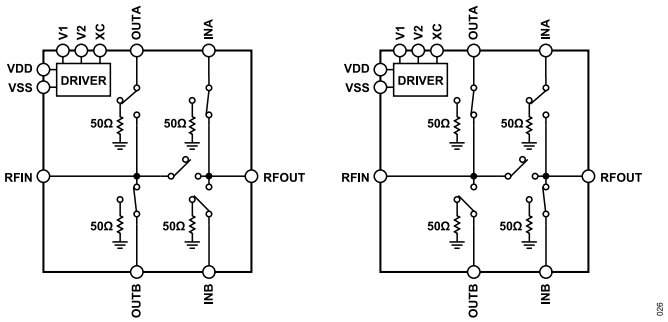

Figure 25. XC Configurations OUTB and INA (Left) or OUTA and INB (Right)

Table 6. Control Voltage Truth Table

RF Path Selection	XC	V1	V2
Through	Don't care	Low	Low
External Path B	Low	Low	High
External Path A	Low	High	Low
All Off (Isolation)	Don't care	High	High
Through	Don't care	Low	Low
Out A and In B	High	Low	High
Out B and In A	High	High	Low
All Off (Isolation)	Don't care	High	High

POWER SUPPLY

The ADRF5060 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Apply the digital control input (XC, V1, and V2). The relative order of the control inputs is not important. However, applying the digital control input pins before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. A series 1kΩ resistor can be used to limit the current flowing into the digital control input pins in such cases. If the digital control input pins are not driven to a valid logic state (that is, the controller output is in a high impedance state) after V_{DD} is powered up, it is recommended to use pull-up and power-down resistors.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

APPLICATIONS INFORMATION

The ADRF5060 has two power supply pins (VDD and VSS) and three control pins (V1, V2, and XC). Figure 26 shows the external components and connections for the supply and control pins. The VDD pin and the VSS pin are decoupled with a 100pF capacitor. The ADRF5060 pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins (RFIN, RFOUT, OUTA, OUTB, INA, and INB) when the RF lines are biased at a voltage different than 0V. Refer to the Pin Configuration and Function Descriptions section for further details.

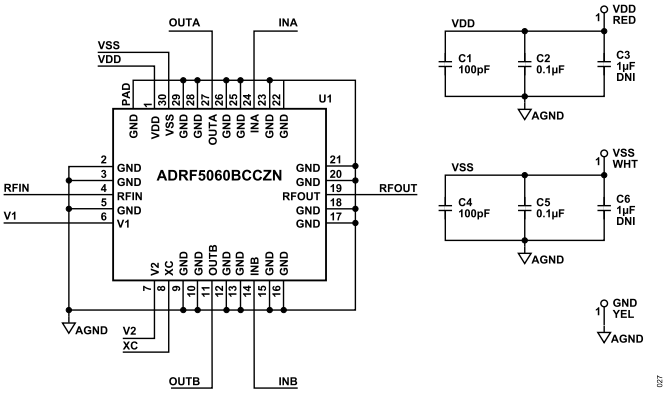

Figure 26. Recommended Schematic

APPLICATION EXAMPLES

Due to its unique RF port configuration, the ADRF5060 can be used to implement complex switching topologies with ease of use and minimum PCB area. Shown in the Gain Ranging section and the Transfer Switch section are two examples that can be realized using the ADRF5060. See Figure 27 for the gain ranging example and see Figure 29 for the transfer switch example.

Gain Ranging

The gain ranging configuration shown in Figure 27 allows the ADRF5060 to be configured as a path selector. See the signal path in Figure 28 and the digital control table in Table 7 for additional information. This configuration requires two digital control pins. Due to the wide bandwidth of the ADRF5060, amplifiers that operate at different frequencies can be implemented as well.

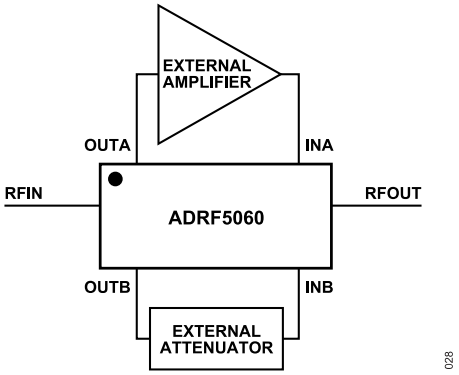

Figure 27. Gain Ranging Block Diagram

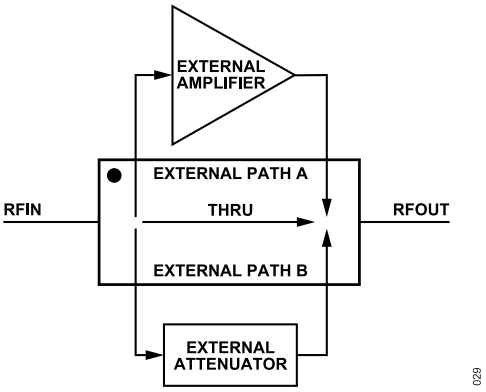

Figure 28. Gain Ranging Signal Path

Users can select an amplifier path, through path, or attenuator path (see Table 7), thus creating a repeatable and compact gain ranging module.

Table 7. Gain Ranging Application Truth Table

V1	V2	Switch State
High	Low	Amplifier selected
Low	High	Attenuator selected
Low	Low	Through path selected

APPLICATIONS INFORMATION

Transfer Switch

In the configuration shown in Figure 29, two ADRF5060 devices are positioned to create a transfer switch circuit. This circuit allows users to switch between configurations as shown in the signal path (see Figure 30) when the digital control pin is toggled between high and low (see Table 8).

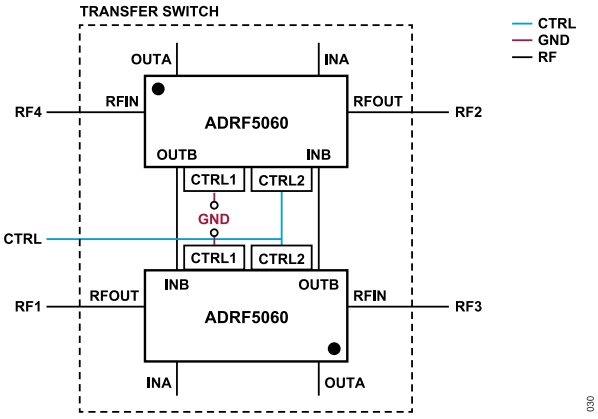

Figure 29. Transfer Switch Application Block Diagram

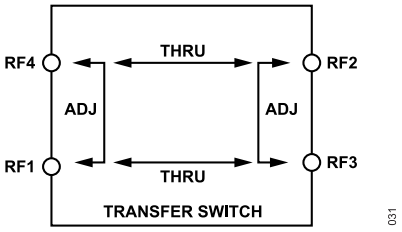

Figure 30. Transfer Switch Signal Path

Table 8. Transfer Switch Application Truth Table

CTRL[1]	Switch State[2]
Low	Through paths selected: RF4 to RF2 and RF1 to RF3
High	Adjacent (ADJ) paths selected: RF4 to RF1 and RF2 to RF3

[1] CTRL refers to the digital control pin (V2).

[2] RF1, RF2, RF3, and RF4 are defined in Figure 29 .

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with 50Ω characteristic impedance on the PCB. Figure 31 shows the referenced CPWG RF trace design for an RF substrate with 8mil thick Rogers RO4003 dielectric material. RF trace with 14mil width and 7mil clearance is recommended for 1.5mil finished copper thickness.

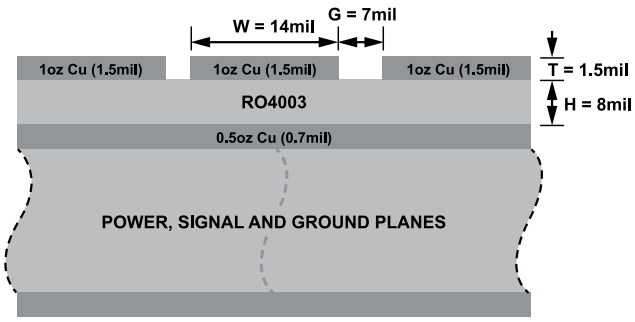

Figure 31. Example PCB Stack-Up

Figure 32 shows the routing of the RF traces, supply, and control signals from the ADRF5060. The ground planes are connected with as many filled, through vias as allowed for optimal RF and thermal performance. The primary thermal path for the ADRF5060 is the bottom side.

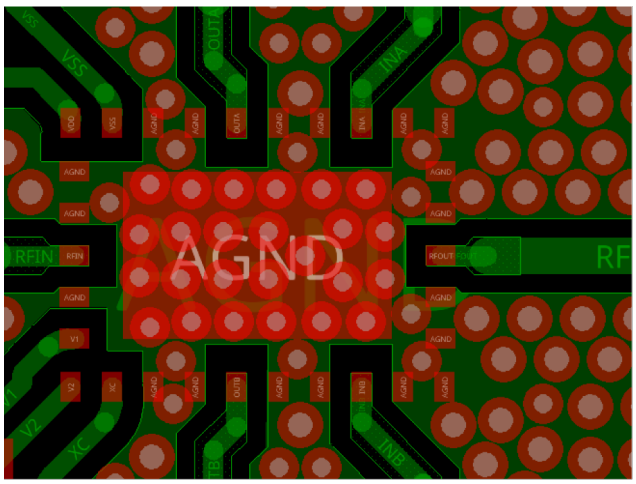

Figure 32. PCB Routings

Figure 33 shows the recommended layout from the device RF pins (RFIN, RFOUT, OUTA, OUTB, INA, and INB) to the 50Ω CPWG on the referenced stack-up. The PCB pads are drawn 1:1 to the device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width till the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

APPLICATIONS INFORMATION

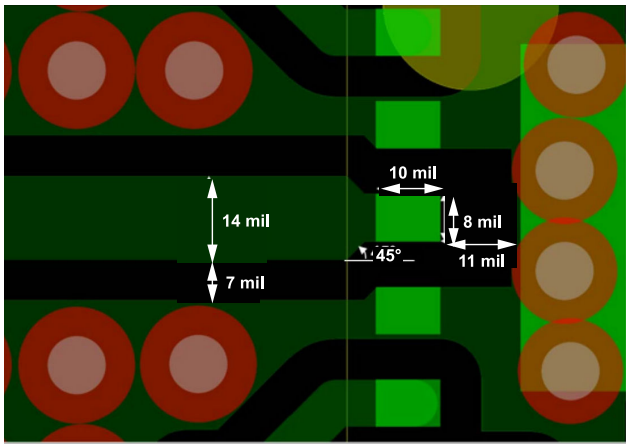

Figure 33. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support for further recommendations.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-30-7	LGA	30-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5060BCCZN	−40°C to +105°C	30-Terminal Land Grid Array [LGA]	Reel, 500	CC-30-7
ADRF5060BCCZN-R7	−40°C to +105°C	30-Terminal Land Grid Array [LGA]	Reel, 500	CC-30-7

[1] Z = RoHS Compliant Part.

Updated: August 24, 2023