ADRF5054

Silicon SP4T Switch, Reflective, 1 GHz to 60 GHz

FEATURES

- Ultrawideband frequency range: 1 GHz to 60 GHz
- Reflective design
- Low insertion loss
  - 2.1 dB typical up to 40 GHz
  - 3.0 dB typical up to 55 GHz
  - 3.2 dB typical up to 60 GHz
- High input linearity
  - P0.1dB: 24 dBm typical
  - IP3: 45 dBm typical
- High RF power handling
  - Through path: 24 dBm
  - Hot switching: 24 dBm
- RF switching time: 25 ns
- 0.1 dB RF settling time: TBD ns
- 24-terminal, 3 mm x 3 mm land grid array (LGA) package

APPLICATIONS

- Industrial Scanner
- Test instrumentation
- Cellular Infrastructure – mmWave 5G
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

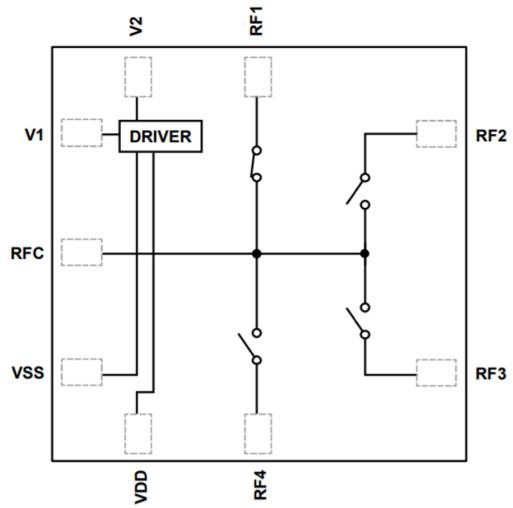

Figure 1.

GENERAL DESCRIPTION

The ADRF5054 is a reflective, single-pole four-throw (SP4T) switch manufactured in the silicon process.

This switch operates from 100 MHz to 60 GHz with better than 3.2 dB of insertion loss and 40 dB of isolation. The ADRF5054 has an RF input power handling capability of 24 dBm for the through path.

The ADRF5054 draws a low current of 150 µA on the positive supply of +3.3 V and 520 µA on negative supply of −3.3 V.

The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5054 RF ports are designed to match a characteristic impedance of 50 Ω.

The ADRF5054 comes in a 24-terminal, 3 mm × 3 mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

TABLE OF CONTENTS

SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, V1=V2 = 0 V or VDD, and case temperature (T_{CASE}) = 25°C for 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		60	GHz
INSERTION LOSS						
Between RFC and RFx (On)		1 GHz to 18 GHz		1.7		dB
		18 GHz to 40 GHz		2.2		dB
		40 GHz to 55 GHz		3.0		dB
		55 GHz to 60 GHz		3.2		dB
RETURN LOSS						
RFC		1 GHz to 18 GHz		19		dB
		18 GHz to 40 GHz		20		dB
		40 GHz to 55 GHz		22		dB
		55 GHz to 60 GHz		18		dB
RFx		1 GHz to 18 GHz		23		dB
		18 GHz to 40 GHz		15		dB
		40 GHz to 55 GHz		22		dB
		55 GHz to 60 GHz		20		dB
ISOLATION						
Between RFC and RFx (Off)		1 GHz to 18 GHz		50		dB
		18 GHz to 40 GHz		45		dB
		40 GHz to 55 GHz		34		dB
		55 GHz to 60 GHz		42		dB
Between RFx and RFx		1 GHz to 18 GHz		40		dB
		18 GHz to 40 GHz		45		dB
		40 GHz to 55 GHz		40		dB
		55 GHz to 60 GHz		43		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		5		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		25		ns
RF Settling Time						
0.1 dB		50% V_{CTRL} to 0.1 dB of final RF output		TBD		ns
INPUT LINEARITY[1]		2.75 GHz to 60 GHz				
0.1 dB Power Compression	P0.1dB			24		dBm
Third-Order Intercept	IP3	Two tone input power = TBD dBm each tone, Δf = 1 MHz		45		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			150		µA
Negative Supply Current	I_{SS}			520		µA
DIGITAL CONTROL INPUTS		V1, V2 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V

SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF Input Power[2]	P_{IN}	f = 2.75 GHz to 60 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to RFC or through connected RF1 and RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			24	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For power derating over frequency, see Figure 2 and Figure 3.

[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input Voltage[1]	
Voltage	−0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power[2] (f = 2.75 GHz to 67 GHz T_{CASE} = 85°C[3])	
Through Path	24.5 dBm
Hot Switching	24.5 dBm
RF Input Power Under Unbiased Condition[1] (V_{DD}, V_{SS} = 0 V)	TBD dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

[1] Over-voltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

[2] For power derating over frequency, see Figure 2.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-24-19, Through Path	370	°C/W

POWER DERATING CURVES

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for the ADRF5054

Table 4. ADRF5054, 24-Terminal LGA

Human Body Model (HBM)	Withstand Threshold (V)	Class
RFC, RF1 and RF2	500	1B
Supply and Digital Pins	1500	1C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

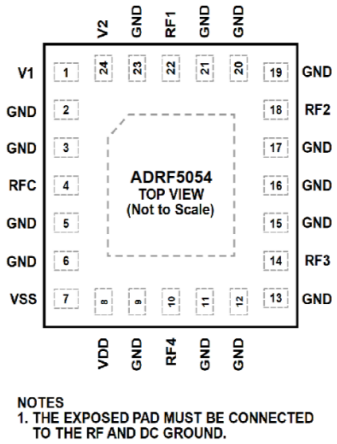

Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V1	Control Input 1. See Figure 6 for the interface schematic.
2, 3, 5, 6, 9, 11, 12, 13, 15, 16, 17, 19, 20, 21, 23	GND	Ground. These pins must be connected to the RF/dc ground of the PCB.
4	RFC	RF Common Port. This pin is dc-coupled to 0V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
7	VSS	Negative Supply Voltage. See Figure 7 for the interface schematic.
8	VDD	Positive Supply Voltage. See Figure 5 for the interface
10	RF4	RF Throw Port 4. This pin is dc-coupled to 0V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
14	RF3	RF Throw Port 3. This pin is dc-coupled to 0V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. This pin is dc-coupled to 0V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
12	RF1	RF Throw Port 1. This pin is dc-coupled to 0V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
24	V2	Control Input 2. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

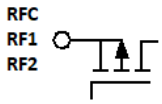

Figure 4. RFx Pins Interface Schematic

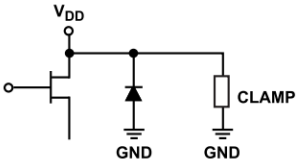

Figure 5. V_{DD} Interface Schematic

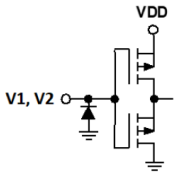

Figure 6. V1, V2 Pin Interface Schematic

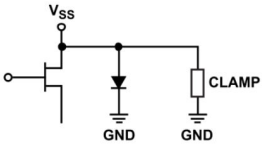

Figure 7. V_{SS} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = –3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF2. V_{CTL} is the digital control input voltage. Measured on the probe matrix board using ground signal ground (GSG) probes close to the RFC, RF1 and RF2 pins.

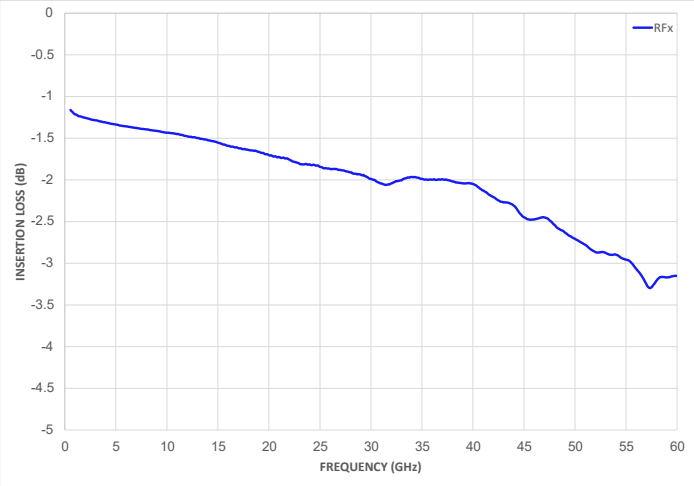

Figure 8. Insertion Loss vs. Frequency for RFx

Figure 10. Insertion Loss vs. Frequency over Temperature

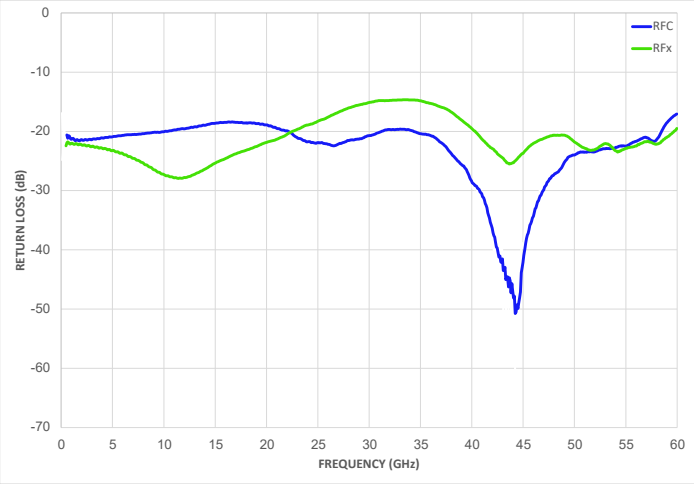

Figure 9. Return Loss vs. Frequency, RFC to RF1 On

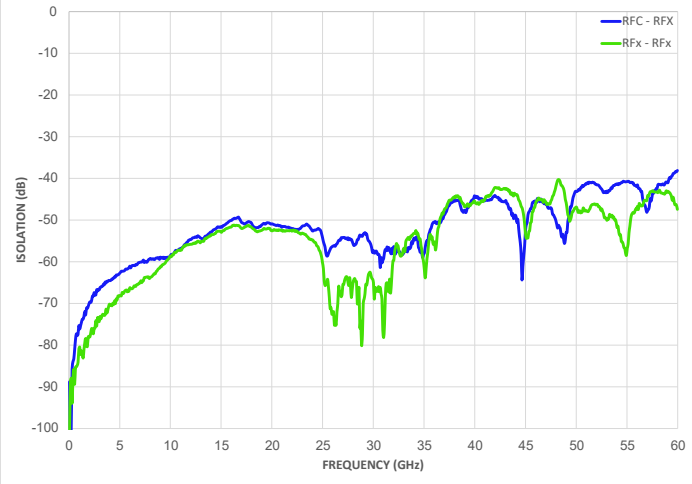

Figure 11. Isolation vs. Frequency, RFC to RFx and RFx to RFx

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF2. V_{CTL} is the digital control input voltage. All large signal performance parameters were measured on the evaluation board.

Figure 12. Input P0.1dB vs. Frequency over Various Temperatures

Figure 14. Input P0.1dB vs. Frequency over Various Temperatures(Low Frequency Detail)

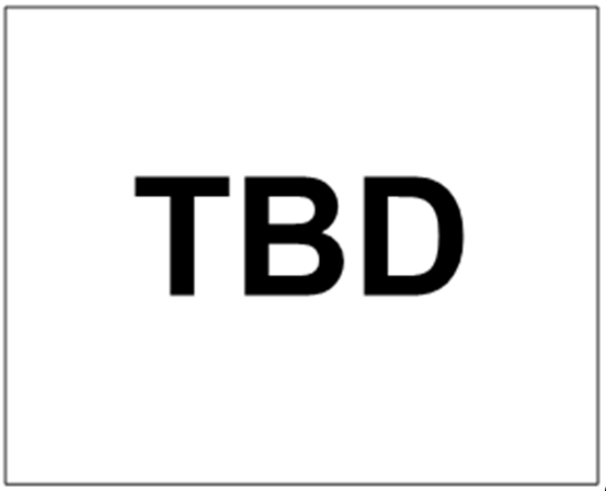

Figure 13. Input IP3 vs. Frequency over Various Temperatures

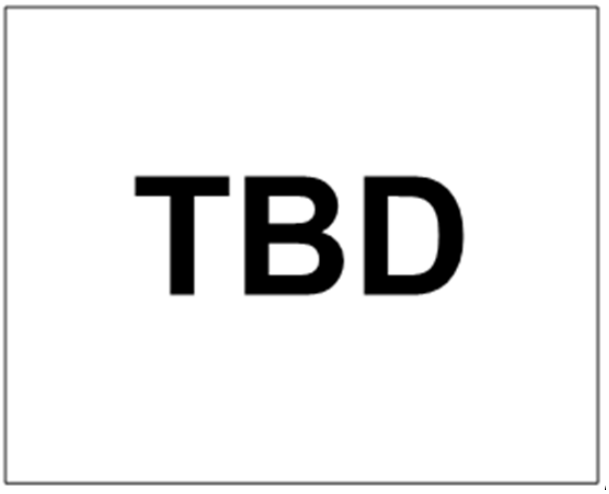

Figure 15. Input IP3 vs. Frequency over Various Temperatures(Low Frequency Detail)

THEORY OF OPERATION

The ADRF5054 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

All of the RF ports (RFC, RF1 to RF4) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. However, impedance matching on transmission lines can be used to improve insertion loss and return loss performance at high frequencies.

The ADRF5054 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS/LVTTL-compatible control interface. This driver features two digital control input pins, V1 and V2. The logic level applied to the control pins determine which RF port is in the insertion loss state and in the isolation state (see Table 6).

The unselected RF port of the ADRF5054 is reflective. The isolation path provides high isolation between the unselected port and the insertion loss path.

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltage Truth Table

Digital Control Inputs		RFx Paths			
V1	**V2**	**RFC to RF1**	**RFC to RF2**	**RFC to RF3**	**RFC to RF4**
Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

EVALUATION BOARD

The design of the ADRF5054-EVALZ serves as a layout recommendation for the ADRF5054 application.

The ADRF5054-EVALZ is a 4-layer evaluation board. The outer copper (Cu) layers are 0.5 oz (18 um) plated to 1.2 oz (42um) and are separated by dielectric materials. Figure 16 shows the ADRF5054-EVALZ stack up.

All RF traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers4003C, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength.

For additional information on application circuit design, see the ADRF5054-EVALZ user guide.

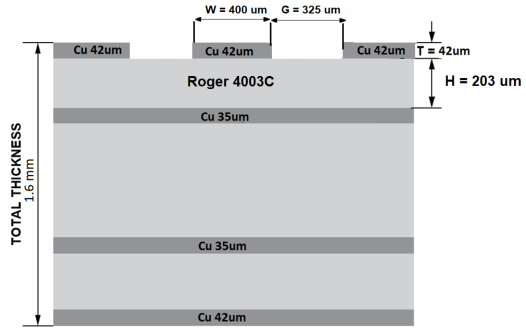

Figure 16. ADRF5054-EVALZ Stack Up

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with trace width of 400 um and ground clearance of 325 um to have a characteristic impedance of 50 Ω.

For optimal RF and thermal grounding, arrange as many plated through vias as possible around the transmission lines and under the exposed pad of the package.

PROBE MATRIX BOARD

The probe matrix board is a 4-layer evaluation board. Figure 17 shows the probe matrix board stack up, Probe matrix board used to perform measurements using GSG probes at the RFC, RF1, and RF2 pins. Probing reduces the reflections caused by mismatch arising from the connectors, cables, and board layout, which results in a more accurate measurement of the insertion loss and the return loss.

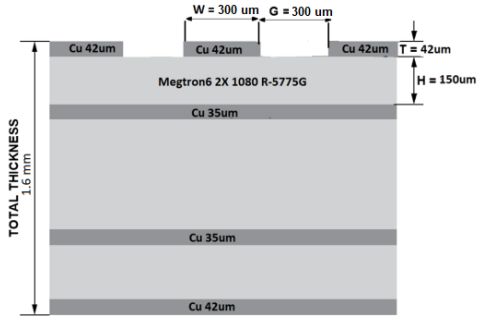

Figure 17. ADRF5054-PMB Stack Up

Small signal measurements in this data sheet are measured on the probe matrix board. Figure 18 shows the simplified application circuit for the probe matrix board.

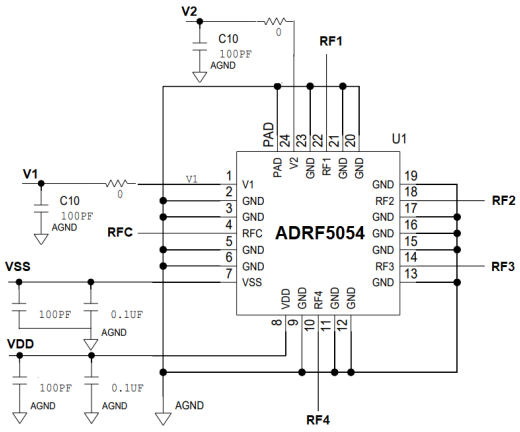

Figure 18. Application Circuit

The probe matrix board includes a through reflect line (TRL) calibration kit allowing board loss de-embedding. The actual board duplicates the same layout in matrix form, which allows multiple devices to assemble at once. Insertion loss and return loss and isolation measurements are made on the probe matrix board, whereas compression and IP3 measurements are made on the ADRF5054-EVALZ. Figure 19 shows the top view of the probe matrix board layout.

TBD

Figure 19. Probe Matrix Board, Top Layer

OUTLINE DIMENSIONS

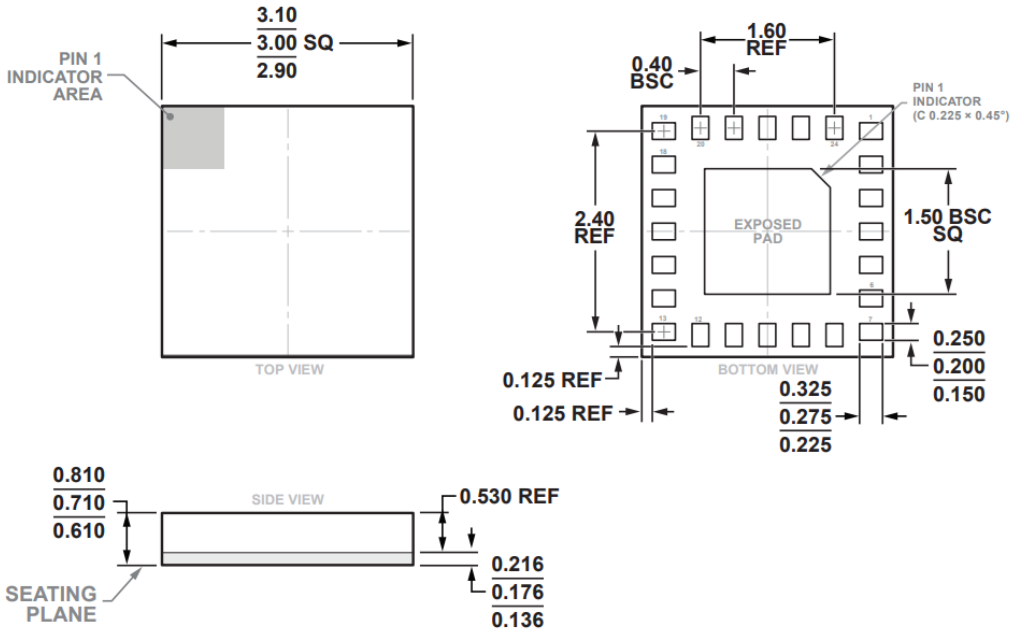

Figure 20. 24-Terminal LGA 3 mm × 3 mm (CC-24-19) Dimensions shown in millimeters