

Commercial Space
Product

Nonreflective, Silicon SP4T Switch, 100MHz to 20GHz

FEATURES

- ▶ Ultrawideband frequency range: 100MHz to 20GHz
- ▶ Nonreflective 50Ω design
- ▶ Low insertion loss
 - ▶ 0.9dB typical to 6GHz
 - ▶ 1.00dB typical to 12GHz
 - ▶ 1.20dB typical to 20GHz
- ▶ High isolation between RF_x and RF_x
 - ▶ 54dB typical to 6GHz
 - ▶ 50dB typical to 12GHz
 - ▶ 47dB typical to 20GHz
- ▶ High input linearity
 - ▶ P_{0.1dB}: 34dBm typical
 - ▶ IP₃: 55dBm typical
- ▶ High RF power handling
 - ▶ Through path: 33dBm up to 20GHz
 - ▶ Terminated path: 18dBm up to 20GHz
- ▶ Switching on and off time: 55ns
- ▶ 0.1dB settling time (50% V_{CTRL} to 0.1dB final RF_{OUT}): 80ns
- ▶ All off state control
- ▶ Logic select control
- ▶ Single-supply operation with derated power handling
- ▶ No low frequency spurs
- ▶ 24-terminal, 3mm × 3mm, land grid array (LGA) package

COMMERCIAL SPACE FEATURES

- ▶ Support aerospace applications
- ▶ Wafer diffusion lot traceability
- ▶ Radiation monitors
 - ▶ Total ionizing dose (TID)
 - ▶ Single event latch-up (SEL) benchmark characterization
 - ▶ Radiation lot acceptance test (RLAT) for production TID assurance
- ▶ Outgassing characterization

APPLICATIONS

- ▶ Test instrumentation
- ▶ Military radios, radars, and electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

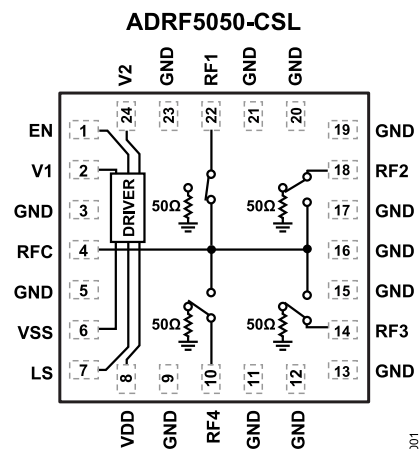


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5050-CSL is a nonreflective SP4T switch manufactured in a silicon on insulator (SOI) process. The ADRF5050-CSL operates from 100MHz to 20GHz with insertion loss less than 1.20dB and isolation higher than 47dB. The device has RF input power handling capability of 33dBm for through paths.

The ADRF5050-CSL operates with a dual-supply voltage +3.3V and -3.3V. The device can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. The single-supply operation condition requires lower operating power while the excellent small signal performance is maintained (see Table 2).

The ADRF5050-CSL employs complimentary metal-oxide semiconductor (CMOS)- and low voltage transistor to transistor logic (LVTTL)-compatible controls. The device has enable and logic select controls to feature all off state and port mirroring, respectively.

The ADRF5050-CSL comes in a 24-terminal, 3mm × 3mm, RoHS compliant, land grid array (LGA) package and can operate from -40°C to +105°C.

Additional application and technical information can be found in the [Commercial Space Products Program](#) brochure and the [ADRF5050](#) data sheet.

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REVISION HISTORY

10/2025—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 3.3V$, $V_{SS} = -3.3V$, Control Input 1 voltage (V_1) and Control Input 2 voltage (V_2) = 0V or V_{DD} , $T_{CASE} = 25^\circ C$, and a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4. V_{CTRL} is the voltages of the digital control inputs, V_1 and V_2 .

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		100		20,000	MHz
INSERTION LOSS						
Between RFC and RFx (On)		100MHz to 6GHz		0.9		dB
		6GHz to 12GHz		1.00		dB
		12GHz to 20GHz		1.20		dB
ISOLATION						
Between RFC and RFx		100MHz to 6GHz		56		dB
		6GHz to 12GHz		54		dB
		12GHz to 20GHz		47		dB
Between RFx and RFx		100MHz to 6GHz		54		dB
		6GHz to 12GHz		50		dB
		12GHz to 20GHz		47		dB
RETURN LOSS						
RFC (On)		100MHz to 6GHz		26		dB
		6GHz to 12GHz		22		dB
		12GHz to 20GHz		22		dB
RFx (On)		100MHz to 6GHz		24		dB
		6GHz to 12GHz		19		dB
		12GHz to 20GHz		18		dB
RFx (Off)		100MHz to 6GHz		20		dB
		6GHz to 12GHz		15		dB
		12GHz to 20GHz		12		dB
SWITCHING						
Rise and Fall Time	t_{RISE} , t_{FALL}	10% to 90% of RF output (RF_{OUT})		12		ns
On and Off Time	t_{ON} , t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		55		ns
0.1dB Settling Time		50% V_{CTRL} to 0.1dB of final RF_{OUT}		80		ns
INPUT LINEARITY ¹						
0.1dB Power Compression	P0.1dB	f = 100MHz to 20GHz		34		dBm
Third-Order Intercept	IP3	Two-tone input power = 15dBm each tone, f = 100MHz to 20GHz, $\Delta f = 1MHz$		55		dBm
Second-Order Intercept	IP2	Two-tone input power = 1 dBm each tone, f = 8GHz, $\Delta f = 1MHz$		110		dBm
VIDEO FEEDTHROUGH ²				30		mV p-p
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			155		μA
Negative Supply Current	I_{SS}			530		μA
DIGITAL CONTROL INPUTS		V1, V2, EN, and LS pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		μA
High	I_{INH}	V1 and V2 pins		3		μA
		LS and EN pins		40		μA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive	V_{DD}	$f = 100\text{MHz to } 20\text{GHz}$, $T_{CASE} = 85^{\circ}\text{C}^4$	3.15		3.45	V
Negative	V_{SS}		-3.45		-3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Power Handling ³						
Through Path					33	dBm
Terminated Path					18	dBm
Hot Switching					30	dBm
Case Temperature	T_{CASE}		-40		+105	$^{\circ}\text{C}$

¹ For input linearity performance over frequency, see the [ADRF5050](#) data sheet.

² Video feedthrough is the peak transient measured at the RF ports in a 50 Ω test setup, without an RF signal present while switching the control voltage.

³ For power derating over frequency, see [Figure 2](#).

⁴ For 105 $^{\circ}\text{C}$ operation, the power handling degrades from the $T_{CASE} = 85^{\circ}\text{C}$ specification by 3dB.

SINGLE-SUPPLY OPERATION SPECIFICATIONS

$V_{DD} = 3.3\text{V}$, $V_{SS} = 0\text{V}$, V_1 and $V_2 = 0\text{V}$ or V_{DD} , $T_{CASE} = 25^{\circ}\text{C}$, and 50 Ω system, unless otherwise noted.

The small signal and bias characteristics are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		20,000	MHz
SWITCHING						
Rise and Fall Time	t_{RISE} , t_{FALL}	10% to 90% of RF_{OUT}		85		ns
On and Off Time	t_{ON} , t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		175		ns
0.1dB Settling Time		50% V_{CTRL} to 0.1dB of final RF_{OUT}		200		ns
INPUT LINEARITY						
0.1dB Power Compression	P0.1dB	$f = 100\text{MHz to } 20\text{GHz}$		17		dBm
Third-Order Intercept	IP3	Two-tone input power = 15dBm each tone, $f = 100\text{MHz to } 20\text{GHz}$, $\Delta f = 1\text{MHz}$		42		dBm
Second-Order Intercept	IP2	Two-tone input power = 15dBm each tone, $f = 8\text{GHz}$, $\Delta f = 1\text{MHz}$		86		dBm
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling ^{1, 2}		$f = 100\text{MHz to } 20\text{GHz}$, $T_{CASE} = 85^{\circ}\text{C}$				
Through Path					22	dBm
Terminated Path					12	dBm
Hot Switching					19	dBm
Case Temperature	T_{CASE}		-40		+105	$^{\circ}\text{C}$

¹ For power derating over frequency, see [Figure 2](#).

² For 105 $^{\circ}\text{C}$ operation, the power handling degrades from the $T_{CASE} = 85^{\circ}\text{C}$ specification by 3dB.

SPECIFICATIONS

RADIATION TEST AND LIMIT SPECIFICATIONS

Electrical characteristics at $V_{DD} = 3.3V$, $V_{SS} = -3.3V$, and $T_A = 25^\circ C$, unless otherwise noted. TID testing to 100krads, and SEL occurs at $\leq 58MeV\text{-}cm^2/mg$ linear energy transfer (LET).

Table 3. Radiation Test and Limit Specifications

Parameter	Symbol	Min	Typ	Max	Unit
INSERTION LOSS					
RF1 and RF4					
Input Frequency (f_{IN}) = 0.65GHz			0.7		dB
$f_{IN} = 10GHz$			1.1		dB
$f_{IN} = 19GHz$			1.3		dB
RF2 and RF3					
$f_{IN} = 0.65GHz$			0.7		dB
$f_{IN} = 10GHz$			1.1		dB
$f_{IN} = 19GHz$			1.2		dB
ISOLATION					
RF1 and RF4					
$f_{IN} = 0.65GHz$			70		dB
$f_{IN} = 10GHz$			53		dB
$f_{IN} = 19GHz$			48		dB
RF2 and RF3					
$f_{IN} = 0.65GHz$			71		dB
$f_{IN} = 10GHz$			51		dB
$f_{IN} = 19GHz$			48		dB
DC CURRENTS					
Positive Supply Current	I_{DD}		230	260	μA
Negative Supply Current	I_{SS}		630	670	μA

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see [Table 1](#) and [Table 2](#).

Table 4. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
V_{DD}	-0.3V to +3.6V
V_{SS}	-3.6V to +0.3V
Digital Control Inputs ¹	
Voltage	-0.3V to $V_{DD} + 0.3V$
Current	3mA
RF Input Power ²	
Dual Supply ($V_{DD} = 3.3V$, $V_{SS} = -3.3V$, frequency = 100MHz to 20GHz, $T_{CASE} = 85^{\circ}C$ ³)	
Through Path	33.5dBm
Terminated Path	18.5dBm
Hot Switching (RFC)	30.5dBm
Single Supply ($V_{DD} = 3.3V$, $V_{SS} = 0V$, frequency = 100MHz to 20GHz, $T_{CASE} = 85^{\circ}C$)	
Through Path	22.5dBm
Terminated Path	12.5dBm
Hot Switching (RFC)	19.5dBm
Unbiased ($V_{DD} = 0V$, $V_{SS} = 0V$)	18dBm
Temperature	
Junction, T_J	135°C
Storage Range	-65°C to +150°C
Reflow	260°C

¹ Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

² For power derating over frequency, see [Figure 2](#).

³ For 105°C operation, the power handling degrades from the $T_{CASE} = 85^{\circ}C$ specification by 3dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC} ¹	Unit
CC-24-16		
Through Path	110	°C/W
Terminated Path	200	°C/W

¹ θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

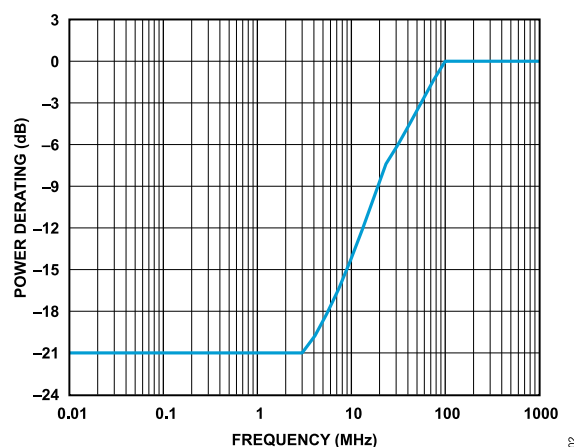


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE} = 85^{\circ}C$

OUTGAS TESTING

The criteria used for the acceptance and rejection of materials must be determined by the user and based on specific component and system requirements. Historically, a total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% have been used as screening levels for rejection of spacecraft materials.

Table 6. Outgas Testing

Specification (Tested per ASTM E595-15)	Value	Unit
Total Mass Lost	0.11	%
Collected Volatile Condensable Material	<0.01	%
Water Vapor Recovered	0.06	%

ABSOLUTE MAXIMUM RATINGS

RADIATION FEATURES

Table 7. Radiation Features

Specifications	Value	Unit
Maximum Total Dose Available (Dose Rate = 50rads to 300rads (Si)/sec) ¹	100	krads (Si)
No SEL Occurs at Effective LET ²	≤58	MeV-cm ² /mg

¹ Guaranteed by device and process characterization. Contact [Analog Devices, Inc., Support](#) for data available up to 100krads.

² Limits are characterized at initial qualification and after any design or process changes that may affect the SEL characteristics but are not production lot tested.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5050-CSL

Table 8. ADRF5050-CSL, 24-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx and RFC Pins	1000	1C
Supply and Control Pins	2000	2
CDM	500	C2A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

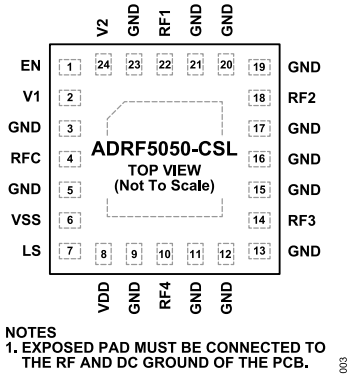


Figure 3. Pin Configuration (Top View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. See the truth table in the ADRF5050 data sheet and Figure 6 for the interface schematic.
2	V1	Control Input 1. See the truth table in the ADRF5050 data sheet and Figure 5 for the interface schematic.
3, 5, 9, 11 to 13, 15 to 17, 19 to 21, 23	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
4	RFC	RF Common Port. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
6	VSS	Negative Supply Voltage. See Figure 8 for the interface schematic.
7	LS	Logic Select Input. See the truth table in the ADRF5050 data sheet and Figure 6 for the interface schematic.
8	VDD	Positive Supply Voltage. See Figure 7 for the interface schematic.
10	RF4	RF Throw Port 4. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
14	RF3	RF Throw Port 3. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
22	RF1	RF Throw Port 1. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
24	V2	Control Input 2. See the truth table in the ADRF5050 data sheet and Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

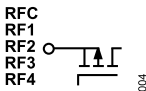


Figure 4. RFC and RF1 to RF4 Pin Interface Schematic

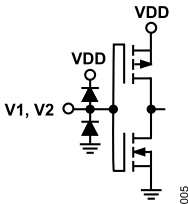


Figure 5. V1 and V2 Pin Interface Schematic

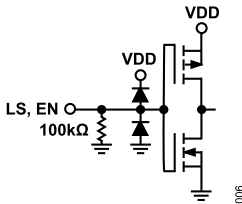


Figure 6. EN and LS Pin Interface Schematic

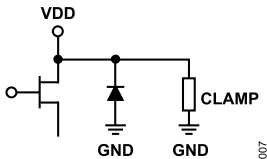


Figure 7. VDD Pin Interface Schematic

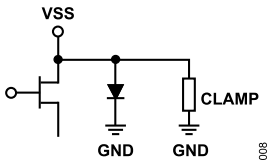


Figure 8. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

See the [ADRF5050](#) data sheet for a full set of typical performance characteristics plots.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-24-16	LGA	24-Terminal Land Grid Array Package

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5050BCCZ-CSL	-40°C to +105°C	24-Terminal Land Grid Array [LGA]	Tape, 500	CC-24-16
ADRF5050BCCZ-CSLR7	-40°C to +105°C	24-Terminal Land Grid Array [LGA]	Reel, 500	CC-24-16

¹ Z = RoHS Compliant Part.