

100 MHz to 20 GHz, Non-Reflective, Silicon SPDT Switch

FEATURES

- ▶ Wideband frequency range, 100 MHz to 20 GHz
- ▶ Non-reflective 50 Ω design
- ▶ Low insertion loss
 - ▶ 0.7 dB typical between 0.1 GHz to 6 GHz
 - ▶ 0.9 dB typical between 6 GHz to 12 GHz
 - ▶ 1.2 dB typical up to 20 GHz
- ▶ High isolation
 - ▶ 55 dB typical between 100 MHz to 6 GHz
 - ▶ 50 dB typical between 6 GHz to 12 GHz
 - ▶ 45 dB typical up to 20 GHz
- ▶ High input linearity
 - ▶ P0.1dB: >36 dBm typical
 - ▶ IP3: >60 dBm typical
- ▶ High RF power handling
 - ▶ Through path: 36 dBm peak/33 dBm average
 - ▶ Terminated path: 36 dBm peak/33 dBm average
 - ▶ Hot switching: 36 dBm peak/33 dBm average
- ▶ CMOS/LVTTL compatible
- ▶ No low-frequency spur; no negative voltage generator
- ▶ RF switching time: 70 ns
- ▶ RF settling time (0.1 dB): 95 ns
- ▶ Single-supply operation capability ($V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$)
- ▶ 20-terminal, 3 mm × 3 mm, LGA package
- ▶ Pin compatible with ADRF5022 and ADRF5026

APPLICATIONS

- ▶ Test instrumentation
- ▶ Military radios, radars, electronic counter measures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

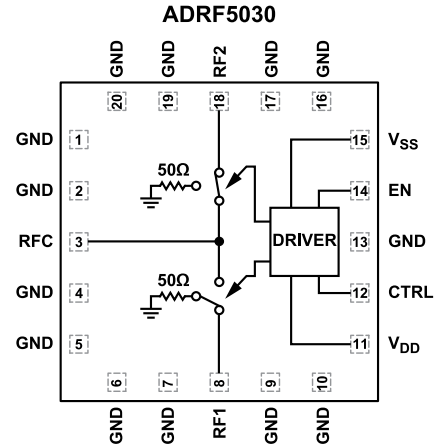


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5030 is a non-reflective, single-pole double-throw (SPDT) switch manufactured using the silicon on insulator (SOI) process. The ADRF5030 operates from 100 MHz to 20 GHz with insertion loss of lower than 1.2 dB and isolation of higher than 45 dB. The device has an RF input power handling capability of 33 dBm average/36 dBm peak for both RFC and RFx through paths, termination paths, and hot switching for both RFC and RFx ports. The ADRF5030 operates with dual-supply voltages of ±3.3 V. The ADRF5030 employs complementary metal-oxide semiconductor (CMOS) and low-voltage transistor to transistor logic (LVTTL)-compatible control.

The ADRF5030 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated. See Table 2 for more details.

The ADRF5030 is pin compatible with the ADRF5022 and ADRF5026, and also pin compatible with ADRF5031, a slow-switching, low cut-off version, which operates between 9 kHz to 20 GHz.

The ADRF5030 is packaged in a 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array (LGA). The ADRF5030 operates from -40°C to +105°C.

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REVISION HISTORY**7/2024—Revision 0: Initial Version**

SPECIFICATIONS

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted. RFx refers to RF1 or RF2.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS						
Between RFC and RFx (On)		0.1 GHz to 6 GHz		0.7		dB
		6 GHz to 12 GHz		0.9		dB
		12 GHz to 20 GHz		1.2		dB
RETURN LOSS						
RFC		0.1 GHz to 20 GHz		21		dB
RFx (On)		0.1 GHz to 20 GHz		19		dB
RFx (Off)		0.1 GHz to 20 GHz		17		dB
ISOLATION						
Between RFC to RFx and RFx to RFx		0.1 GHz to 6 GHz		55		dB
		6 GHz to 12 GHz		50		dB
		12 GHz to 20 GHz		45		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE} , t_{FALL}	10% to 90% of RF output		13		ns
On and Off Time	t_{ON} , t_{OFF}	50% V_{CTRL} to 90% of RF output		70		ns
Settling Time (0.1 dB)		50% V_{CTRL} to 0.1 dB of final RF output		95		ns
INPUT LINEARITY ¹		f = 0.1 GHz to 20 GHz				
Input Compression	P0.1dB			36		dBm
Third-Order Intercept	IP3	Two-tone input power = 14 dBm each tone, f = 0.1 GHz to 20 GHz, $\Delta f = 1\text{ MHz}$		60		dBm
Second-Order Intercept	IP2	Two-tone input power = 14 dBm each tone, f = 8 GHz. $\Delta f = 1\text{ MHz}$		110		dBm
VIDEO FEEDTHROUGH				45		mV _{p-p}
SUPPLY CURRENT		V_{DD} and V_{SS} pins				
Positive Supply Current	I_{DD}			150		μA
Negative Supply Current	I_{SS}			520		μA
DIGITAL CONTROL INPUTS		CTRL, EN pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		μA
High	I_{INH}			33		μA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		-3.45		-3.15	V
Digital Control Inputs Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power ^{2,3}	P_{IN}	f = 0.1 GHz to 20 GHz, $T_{CASE} = 85^\circ\text{C}$				
Through Path		RF signal is applied to RFC or through connected RFx (RF1/RF2).				
Average					33	dBm
Peak, Pulse ^{4,5}					36	dBm
Terminated Path		RF signal is applied to unselected RFx (terminated within internal resistor).				
Average					33	dBm
Peak, Pulse					36	dBm

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hot Switching Average Peak, Pulse		RF signal is applied to RFC or RFx while switching in between RF1/RF2.			33	dBm
Case Temperature	T _{CASE}		-40		+105	°C

- ¹ For input linearity performance over frequency, see Figure 12 to Figure 15.
- ² For power derating over frequency, see the Power Derating Curves section.
- ³ For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.
- ⁴ Peak: (<100 ns pulse duration, 5% duty cycle).
- ⁵ Pulse: (>100 ns pulse duration, 15% duty cycle).

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C for 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operational Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t _{RISE} , t _{FALL}	10% to 90% of RF output		110		ns
On and Off Time	t _{ON} , t _{OFF}	50% V _{CTRL} to 90% of RF output		230		ns
Settling Time (0.1 dB)		50% V _{CTRL} to 0.1 dB of final RF output		250		ns
INPUT LINEARITY		f = 0.1 GHz to 20 GHz				
Input Compression	P0.1dB			22		dBm
Third-Order Intercept	IP3	Two-tone input power = 6 dBm each tone, f = 0.1 GHz to 20 GHz, Δf = 1 MHz		52		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power Through Path	P _{IN}	f = 0.1 GHz to 20 GHz, T _{CASE} = 85°C RF signal is applied to RFC or through connected to RFx.			22	dBm
Terminated Path		RF signal is applied to unselected RFx (terminated within internal resistor).			22	dBm
Hot Switching		RF signal is applied to RFC or RFx while switching in between RF1/RF2.			22	dBm

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see [Table 1](#).

Table 3. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	-0.3 V to +3.6 V
Negative Supply Voltage	-3.6 V to +0.3 V
Digital Control Input ¹	
Voltage	-0.3 V to $V_{DD} + 0.3$ V
Current	3 mA
RF Input Power, Dual Supply ² ($V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, $f = 0.1$ GHz to 20 GHz, $T_{CASE} = 85^{\circ}\text{C}^3$)	
Through Path	
Average	34 dBm
Peak	37 dBm
Terminated Path	
Average	33.5 dBm
Peak	36.5 dBm
Hot Switching	
Average	34 dBm
Peak	37 dBm
RF Input Power, Single Supply ($V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $f = 0.1$ GHz to 20 GHz, $T_{CASE} = 85^{\circ}\text{C}^3$)	
Through Path	23 dBm
Terminated Path	23 dBm
Hot Switching	23 dBm
RF Input Power, Unbiased ($V_{DD}, V_{SS} = 0$ V)	
Average	31 dBm
Peak ⁴	37 dBm
Temperature	
Junction, T_J	135°C
Storage Range	-65°C to +150°C
Reflow	260°C

¹ Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

² For power derating over frequency, see [Figure 2](#).

³ For 105°C operation, the power handling degrades from the $T_{CASE} = 85^{\circ}\text{C}$ specification by 3 dB for dual supply.

⁴ Peak: (≤ 100 ns pulse duration, 5% duty cycle)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction-to-case bottom (channel-to-package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}^1	Unit
CC-20-21, Through Path	93	°C/W
CC-20-21, Terminated Path	25	°C/W

¹ θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

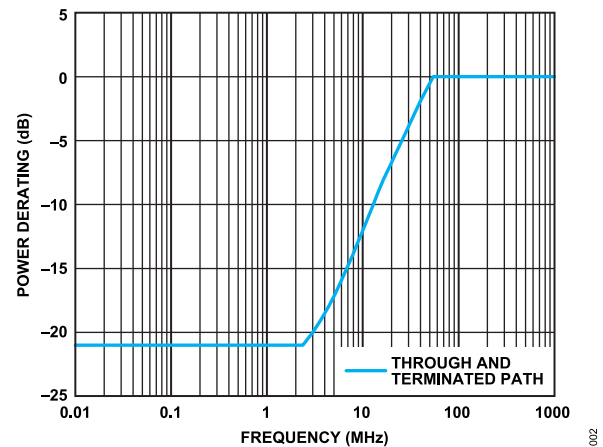


Figure 2. Power Derating vs. Frequency, Low-Frequency Detail, $T_{CASE} = 85^{\circ}$

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5030

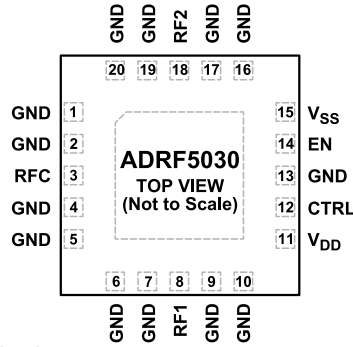
Table 5. ADRF5030, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	1.5 kV for RF pins	1C
	2 kV for supply and digital control pins	2
CDM	500 V for all pins	C2A

ABSOLUTE MAXIMUM RATINGS**ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND OF THE PCB.

003

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 6, 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. These pins must be connected to the RF/DC ground of the PCB.
3	RFC	RF Common Port. This pin is DC-coupled to 0 V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
8	RF1	RF Port 1. This pin is DC-coupled to 0 V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
11	V _{DD}	Positive Supply Voltage. See Figure 6 for the interface schematic.
12	CTRL	Control Input Voltage. See for the truth table. See Figure 5 for the interface schematic.
14	EN	Enable Input Voltage. See for the truth table. See Figure 5 for the interface schematic.
15	V _{SS}	Negative Supply Voltage. See Figure 7 for the interface schematic.
18	RF2	RF Port 2. This pin is DC-coupled to 0 V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

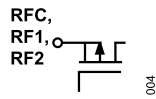


Figure 4. RFC, RF1, RF2 Pins

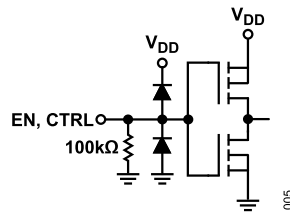


Figure 5. EN, CTRL Pins

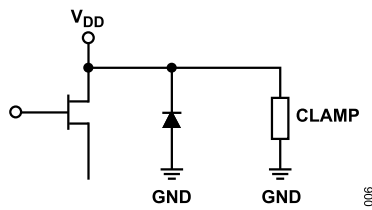


Figure 6. V_{DD} Pin

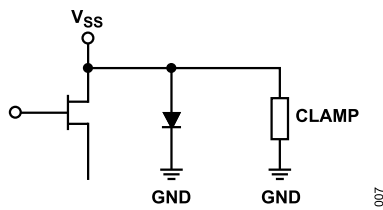


Figure 7. V_{SS} Pin

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , and $T_{CASE} = 25^\circ\text{C}$, and a $50\ \Omega$ system, unless otherwise noted. RFx refers to RF1 or RF2.

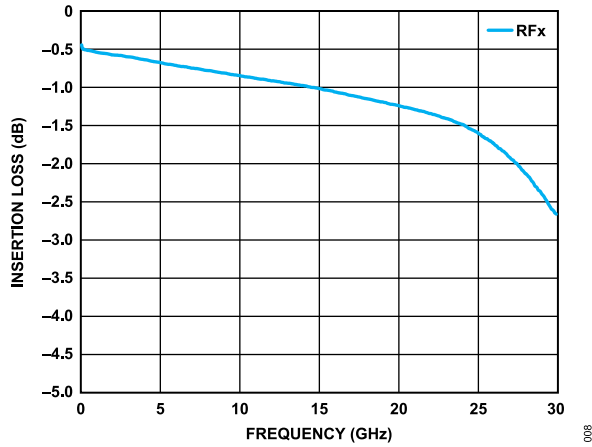


Figure 8. Insertion Loss vs. Frequency RF1 and RF2

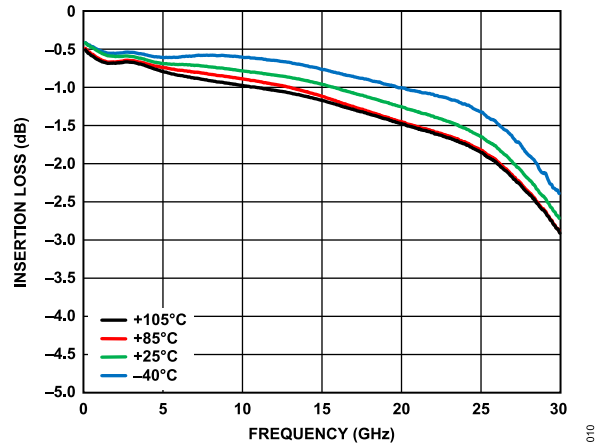


Figure 10. Insertion Loss vs. Frequency over Various Temperatures

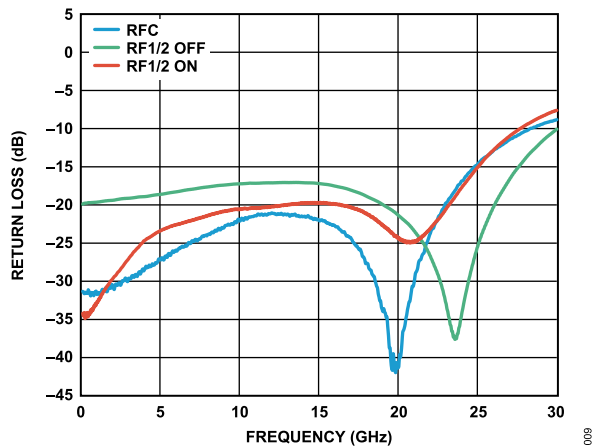


Figure 9. Return Loss vs. Frequency

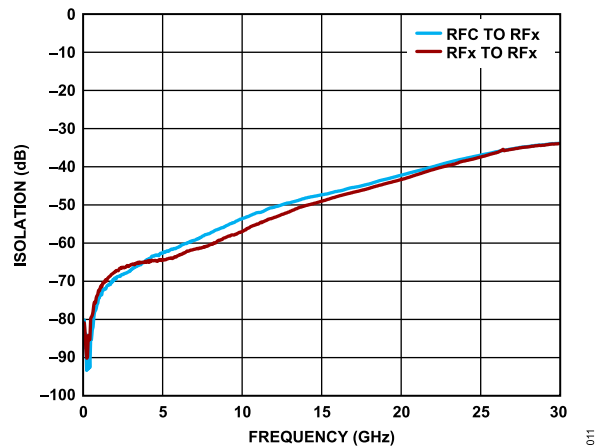


Figure 11. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3$, $V_{CTRL} = 0\text{ V}$ or V_{DD} , and $T_{CASE} = 25^\circ\text{C}$ for a $50\ \Omega$ system, unless otherwise noted.

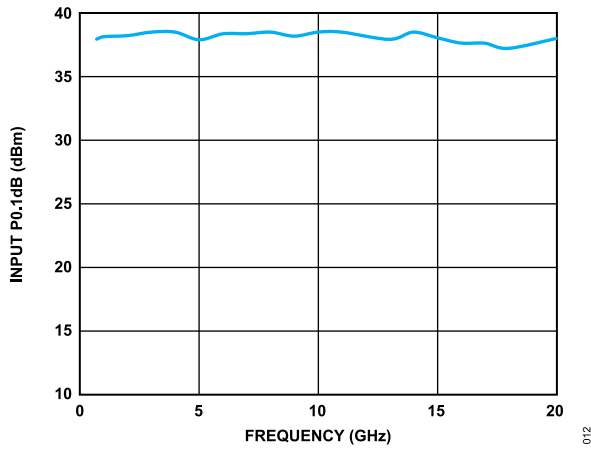


Figure 12. Input P0.1dB vs. Frequency

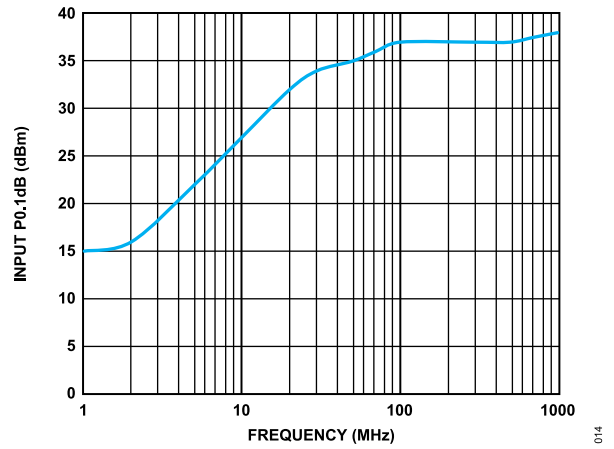


Figure 14. Input P0.1dB vs. Frequency (Low-Frequency Detail)

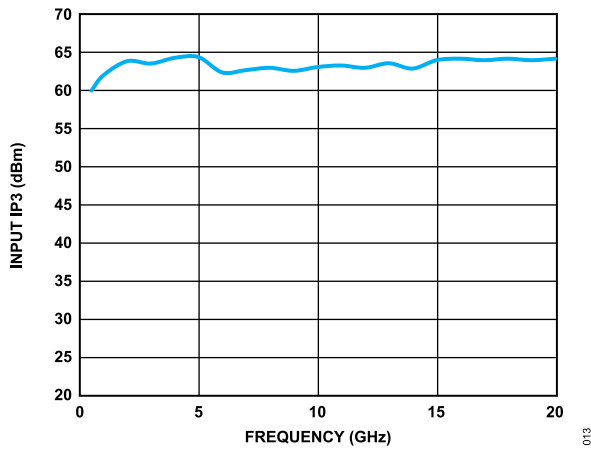


Figure 13. Input IP3 vs. Frequency

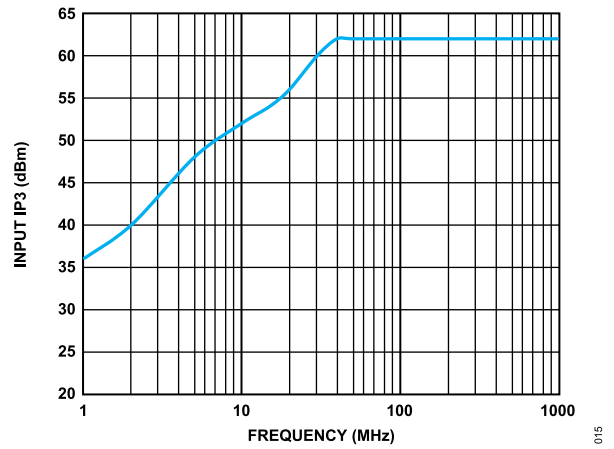


Figure 15. Input IP3 vs. Frequency (Low-Frequency Detail)

THEORY OF OPERATION

The ADRF5030 integrates a driver to perform logic functions internally and to provide the advantage of a simplified CMOS/LVTTL-compatible control interface. There are two digital control input pins (EN, CTRL) that determine which RF port is in the insertion loss state and in the isolation state. See [Table 7](#) for the control voltage truth table.

When the EN pin is logic high, all RF paths are in isolation state regardless of the logic state of the other pin. The RFx ports are terminated to internal 50 Ω resistors, and RFC becomes reflective.

RF INPUT AND OUTPUT

The RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC-blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω .

The ADRF5030 is bidirectional with equal power-handling capabilities. The RF input signal can be applied to the RFC port or the selected RFx throw port.

The insertion loss path conducts the RF signal between the selected RFx throw port and the RFC (common) port. The isolation paths provide high loss between the insertion loss path and the unselected RFx throw port. The unselected RFx port of the ADRF5030 is non-reflective.

Table 7. Control Voltage Truth Table

Digital Control Input		RFx Paths	
EN	CTRL	RF1 to RFC	RF2 to RFC
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low or High	Isolation (off)	Isolation (off)

The power handling of the ADRF5030 derates with frequencies below 100 MHz. See [Figure 2](#) for derating of the RF power towards lower frequencies.

POWER SUPPLY

The ADRF5030 requires a positive supply voltage to be applied to the V_{DD} pin and a negative supply voltage to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up V_{DD} and V_{SS} . Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 k Ω resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after V_{DD} is powered up and the control pins are not driven to a valid logic state.
4. Apply RF input signal.

APPLICATIONS INFORMATION

The ADRF5030 has two power-supply pins (V_{DD} and V_{SS}) and two control pins (EN, CTRL). Figure 16 shows the external components and connections for the supply pin. The V_{DD} and V_{SS} pins are decoupled with a 100 pF capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC-blocking capacitors on the RF pins when the RF lines are biased at a voltage other than 0 V. See Table 6 for details.

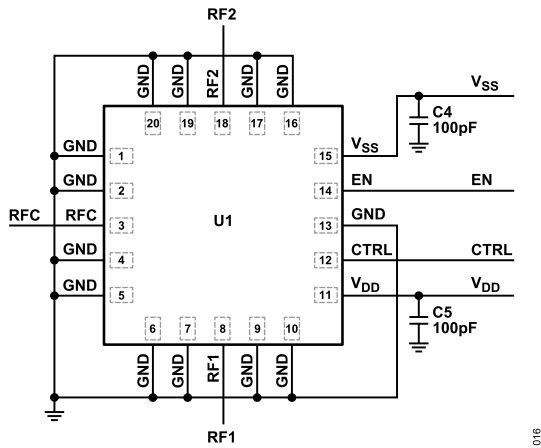


Figure 16. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 17 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003C dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

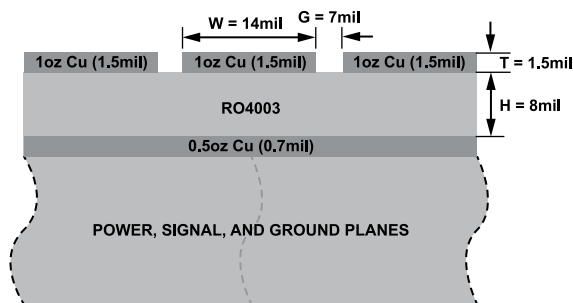


Figure 17. Example PCB Stack-up

Figure 18 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

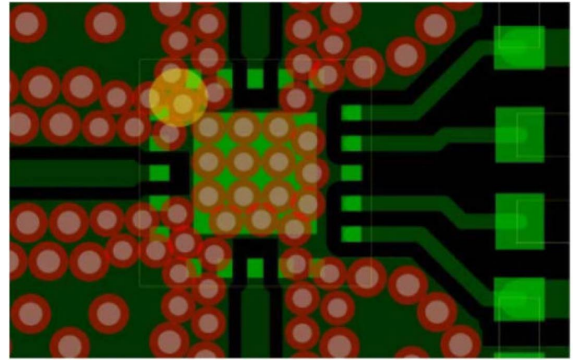


Figure 18. PCB Layout

Figure 19 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width to the package edge and tapered to RF trace. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

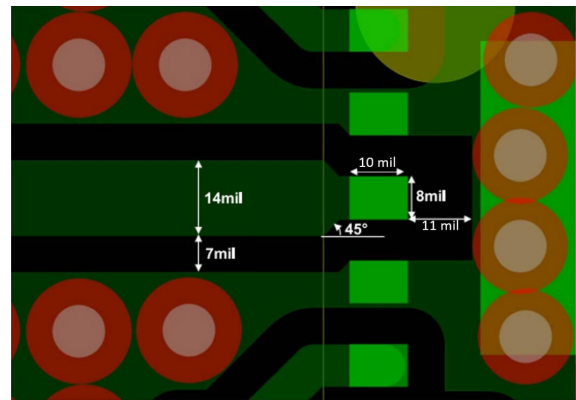
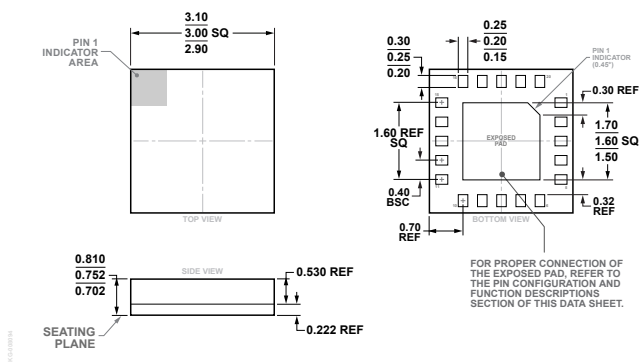


Figure 19. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and RF trace design, contact Analog Devices Technical Support for further recommendations.

OUTLINE DIMENSIONS



**Figure 20. 20-Terminal Land Grid Array [LGA]
3 mm x 3 mm Body and 0.75 mm Package Height (CC-20-21)
Dimensions Shown in Millimeters**

Updated: March 28, 2024

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5030BCCZN	-40°C to +105°C	20-Terminal LGA (3.0 mm x 3.0 mm x 0.75 mm)		CC-20-21
ADRF5030BCCZN-R7	-40°C to +105°C	20-Terminal LGA (3.0 mm x 3.0 mm x 0.75 mm)	REEL, 1500	CC-20-21
ADRF5030-EVALZ		Evaluation Board		

¹ Z = RoHS Compliant Part.