Data Sheet

ADPL83200

Low Loss PowerPath Controller in a ThinSOT Package

FEATURES

- **Very Low Loss Replacement for Power Supply OR'ing Diodes**
- **Minimal External Components**
- **Automatic Switching Between DC Sources**
- **Simplifies Load Sharing with Multiple Batteries**
- **Low Quiescent Current: 11µA**
- 3V to 28V AC/DC Adapter Voltage Range
- 2.5V to 28V Battery Voltage Range
- Reverse Battery Protection
- Drives Almost Any Size MOSFET for a Wide Range of Current Requirements
- MOSFET Gate Protection Clamp
- Manual Control Input
- Low Profile (1mm) ThinSOT™ Package

APPLICATIONS

- Cellular Phones
- Notebook and Handheld Computers
- Digital Cameras
- USB-Powered Peripherals
- Uninterruptible Power Supplies
- Logic Controlled Power Switch

GENERAL DESCRIPTION

The **ADPL83200** controls an external P-channel MOSFET to create a near-ideal diode function for power switchover or load sharing. This permits highly efficient OR'ing of multiple power sources for extended battery life and low self-heating. When conducting, the voltage drop across the Metal-oxide-semiconductor field-effect transistor (MOSFET) is typically 20mV. For applications with a wall adapter or other auxiliary power source, the load is automatically disconnected from the battery when the auxiliary source is connected. Two or more ADPL83200s can be interconnected to allow load sharing between multiple batteries or charging multiple batteries from a single charger.

The wide supply operating range supports operation from one to six Li-Ion cells in series. The low quiescent current (11µA typical) is independent of the load current. The gate driver includes an internal voltage clamp for MOSFET protection.

The STAT pin can be used to enable an auxiliary P-channel MOSFET power switch when an auxiliary supply is detected. This pin may also be used to indicate to a microcontroller that an auxiliary supply is connected. The control (CTL) input enables the user to force the primary MOSFET off and the STAT pin low.

The ADPL83200 is available in a low-profile (1mm) ThinSOT package.

TYPICAL APPLICATION

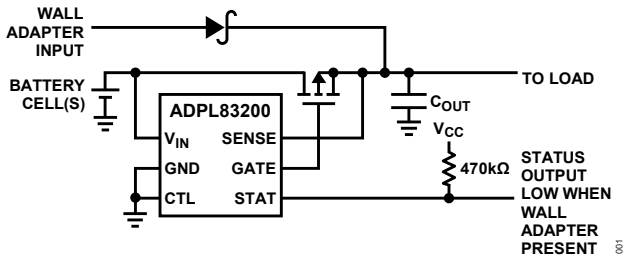

Figure 1. Automatic Switchover of Load between a Battery and a Wall Adapter

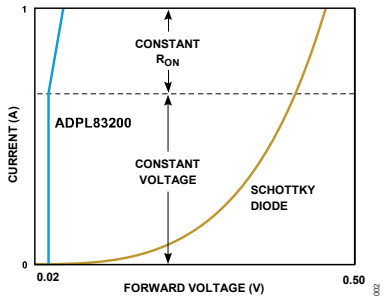

Figure 2. ADPL83200 vs. Schottky Diode Forward Voltage Drop

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	07/25	Initial Release.	—
A	10/25	Updated Features, Absolute Maximum Ratings, and Ideal Diode Control with a Microcontroller sections	1, 7, 18

SPECIFICATIONS

Table 1. Electrical Characteristics

(The -40°C ≤ T_J ≤ 150°C denotes the specifications that apply over the full operating junction temperature range. Unless otherwise noted, specifications are at T_A = 25°C, V_{IN} = 12V, CTL, and GND = 0V. Current into a pin is positive, and current out of a pin is negative. All voltages are referenced to GND, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Operating supply range	V_{IN}, V_{SENSE}	V_{IN} and/or V_{SENSE} must be in this range for proper Operation -40°C ≤ T_J ≤ 150°C	2.5		28	V
Quiescent supply current at low supply while in forward regulation	I_{QFL}	V_{IN} = 3.6V. Measure the combined current at V_{IN} and SENSE pins, averaged with V_{SENSE} = 3.5V and V_{SENSE} = 3.6V[1] -40°C ≤ T_J ≤ 150°C		11	20	µA
Quiescent supply current at high supply while in forward regulation	I_{QFH}	V_{IN} = 28V. Measure the combined current at V_{IN} and SENSE pins averaged with V_{SENSE} = 27.9V and V_{SENSE} = 28V[1] -40°C ≤ T_J ≤ 150°C		15	26	µA
Quiescent supply current at low supply while in reverse turn-off	I_{QRL}	V_{IN} = 3.6V, V_{SENSE} = 3.7V. Measure the combined current of V_{IN} and SENSE pins		10	20	µA
Quiescent supply current at high supply while in reverse turn-off	I_{QRH}	V_{IN} = 27.9V, V_{SENSE} = 28V. Measure the combined current of V_{IN} and SENSE pins		16	30	µA
Quiescent supply current at low supply with CTL active	I_{QCL}	V_{IN} = 3.6V, V_{SENSE} = 0V, V_{CTL} = 1V		7	14	µA
Quiescent supply current at high supply with CTL active	I_{QCH}	V_{IN} = 28V, V_{SENSE} = 0V, V_{CTL} = 1V		12	20	µA
V_{IN} and SENSE pin leakage currents when other pin supply power	I_{LEAK}	V_{IN} = 28V, V_{SENSE} = 0V; V_{SENSE} = 28V, V_{IN} = 0V; V_{IN} = 14V, V_{SENSE} = –14V; V_{SENSE} = 14V, V_{IN} = –14V	–3	0	1	µA

(The -40°C ≤ T_J ≤ 150°C denotes the specifications that apply over the full operating junction temperature range. Unless otherwise noted, specifications are at T_A = 25°C, V_{IN} = 12V, CTL, and GND = 0V. Current into a pin is positive, and current out of a pin is negative. All voltages are referenced to GND, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
PowerPath™ Controller						
PowerPath switch forward regulation voltage	V_{FR}	$V_{IN} - V_{SENSE}$, 2.5V ≤ V_{IN} ≤ 28V	10	20	32	mV
PowerPath switch reverse turn-off threshold voltage	V_{RTO}	$V_{SENSE} - V_{IN}$, 2.5V ≤ V_{IN} ≤ 28V	10	20	32	mV
GATE and STAT Outputs						
GATE active forward regulation source current	$I_{G(SRC)}$	[2]	–1	–2.5	–5	µA
GATE active forward regulation sink current	$I_{G(SNK)}$	[2]	25	50	85	µA
GATE clamp voltage	$V_{G(ON)}$	Apply I_{GATE} = 1µA, V_{IN} = 12V, V_{SENSE} = 11.9V, Measure $V_{IN} - V_{GATE}$	6.3	7	7.7	V
GATE-Off voltage	$V_{G(OFF)}$	Apply I_{GATE} = –5µA, V_{IN} = 12V, V_{SENSE} = 12.1V, Measure $V_{SENSE} - V_{GATE}$		0.13	0.25	V
GATE turn-on time	$t_{G(ON)}$	V_{GS} < –3V, C_{GATE} = 1nF[3]		110	175	µs
GATE turn-off time	$t_{G(OFF)}$	V_{GS} > –1.5V, C_{GATE} = 1nF[4]		13	22	µs
STAT off current	$I_{S(OFF)}$	2.5V ≤ V_{IN} ≤ 28V[5]	–1	0	1	µA
STAT Sink Current	$I_{S(SNK)}$	2.5V ≤ V_{IN} ≤ 28V[5]	6	10	18	µA
STAT turn-on time	$t_{S(ON)}$	[6]		4.5	30	µs
STAT turn-off time	$t_{S(OFF)}$	[6]		40	100	µs
CTL Input						
CTL input low voltage	V_{IL}	2.5V ≤ V_{IN} ≤ 28V		0.5	0.35	V
CTL input high voltage	V_{IH}	2.5V ≤ V_{IN} ≤ 28V	0.9	0.635		V
CTL input pull-down current	I_{CTL}	0.35V ≤ V_{CTL} ≤ 28V	1	3.5	7	µA
CTL hysteresis	H_{CTL}	2.5V ≤ V_{IN} ≤ 28V		135		mV

1 This results in the same supply current as would be observed with an external P-channel MOSFET connected to the ADPL83200 and operating in forward regulation.

2 V_{IN} is held at 12V, and GATE is forced to 10.5V. SENSE is set to 12V to measure the source current at the GATE. SENSE is set to 11.9V to measure sink current at the GATE.

3 V_{IN} is held at 12V, and SENSE is stepped from 12.2V to 11.8V to trigger the event. GATE voltage is initially $V_{G(OFF)}$.

4 V_{IN} is held at 12V, and SENSE is stepped from 11.8V to 12.2V to trigger the event. GATE voltage is initially internally clamped at $V_{G(ON)}$.

5 STAT is forced to V_{IN} – 1.5V. SENSE is set at V_{IN} – 0.1V to measure the off current at STAT. SENSE is set at V_{IN} + 0.1V to measure the sink current at the STAT pin.

6 STAT is forced to 9V, and V_{IN} is held at 12V. SENSE is stepped from 11.8V to 12.2V to measure the STAT turn-on time defined when I_{STAT} reaches one-half the measured $I_{S(SNK)}$. SENSE is stepped from 12.2V to 11.8V to measure the STAT turn-off time defined when I_{STAT} reaches one-half the measured $I_{S(SNK)}$.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Supply Voltage (V_{IN})	–14V to 36V
Voltage from V_{IN} to SENSE	–28V to 28V
Input Voltage CTL	–0.3V to 36V
Input Voltage SENSE	–14V to 36V
Output Voltage GATE	–0.3V to the Higher of V_{IN} + 0.3V or SENSE + 0.3V
Output Voltage STAT	–0.3V to 36V
Operating Junction Temperature Range[1]	–55°C to 150°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] The ADPL83200 is tested under pulsed load conditions such that $T_J \approx T_A$. The ADPL83200 is guaranteed over the -40°C to 85°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetimes are further degraded for junction temperatures exceeding 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \times \Theta_{JA})$, where Θ_{JA} = 230°C/W for the TSOT-23 package.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

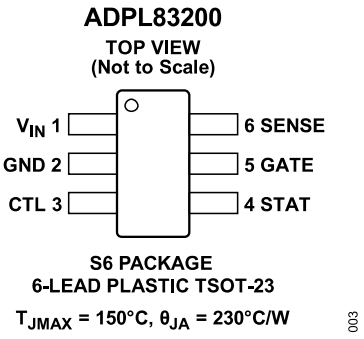


Figure 3. Pin Configuration

Pin Descriptions

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	V_{IN}	Primary Input Supply Voltage. Supplies power to the internal circuitry and is one of two voltage sense inputs to the internal analog controller (The other input to the controller is the SENSE pin). This input usually supplies power from a battery or other power source that supplies current to the load. This pin can be bypassed to ground with a capacitor in the range of 0.1µF to 10µF if needed, to suppress load transients.
2	GND	Ground. Provides a power return for all the internal circuits.
3	CTL	Digital Control Input. A logical high input (V_{IH}) on this pin forces the gate to source voltage of the primary P-channel MOSFET power switch to a small voltage (V_{GOFF}). This will turn the MOSFET off, and no current will flow from the primary power input at V_{IN} if the MOSFET is configured so that the drain to the source diode does not forward bias. A high input also forces the STAT pin to sink 10µA of current ($I_{S(SNK)}$). If the STAT pin is used to control an auxiliary P-channel power switch, then a second active source of power, such as an AC wall adaptor, will be connected to the load (see the *Applications Information* section for more details). An internal current sink will pull the CTL pin voltage to ground (logical low) if the pin is open.
4	STAT	Open-Drain Output Status Pin. When the SENSE pin is pulled above the V_{IN} pin with an auxiliary power source by about 20mV or more, the reverse turnoff threshold (V_{RTO}) is reached. The STAT pin will then go from an open state to a 10µA current sink ($I_{S(SNK)}$). The STAT pin current sink can be used, along with an external resistor, to turn on an auxiliary P-channel power switch and/or signal the presence of an auxiliary power source to a microcontroller.
5	GATE	Primary P-Channel MOSFET Power Switch Gate Drive Pin. This pin is directed by the power controller to maintain a forward regulation voltage (V_{FR}) of 20mV between the V_{IN} and SENSE pins when an auxiliary power source is not present.

PIN	NAME	DESCRIPTION
		When an auxiliary power source is connected, the GATE pin will pull up to the SENSE pin voltage, turning off the primary P-channel power switch.
6	SENSE	Power Sense Input Pin. This pin supplies power to the internal circuitry and is a voltage sense input to the internal analog controller (The other input to the controller is the V_{IN} pin). This input is usually supplied power from an auxiliary source such as an AC adapter or backup battery, which also supplies current to the load.

TYPICAL PERFORMANCE CHARACTERISTICS

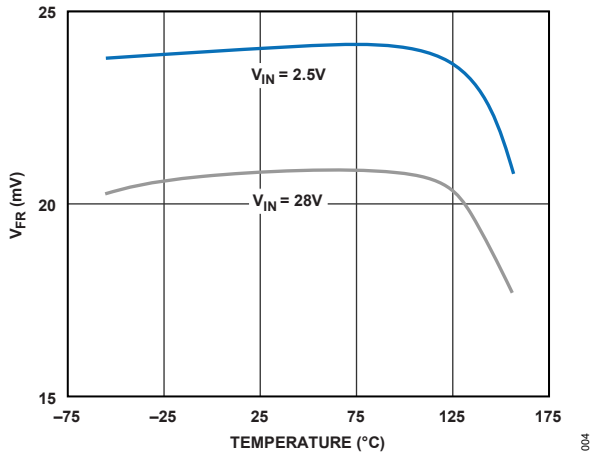


Figure 4. V_{FR} vs. Temperature and Supply Voltage

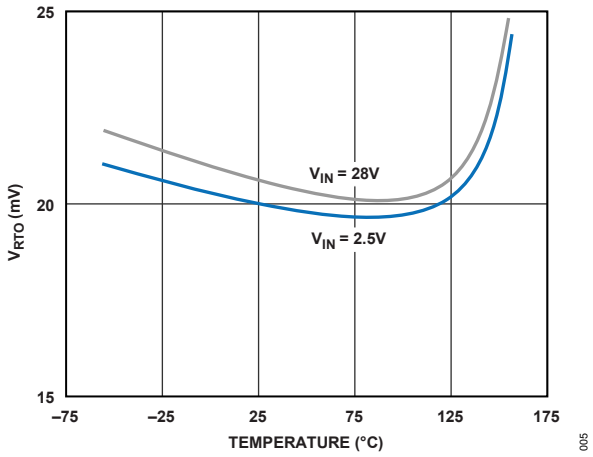


Figure 5. V_{RTO} vs. Temperature and Supply Voltage

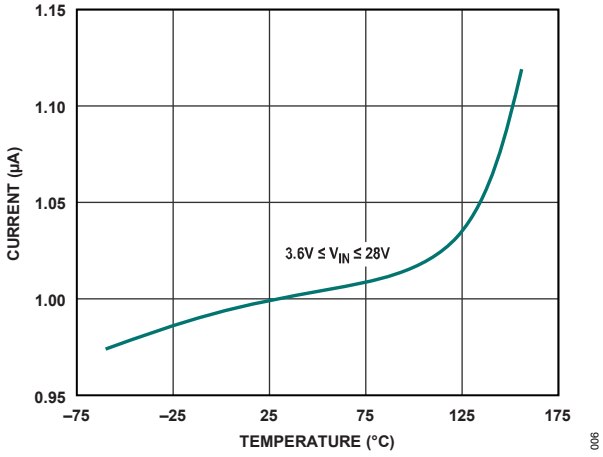


Figure 6. Normalized Quiescent Supply Current vs. Temperature

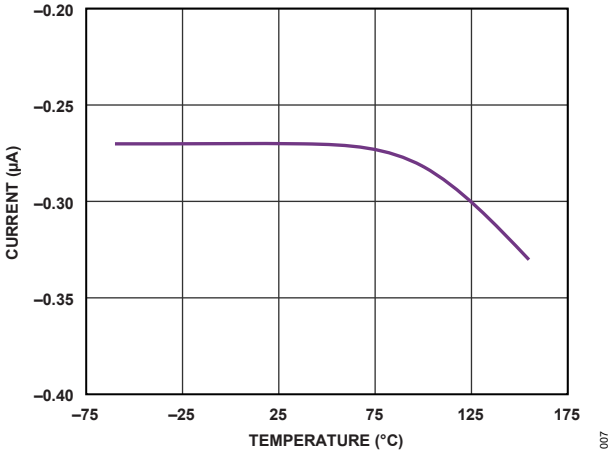


Figure 7. I_{LEAK} vs. Temperature

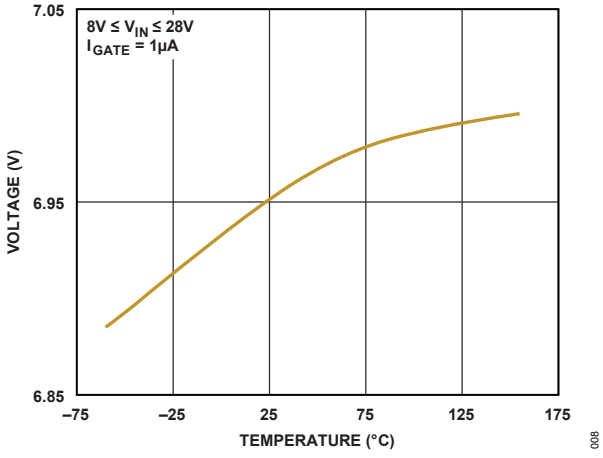


Figure 8. $V_{G(ON)}$ vs. Temperature

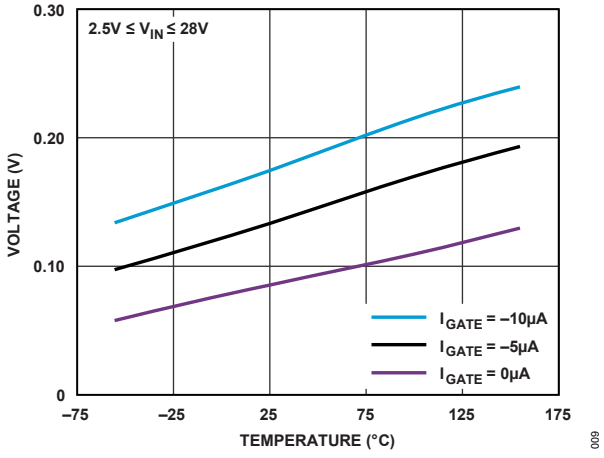


Figure 9. $V_{G(OFF)}$ vs. Temperature and I_{GATE}

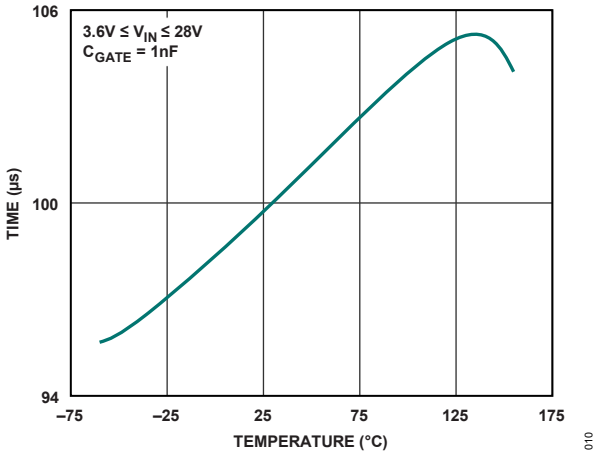


Figure 10. $t_{G(ON)}$ vs. Temperature

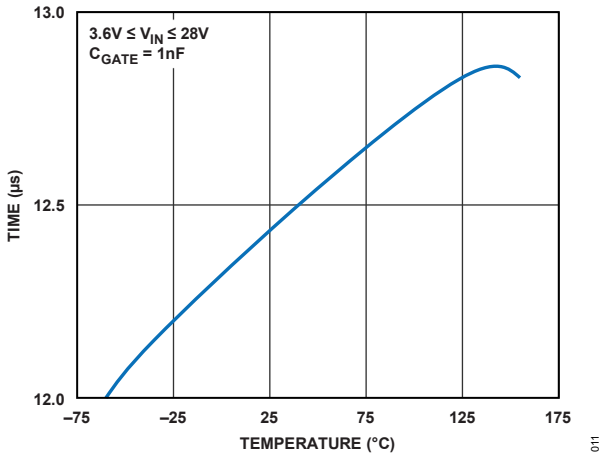


Figure 11. $t_{G(OFF)}$ vs. Temperature

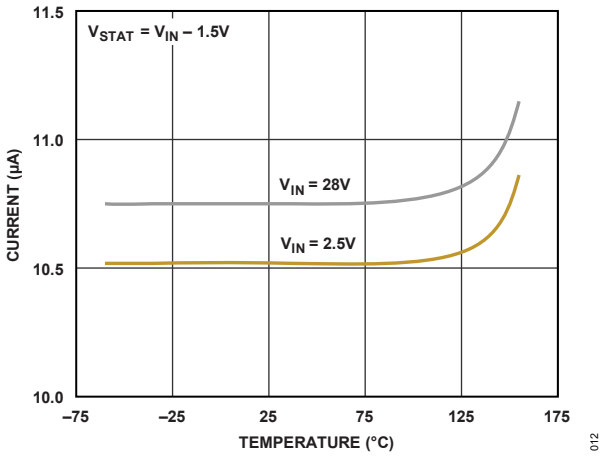


Figure 12. $I_{S(SNK)}$ vs. Temperature and V_{IN}

BLOCK DIAGRAM

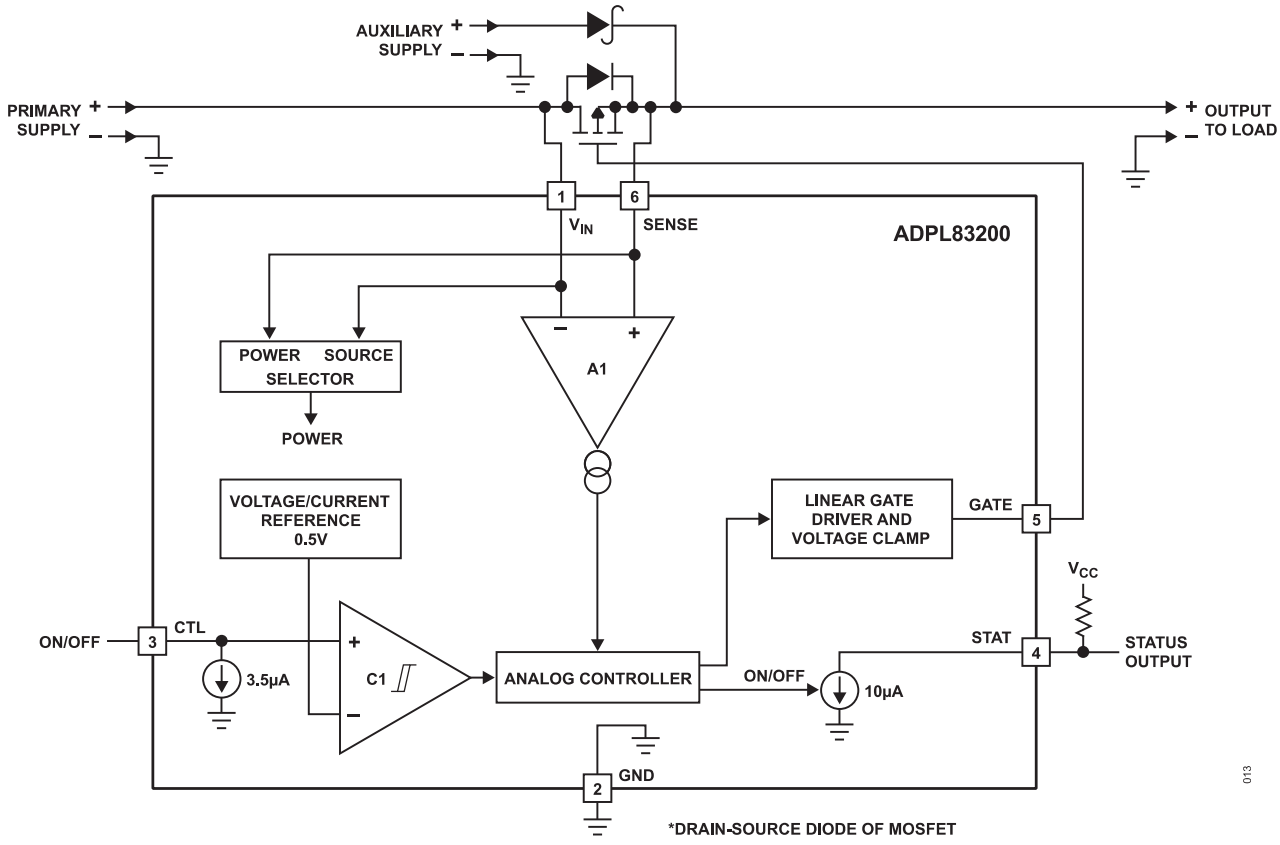


Figure 13. ADPL83200 Block Diagram

THEORY OF OPERATION

See the *Figure 13* (Block Diagram) for the best understanding of the operation, which illustrates the internal circuit blocks along with the few external components, and the graph that accompanies *Figure 1*. The terms **primary** and **auxiliary** are arbitrary and may be changed to suit the application. Operation begins when either or both power sources are applied, and the CTL control pin is below the input low voltage of 0.35V (V_{IL}). If only the primary supply is present, the Power Source Selector will power the ADPL83200 from the V_{IN} pin. Amplifier A1 will deliver a current to the Analog Controller block that is proportional to the voltage difference between the V_{IN} and SENSE pins. While the voltage on SENSE is lower than V_{IN} – 20mV (V_{FR}), the Analog Controller will instruct the Linear gate driver and Voltage clamp block to pull down the GATE pin voltage and turn on the external P-channel MOSFET. The dynamic pull-down current of 50µA ($I_{G(SNK)}$) stops when the GATE voltage reaches ground or the gate clamp voltage. The gate clamp voltage is 7V ($V_{G(ON)}$) below the higher of V_{IN} or V_{SENSE}. As the SENSE voltage pulls up to V_{IN} – 20mV, the ADPL83200 will regulate the GATE voltage to maintain a 20mV difference between V_{IN} and V_{SENSE}, which is also the V_{DS} of the MOSFET. The system is now in the forward regulation mode, and the load will be powered from the primary supply. As the load current varies, the GATE voltage will be controlled to maintain the 20mV difference. If the load current exceeds the P-channel MOSFET's ability to deliver the current with a 20mV V_{DS}, the GATE voltage will clamp, the MOSFET will behave as a fixed resistor, and the forward voltage will increase slightly. While the MOSFET is on, the STAT pin is an open circuit.

When an auxiliary supply is applied, the SENSE pin will be pulled higher than the V_{IN} pin through the external diode. The Power source selector will power the ADPL83200 from the SENSE pin. As the SENSE voltage pulls above V_{IN} – 20mV, the Analog controller instructs the Linear Gate Driver and Voltage clamp block to pull the GATE voltage up to turn off the P-channel MOSFET. When the voltage on SENSE is higher than V_{IN} + 20mV (V_{RTO}), the Analog Controller will instruct the Linear gate driver and Voltage clamp block to rapidly pull the GATE pin voltage to the SENSE pin voltage. This action will quickly finish turning off the external P-channel MOSFET if it hasn't already turned completely off. For a clean transition, the reverse turn-off threshold has hysteresis to prevent uncertainty. The system is now in the reverse turn-off mode. Power to the load is delivered through the external diode, and no current is drawn from the primary supply. The external diode protects in case the auxiliary supply is below the primary supply, sinks current to ground, or is connected to reverse polarity. During the reverse turn-off mode of operation, the STAT pin will sink 10µA of current ($I_{S(SNK)}$) if connected. Note that the external MOSFET is wired so that the drain-to-source diode will momentarily forward-bias when power is first applied to V_{IN} and will become reverse-biased when an auxiliary supply is applied.

When the CTL (control) input is asserted high, the external MOSFET will have its gate to source voltage forced to a small voltage $V_{G(OFF)}$, and the STAT pin will sink 10µA of current if connected. This feature is useful to allow controlled input switching of the load between two power sources, as shown in *Figure 17* or as a switchable high-side driver, as shown in *Figure 19*. A 3.5µA internal pull-down current (I_{CTL}) on the CTL pin will ensure a low-level input if the pin should become open.

APPLICATIONS INFORMATION

Introduction

The system designer will find the ADPL83200 useful in a variety of cost and space-sensitive power control applications that include low loss diode OR'ing, fully automatic switchover from a primary to an auxiliary source of power, microcontroller controlled switchover from a primary to an auxiliary source of power, load sharing between two or more batteries, charging of multiple batteries from a single charger and high-side power switching.

External P-Channel MOSFET Transistor Selection

Important parameters for the selection of MOSFETs are the maximum drain-source voltage $V_{DS(MAX)}$, threshold voltage $V_{GS(VT)}$, and on-resistance $R_{DS(ON)}$.

The maximum allowable drain-source voltage, $V_{DS(MAX)}$, must be sufficiently high to withstand the maximum drain-source voltage encountered in the application.

The maximum gate drive voltage for the primary MOSFET is set by the smaller of the V_{IN} supply voltage or the internal clamping voltage $V_{G(ON)}$. A logic-level MOSFET is commonly used; however, if a low supply voltage limits the gate voltage, a sub-logic-level threshold MOSFET should be considered. The maximum gate drive voltage for the auxiliary MOSFET, if used, is determined by the external resistor connected to the STAT pin and the STAT pin sink current.

As a general rule, select a MOSFET with a low enough $R_{DS(ON)}$ to obtain the desired V_{DS} while operating at full load current and an achievable V_{GS}. The MOSFET normally operates in the linear region, acting like a voltage-controlled resistor. If the MOSFET is grossly undersized, it can enter the saturation region, resulting in a large V_{DS}. However, the drain-source diode of the MOSFET, if forward biased, will limit V_{DS}. A large V_{DS}, combined with the load current, will likely result in excessively high MOSFET power dissipation. Note that the ADPL83200 will regulate the forward voltage drop across the primary MOSFET at 20mV if $R_{DS(ON)}$ is low enough. The required $R_{DS(ON)}$ can be calculated by dividing 0.02V by the load current in amps. Achieving forward regulation will minimize power loss and heat dissipation, but it is not a necessity. If a forward voltage drop of more than 20mV is acceptable, then a smaller MOSFET can be used, but it must be sized and compatible with the higher power dissipation. Care should be taken to ensure that the power dissipated is never exceeds the manufacturer's recommended maximum level. The auxiliary MOSFET power switch, if used, has similar considerations, but its V_{GS} can be tailored by resistor selection. When choosing the resistor value, consider the full range of STAT pin current ($I_{S(SNK)}$) that may flow through it.

V_{IN} and SENSE Pin Bypass Capacitors

Many types of capacitors, ranging from 0.1µF to 10µF and located close to the ADPL83200, will provide adequate V_{IN} bypassing if needed. Voltage droop can occur at the load during a supply switchover because some time is required to turn on the MOSFET power switch. Factors that determine the magnitude of the voltage droop include the supply rise and fall times, the MOSFET's characteristics, the value of C_{OUT}, and the load current. Droop can be made insignificant by the proper choice of C_{OUT}, since the droop is inversely proportional to the capacitance. Bypass capacitance for the load also depends on the application's dynamic load requirements and typically ranges from 1µF to 47µF. In all cases, the maximum droop is limited to the drain-source diode forward drop inside the MOSFET.

Caution must be exercised when using multilayer ceramic capacitors. Due to the self-resonance and high-Q characteristics of certain types of ceramic capacitors, high-voltage transients can be generated under specific start-up conditions, such as connecting a supply input to a hot power source. To reduce the Q and prevent these transients from exceeding the ADPL83200's absolute maximum voltage rating, the capacitor's ESR can be increased by adding up to several ohms of resistance in series with the ceramic capacitor. Refer to *Analog Devices Application Note 88*.

The selected capacitance value and the capacitor's Equivalent series resistance (ESR) can be verified by observing V_{IN} and SENSE for acceptable voltage transitions during dynamic conditions over the full load current range. This should also be checked with each power source. Ringing may indicate an incorrect bypass capacitor value and/or too low an ESR.

V_{IN} and SENSE Pin Usage

Since the analog controller's thresholds are small (±20mV), the V_{IN} and SENSE pin connections should be made in a way to avoid unwanted I x R drops in the power path. Both pins are protected from negative voltages.

GATE Pin Usage

The GATE pin controls the external P-channel MOSFET, which is connected between the V_{IN} and SENSE pins, when the load current is supplied by the power source at V_{IN}. In this mode of operation, the internal current source, which is responsible for pulling the GATE pin up, is limited to a few microamps ($I_{G(SRC)}$). If external opposing leakage currents exceed this, the GATE pin voltage will reach the clamp voltage (V_{GON}), and V_{DS} will be smaller. The internal current sink, which is responsible for pulling the GATE pin down, has a higher current capability ($I_{G(SNK)}$). With an auxiliary supply input pulling up on the SENSE pin and exceeding the V_{IN} pin voltage by 20mV (V_{RTO}), the device enters the reverse turn-off mode, and a much stronger current source is available to oppose external leakage currents and turn off the MOSFET (V_{GOFF}).

While in forward regulation, if the on-resistance of the MOSFET is too high to maintain forward regulation, the GATE pin will maximize the MOSFET's V_{GS} to that of the clamp voltage (V_{GON}). The clamping action takes place between the higher of V_{IN} or V_{SENSE} and the GATE pin.

Status Pin Usage

During normal operation, the open-drain STAT pin can be biased at any voltage between ground and 28V regardless of the supply voltage to the ADPL83200. It is usually connected to a resistor, whose other end IS connected to a voltage source. In the forward regulation mode, the STAT pin will be open ($I_{S(OFF)}$). When a wall adaptor input or other auxiliary supply is connected to that input, and the voltage on SENSE is higher than V_{IN} + 20mV (V_{RTO}), the system is in the reverse turn-off mode. During this mode of operation, the STAT pin will sink 10µA of current ($I_{S(SNK)}$). This will result in a voltage change across the resistor, depending on the resistance, which is useful to turn on an auxiliary P-channel MOSFET or signal to a microcontroller that an auxiliary power source is connected. External leakage currents, if significant, should be accounted for when determining the voltage across the resistor when the STAT pin is either on or off.

Control Pin Usage

This is a digital control input pin with low threshold voltages (V_{IL} and V_{IH}) for use with logic powered from as little as 1V. During normal operation, the CTL pin can be biased at any voltage between ground and 28V, regardless of the supply voltage to the ADPL83200. A logical high input on this pin forces the gate-to-source voltage of the primary P-channel MOSFET power switch to a small voltage (V_{GOFF}). This will turn the MOSFET off, and no current will flow from the primary power input at V_{IN} if the MOSFET is configured so that the drain to the source diode is not forward-biased. The high input also forces the STAT pin to sink 10µA of current ($I_{S(SNK)}$). See the *Typical Applications* for various examples of using the STAT pin. A 3.5µA internal pulldown current (I_{CTL}) on the CTL pin will ensure a logical low-level input if the pin should be open.

Protection

Most of the application circuits shown provide some protection against supply faults such as shorted, low, or reversed supply inputs. The fault protection does not protect shorted supplies but can isolate other supplies and the load from faults. A necessary condition of this protection is that all components have sufficient breakdown voltages. In some cases, if protection of the auxiliary input (sometimes referred to as the wall adapter input) is not required, then the series diode or MOSFET may be eliminated.

Internal protection for the ADPL83200 is provided to prevent damaging pin currents and excessive internal self-heating during a fault condition. These fault conditions can be a result of any ADPL83200 pins shorted to ground or to a power source that is within the pin's absolute maximum voltage limits. Both the V_{IN} and SENSE pins are capable of being taken significantly below ground without current drain or damage to the IC (Absolute Maximum Voltage Limits). This feature allows for reverse-battery conditions without current drain or damage. This internal protection is not designed to prevent overcurrent or overheating of external components.

TYPICAL APPLICATIONS

Automatic PowerPath Control

The applications shown in *Figure 1*, *Figure 14*, and *Figure 15* are automatic ideal diode controllers that require no assistance from a microcontroller. Each of these will automatically connect the higher supply voltage, after accounting for certain diode forward voltage drops, to the load with application of the higher supply voltage.

Figure 1 illustrates an application circuit for automatic switchover of a load between a battery and a wall adapter or other power input. With application of the battery, the load will initially be pulled up by the drain-source diode of the P-channel MOSFET. As the ADPL83200 comes into action, it will control the MOSFET's gate to turn it on, reducing the MOSFET's voltage drop from a diode drop to 20mV. The system is now in the low-loss forward regulation mode. When the wall adapter input is applied, the Schottky diode pulls the SENSE pin, connected to the load, above the battery voltage, and the ADPL83200 turns the MOSFET off. The STAT pin will then sink current, indicating an auxiliary input is connected. The battery is now supplying no load current, and all the load current flows through the Schottky diode. A silicon diode could be used instead of the Schottky, but it would result in higher power dissipation and heating due to the higher forward voltage drop.

Figure 14 illustrates an application circuit for automatic switchover of load between a battery and a wall adapter that features the lowest power loss. The operation is similar to *Figure 1* except that an auxiliary P-channel MOSFET replaces the diode. The STAT pin is used to turn on the MOSFET once the SENSE pin voltage exceeds the battery voltage by 20mV. When the wall adapter input is applied, the drain-source diode of the auxiliary MOSFET will turn on first to pull up the SENSE pin and turn off the primary MOSFET, followed by turning on the auxiliary MOSFET. Once the auxiliary MOSFET has turned on, the voltage drop across it can be very low, depending on the MOSFET's characteristics.

Figure 15 illustrates an application circuit for the automatic switchover of a load between a battery and a wall adapter in the comparator mode. It also shows how a battery charger can be connected. This circuit differs from *Figure 1* in the way the SENSE pin is connected. The SENSE pin is connected directly to the auxiliary power input, not to the load. This change forces the ADPL83200's control circuitry to operate in an open-loop comparator mode. While the battery supplies the system, the GATE pin voltage will be forced to its lowest clamped potential, instead of being regulated to maintain a 20mV drop across the MOSFET. This has the advantage of minimizing power loss in the MOSFET by minimizing its R_{ON} and not having the influence of a linear control loop's dynamics. A possible disadvantage is that if the auxiliary input ramps up slowly enough, the load voltage will initially droop before rising. This is due to the SENSE pin voltage rising above the battery voltage and turning off the MOSFET before the Schottky diode turns on. The factors that determine the magnitude of the voltage droop are the auxiliary input rise time, the type of diode used, the value of C_{OUT}, and the load current.

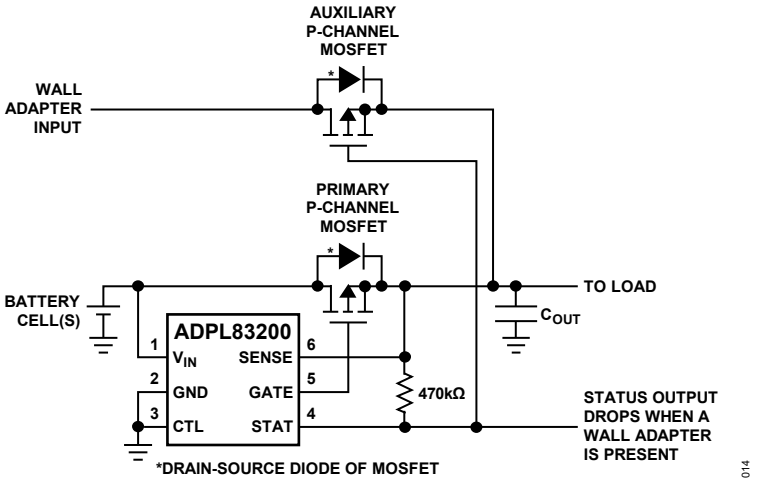


Figure 14. Automatic Switchover of Load between a Battery and a Wall Adapter with Auxiliary P-Channel MOSFET for Lowest Loss

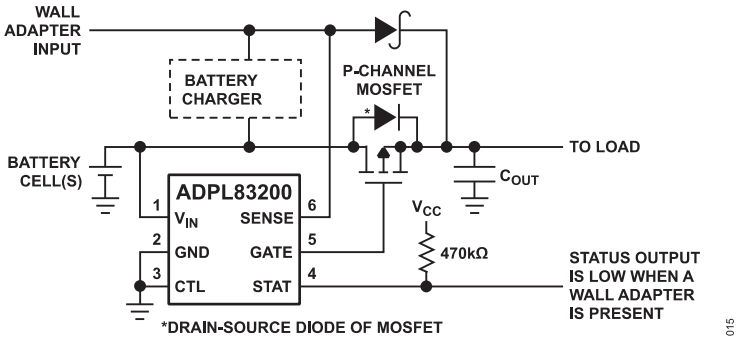


Figure 15. Automatic Switchover of Load between a Battery and a Wall Adapter in Comparator Mode

Ideal Diode Control with a Microcontroller

Figure 16 illustrates an application circuit for microcontroller monitoring and control of two power sources. The microcontroller's analog inputs, perhaps with the aid of a resistor voltage divider, monitor each supply input and command the ADPL83200 through the CTL input. Back-to-back MOSFETs are used so that the drain-source diode will not power the load when the MOSFET is turned off (dual MOSFETs in one package are commercially available).

With a logical low input on the CTL pin, the primary input supplies power to the load regardless of the auxiliary voltage. When CTL is switched high, the auxiliary input will power the load whether or not it is higher or lower than the primary power voltage. Once the auxiliary is on, the primary power can be removed, and the auxiliary will continue to power the load. Only when the primary voltage exceeds the auxiliary voltage will taking the CTL low switch back to the primary power, otherwise the auxiliary stays connected. When the primary power is disconnected and V_{IN} falls below V_{LOAD}, it will turn on the auxiliary MOSFET if CTL is low, but V_{LOAD} must stay up long enough for the MOSFET to turn on. At a minimum, C_{OUT} capacitance must be sized to hold up V_{LOAD} until the transition between the sets of MOSFETs is complete. Sufficient capacitance on the load, and low or no capacitance on V_{IN} will help ensure this. If desired, this can be avoided by the use of a capacitor on V_{IN} to ensure that V_{IN} falls more slowly than V_{LOAD}.

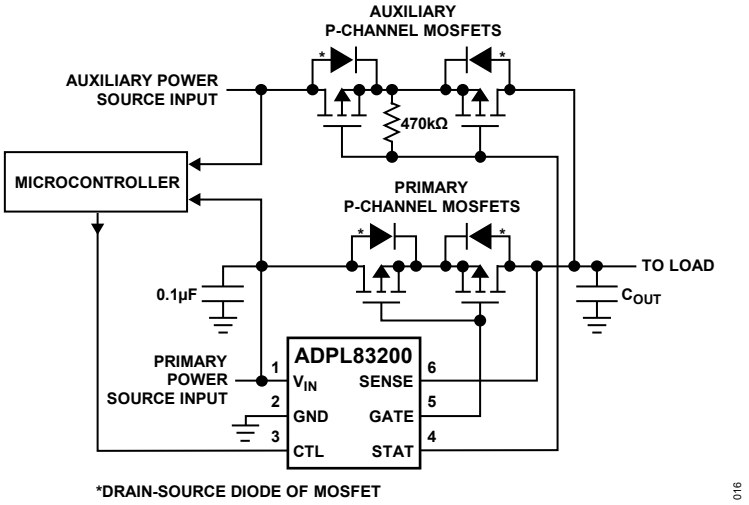


Figure 16. Microcontroller Monitoring and Control of Two Power Sources

Load Sharing

Figure 17 illustrates an application circuit for dual-battery load sharing with an automatic switchover of load from batteries to a wall adapter. Whichever battery can supply the higher voltage will provide the load current until it is discharged to the voltage of the other battery. The load will then be shared between the two batteries according to the capacity of each battery. The higher-capacity battery will provide a proportionally higher current to the load. When a wall adapter input is applied, both MOSFETs will turn off, and no-load current will be drawn from the batteries. The STAT pins provide information as to which input is supplying the load current. This concept can be expanded to more power inputs.

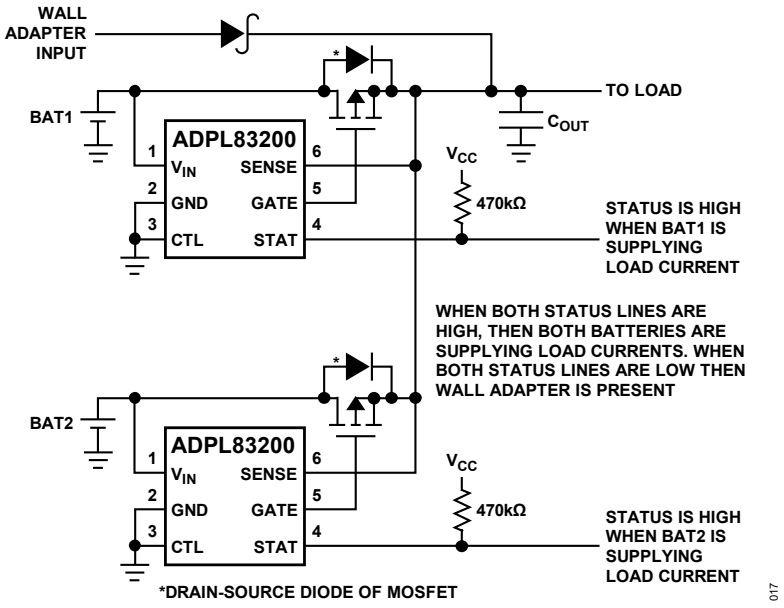


Figure 17. Dual Battery Load Sharing with Automatic Switchover of Load from Batteries to Wall Adapter

Multiple Battery Charging

Figure 18 illustrates an application circuit for automatic dual battery charging from a single charger. Whichever battery has the lower voltage will receive the charging current until both battery voltages are equal, then both will be charged. When both are charged simultaneously, the higher-capacity battery will get a proportionally higher current from the charger. For Li-Ion batteries, both batteries will achieve the float voltage minus the forward regulation voltage of 20mV. This concept can apply to more than two batteries. The STAT pins provide information as to which batteries are being charged. For intelligent control, the CTL pin input can be used with a microcontroller and back-to-back MOSFETs, as shown in *Figure 16*. This allows complete control for disconnection of the charger from either battery.

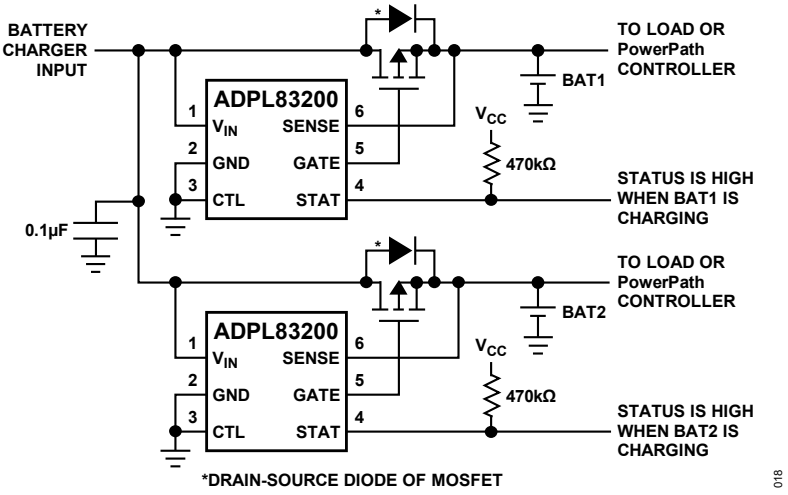


Figure 18. Automatic Dual Battery Charging from Single Charging Source

High Side Power Switch

Figure 19 illustrates an application circuit for a logic-controlled high-side power switch. When the CTL pins a logical low, the ADPL83200 will turn on the MOSFET. Because the SENSE pin is grounded, the ADPL83200 will apply a maximum clamped gate drive voltage to the MOSFET. When the CTL pin is at a logical high, the ADPL83200 will turn off the MOSFET by pulling its gate voltage up to the supply input voltage and thus deny power to the load. The MOSFET is connected with its source connected to the power source. This disables the drain-source diode from supplying voltage to the load when the MOSFET is off. Note that if the load is powered from another source, then the drain-source diode can forward-bias and deliver current to the power supply connected to the V_{IN} pin.

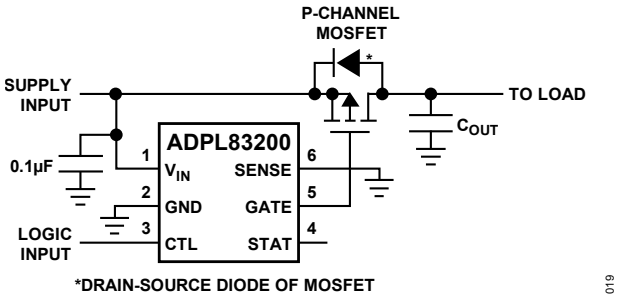


Figure 19. Logic Controlled High-Side Power Switch

ORDERING GUIDE

Table 4. Ordering Guide

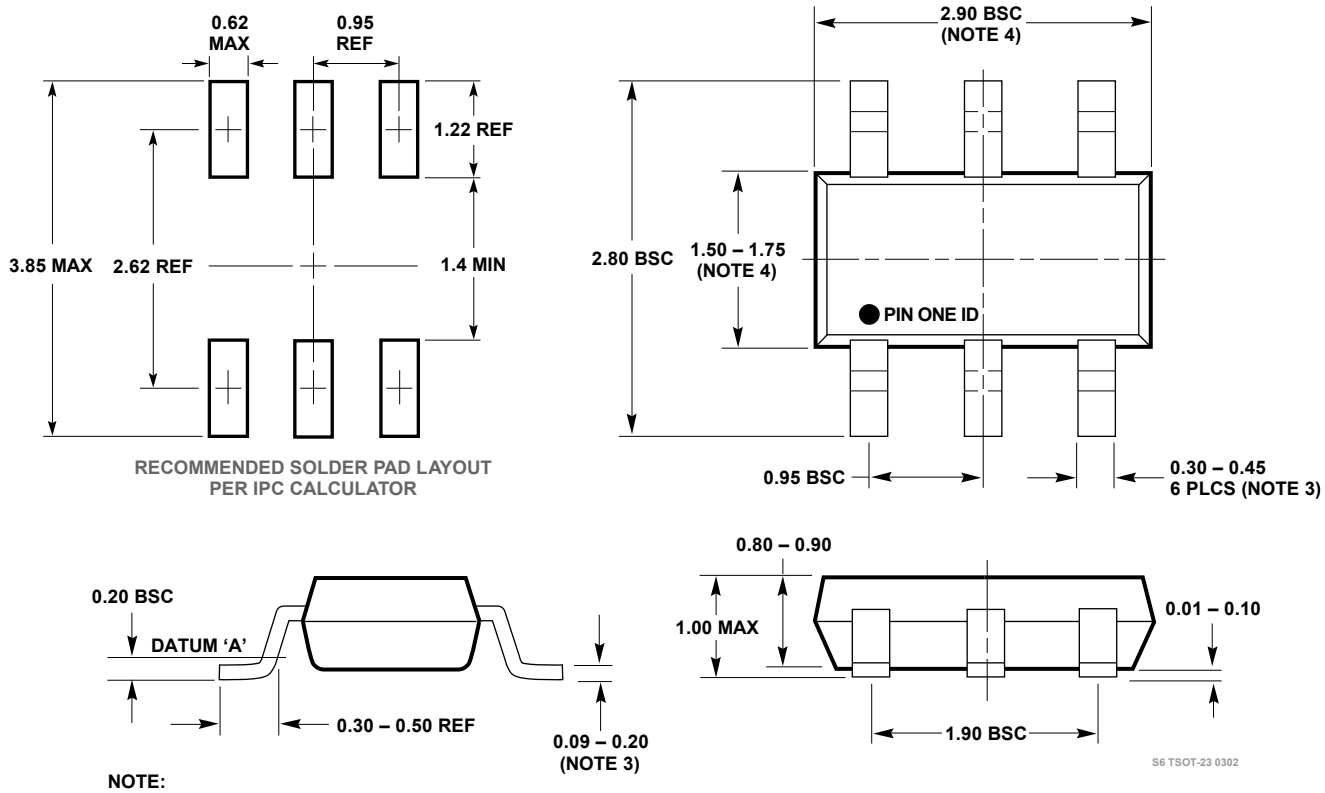
TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
ADPL83200IS6#TRMPBF	ADPL83200IS6#TRPBF	ADHXQ	6-Lead Plastic TSOT-23	–40°C to 85°C

Contact the factory for specified parts with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead-free part marking, refer to *Material Declarations*.

Tape and reel specifications. Some packages are available in 500-unit reels through designated sales channels with the #TRMPBF suffix.

OUTLINE DIMENSIONS



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Figure 20.S6 Package 6-Lead Plastic TSOT-23 (Reference LTC DWG # 05-08-1636)