Data Sheet

ADPL42092

–20V, −200mA, Low-Noise Linear Regulator

FEATURES

- Low Noise: 25µV_{RMS}
- Power Supply Rejection Ratio (PSRR): 55dB at 10kHz at V_{OUT} = −3V
- Positive or Negative Enable Logic
- Stable with small 2.2µF Ceramic Output Capacitor
- Input Voltage Range: −2.7V to −20V
- Maximum Output Current: −200mA
- Low Dropout Voltage: −200mV at −200mA load
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature
  - +2% Maximum/−3% Minimum
- Low Quiescent Current, I_{GND} = −900µA with −200mA load
- Low Shutdown Current: −2µA
- Adjustable Output from −1.22V to $-V_{IN} + V_{DO}$
- Current-Limit and Thermal Overload Protection
- 6-Lead Lead Frame Chip Scale Package (LFCSP) and 5-Lead Thin Small Outline Transistor (TSOT)

APPLICATIONS

- Regulation of Noise-Sensitive Applications
  - Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) circuits, precision amplifiers
- Communications and Infrastructure
- Medical and Healthcare
- Industrial and Instrumentation

GENERAL DESCRIPTION

The **ADPL42092** is a complementary metal-oxide-semiconductor (CMOS) low-dropout (LDO) linear regulator that operates from −2.7V to −20V and provides up to −200mA of output current. This high input voltage LDO is ideal for regulating high performance analog and mixed-signal circuits operating from −19V to −1.2V rails. Using an advanced proprietary architecture, the device provides high power supply rejection and low noise, and achieves excellent line and load-transient response with a small 2.2µF ceramic output capacitor.

The ADPL42092 is available in a fixed output voltage and an adjustable version that allows the output voltage to range from −1.22V to $-V_{IN} + V_{DO}$ using an external feedback divider.

The following fixed output voltages are available as standard options: -1.8V, -2.5V, -5V in TSOT, and -5V in LFCSP.

The ADPL42092 regulator's output noise is 25µV_{RMS}, independent of the output voltage. The enable logic can interface with positive or negative logic levels for maximum flexibility.

The ADPL42092 is available in 5-lead TSOT and 6-lead LFCSP packages for a small, low-profile footprint.

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TYPICAL APPLICATION CIRCUITS

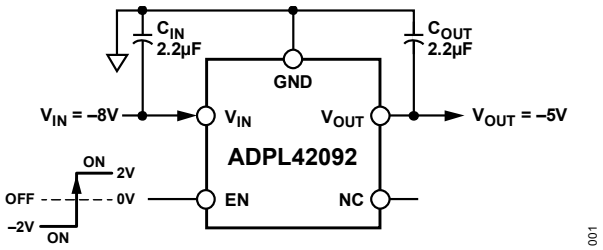

Figure 1. ADPL42092 with Fixed Output Voltage, V_{OUT} = −5V

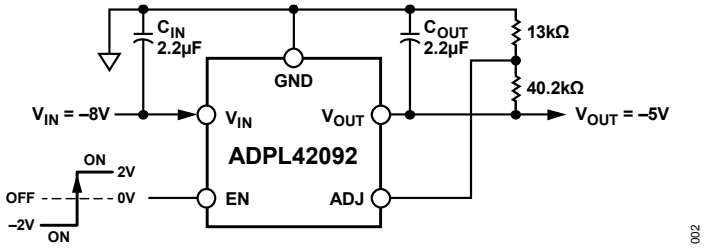

Figure 2. ADPL42092 with Adjustable Output Voltage, V_{OUT} = −5V

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/26	Initial release	—
1	7/26	Updated Table 8. Evaluation Boards	27

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = (V_{OUT} − 0.5V) or −2.7V (whichever is more negative), EN = V_{IN}, I_{OUT} = −10mA, C_{IN} = C_{OUT} = 2.2µF, T_J = −40°C to +125°C for minimum/maximum specifications, T_A = 25°C for typical specifications, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		−2.7		−20	V
Operating Supply Current	I_{GND}	I_{OUT} = 0µA		−45	−53	µA
		I_{OUT} = −10mA		−100	−150	µA
		I_{OUT} = −200mA		−900	−1100	µA
Shutdown Current	I_{GND-SD}	EN = GND		−2		µA
		EN = GND, V_{IN} = −2.7V to −20V			−8	µA
Fixed Output Voltage Accuracy	V_{OUT}	I_{OUT} = −10mA, T_A = 25°C	−1		+1	%
		−1mA < I_{OUT} < −200mA, V_{IN} = (V_{OUT} − 0.5V) to −20V	−3		+2	%
Adjustable Output Voltage Accuracy	V_{ADJ}	I_{OUT} = −10mA	−1.208	−1.22	−1.232	V
		−1mA < I_{OUT} < −200mA, V_{IN} = (V_{OUT} − 0.5V) to −20V	−1.184		−1.244	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} − 0.5V) to −20 V	−0.01		+0.01	%/V
Load Regulation[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = −1mA to −200mA		0.001	0.006	%/mA
ADJ Input Bias Current	ADJ_{I-BIAS}	−1mA < I_{OUT} < −200mA, V_{IN} = (V_{OUT} − 0.5V) to −20V		10		nA
Dropout Voltage[2]	V_{DO}	I_{OUT} = −10mA		−25	−70	mV
		I_{OUT} = −50mA		−46	−90	mV
		I_{OUT} = −200mA		−200	−385	mV
Start-up Time[3]	$t_{START-UP}$	V_{OUT} = −5V		550		µs
		V_{OUT} = −2.8V		375		µs
Current-Limit Threshold[4]	I_{LIMIT}		−230	−350	−500	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C

(V_{IN} = (V_{OUT} − 0.5V) or −2.7V (whichever is more negative), EN = V_{IN}, I_{OUT} = −10mA, C_{IN} = C_{OUT} = 2.2µF, T_J = −40°C to +125°C for minimum/maximum specifications, T_A = 25°C for typical specifications, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
EN THRESHOLD						
Positive Rise	$V_{EN-POS-RISE}$	V_{OUT} = off to on (positive)			1.2	V
Negative Rise	$V_{EN-NEG-RISE}$	V_{OUT} = off to on (negative)	−2.0			V
Positive Fall	$V_{EN-POS-FALL}$	V_{OUT} = on to off (positive)	0.3			V
Negative Fall	$V_{EN-NEG-FALL}$	V_{OUT} = on to off (negative)			−0.55	V
INPUT VOLTAGE LOCKOUT						
Start Threshold	V_{START}		−2.695	−2.49		V
Shutdown Threshold	$V_{SHUTDOWN}$			−2.34	−2.1	V
Hysteresis				150		mV
Output Noise	OUT_{NOISE}	10Hz to 100kHz, V_{OUT} = −1.5V, V_{OUT} = −3V, and V_{OUT} = −5V		25		μV_{RMS}
		10Hz to 100kHz, V_{OUT} = −5V, adjustable mode, C_{NR} = open, R_{NR} = open, R_{FB1} = 147kΩ, and R_{FB2} = 13kΩ		150		μV_{RMS}
		10Hz to 100kHz, V_{OUT} = −5V, adjustable mode, C_{NR} = 100nF, R_{NR} = 13kΩ, R_{FB1} = 147kΩ, and R_{FB2} = 13kΩ		33		μV_{RMS}
Power Supply Rejection Ratio	PSRR	1MHz, V_{IN} = −4V, V_{OUT} = −3V		40		dB
		1MHz, V_{IN} = −6V, V_{OUT} = −5V		32		dB
		100kHz, V_{IN} = −4V, V_{OUT} = −3V		40		dB
		100kHz, V_{IN} = −6V, V_{OUT} = −5V		45		dB
		10kHz, V_{IN} = −4V, V_{OUT} = −3V		55		dB
		10kHz, V_{IN} = −6V, V_{OUT} = −5V		66		dB

(V_{IN} = (V_{OUT} − 0.5V) or −2.7V (whichever is more negative), EN = V_{IN}, I_{OUT} = −10mA, C_{IN} = C_{OUT} = 2.2µF, T_J = −40°C to +125°C for minimum/maximum specifications, T_A = 25°C for typical specifications, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
		1MHz, V_{IN} = −16V, V_{OUT} = −15V, adjustable mode, C_{NR} = 100nF, R_{NR} = 13kΩ, R_{FB1} = 13kΩ, R_{FB2} = 147kΩ		45		dB
		100kHz, V_{IN} = −16V, V_{OUT} = −15V, adjustable mode, C_{NR} = 100nF, R_{NR} = 13kΩ, R_{FB1} = 13kΩ, R_{FB2} = 147kΩ		45		dB
		10kHz, V_{IN} = −16V, V_{OUT} = −15V, adjustable mode, C_{NR} = 100nF, R_{NR} = 13kΩ, R_{FB1} = 13kΩ, R_{FB2} = 147kΩ		66		dB

1 Based on an endpoint calculation using −1mA and −200mA loads. See *Figure 8* for the typical load regulation performance for loads less than 1mA.

2 Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages below −3V.

3 Start-up time is defined as the time from the rising edge of EN to the time at which V_{OUT} reaches 90% of its nominal value.

4 The current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current-limit for a −5V output voltage is defined as the current that causes the output voltage to drop to 90% of −5V, or −4.5V.

Input and Output Capacitance, Recommended Specifications

Table 2. Input and Output Capacitors, Recommended Specifications

PARAMETER	SYMBOL	TEST CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CAPACITANCE						
Minimum Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	1.5	2.2		µF
Capacitor Effective Series Resistance (ESR)	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

[1]The minimum input and output capacitance must be greater than 1.5µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} to GND	+0.3V to -22V
V_{OUT} to GND	0.3 to V_{IN}
EN to GND	5V to V_{IN}
EN to V_{IN}	+30V to –30V
ADJ to GND	+0.3 to V_{OUT}
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Operating Ambient Temperature Range	–40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Data

Absolute maximum ratings apply to each parameter individually and must not be combined. The ADPL42092 can be damaged if the junction temperature exceeds its limits. Monitoring ambient temperature does not guarantee that junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit, provided the junction temperature remains within specification limits. The T_J of the device depends on the ambient temperature (T_A), the device's power dissipation (P_D), and the package's junction-to-ambient thermal resistance (θ_{JA}).

Maximum T_J is calculated from T_A and P_D using the following formula:

$$T_J = T_A + (P_D \times \vartheta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout.

In applications with high maximum power dissipation, close attention to thermal board design is required. The value of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. Refer to the JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, refer to the AN-617 Application Note: MicroCSP™ Wafer-Level Chip Scale Package.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The package's Ψ_{JB} is based on modeling and calculations using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are distinct from thermal resistances. The Ψ_{JB} parameter represents the component power dissipated through multiple thermal paths, whereas the single-path assumption of the θ_{JB} thermal resistance applies only to a single path. Therefore, Ψ_{JB} thermal paths include convection from the top of the package and radiation from the package, both of which make Ψ_{JB} more useful in real-world applications. Maximum junction temperature is calculated from the board temperature (T_B) and power dissipation using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to the JESD51-8 and JESD51-12 for more detailed information on Ψ_{JB}.

Thermal Resistance

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

PACKAGE TYPE	θ_{JA}	θ_{JC}	Ψ_{JB}	UNITS
6-Lead LFCSP	68.9	42.29	44.1	°C/W
5-Lead TSOT	170	Not applicable	43	°C/W

Electrostatic Discharge (ESD)

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

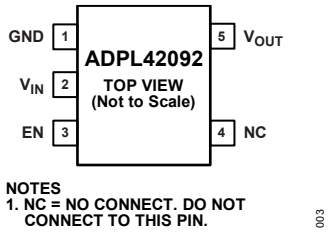

Figure 3. 5-Lead TSOT Pin Configuration, Fixed Output Voltage

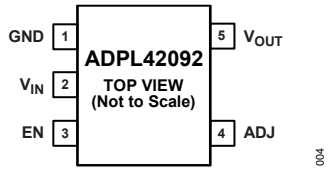

Figure 4. 5-Lead TSOT Pin Configuration, Adjustable Output Voltage

Pin Descriptions

Table 5. 5-Lead TSOT Pin Function Descriptions

TSOT PIN NO.		NAME	DESCRIPTION
FIXED OUTPUT VOLTAGE	ADJUSTABLE OUTPUT VOLTAGE		
1	1	GND	Ground.
2	2	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 2.2µF or greater capacitor.
3	3	EN	Drive EN 2V above or below ground to enable the regulator, or drive EN to ground to turn off the regulator. For automatic startup, connect EN to V_{IN}.
4	Not Applicable	NC	No Connect. Do not connect to this pin.
Not Applicable	4	ADJ	Adjustable Input. An external resistor divider sets the output voltage.
5	5	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 2.2µF or greater capacitor.

NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO V_{IN} INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE V_{IN} PLANE ON THE BOARD FOR PROPER OPERATION. BECAUSE THIS IS A NEGATIVE VOLTAGE REGULATOR, V_{IN} IS THE MOST NEGATIVE POTENTIAL IN THE CIRCUIT.

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Figure 5. 6-Lead LFCSP Pin Configuration, Fixed Output Voltage

NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD ON THE BOTTOM OF THE LFCSP PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO V_{IN} INSIDE THE PACKAGE. THE EXPOSED PAD MUST BE CONNECTED TO THE V_{IN} PLANE ON THE BOARD FOR PROPER OPERATION. BECAUSE THIS IS A NEGATIVE VOLTAGE REGULATOR, V_{IN} IS THE MOST NEGATIVE POTENTIAL IN THE CIRCUIT.

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Figure 6. 6-Lead LFCSP Pin Configuration, Adjustable Output Voltage

Pin Descriptions

Table 6. 6-Lead LFCSP Pin Function Descriptions

LFCSP PIN NO.		NAME	DESCRIPTION
FIXED OUTPUT VOLTAGE	ADJUSTABLE OUTPUT VOLTAGE		
1	1	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 2.2µF or greater capacitor.
Not Applicable	2	ADJ	Adjustable Input. An external resistor divider sets the output voltage.
3	3	EN	Drive EN 2V above or below ground to enable the regulator, or drive EN to ground to turn off the regulator. For automatic startup, connect EN to V_{IN}.
2, 4	4	NC	No Connect. Do not connect to this pin.
5	5	GND	Ground.
6	6	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 2.2µF or greater capacitor.
7	7	EPAD	Exposed pad. The exposed pad on the bottom of the LFCSP package enhances thermal performance and is electrically connected to V_{IN} inside the package. The exposed pad must be connected to the V_{IN} plane on the board for proper operation. Because this is a negative voltage regulator, V_{IN} is the most negative potential in the circuit.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = −3.5V, V_{OUT} = −3V, I_{OUT} = −10mA, C_{IN} = C_{OUT} = 2.2µF, T_A = 25°C, unless otherwise noted.

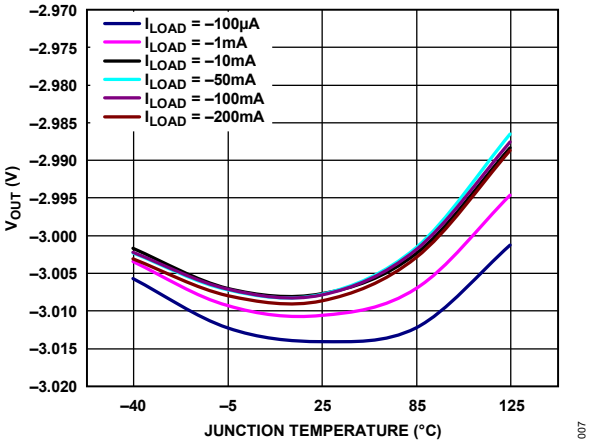

Figure 7. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J)

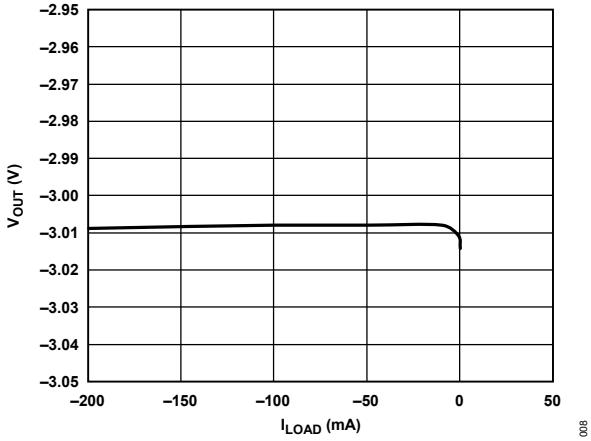

Figure 8. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

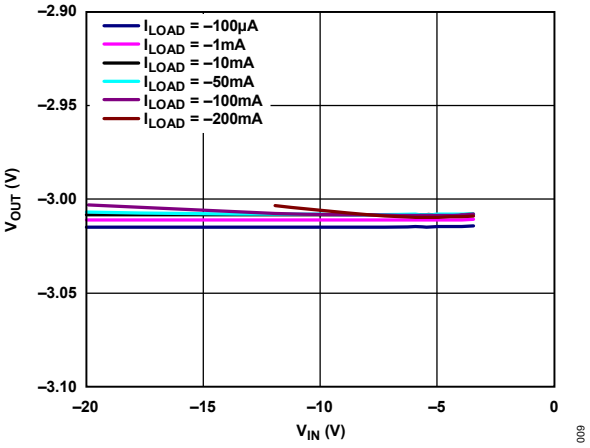

Figure 9. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

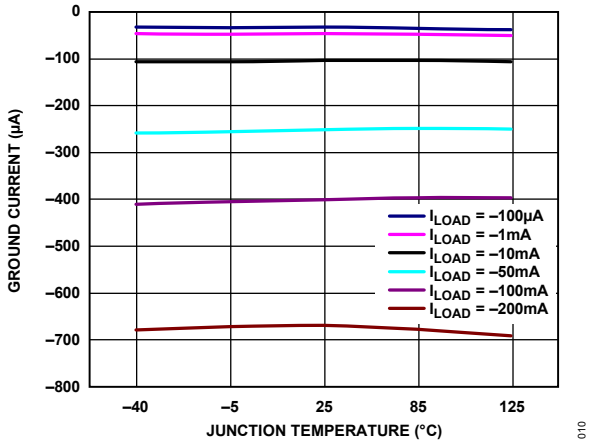

Figure 10. Ground Current vs. Junction Temperature (T_J)

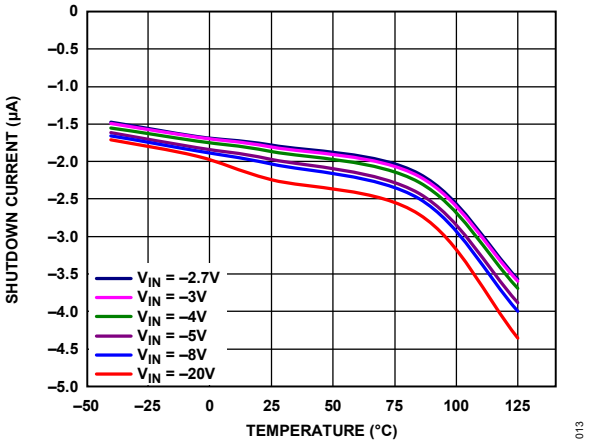

Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

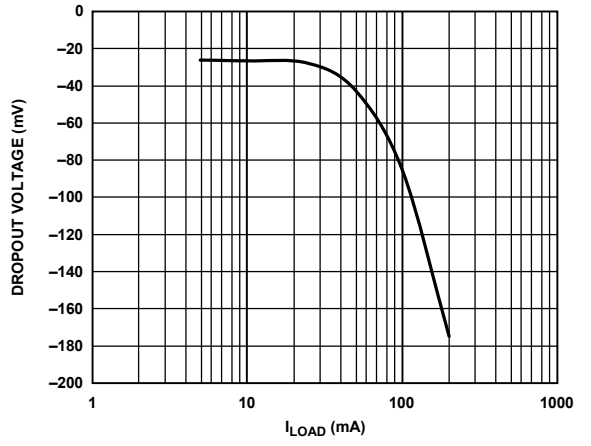

Figure 12. Dropout Voltage vs. Load Current (I_{LOAD})

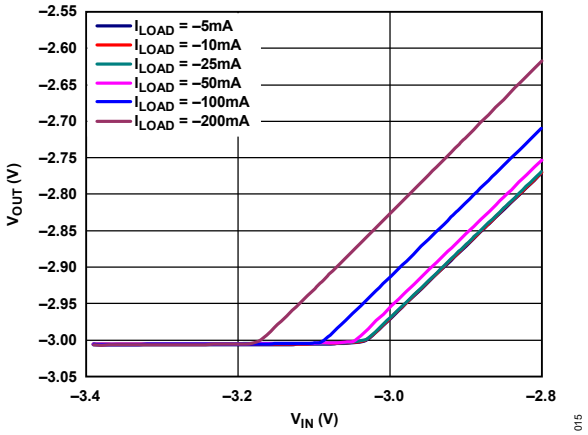

Figure 13. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout

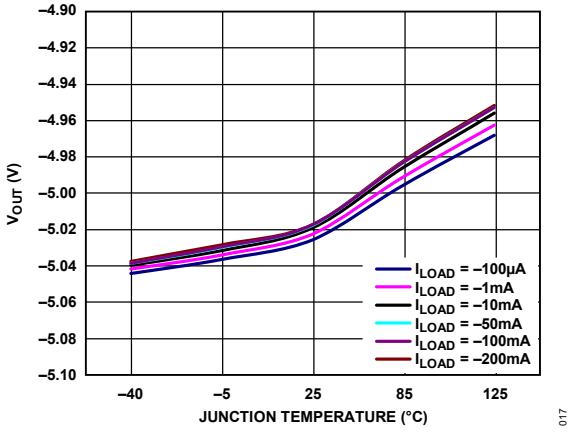

Figure 14. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = –5V

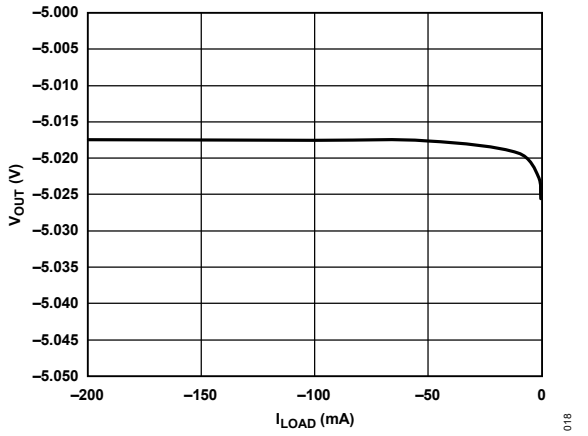

Figure 15. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = –5V

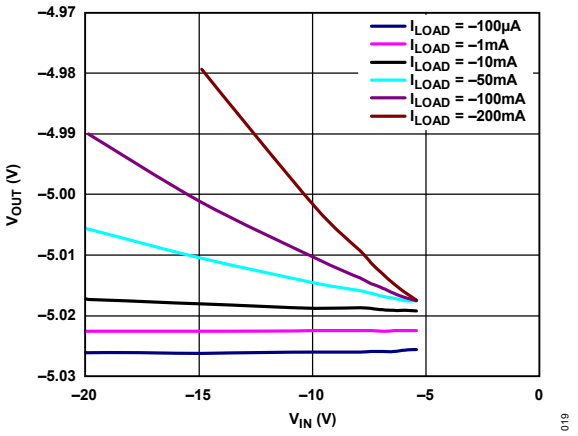

Figure 16. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = –5V

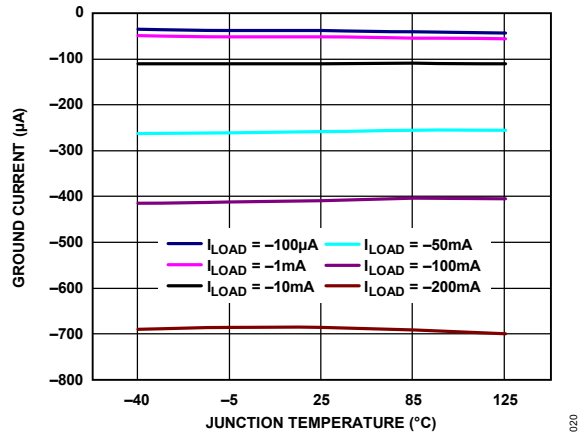

Figure 17. Ground Current vs. Junction Temperature (T_J), V_{OUT} = –5V

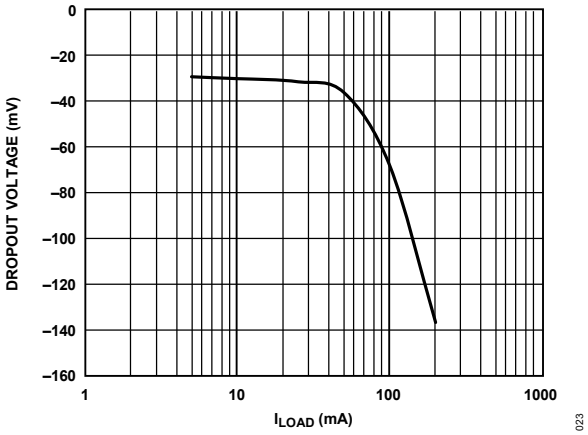

Figure 18. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = –5V

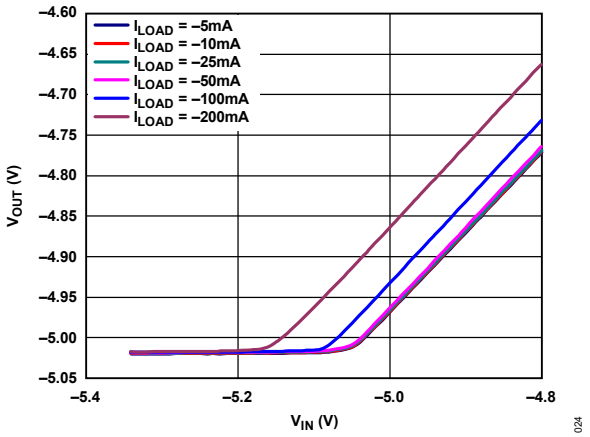

Figure 19. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = −5V

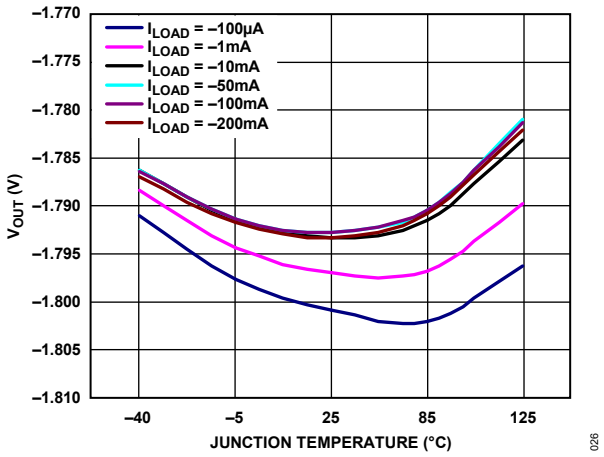

Figure 20. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = −1.8V

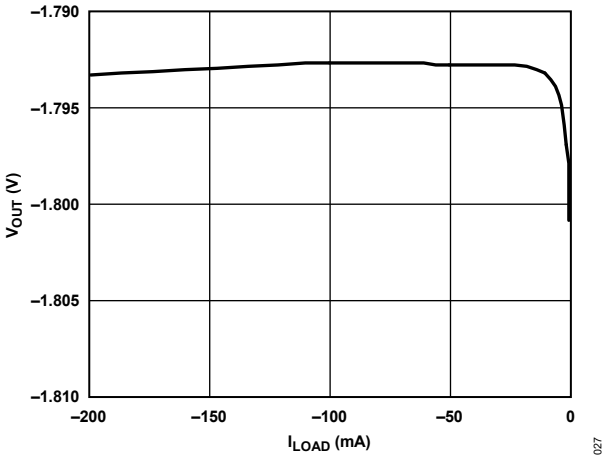

Figure 21. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = −1.8V

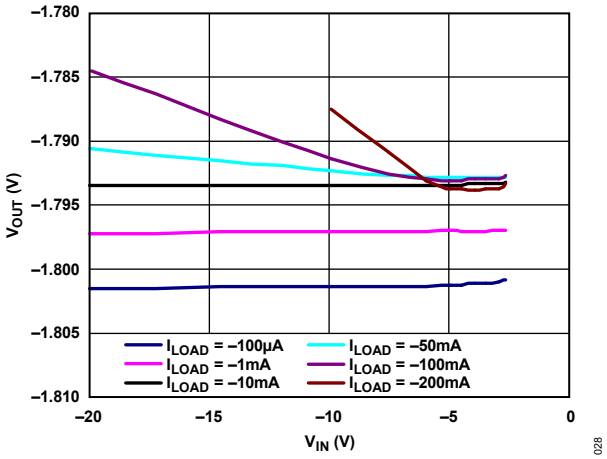

Figure 22. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = −1.8V

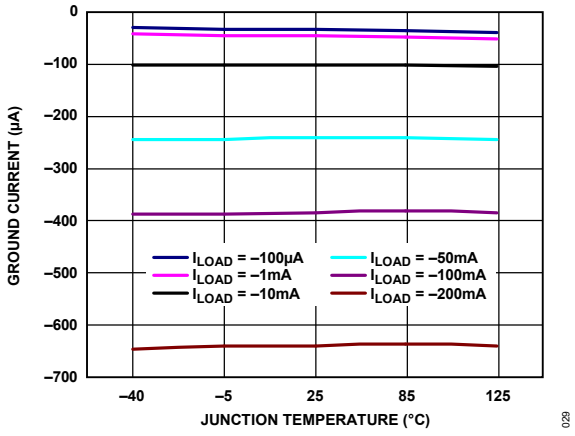

Figure 23. Ground Current vs. Junction Temperature (T_J), V_{OUT} = −1.8V

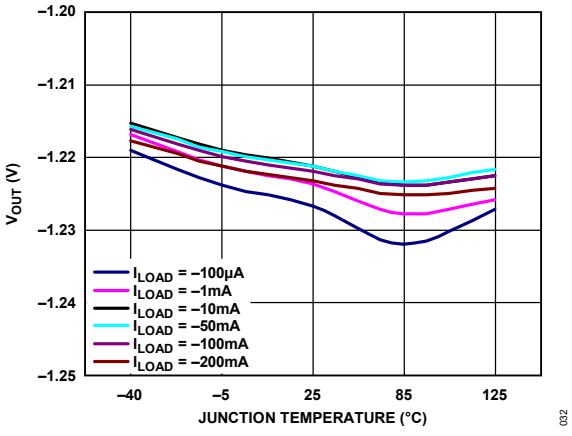

Figure 24. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = −1.22V

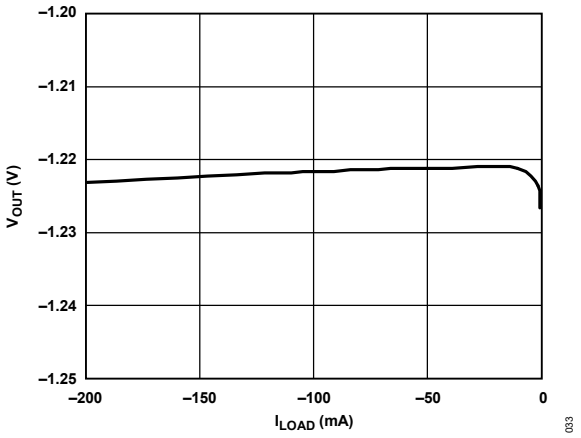

Figure 25. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = −1.22V

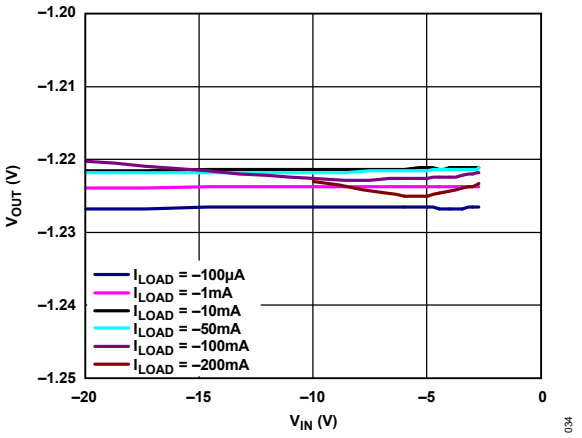

Figure 26. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = −1.22V

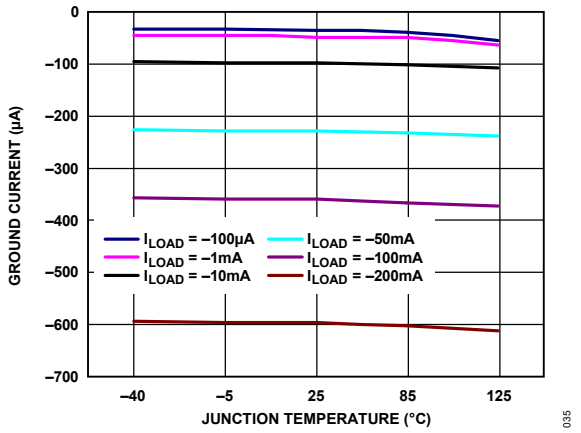

Figure 27. Ground Current vs. Junction Temperature (T_J), V_{OUT} = −1.22V

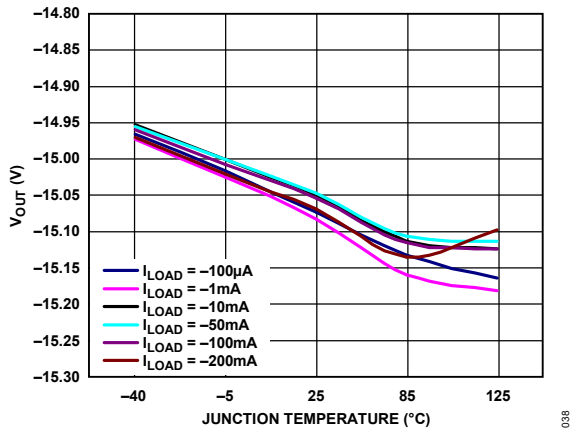

Figure 28. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), Adjustable Output Voltage, V_{OUT} = −15V

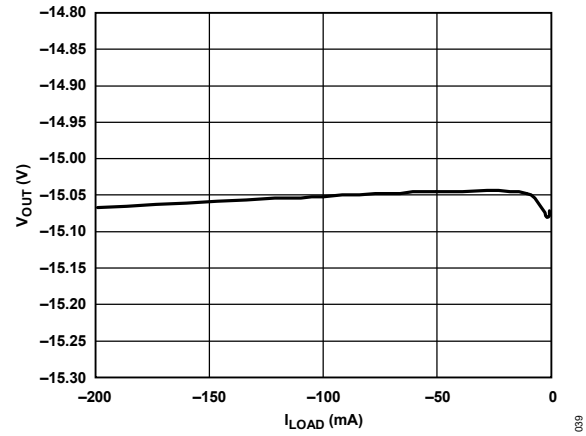

Figure 29. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), Adjustable Output Voltage, V_{OUT} = −15V

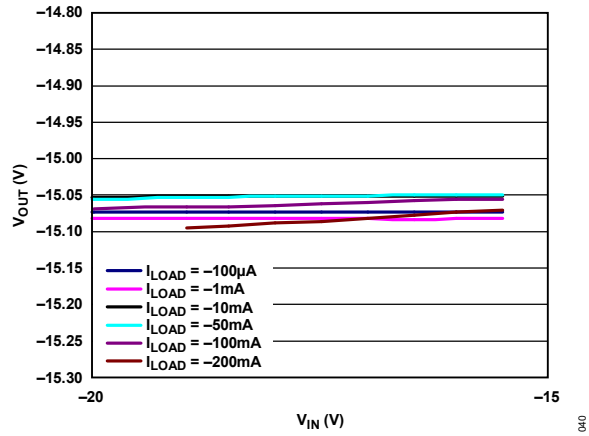

Figure 30. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), Adjustable Output Voltage, V_{OUT} = −15V

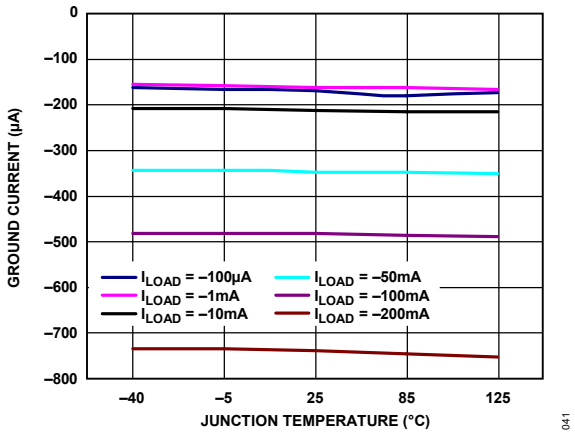

Figure 31. Ground Current vs. Junction Temperature (T_J), Adjustable Output Voltage, V_{OUT} = −15V

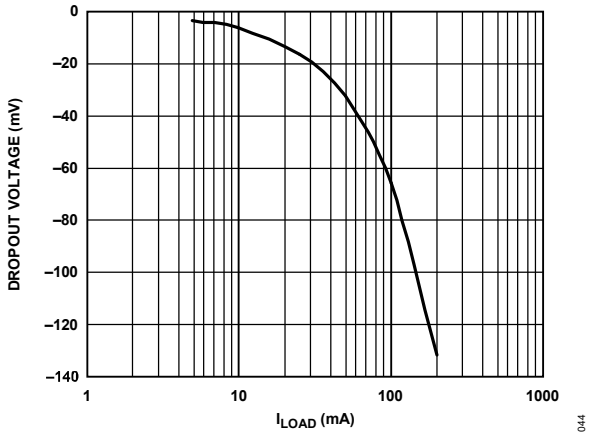

Figure 32. Dropout Voltage vs. Load Current (I_{LOAD}), Adjustable Output Voltage, V_{OUT} = −15V

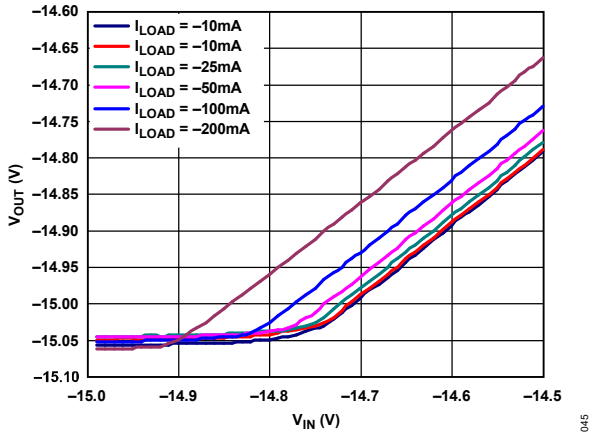

Figure 33. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, Adjustable Output Voltage, V_{OUT} = −15V

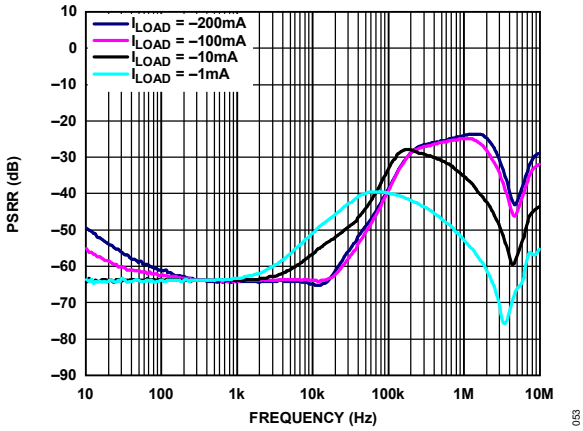

Figure 34. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −3V vs. Different Load Currents (I_{LOAD}), V_{IN} = −4.0V

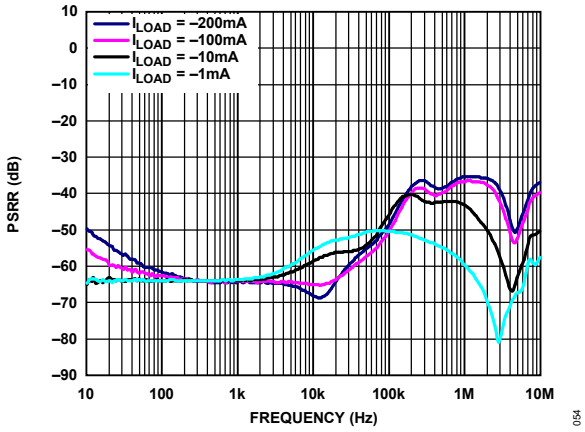

Figure 35. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = −3V vs. Different Load Currents (I_{LOAD}), V_{IN} = −5.5V

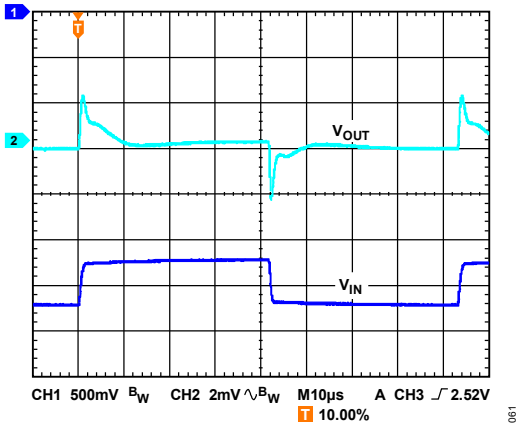

Figure 36. Line Transient Response, 500mV Step, V_{OUT} = −1.22V, I_{LOAD} = −200mA

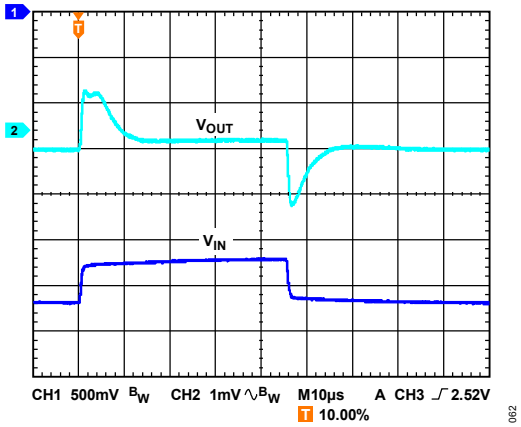

Figure 37. Line Transient Response, 500mV Step, V_{OUT} = −1.22V, I_{LOAD} = −10mA

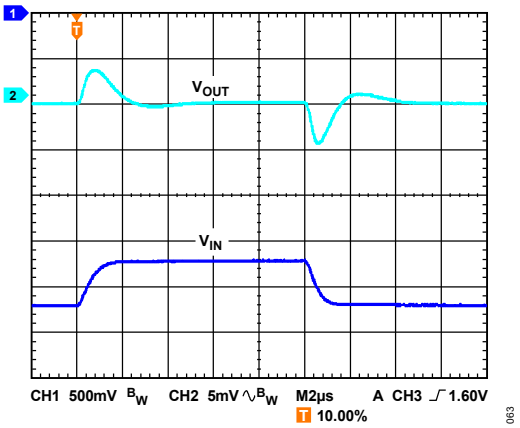

Figure 38. Line Transient Response, 500mV Step, V_{OUT} = −1.8V, I_{LOAD} = −200mA

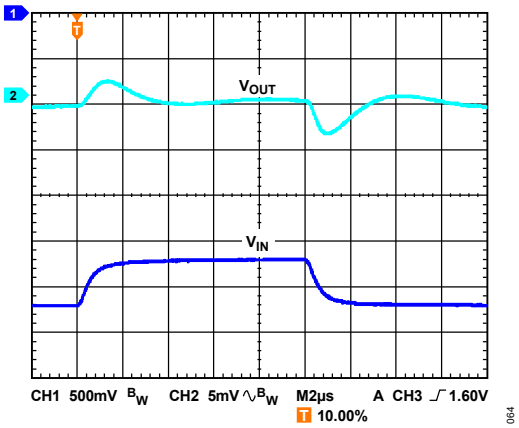

Figure 39. Line Transient Response, 500mV Step, V_{OUT} = −1.8V, I_{LOAD} = −10mA

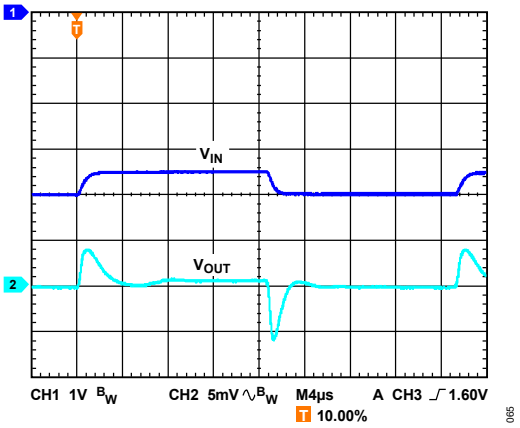

Figure 40. Line Transient Response, 500mV Step, V_{OUT} = −3V, I_{LOAD} = −200mA

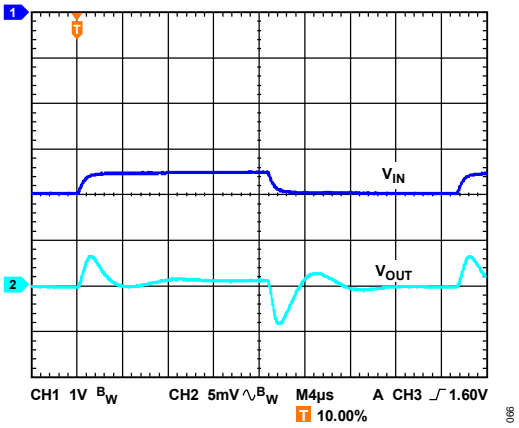

Figure 41. Line Transient Response, 500mV Step, V_{OUT} = −3V, I_{LOAD} = −10mA

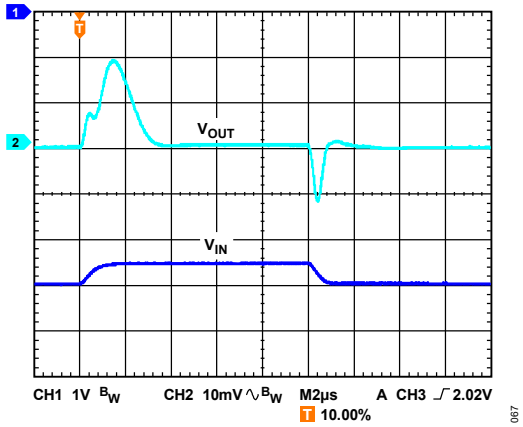

Figure 42. Line Transient Response, 500mV Step, V_{OUT} = −5V, I_{LOAD} = −200mA

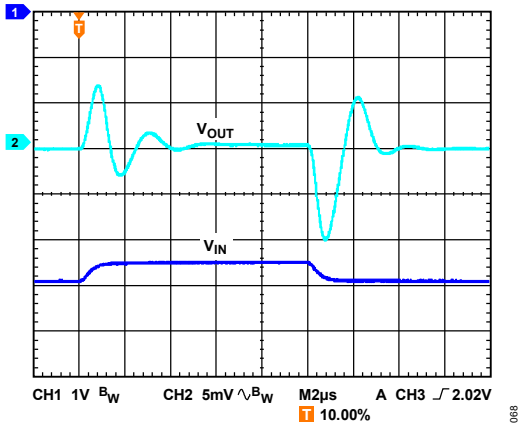

Figure 43. Line Transient Response, 500mV Step, V_{OUT} = −15V, Noise Reduction Network, I_{LOAD} = −10mA

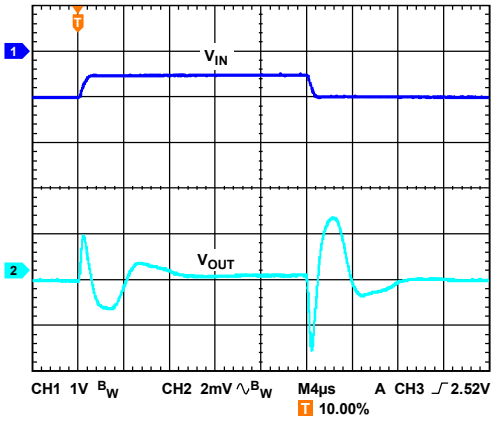

Figure 44. Line Transient Response, 500mV Step, V_{OUT} = −5V, I_{LOAD} = −10mA

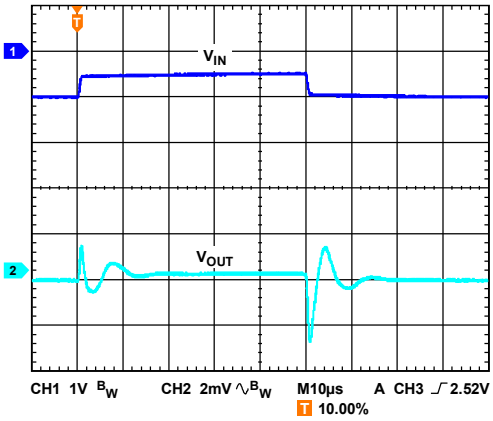

Figure 45. Load Transient Response, V_{OUT} = −1.22V, I_{LOAD} = −1mA to −200mA, Load Step = 1A/µs

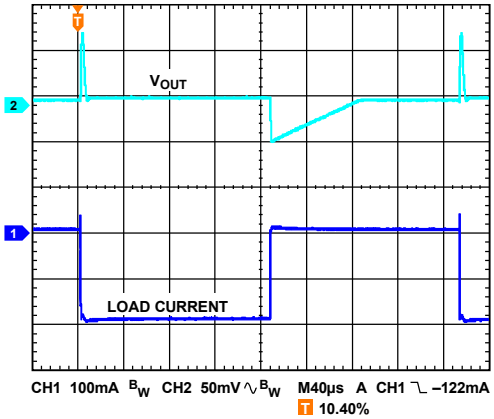

Figure 46. Line Transient Response, 500mV Step, V_{OUT} = −15V, Noise Reduction Network, I_{LOAD} = −200mA

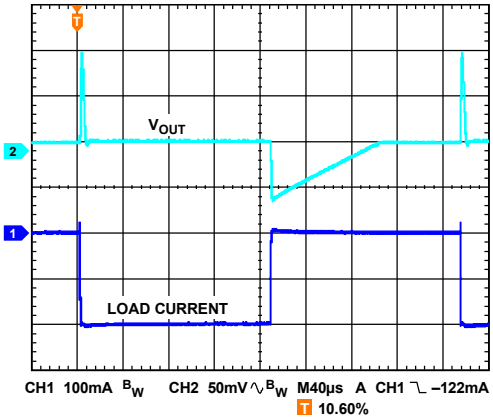

Figure 47. Load Transient Response, V_{OUT} = −3V, I_{LOAD} = −1mA to −200mA, Load Step = 1A/µs

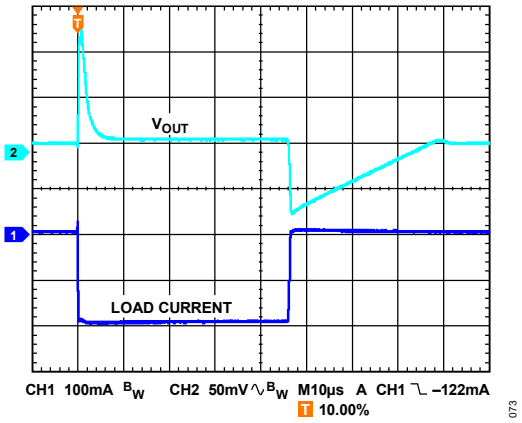

Figure 48. Load Transient Response, V_{OUT} = −5V, I_{LOAD} = −1mA to −200mA, Load Step = 1A/µs

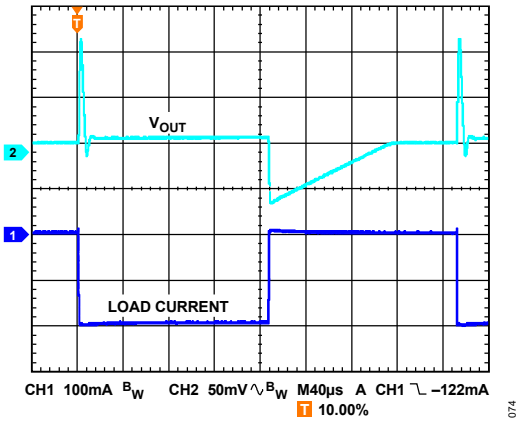

Figure 49. Load Transient Response, V_{OUT} = −15V, I_{LOAD} = −1mA to −200 mA, Load Step = 1A/µs, Noise Reduction Network

THEORY OF OPERATION

The ADPL42092 is a low-quiescent-current LDO linear regulator that operates from −2.7V to −20V and can provide up to −200mA of output current. Drawing a low quiescent current of -900µA (typical) at full load makes the ADPL42092 ideal for battery-powered portable equipment. The maximum shutdown current is −8µA at room temperature.

The device is optimized for use with small 2.2µF ceramic capacitors; the ADPL42092 provides an excellent transient performance.

Internally, the ADPL42092 consists of a reference, an error amplifier, a feedback voltage divider, and an n-channel metal-oxide-semiconductor (NMOS) pass transistor. The output current is delivered through the NMOS pass transistor, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is more positive than the reference voltage, the NMOS transistor's gate is pulled toward GND, allowing more current to flow and increasing the output voltage. If the feedback voltage is more negative than the reference voltage, the NMOS transistor's gate is pulled toward $-V_{IN}$, reducing the current and lowering the output voltage.

Adjustable Mode of Operation

The ADPL42092 is available in fixed and adjustable output voltage versions, with the output voltage set between −1.22V and −19V using an external voltage divider. The output voltage can be set according to the following formula:

$$-V_{OUT} = -1.22V\ (1 + R_{FB1}/R_{FB2})$$

where R_{FB1} and R_{FB2} are the resistors in the output voltage divider, as shown in *Figure 50*.

R_{FB2} must be less than 120kΩ to minimize output voltage errors caused by the leakage current of the ADJ pin. The error voltage caused by the ADJ pin leakage current is the parallel combination of R_{FB1} and R_{FB2} multiplied by the ADJ pin leakage current.

For example, when $R_{FB1} = R_{FB2} = 120k\Omega$, the output voltage is −2.44V, and the error due to the typical ADJ pin leakage current (10nA) is 60kΩ x 10nA, or 0.6mV. This example results in an output voltage error of 0.0245%.

Adding a small capacitor (~100 pF) in parallel with R_{FB1} can improve the stability of the ADPL42092. Larger capacitance values also reduce noise and improve PSRR. See the *Noise Reduction of the Adjustable ADPL42092* section for more details.

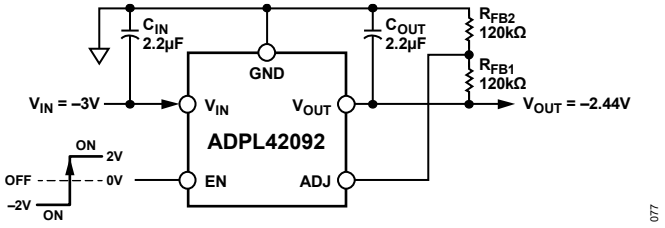

Figure 50. Setting Adjustable Output Voltage

APPLICATIONS INFORMATION

Design Tools

The ADPL42092 is supported by the LTpowerCAD® and LTspice® design tools to produce complete power designs and simulations. Refer to the **ADPL42092 product page** for more information on design tools.

Capacitor Selection

Output Capacitor

The ADPL42092 is optimized for use with small, space-efficient ceramic capacitors, but is also compatible with most commonly used capacitor types, provided the equivalent series resistance (ESR) is taken into consideration. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum capacitance of 2.2µF and an ESR of 0.2Ω or less are recommended to ensure the device's stability. The transient response to changes in load current is also affected by the output capacitance. Using a higher output capacitance improves the device's transient response to large changes in load current. *Figure 51* shows the transient responses for an output capacitance value of 2.2µF.

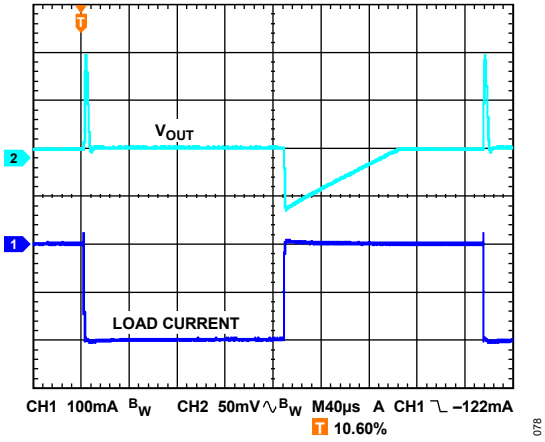

Figure 51. Output Transient Response, C_{OUT} = 2.2µF

Input Bypass Capacitor

Connecting a 2.2µF capacitor from V_{IN} to GND reduces the circuit sensitivity to PCB layout, particularly when long input traces or high source impedance are encountered. When the output capacitance exceeds 2.2µF, increase the input capacitance accordingly to maintain proper operation.

Enable Pin Operation

The ADPL42092 uses the EN pin to enable and disable the V_{OUT} pin under normal operating conditions. When EN is at ±2V with respect to GND, V_{OUT} turns on, and when EN is at 0V, V_{OUT} turns off. For automatic startup, EN can be connected to V_{IN}. When the device is disabled, a ~220kΩ resistor connects to the V_{OUT} pin, pulling it up to GND.

The device provides a dual-polarity enable pin (EN) that turns on the LDO when $|V_{EN}| \geq 2V$. The enable voltage can be either positive or negative with respect to ground.

Figure 52 shows the typical hysteresis of the EN pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points. *Figure 53* shows typical EN thresholds when the input voltage varies from −2.7V to −20V.

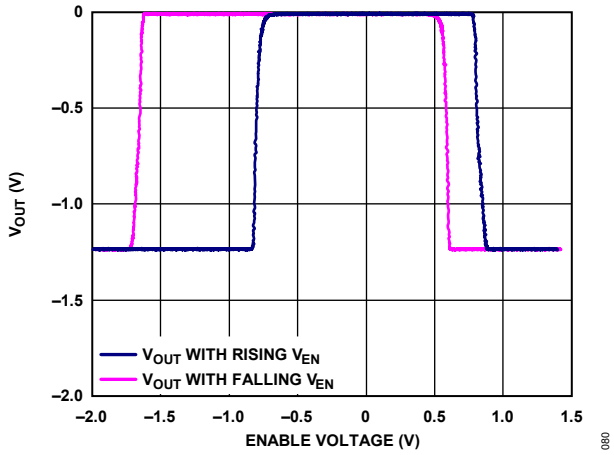

Figure 52. Typical EN Pin Operation

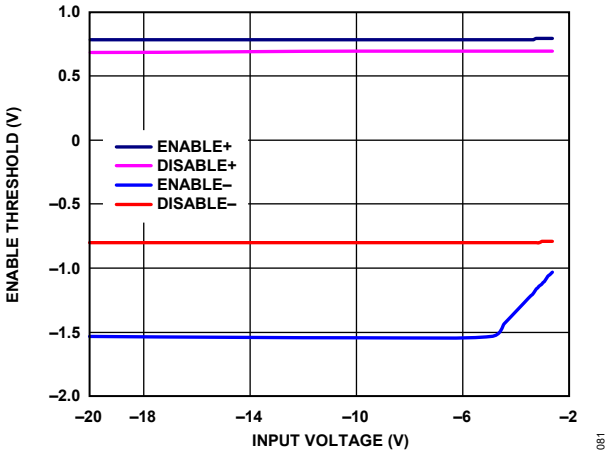

Figure 53. Typical EN Pin Threshold vs. Input Voltage

Figure 54 and *Figure 55* show the start-up behavior for a −5V output with positive and negative-going enable signals.

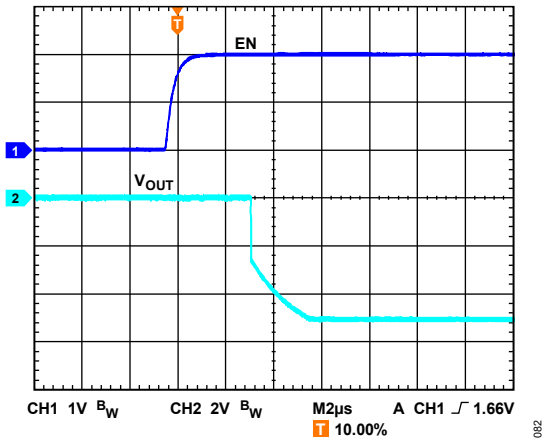

Figure 54. Typical Start-Up Behavior, Positive going Enable

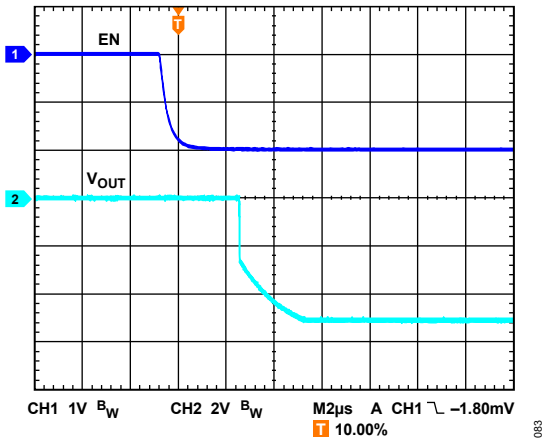

Figure 55. Typical Start-Up Behavior, Negative going Enable

Soft-Start

The ADPL42092 uses an internal soft-start to limit the inrush current when the output is enabled. The start-up time for the −5V option is approximately 550µs from the time the EN active threshold is crossed to the time the output reaches 90% of its final value. As shown in *Figure 56*, the start-up time depends on the output voltage setting.

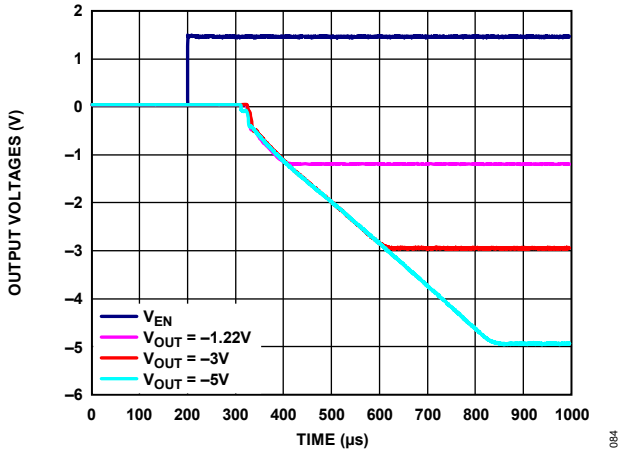

Figure 56. Typical Start-Up Behavior in Different Output Voltages

Noise Reduction of the Adjustable ADPL42092

The ultralow output noise of the fixed output ADPL42092 is achieved by keeping the LDO error amplifier at unity gain and setting the reference voltage to the output voltage. This architecture is not suitable for an adjustable output voltage LDO. The adjustable output ADPL42092 uses a more conventional architecture in which the reference voltage is fixed and the error amplifier gain is a function of the output voltage. The disadvantage of the conventional LDO architecture is that the output voltage noise is proportional to the output voltage.

The adjustable LDO circuit can be slightly modified to reduce the output voltage noise to levels close to those of the ADPL42092's fixed output. The circuit shown in *Figure 57* adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_{FB1} to reduce the AC gain of the error amplifier. R_{NR} is chosen to be nearly equal to R_{FB2}; this limits the AC gain of the error amplifier to approximately 6dB. The actual gain is the parallel combination of R_{NR} and R_{FB1} divided by R_{FB2}. This resistance ensures that the error amplifier always operates at a gain greater than unity.

C_{NR} is chosen by setting the reactance of C_{NR} equal to R_{FB1} − R_{NR} at a frequency between 10Hz and 100Hz. This capacitance sets the frequency at which the AC gain of the error amplifier drops by 3dB from the DC gain.

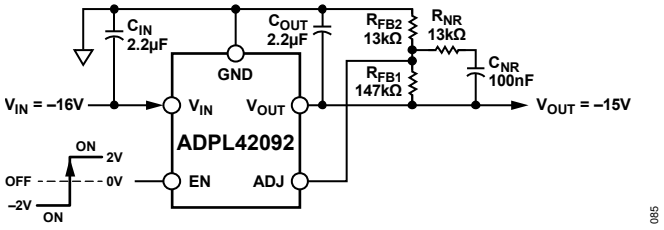

Figure 57. Noise Reduction Modification to Adjustable LDO

Current-Limit and Thermal Overload Protection

The ADPL42092 is protected against damage from excessive power dissipation by current-limit and thermal overload protection circuits. The ADPL42092 is designed to limit current when the output load reaches −350mA (typical). When the output load exceeds −350mA, the output voltage is reduced to maintain a constant current-limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (for example, high ambient temperature and high power dissipation), if the junction temperature exceeds 150°C, the output is turned off, reducing the output current to 0mA. When the junction temperature drops below 135°C, the output turns back on, and the output current returns to its nominal value.

For example, a hard short from V_{OUT} to ground occurs. Initially, the ADPL42092 limits the current so that only −350mA flows into the short. If self-heating at the junction is sufficient to raise the temperature above 150°C, thermal shutdown is activated, turning off the output and reducing the output current to 0mA. As the junction temperature cools and falls below 135°C, the output turns on and conducts −350mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between −350mA and 0mA that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperatures do not exceed 125°C.

PCB Layout Considerations

Place the input capacitor as close as possible to the V_{IN} and GND pins. Place the output capacitor as close as possible to the V_{OUT} and GND pins. The use of 1206- or 0805-size capacitors and resistors achieves the smallest possible footprint on boards with limited space.

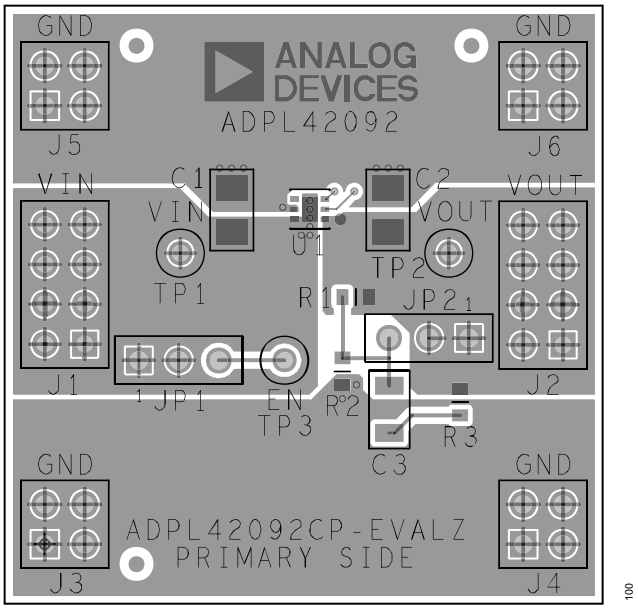

Figure 58. Example of a 6-Lead LFCSP PCB Layout

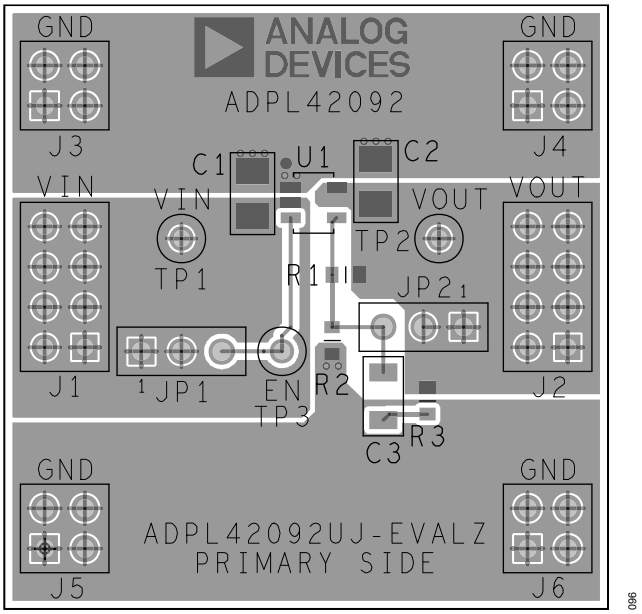

Figure 59. Example of a 5-Lead TSOT PCB Layout

OUTLINE DIMENSIONS

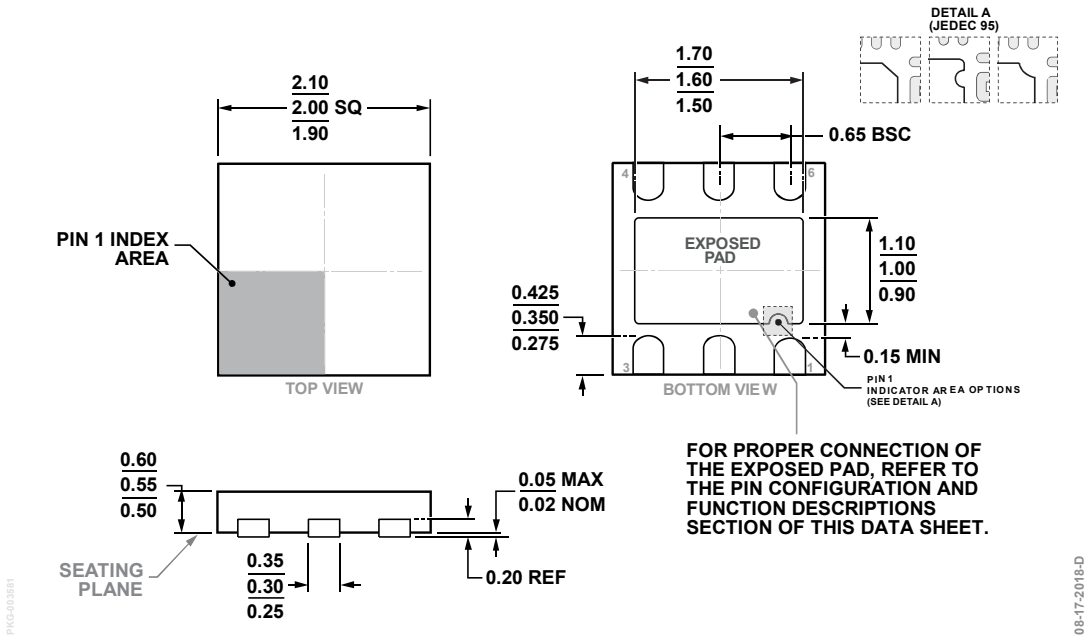

Figure 60. 6-Lead LFCSP 2mm × 2mm Body and 0.55mm Package Height (CP-6-3), Dimensions shown in millimeters

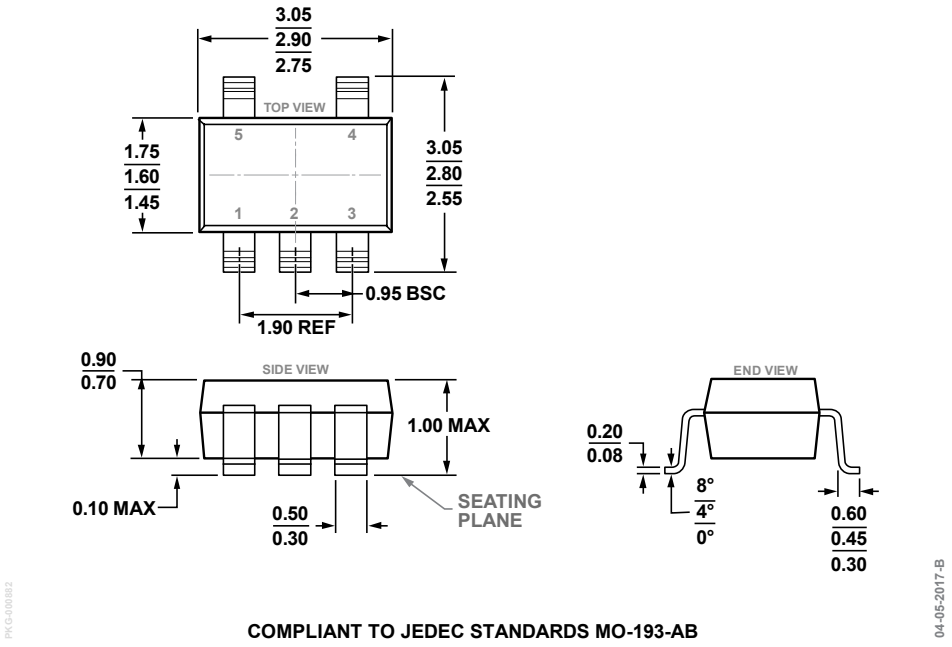

Figure 61. 5-Lead TSOT (UJ-5), Dimensions shown in millimeters

ORDERING GUIDE

Table 7. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	OUTPUT VOLTAGE (V)[2]	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING CODE
ADPL42092AUJZ-R7	-40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	LYA
ADPL42092AUJZ-1.8-R7	-40°C to +125°C	–1.8	5-Lead TSOT	UJ-5	LYE
ADPL42092AUJZ-2.5-R7	-40°C to +125°C	–2.5	5-Lead TSOT	UJ-5	LYD
ADPL42092AUJZ-5.0-R7	-40°C to +125°C	–5	5-Lead TSOT	UJ-5	LYB
ADPL42092ACPZN-R7	-40°C to +125°C	Adjustable	6-Lead LFCSP	CP-6-3	K6
ADPL42092ACPZN-5.0-R7	-40°C to + 125°C	–5	6-Lead LFCSP	CP-6-3	K5

[1] Z = RoHS-compliant part.
[2] For additional output voltage options, contact your local Analog Devices Inc. sales or distribution representative.

Table 8. Evaluation Boards

MODEL[1, 2]	PACKAGE DESCRIPTION
ADPL42092CP-EVALZ	LFCSP Evaluation Board
ADPL42092UJ-EVALZ	TSOT Evaluation Board

[1] Z = RoHS-compliant part.
[2] The evaluation boards are preconfigured with an adjustable ADPL42092.

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