5.5V, 500mA LDO Linear Regulator with Low-Power Mode

ADPL40505A

General Description

The ADPL40505A is a 5.5V, P-Channel Metal-Oxide Semiconductor (PMOS) Low Drop-Out (LDO) linear regulator that delivers up to 500mA load current. The ADPL40505A features a low-power mode of operation that consumes very low quiescent current from the supply.

The regulator is fully protected from damage by internal circuitry that provides programmable inrush current limiting, output overcurrent limiting, reverse current limiting, and thermal overload protection. The ADPL40505A has an 800Ω active discharge feature to quickly discharge output capacitors.

The ADPL40505A provides enhanced flexibility with an adjustable output voltage in the range of 0.8V to 5.0V by using two external feedback resistors.

The ADPL40505A is available in an 8-pin, 2mm x 2mm Thin Dual Flat No-Lead (TDFN) package.

Applications

- Mobile Phones
- Digital Camera and Audio Devices
- Portable and Battery-Powered Equipment

Features

- 1.7V to 5.5V Input Supply Range
- 0.8V to 5.0V Output Voltage Range
- 500mA Maximum Output Current
- 120mV Maximum Dropout at 500mA Load ($3.6V_{IN}$)
- 20µA No-Load Supply Current in Low-Power Mode
- 350µA Supply Current in Normal Mode
- <1µA Shutdown Supply Current
- $45\mu V_{RMS}$ Output Noise, 10Hz to 100kHz
- 60dB PSRR at 10kHz, 250mA Load Current, and 300mV Input and Output Voltage Separation
- ±2% DC Accuracy Over Load, Line, and Temperature Variations
- Active Discharge of 800Ω at OUT
- Stable with 2µF (Minimum Effective) Output Capacitance
- Programmable Soft-Start Rate
- Overcurrent and Overtemperature Protection
- Reverse-Current Protection
- Power-OK Output
- 2mm x 2mm, 8-Pin TDFN Package
- -40°C to +125°C Operating Temperature

***Ordering Information* appears at end of data sheet**

Application Diagram

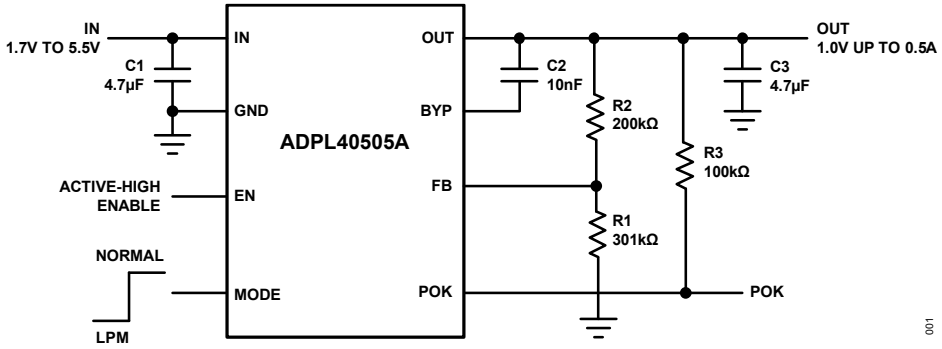


Figure 1. Application Diagram

19-102051; Rev 0; 10/25

TABLE OF CONTENTS

Absolute Maximum Ratings

IN, OUT, EN, FB to GND .....-0.3V to 6V

MODE, BYP, POK to GND .....-0.3V to 6V

Output Short-Circuit Duration .....Continuous

Continuous Power Dissipation (T_A = +70°C) .....

TDFN (derate 11.7mW/°C above +70°C) 937.9mW

Operating Junction Temperature Range .....-40˚C to +125˚C

Maximum Junction Temperature..... +150˚C

Storage Temperature Range .....-65˚C to +150˚C

Lead Temperature (Soldering, 10s) ..... +300˚C

Soldering Temperature (Reflow)..... +260˚C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T822+3C
Outline Number	*21-0168*
Land Pattern Number	*90-0065*
Thermal Resistance, Four-Layer Board	
Junction to Ambient (θ_{JA})	85.3°C/W
Junction to Case (θ_{JC})	8.9°C/W

For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 1.8V, T_J = -40˚C to +125˚C, C_{BYP} = 10nF, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, MODE = HIGH, unless mentioned otherwise, Typical values are at T_J = +25˚C, unless otherwise specified, see Note 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by output accuracy $V_{OUT} < V_{IN} - V_{DO}$		1.7		5.5	V
Input Undervoltage Lockout	V_{UVLO}	V_{IN} rising, 100mV hysteresis		1.5	1.6	1.7	V
Output Voltage Range	V_{OUT}	Guaranteed by output accuracy, programmed using external resistor-divider		0.8		5.0	V
Feedback (FB) Accuracy	V_{FB}	MODE = HIGH, I_{OUT} from 0.1mA to 500mA, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V		0.588	0.6	0.612	V
		MODE = LOW, I_{OUT} from 0.1mA to 20mA, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{IN} > 1.7V		0.588	0.6	0.612	
Output Capacitance	C_{OUT}	Effective capacitance required for stability and proper operation		2	4.7		µF
Input Supply Current	I_{SD}	V_{EN} = 0V	T_J = +25°C		0.01	1	µA
			T_J = +125°C		1.6		
	I_Q	EN = HIGH, MODE = HIGH, I_{OUT} = 0mA			350	750	
		EN = HIGH, MODE = LOW, I_{OUT} = 0mA			20	50	
Line Regulation	ACC_{LINE_REG}	V_{IN} from 3.6V to 5.5V, I_{OUT} = 500mA, V_{OUT} = 3.3V			0.068		%/V
Load Regulation	ACC_{LOAD_REG}	I_{OUT} from 0.1mA to 500mA, V_{IN} = V_{OUT} + 0.3V			0.078		%
Load Transient		I_{OUT} = 50mA to 500mA or 500mA to 50mA, t_{RISE} = t_{FALL} = 1µs			48		mV
Line Transient		V_{IN} = 2.1V to 2.5V to 2.1V, I_{OUT} = 500mA, t_{RISE} = t_{FALL} = 5µs			5		mV
Output Transient at MODE Transition		MODE rising or falling, I_{OUT} = 1mA			20.5		mV
MODE Transition Time		MODE from LOW to HIGH to I_{OUT} = 500mA			50		µs
Power-Supply Rejection Ratio	PSRR	V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 100mA	f = 1kHz		70		dB
			f = 10kHz		68		
			f = 100kHz		50		
			f = 1MHz		34		
Active Discharge Resistance	R_{DIS}	V_{EN} = 0V			800		Ω
Output Noise		V_{IN} = 2.1V, I_{OUT} = 100mA, 10Hz to 100kHz	C_{BYP} = 47nF		45		$µV_{RMS}$
Dropout Voltage (Note 2)	V_{DO}	I_{OUT} = 500mA, when MODE = HIGH	V_{IN} = 3.6V		60	120	mV
Dropout Voltage (Note 2)	V_{DO}	I_{OUT} = 20mA, when MODE = LOW	V_{IN} = 3.6V		54	108	mV

(V_{IN} = 3.6V, V_{OUT} = 1.8V, T_J = -40˚C to +125˚C, C_{BYP} = 10nF, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, MODE = HIGH, unless mentioned otherwise, Typical values are at T_J = +25˚C, unless otherwise specified, see *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Current Limit	I_{LIM}	MODE = HIGH, V_{OUT} = 0.9 x $V_{OUT\_NOMINAL}$, $V_{OUT\_NOMINAL}$ = 1.8V, $V_{IN} - V_{OUT}$ = 500mV		600	700	800	mA
		MODE = LOW, $V_{OUTS/OUT}$ = 0.9 x $V_{NOMINAL}$, $V_{OUT\_NOMINAL}$ = 1.8V		22			
BYP Capacitor Range	C_{BYP}			0.001		0.1	µF
BYP Soft-Start Current		From BYP to GND during startup			50		µA
EN/MODE Input Threshold	V_{IH}	V_{IN} from 1.7V to 5.5V	V_{EN} and V_{MODE} rising		0.8	1.2	V
	V_{IL}	V_{IN} from 1.7V to 5.5V	V_{EN} and V_{MODE} falling	0.4	0.7		
EN/MODE Input Leakage Current	I_{EN_LK}, I_{MODE_LK}	V_{EN} and V_{MODE} from 0 to 5.5V	T_J = +25°C	-1	0.001	1	µA
			T_J = +125°C		0.01		
POK Threshold		V_{OUT} when POK switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		
POK Voltage Low	V_{OL}	I_{POK} = 1mA			10	100	mV
POK Leakage Current	I_{POK_LK}	V_{POK} = 5.5V	T_J = +25°C	-0.1	0.001	0.1	µA
			T_J = +125°C		0.01		
IN Reverse Current Threshold		V_{OUT} = 3.6V, when V_{IN} falls to 0V	MODE = HIGH		200		mA
			MODE = LOW		10		
Thermal Shutdown Threshold		T_J, when the output turns on/off	T_J rising		165		˚C
			T_J falling		150		

Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

Note 2: Dropout voltage is defined as ($V_{IN} - V_{OUT}$) when V_{OUT} is 95% of its nominal value.

Typical Operating Characteristics

V_{IN} = 2.1V, V_{OUT} = 1.8V, T_A = +25°C, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, C_{BYP} = 10nF, unless otherwise noted.

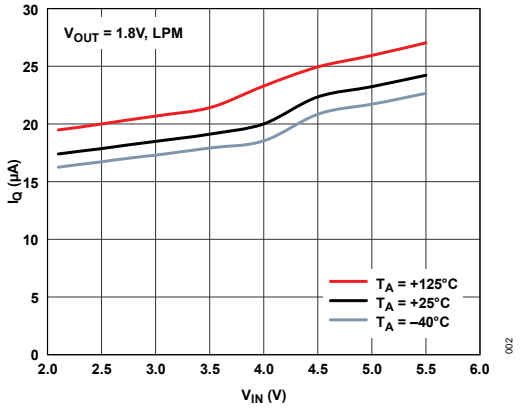


Figure 2. Quiescent Current vs. Input Voltage

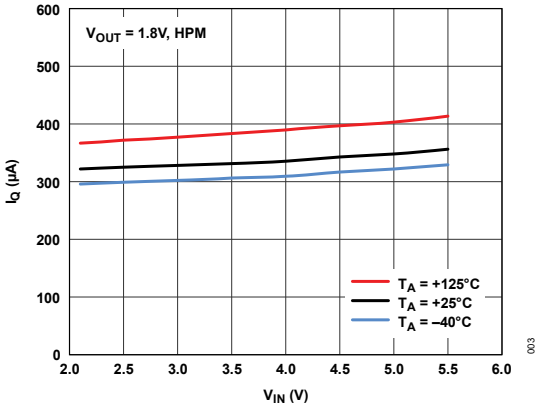


Figure 3. Quiescent Current vs. Input Voltage

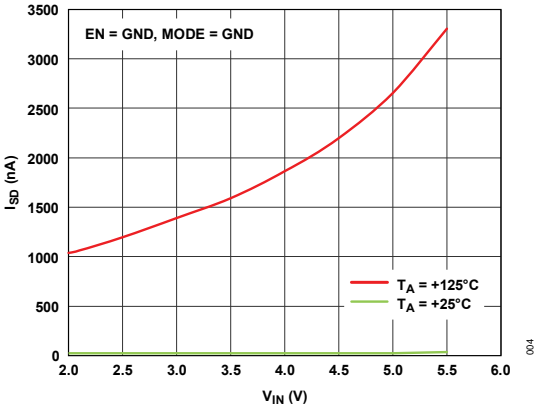


Figure 4. Shutdown Current vs. Input Voltage

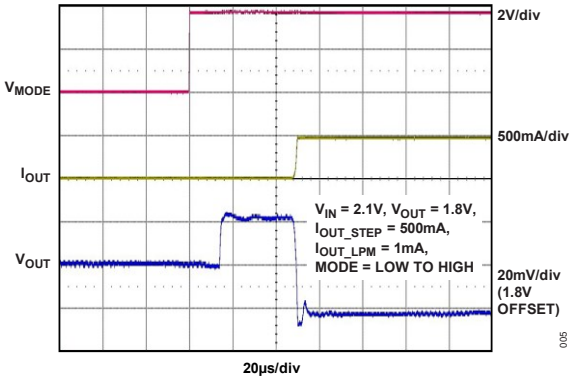


Figure 5. Mode and Load Transient Response

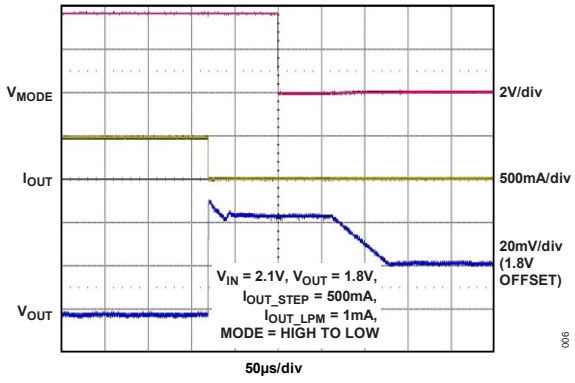


Figure 6. Mode and Load Transient Response

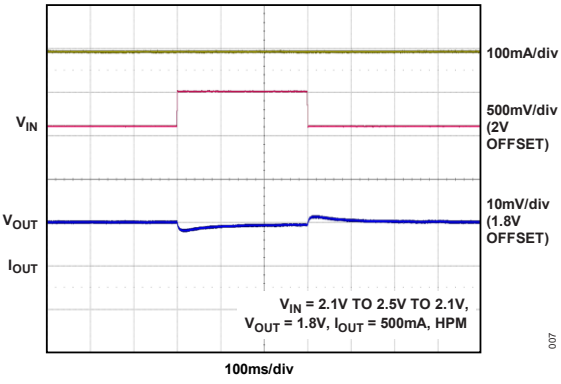


Figure 7. Line Transient Response

V_{IN} = 2.1V, V_{OUT} = 1.8V, T_A = +25°C, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, C_{BYP} = 10nF, unless otherwise noted.

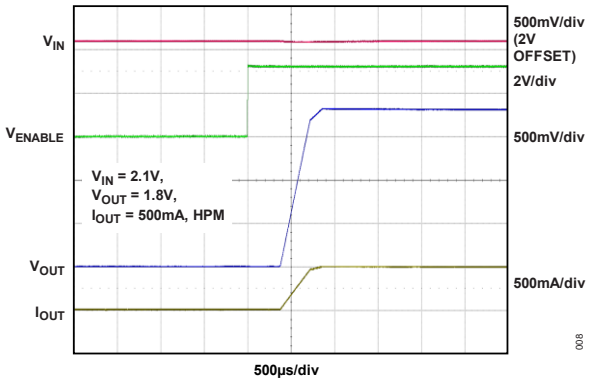


Figure 8. Soft-Start Response

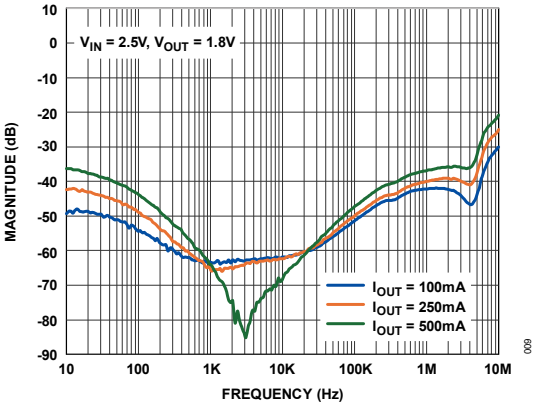


Figure 9. Input Supply PSSR vs. Frequency

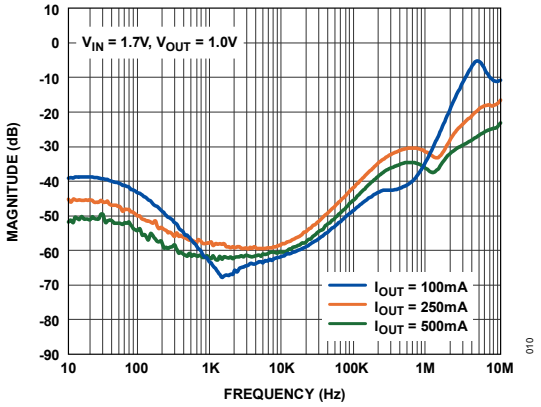
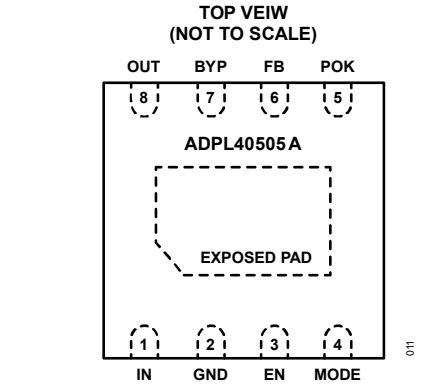


Figure 10. Input Supply PSSR vs. Frequency

Pin Configuration



TDFN PACKAGE
8-PIN (2mm x 2mm x 0.75mm)

NOTES:
THE EXPOSED PAD ON THE UNDERSIDE OF THE PACKAGE MUST BE SOLDERED TO THE GROUND PLANE TO INCREASE THE RELIABILITY OF THE SOLDER JOINTS AND TO MAXIMIZE THE THERMAL CAPABILITY OF THE PACKAGE.

Figure 11. Pin Configurations

Pin Descriptions

PIN	NAME	FUNCTION
1	IN	Regulator Supply Input Pin. Connect to voltage between 1.7V and 5.5V, and bypass with a 4.7µF capacitor from IN to GND.
2	GND	Regulator Ground Pin. Bring IN and OUT bypass capacitor GND connections to this pin for best performance. Short the pin to EP in the Printed Circuit Board (PCB) layout.
3	EN	Enable Input Pin. Connect this pin to a logic signal to enable (V_{EN} high) or disable (V_{EN} low) the regulator output. Connect to IN to keep the output enabled whenever a valid supply voltage is present. When EN is pulled low or disabled, output is shorted to GND through an 800Ω internal active discharge circuit.
4	MODE	Mode-Select Pin. Connect this pin to a logic-high signal if normal operation is desired, and connect it to a logic-low signal if low-power operation is desired. When the MODE is high, the maximum output load current when the LDO is in regulation is 500mA, and when the MODE is low, the maximum output load current is 20mA.
5	POK	Power-OK Output Pin. Connect a pull-up resistor from this pin to a supply to create a signal that goes high after the regulator output has reached its regulation voltage.
6	FB	Feedback Input Pin. Connect a resistor-divider string from OUT to GND with the midpoint tied to this pin to set the output voltage. In a typical application circuit, $V_{OUT} = 0.6V \times (1 + R_{FBTOP}/R_{FBBOT})$.
7	BYP	Bypass Capacitor Input Pin. Connect a 0.001µF to 0.1µF capacitor between OUT and BYP to reduce output noise and set the regulator soft-start rate.
8	OUT	Regulator Output Pin. Sources up to 500mA when MODE = HIGH and up to 20mA when MODE = LOW at programmed output regulation voltage. Bypass with a 4.7µF (2µF minimum effective capacitance), low-Equivalent Series Resistance (ESR) (< 0.03Ω) capacitor to GND.
EP	EP	Exposed Pad. Connect the exposed pad to a ground plane with low thermal resistance to provide the best heat sinking. Connected to GND internally.

Typical Application Circuits

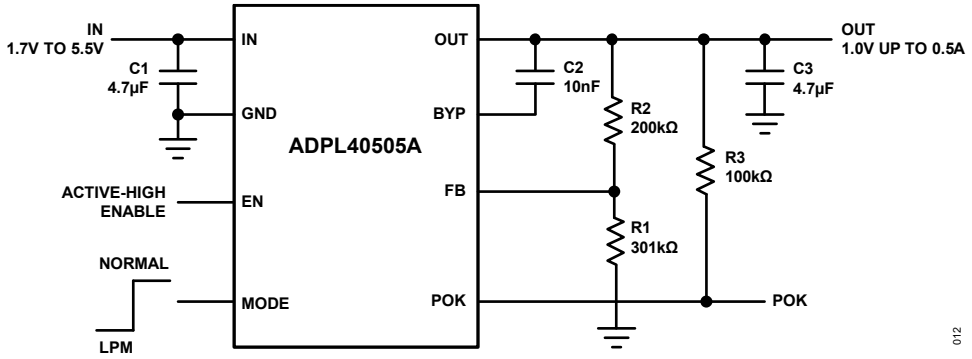


Figure 12. Typical Application Circuit

Simplified Block Diagram

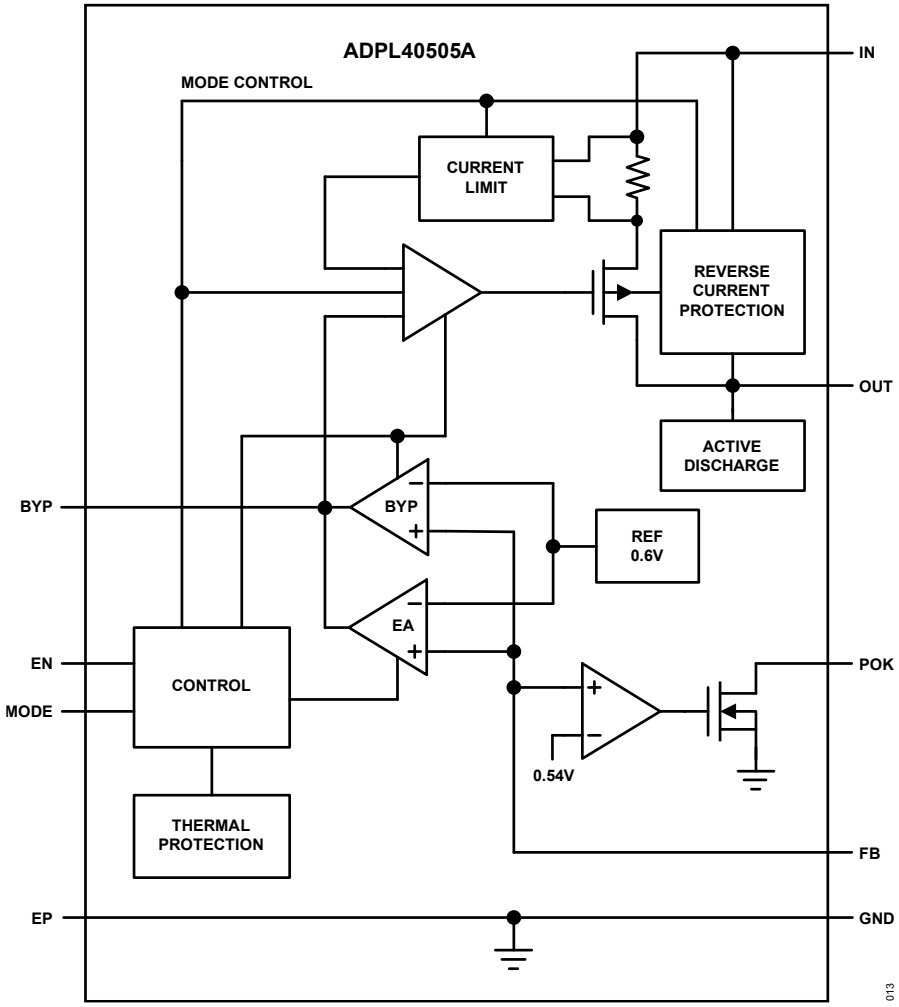


Figure 13. Simplified Block Diagram

Detailed Description

The ADPL40505A is a 5.5V, PMOS linear regulator that delivers up to 500mA load current. This regulator maintains ±2% output accuracy over line, load, and temperature variations. The device features a low-power mode of operation, consuming very low quiescent current from the supply. In low-power mode, the device can deliver up to 20mA load current and have a no-load quiescent current of 20µA.

The regulator supports a wide input supply range from 1.7V up to 5.5V. The output voltage can be adjusted to a value in the range of 0.8V to 5.0V. The output voltage on the ADPL40505A can be adjusted using two external feedback resistors.

The regulator is fully protected from damage by internal circuitry that provides programmable inrush current limiting, output over-current limiting, reverse current limiting, and thermal overload protection.

Modes of Operation

The ADPL40505A features low-power and high-power modes of operation. The modes are selected based on the state of the MODE pin. The device will always be in the high-power mode during startup, regardless of the state of the MODE pin. Upon completion of the soft-start, the device will read the state of the MODE pin and adjust the mode of operation, if required.

Low-Power Mode of Operation

The ADPL40505A enters low-power mode if the MODE pin is pulled low. In this mode, the device consumes 20µA of current and can source up to 20mA.

High-Power Mode of Operation

The ADPL40505A enters high-power mode if the MODE pin is pulled high. In this mode, the device consumes 350µA of current and can source up to 500mA.

MODE Transition

Transitioning from low-power mode to high-power mode will adjust the internal regulation point, resulting in a transient excursion at the output. The excursion is a function of load current and temperature, the maximum being at maximum load current in low-power mode (20mA) and at an elevated die temperature. To minimize output voltage transient excursion at the MODE transition, it is recommended to keep the load current at 1mA level or below. It will take 50µs of settling time before the host is able to apply the load current that is supported in high-power mode.

When the host is ready to place the device back into the low-power mode, host must reduce the load current to levels supported in low-power mode 80µs prior to driving the MODE pin low. Similarly, the MODE pin transition from high to low causes transient excursion at the output. The load current must be kept constant during the settling period, after which it can be adjusted.

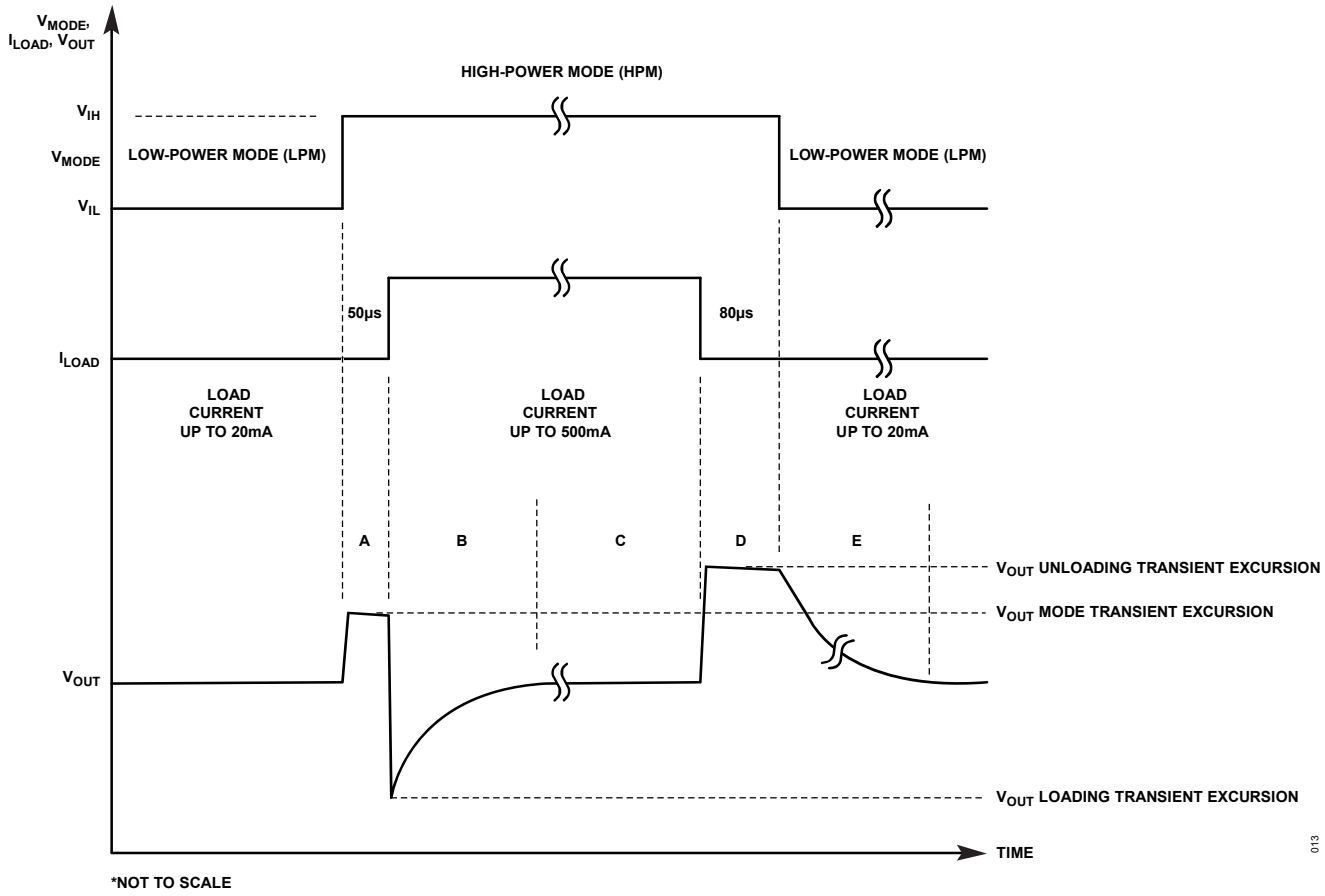


Figure 14. MODE Transition

The MODE transition is illustrated in *Figure 14*. Different operating regions are:

- A – The MODE transitions from low to high while the load current is kept in the low-power mode range. The output voltage increases due to the mode transient and then starts to settle. The high-power mode current step can be applied after a 50µs time period elapses.
- B – The high-power mode load step is applied after 50µs. The output voltage is recovering from the loading transient.
- C – The device has fully recovered from the loading transient.
- D – The host lowers the load current prior to MODE changes to the low-power mode. This creates an unloading transient event, after which the output voltage starts to settle. After 80µs of settling time, the host can transition the MODE pin to low.
- E – The output voltage comes back to the target level.

Enable (EN)

The ADPL40505A includes an enable input (EN). Pull EN low to shut down the output. In shutdown mode, the device consumes 10nA of current from the input supply. Drive EN high to enable the output. If a separate shutdown signal is not available, connect EN to IN. When EN is pulled low, output is pulled to ground through a 800Ω active discharge circuit.

Bypass (BYP)

The capacitor that is connected from BYP to OUT filters the noise of the reference, feedback resistors, and regulator input stage, and it provides a high-speed feedback path for improved transient response. A 0.01µF capacitor rolls off input noise at approximately 32Hz. The slew rate of the output voltage during startup is also determined by the BYP capacitor. A 0.01µF capacitor sets the slew rate to 5V/ms. This startup rate results in a 23.5mA slew current drawn from the input at startup to charge the 4.7µF output capacitance.

The BYP capacitor value can be adjusted from 0.001µF to 0.1µF to change the startup slew rate according to the following formula:

$$\text{Startup Slew Rate} = (5V/ms) \times (0.01\mu F/C_{BYP})$$

where C_{BYP} is measured in µF.

Selecting a BYP capacitor larger than 10nF is primarily to slow down the soft-start rate and minimize the inrush current since the output noise will remain very constant with improvement of about $1.0\mu V_{RMS}$.

Note that this slew rate applies only at startup. The recovery from an overload condition occurs at a slew rate approximately 500 times slower. Also note that, being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Power-OK (POK)

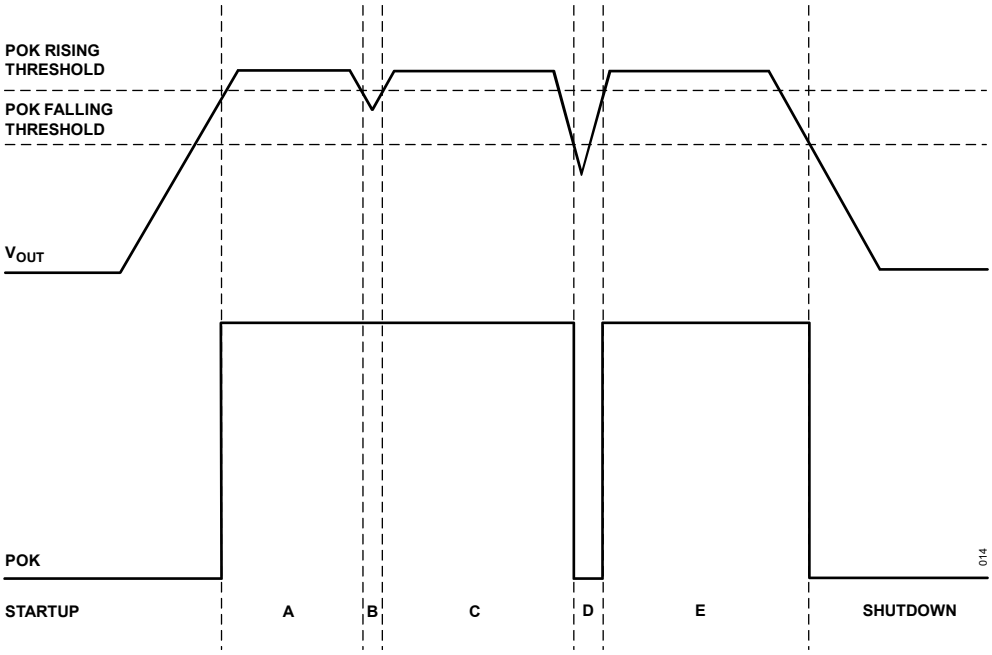


Figure 15. Typical POK Operation

The POK operation versus the output voltage is shown in *Figure 15*. The different operating regions are:

- A – The device is in regulation.
- B – V_{OUT} sags, but does not reach the POK falling threshold.
- C – The device is in regulation.
- D – V_{OUT} sags low enough to cross the POK falling threshold. The POK is driven low until V_{OUT} recovers above the POK rising threshold.
- E – The device is in regulation.

The Power-OK (POK) function monitors the output voltage to indicate that it is in regulation. The POK pin is open-drain and requires a pullup resistor to an external supply to properly report the device regulation status to other devices, so that it can be used for sequencing. Check if the external pullup supply voltage results in a valid logic levels for the receiving device or devices. The range of the pullup resistance is between 10kΩ and 200kΩ. Its lower limit is derived from the pulldown strength of the POK transistor, while the higher limit is determined by the maximum leakage current at the POK pin. The signal is low while the device is in shutdown.

The POK is driven low during startup. It gets released and pulled up once the output voltage reaches the POK rising threshold (91% of the regulation target). If the output voltage sags to below the POK falling threshold during regulation, the POK signal is driven low to indicate that the output voltage dropped out of regulation. During shutdown, the POK signal is driven low once the output voltage crosses the POK falling threshold (88% of the regulation target). The POK signal is active during the output voltage transition.

Protection

The ADPL40505A is fully protected from an overload condition by current-limiting and thermal-overload protection circuits. If the output is shorted to GND, the output current will be limited to 700mA (typ) after the output capacitor discharges through the shorting path. Under these conditions, the device quickly heats up. When the junction temperature reaches +165°C, the thermal-protection circuit shuts the output device off. Once the device cools to +150°C, the regulator enables reestablishment of regulation. If the fault persists, the output cycles on and off as the junction temperature slews between +150°C and +165°C. Continuously operating in the fault conditions or above a +125°C junction temperature is not recommended since long-term reliability may be reduced. In dropout, the current limit will trigger at 850mA (typ). Once the limit is triggered, the device will limit the current to 700mA.

The ADPL40505A provides reverse-current protection when the output voltage is higher than the input. The ADPL40505A includes a reverse-voltage detector that trips when IN drops below OUT, shutting off the regulator and opening the body diode connection, thus preventing any reverse current. The reverse current is a current that flows through the body diode of the pass element and is undesired due to its impact on power dissipation and long-term reliability, especially at higher current levels. Thermal protection can also be triggered when the device is exposed to excessive heat in the system, causing the die temperature to reach undesired levels.

Active Discharge

When EN is pulled low, the ADPL40505A connects an 800Ω resistor from OUT to GND to discharge the output capacitor. This feature reduces the time required to discharge the output capacitor, which will simplify the system power sequencing.

Undervoltage Lockout (UVLO)

The ADPL40505A undervoltage lockout (UVLO) circuit responds quickly to input voltage glitches and will disable the device's output if the rail dips below the UVLO falling threshold. The local input capacitance prevents transient brownout conditions in most applications. The device is ready once the input voltage exceeds the UVLO rising threshold during power-up.

During V_{IN} power-up, the ADPL40505A begins V_{OUT} soft-start after V_{IN} crosses the V_{IN} UVLO rising threshold. This assures proper V_{OUT} ramp-up and transition to regulation. The V_{OUT} soft-start rate should be kept at or slower than the V_{IN} slew rate to avoid entering the dropout. In some situations, V_{IN} transients can place the regulator into dropout. As V_{IN} starts climbing again and the device comes out of the dropout, the output can overshoot. This condition is avoided by using an enable signal or by increasing the soft-start time with a larger C_{BYP}.

Output Voltage Configuration

The ADPL40505A uses external feedback resistors to set the output regulation voltage. The output voltage can be set from 0.8V to 5.0V. Set the bottom feedback resistor R1 to 301kΩ or less to minimize the FB input bias current error. Calculate the value of the top feedback resistor R2 as follows:

$R2 = R1 \times (V_{OUT}/V_{FB} - 1)$

where V_{FB} is the feedback regulation voltage of 0.6V.

To set the output to 1.0V, for example, R2 should be:

$R2 = 301k\Omega \times (1.0V/0.6V - 1) = 200k\Omega$

A smaller R1 is recommended to optimize for noise performance.

The values of the resistor-divider and its tolerance will have a direct impact on V_{OUT} accuracy. Resistors of 1% or better are recommended. *Table 1* shows the recommended values for the feedback resistors.

Table 1. Recommended Feedback Resistor Values

TARGETED OUTPUT VOLTAGE (V)	TOP FEEDBACK RESISTOR VALUES (kΩ)	BOTTOM FEEDBACK RESISTOR VALUES (kΩ)	CALCULATED OUTPUT VOLTAGE (V)
0.8	100	301	0.799
1.0	200	301	0.999
1.2	301	301	1.200
1.5	453	301	1.503
1.8	604	301	1.804
2.5	953	301	2.500
3.0	1210	301	3.012
3.3	1370	301	3.331
5.0	2210	301	5.005

Application Information

Input and Output Capacitors

The ADPL40505A is designed to have stable operation using low equivalent series resistance (ESR) ceramic capacitors at the input and output pins. Multilayer ceramic capacitors (MLCC) with X7R dielectric are commonly used for these types of applications and are recommended due to their relatively stable capacitance across temperature. Nevertheless, the amount of effective capacitance depends on the operating DC bias, capacitance tolerance with temperature, and choice of dielectric. Therefore, the capacitor data sheet must be properly examined.

The ADPL40505A is designed and characterized for operation with X7R ceramic capacitors of 4.7µF (2.0µF of effective capacitance) at both the input and output. These capacitors shall be placed as close as possible to the respective input and output pins to minimize trace parasitics. There is no maximum output capacitance limitation due to stability. However, for 5V output voltage applications, it is recommended to keep the output capacitance to a maximum of 4.7µF effective capacitance to minimize short-circuit current buildup in an inductive shorting path.

Thermal Consideration

To optimize the ADPL40505A performance, special consideration is given to the device power dissipation and PCB thermal design. Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. This can be calculated by the following equation:

$$\text{Power Loss (W)} = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

The optimal power dissipation can be achieved by carefully choosing the input voltage for a given output target voltage.

The main thermal conduction path for the device is through the exposed pad of the package. As a result, the thermal pad must be soldered to a copper pad area under the device. Thermal plated vias must be placed inside the thermal PCB pad to transfer heat to different GND layers in the system. The vias should be capped to minimize solder voids. The maximum power dissipation is determined by using thermal resistance from the device junction to ambient, keeping the maximum junction temperature below +125°C. Thermal properties of the package are given in the *Package Information* section.

The first-order power dissipation estimate for the V_{IN} = 3.3V and V_{OUT} = 2.5V with a load current of 300mA is:

$$\text{Loss (W)} = (V_{IN} - V_{OUT}) \times I_{LOAD} = (3.3V - 2.5V) \times 0.3A = 0.24W$$

Assuming the ADPL40505AATA+ is used with ambient temperature T_A = 25°C, this power dissipation will raise the junction temperature to:

$$T_J = (PD \times \theta_{JA}) + T_A = (0.24W \times 85.3°C/W) + 25°C = 45.47°C$$

Ordering Information

PART	TEMPERATURE RANGE	PIN-PACKAGE	FEATURE
ADPL40505AATA+	-40°C to +125°C	8-pin, 2mm x 2mm TDFN	MODE pin, FB pin with external feedback divider network, POK output
ADPL40505AATA+T	-40°C to +125°C	8-pin, 2mm x 2mm TDFN	MODE pin, FB pin with external feedback divider network, POK output

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	—

NOTES