Data Sheet

ADPL40501

Ultra-Low Quiescent Current, 100mA, CMOS Linear Regulators

FEATURES

- Ultra-low Quiescent Current
  - I_Q = 600nA with 0µA Load
  - I_Q = 860nA with 1µA Load
- Stable with 1µF Ceramic Input and Output Capacitors
- Maximum Output Current: 100mA
- Input Voltage Range: 2.2V to 5.5V
- Low Shutdown Current: < 50nA Typical
- Low Dropout Voltage: 180mV at 100mA Load
- Initial Accuracy: ±1%
- Accuracy Over Line, Load, and Temperature: ±3.5%
- 7 Fixed Output Voltage Options: 1.2V to 3.3V
- Adjustable Output Voltage Option Available
- Integrated Output Discharge Resistor
- Current Limit and Thermal Overload Protection
- Logic-Control Enable
- PSRR Performance of up to 72dB at 100Hz
- 5-Lead TSOT Package
- 4-Ball, 0.5mm Pitch WLCSP

APPLICATIONS

- High-Speed and High-Precision ADC/DAC Power
- Mobile Phones
- Portable and Battery-Powered Equipment
- Power for Low-Noise Instrumentation and Medical Products
- Post DC-to-DC Regulation

GENERAL DESCRIPTION

The ADPL40501 is an ultra-low quiescent current, low dropout (LDO), linear regulator that operates from 2.2V to 5.5V and provides up to 100mA of output current. The low 180mV dropout voltage at 100mA load improves efficiency and allows operation over a wide input voltage range.

The ADPL40501 is specifically designed for stable operation with a small 1µF ±30% ceramic input and output capacitors to meet the requirements of high-performance, space-constrained applications.

The ADPL40501 is available in 7 fixed output voltage options across package offerings, ranging from 1.2V to 3.3V. The ADPL40501 also includes a switched resistor to discharge the output automatically when the LDO is disabled.

The ADPL40501 is also available with adjustable output voltage but only in a 5-lead TSOT package.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADPL40501 is available in a tiny 5-lead TSOT and a 4-ball, 0.5mm pitch WLCSP package for the smallest footprint solution to meet a variety of portable power applications.

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TYPICAL APPLICATION CIRCUITS

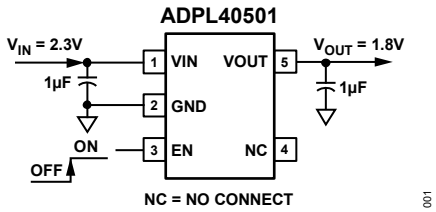

Figure 1. 5-Lead TSOT with Fixed Output Voltage, 1.8V

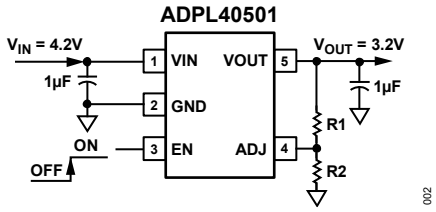

Figure 2. 5-Lead TSOT with Adjustable Output Voltage, 3.2V

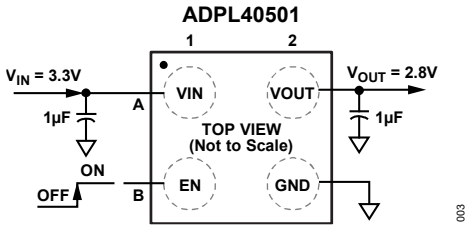

Figure 3. 4-Ball WLCSP with Fixed Output Voltage, 2.8V

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/26	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = (V_{OUT} + 0.5V) or 2.2V, whichever is greater; EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	T_J = −40°C to +125°C	2.2		5.5	V
Operating Supply Current	I_{GND}	I_{OUT} = 0µA		600	1250	nA
		I_{OUT} = 0µA, T_J = −40°C to +125°C			2.3	µA
		I_{OUT} = 1µA		860	1800	nA
		I_{OUT} = 1µA, T_J = −40°C to +125°C			2.8	µA
		I_{OUT} = 100µA		2.6	4.5	µA
		I_{OUT} = 100µA, T_J = −40°C to +125°C			5.8	µA
		I_{OUT} = 10mA		11		µA
		I_{OUT} = 10mA, T_J = −40°C to +125°C			19	µA
		I_{OUT} = 100mA		42		µA
		I_{OUT} = 100mA, T_J = −40°C to +125°C			65	µA
Shutdown Current	I_{GND-SD}	EN = GND		50		nA
		EN = GND, T_J = −40°C to +125°C			1	µA
Output Voltage Accuracy	V_{OUT}	I_{OUT} = 10mA	-1		+1	%
		0µA < I_{OUT} < 100mA, V_{IN} = (V_{OUT} + 0.5V) to 5.5V	-2		+2	%
		0µA < I_{OUT} < 100mA, V_{IN} = (V_{OUT} + 0.5V) to 5.5V, T_J = −40°C to +125°C	−3.5		+3.5	%
Adjustable-Output Voltage Accuracy[1]	V_{ADJ}	I_{OUT} = 10mA	0.99	1.0	1.01	V
		0µA < I_{OUT} < 100mA, V_{IN} = (V_{OUT} + 0.5V) to 5.5V	0.98		1.02	V
		0µA < I_{OUT} < 100mA, V_{IN} = (V_{OUT} + 0.5V) to 5.5V, T_J = −40°C to +125°C	0.97		1.03	V
Regulation						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5V) to 5.5V, T_J = −40°C to +125°C	-0.1		+0.1	%/V
Load Regulation[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100µA to 100mA		0.004		%/mA

(V_{IN} = (V_{OUT} + 0.5V) or 2.2V, whichever is greater; EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		I_{OUT} = 100µA to 100mA, T_J = −40°C to +125°C			0.01	%/mA
Dropout Voltage[3]						
4-Ball WLCSP	$V_{DROPOUT}$	I_{OUT} = 10mA, V_{OUT} = 3.3V		7		mV
		I_{OUT} = 10mA, T_J = −40°C to +125°C, V_{OUT} = 3.3V			13	mV
		I_{OUT} = 100mA, V_{OUT} = 3.3V		105		mV
		I_{OUT} = 100mA, T_J = −40°C to +125°C, V_{OUT} = 3.3V			180	mV
5-Lead TSOT	$V_{DROPOUT}$	I_{OUT} = 10mA, V_{OUT} = 3.3V		8		mV
		I_{OUT} = 10mA, T_J = −40°C to +125°C, V_{OUT} = 3.3V			15	mV
		I_{OUT} = 100mA, V_{OUT} = 3.3V		120		mV
		I_{OUT} = 100mA, T_J = −40°C to +125°C, V_{OUT} = 3.3V			225	mV
ADJ Input Bias Current	ADJ_{I-BIAS}	2.2V ≤ V_{IN} ≤ 5.5V, ADJ connected to V_{OUT}		10		nA
Active Pull-Down Resistance	R_{PD}	V_{OUT} = 2.8V, R_{LOAD} = ∞		300	600	Ω
Start-Up Time[4]	$T_{START-UP}$	V_{OUT} = 3.3V		1100		µs
Current Limit Threshold[5]	I_{LIMIT}		220	320	500	mA
Thermal Shutdown						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}	T_J rising		15		°C
EN Input						
EN Input Logic High	V_{IH}	2.2V ≤ V_{IN} ≤ 5.5V	1.2			V
EN Input Logic Low	V_{IL}	2.2V ≤ V_{IN} ≤ 5.5V			0.4	V
EN Input Leakage Current	I_{LEAK}	EN = V_{IN} or GND		0.1		µA
		EN = V_{IN} or GND, T_J = −40°C to +125°C			1	µA
Undervoltage Lockout						
Input Voltage Rising	$UVLO_{RISE}$				2.19	V

(V_{IN} = (V_{OUT} + 0.5V) or 2.2V, whichever is greater; EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Falling	$UVLO_{FALL}$		1.60			V
Hysteresis	$UVLO_{HYS}$			100		mV
Output Noise	OUT_{NOISE}	10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 3.3V		105		µVrms
		10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 2.5V		100		µVrms
		10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 1.2V		80		µVrms
Power Supply Rejection Ratio	PSRR	100Hz, V_{IN} = 5V, V_{OUT} = 3.3V		60		dB
		100Hz, V_{IN} = 5V, V_{OUT} = 2.5V		65		dB
		100Hz, V_{IN} = 5V, V_{OUT} = 1.2V		72		dB
		1kHz, V_{IN} = 5V, V_{OUT} = 3.3V		50		dB
		1kHz, V_{IN} = 5V, V_{OUT} = 2.5V		50		dB
		1kHz, V_{IN} = 5V, V_{OUT} = 1.2V		62		dB

1 Accuracy when V_{OUT} is connected directly to ADJ. When the V_{OUT} voltage is set by external feedback resistors, the absolute accuracy in adjust mode depends on the tolerances of the resistors used.

2 Based on an endpoint calculation using 0A and 100mA loads.

3 Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 2.2V.

4 Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 90% of its nominal value.

5 Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0V or 2.7V.

Table 2. Input and Output Capacitor, Recommended Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	0.7			µF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

1 The minimum input and output capacitance should be greater than 0.7µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; however, Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} to GND	−0.3V to +6.5V
V_{OUT} to GND	−0.3V to V_{IN}
EN to GND	−0.3V to +6.5V
ADJ to GND	−0.3V to V_{IN}
NC to GND	−0.3V to V_{IN}
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Data

Absolute maximum ratings only apply individually; they do not apply in combination. The ADPL40501 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inches × 3 inches, circuit board. Refer to JESD 51-7 and JESD 51-9 for detailed information on the board construction. For additional information, see the *AN-617 Application Note, MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction to board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, Guidelines for Reporting and Using Electronic Package Thermal Information, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. The maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

Thermal Resistance

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. Ψ_{JB} is the junction-to-board thermal-characterization parameter, measured in units of °C/W.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W
4-Ball, 0.5mm Pitch WLCSP	260	58	°C/W

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

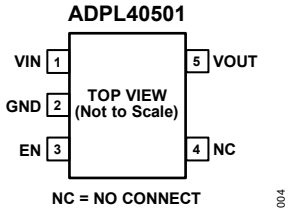

Figure 4. 5-Lead TSOT, Fixed Output Pin Configuration

Pin Descriptions

Table 5. 5-Lead TSOT, Fixed Output Pin Functions

PIN	NAME	DESCRIPTION
1	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 1µF or greater capacitor.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN}.
4	NC	No Connect. This pin is not connected internally. Connect this pin to GND or leave open.
5	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 1µF or greater capacitor.

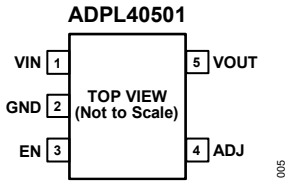

Figure 5. 5-Lead TSOT, Adjustable Output Pin Configuration

Pin Descriptions

Table 6. 5-Lead TSOT, Adjustable Output Pin Functions

PIN	NAME	DESCRIPTION
1	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 1µF or greater capacitor.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN}.
4	ADJ	Output Voltage Adjust Pin. Connect the midpoint of the voltage divider between V_{OUT} and GND to this pin to set the output voltage.
5	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 1µF or greater capacitor.

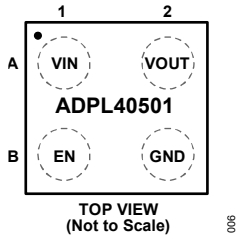

Figure 6. 4-Ball WLCSP Pin Configuration

Pin Descriptions

Table 7. 4-Ball WLCSP Pin Functions

PIN	NAME	DESCRIPTION
A1	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 1µF or greater capacitor.
B1	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN}.
A2	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 1µF or greater capacitor.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise noted.

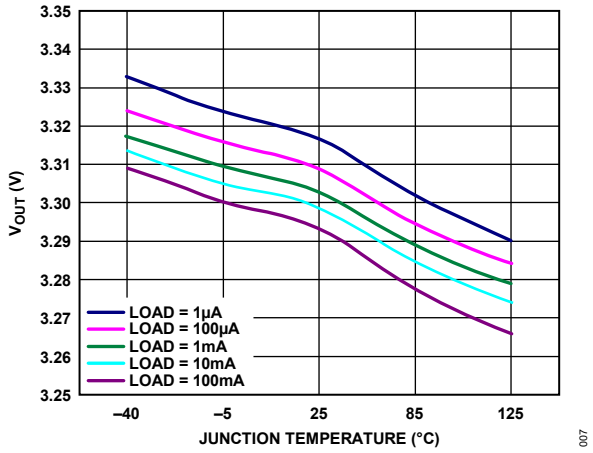

Figure 7. Output Voltage (V_{OUT}) vs. Junction Temperature

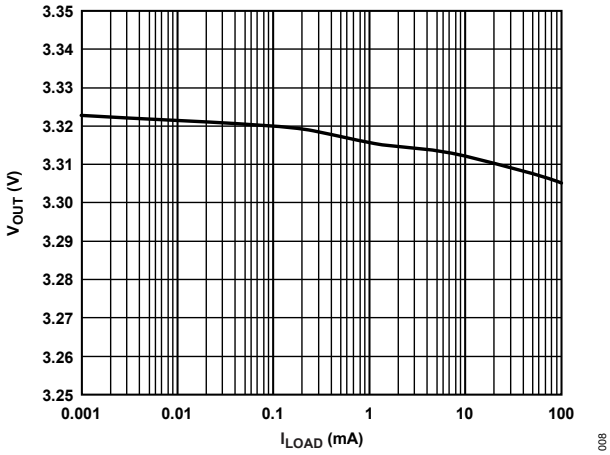

Figure 8. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

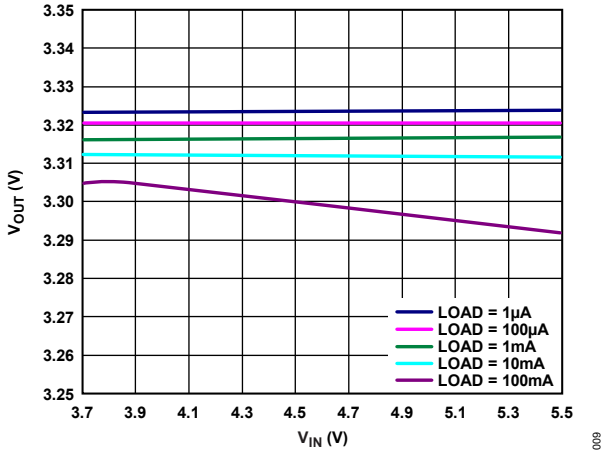

Figure 9. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

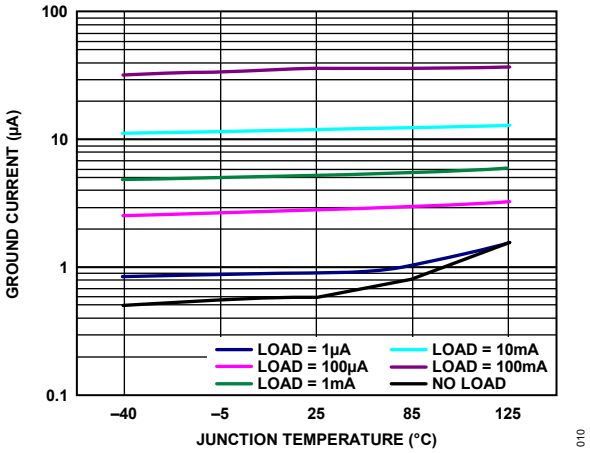

Figure 10. Ground Current vs. Junction Temperature

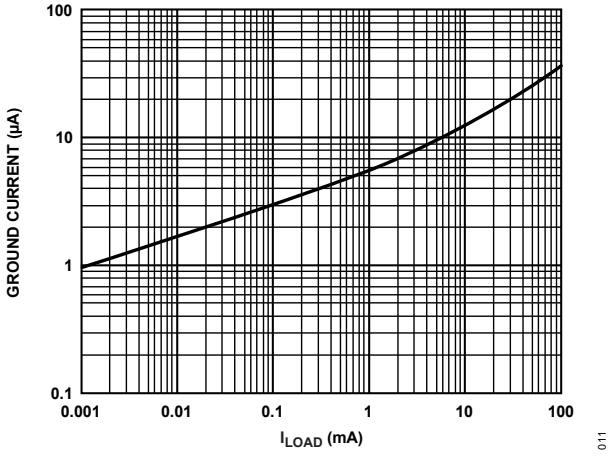

Figure 11. Ground Current vs. Load Current (I_{LOAD})

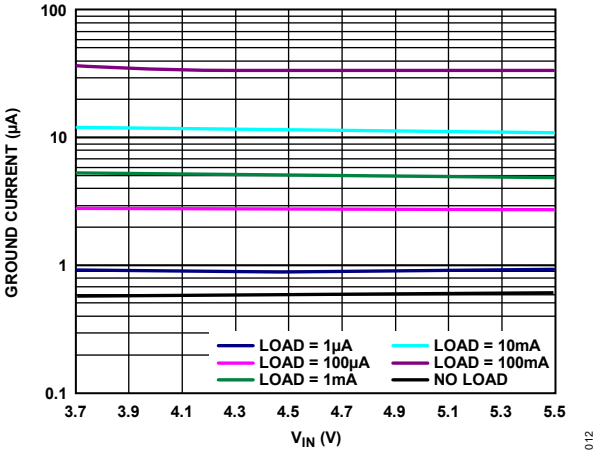

Figure 12. Ground Current vs. Input Voltage (V_{IN})

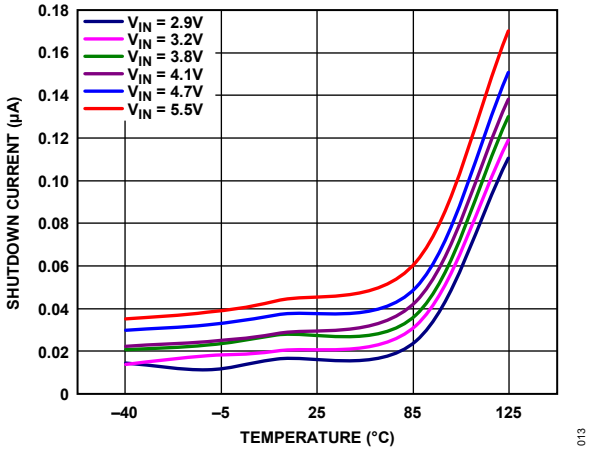

Figure 13. Shutdown Current vs. Temperature at Various Input Voltages

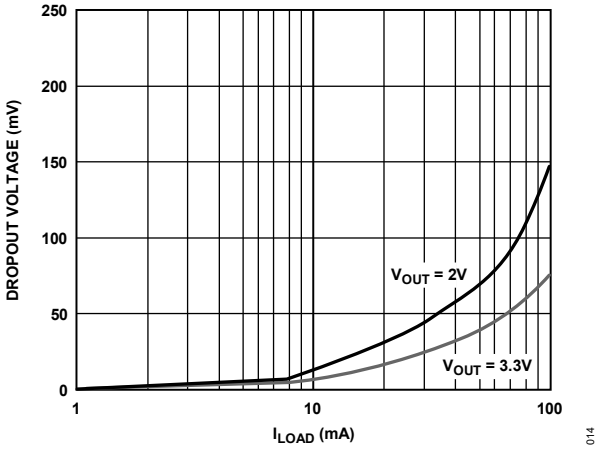

Figure 14. Dropout Voltage vs. Load Current (I_{LOAD})

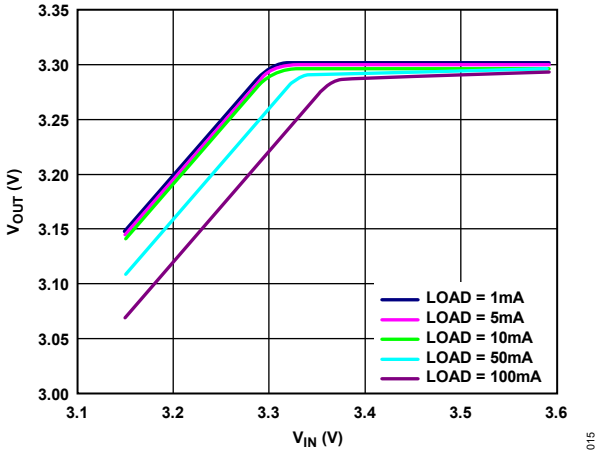

Figure 15. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout

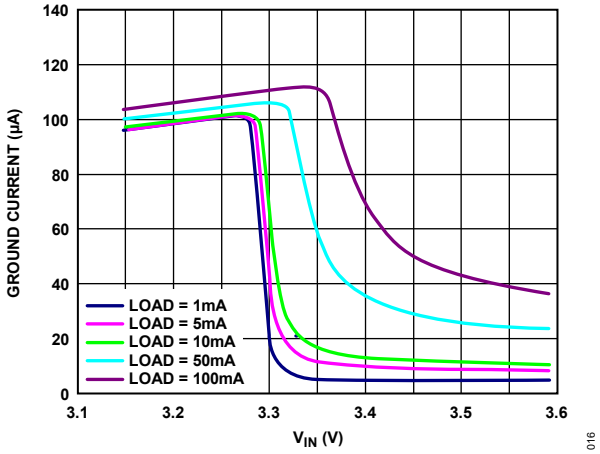

Figure 16. Ground Current vs. Input Voltage (V_{IN}) in Dropout

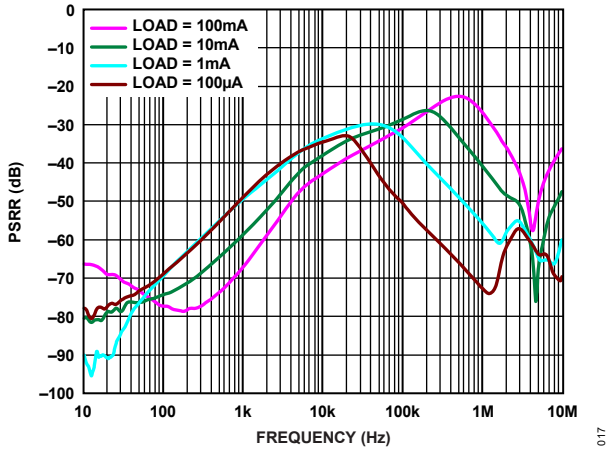

Figure 17. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.2V, V_{IN} = 2.2V

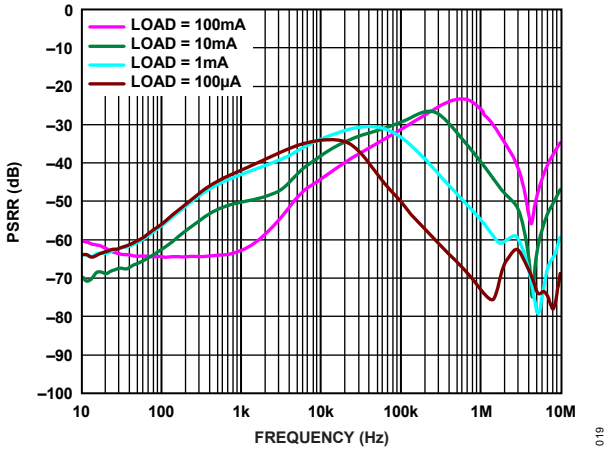

Figure 18. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3V, V_{IN} = 4.3V

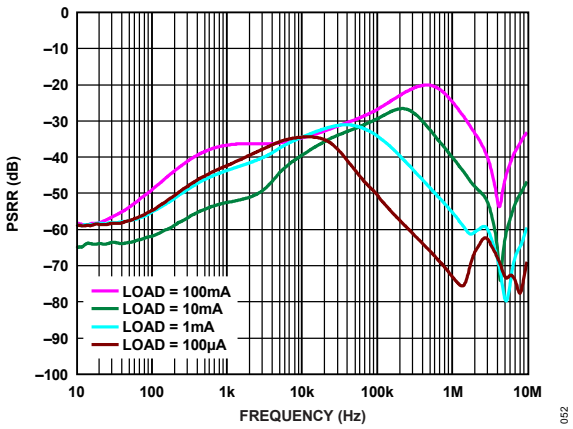

Figure 19.Power Supply Rejection Ratio vs. Frequency Various Output Voltages and Load Currents, V_{OUT} = 3.3V, V_{IN} = 3.8V

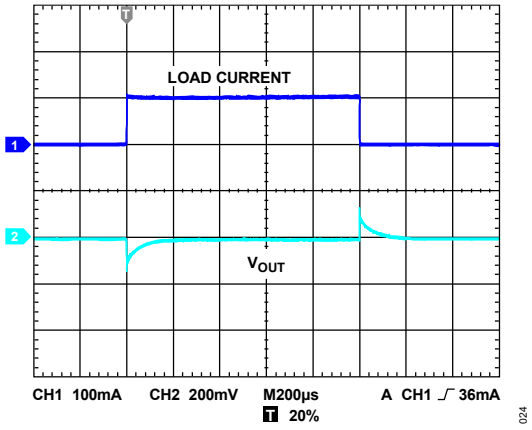

Figure 20.Load Transient Response, C_{IN}, C_{OUT} = 1µF, I_{LOAD} = 1mA to 100mA, 200ns Rise Time, CH1 = Load Current, CH2 = V_{OUT}

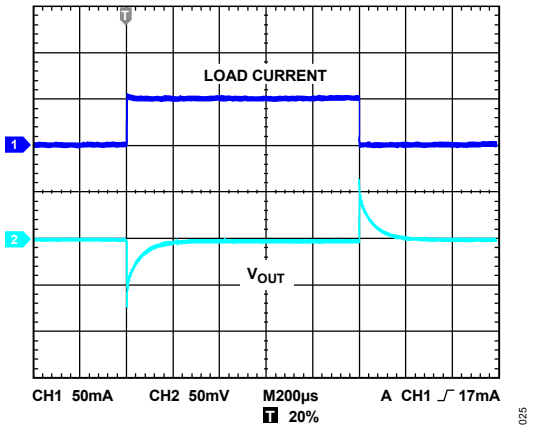

Figure 21. Load Transient Response, C_{IN}, C_{OUT} = 1µF, I_{LOAD} = 1mA to 50mA, 200ns Rise Time, CH1 = Load Current, CH2 = V_{OUT}

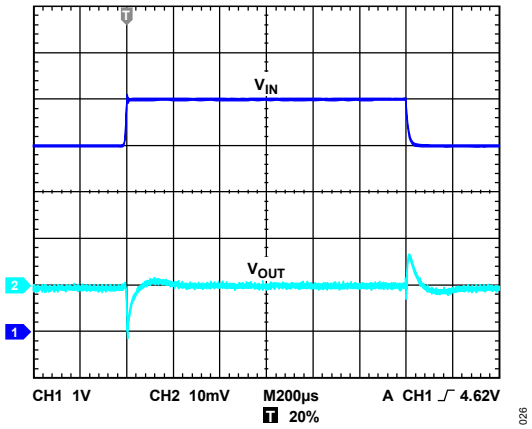

Figure 22. Line Transient Response, V_{IN} = 4V to 5V, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 100mA, CH1 = V_{IN}, CH2 = V_{OUT}

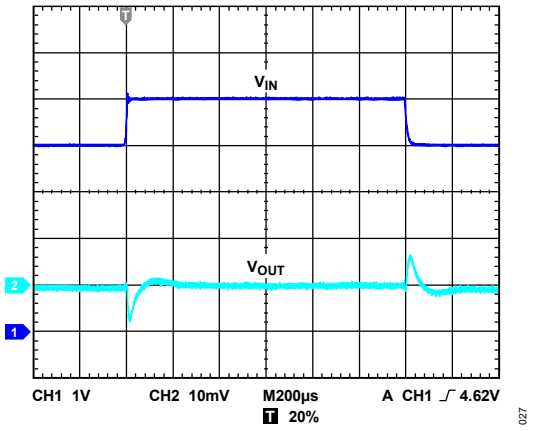

Figure 23. Line Transient Response, V_{IN} = 4V to 5V, C_{IN} = 1µF, C_{OUT} = 10µF, I_{LOAD} = 100mA, CH1 = V_{IN}, CH2 = V_{OUT}

THEORY OF OPERATION

The ADPL40501 is an ultra-low quiescent current, LDO linear regulator that operates from 2.2V to 5.5V and provides up to 100mA of output current. Drawing only 600nA (typical) at no load and a low 42µA of quiescent current (typical) at full load makes the ADPL40501 ideal for battery-operated portable equipment. Shutdown current consumption is typically 50nA.

Using new innovative design techniques, the ADPL40501 provides ultra-low quiescent current and superior transient performance for digital and RF applications. The ADPL40501 is also optimized for use with small 1µF ceramic capacitors.

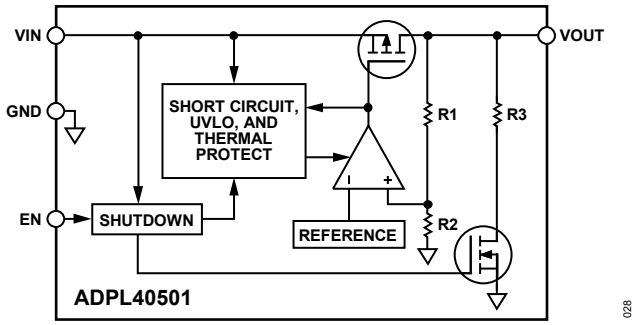

Figure 24. Internal Block Diagram, Fixed Output with Output Discharge Function

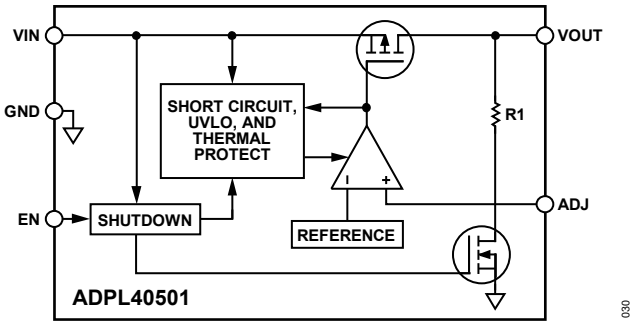

Figure 25. Internal Block Diagram, Adjustable Output with Output Discharge Function

Internally, the ADPL40501 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered through the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The adjustable ADPL40501 has an output voltage range of 1.0V to 4.2V. The output voltage is set by the ratio of two external resistors, as shown in *Figure 2*. The device servos the output to maintain the voltage at the ADJ pin at 1.0V referenced to ground. The current in R2 is then equal to 1.0V/R2, and the current in R1 is the current in R2 plus the ADJ pin bias current. The ADJ pin bias current, 10nA at 25°C, flows through R1 into the ADJ pin.

The output voltage can be calculated using the following equation:

$$V_{OUT} = 1.0V(1 + R1/R2) + (ADJ_{I\text{-}BIAS})(R1)$$

The value of R1 should be less than 200kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. For example, when R1 and R2 each equal 200kΩ, the output voltage is 2.0V. The output voltage error introduced by the ADJ pin bias current is 2mV or 0.05%, assuming a typical ADJ pin bias current of 10nA at 25°C.

To minimize quiescent current in the ADPL40501 Analog Devices, Inc., recommends using high values of resistance for R1 and R2. Using a value of 1MΩ for R2 keeps the total no-load quiescent current below 2µA. Note, however, that high value of resistance introduces a small output voltage error. For example, assuming R1 and R2 are 1MΩ, the output voltage is 2V. Taking into account the nominal ADJ pin bias current of 10nA, the output voltage error is 0.25%. Note that in shutdown, the output is turned off and the divider current is zero.

The ADPL40501 also includes an output discharge resistor that forces the output voltage to zero when the LDO is disabled. This ensures that the output of the LDO is always in a well-defined state, whether it is enabled or disabled.

The ADPL40501 is available in 7 output voltage options, ranging from 1.2V to 3.3V. The ADPL40501 uses the EN pin to enable and disable the V_{OUT} pin under normal operating conditions. When EN is high, V_{OUT} turns on, and when EN is low, V_{OUT} turns off. For automatic startup, EN can be tied to V_{IN}.

APPLICATIONS INFORMATION

Capacitor Selection

Output Capacitor

The ADPL40501 is designed to operate with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken regarding the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum capacitance of 1µF with an ESR of less than 1Ω is recommended to ensure stability of the ADPL40501. The transient response to changes in load current is also affected by the output capacitance. Using a larger value of output capacitance improves the transient response of the ADPL40501 to large changes in load current. *Figure 26* and *Figure 27* show the transient responses for output capacitance values of 1µF and 10µF, respectively.

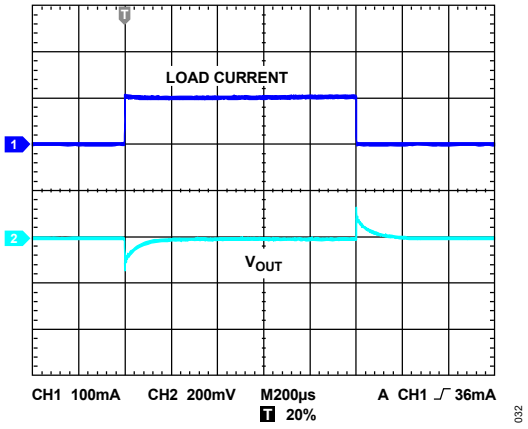

Figure 26. Output Transient Response, C_{OUT} = 1µF, CH1 = Load Current, CH2 = V_{OUT}

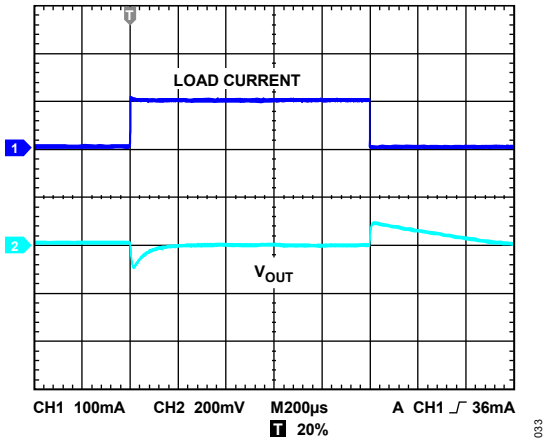

Figure 27. Output Transient Response, C_{OUT} = 10µF, CH1 = Load Current, CH2 = V_{OUT}

Input Bypass Capacitor

Connecting a 1µF capacitor from V_{IN} to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADPL40501, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and DC bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3V or 10V are recommended. Y5V and Z5U dielectrics are not recommended due to their poor temperature and DC bias characteristics.

Figure 28 depicts the capacitance vs. voltage bias characteristic of a 0402, 1µF, 10V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

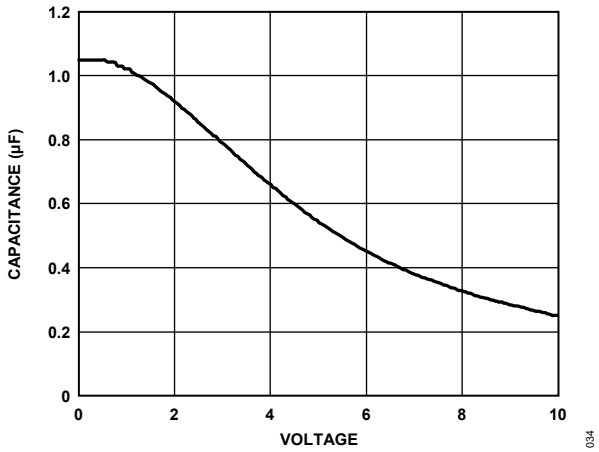

Figure 28. Capacitance vs. Voltage Characteristic

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94µF at 1.8V, as shown in *Figure 28*.

Substituting these values in Equation 1 yields:

$$C_{EFF} = 0.94\mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADPL40501, it is imperative that the effects of DC bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each.

Enable Feature

The ADPL40501 uses the EN pin to enable and disable the V_{OUT} pin under normal operating conditions. As shown in *Figure 29*, when a rising voltage on EN crosses the active threshold, V_{OUT} turns on. When a falling voltage on EN crosses the inactive threshold, V_{OUT} turns off.

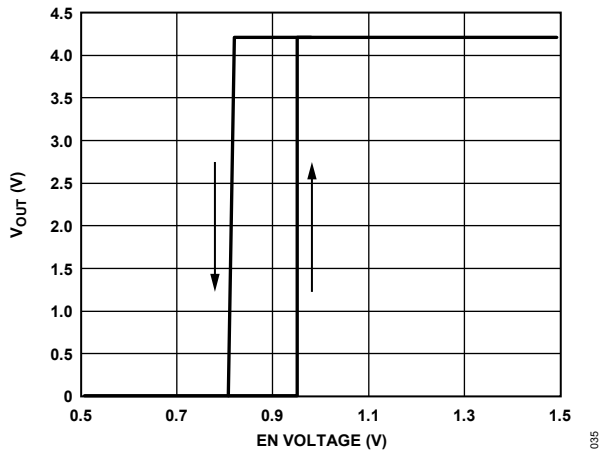

Figure 29. Typical EN Pin Operation

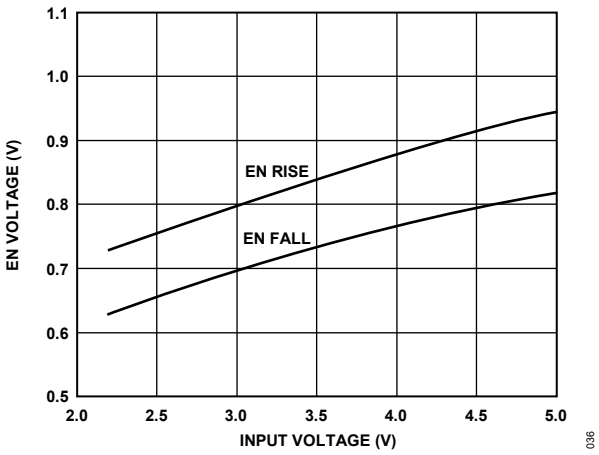

Figure 30. Typical EN Pin Thresholds vs. Input Voltage

As shown in *Figure 29*, the EN pin has built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the V_{IN} voltage; therefore, these thresholds vary with the input voltage. *Figure 30* shows typical EN active/inactive thresholds when the input voltage varies from 2.2V to 5.5V.

The start-up behavior of the ADPL40501 is shown in *Figure 31*, and the shutdown behavior of the ADPL40501 is shown in *Figure 32*.

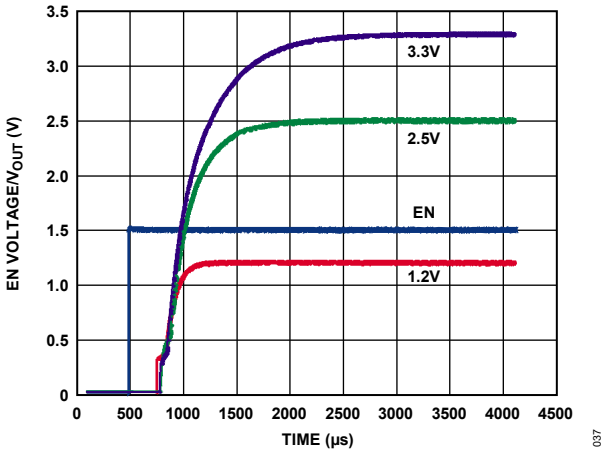

Figure 31. Typical Start-Up Behavior

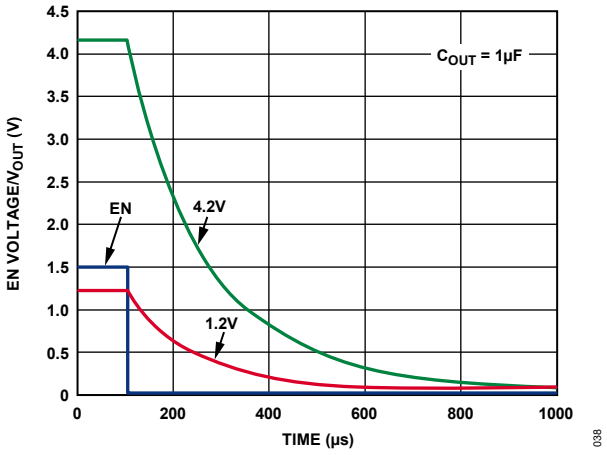

Figure 32. Typical Shutdown Behavior, No Load

Current Limit and Thermal Overload Protection

The ADPL40501 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. It is designed to current limit when the output load reaches 320mA (typical). When the output load exceeds 320mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from OUT to ground occurs. At first, the ADPL40501 current limits so that only 320mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 320mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 320mA and 0mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, the device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

PCB Layout Considerations

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADPL40501.

Place the input capacitor as close as possible to the V_{IN} and GND pins. Place the output capacitor as close as possible to the V_{OUT} and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

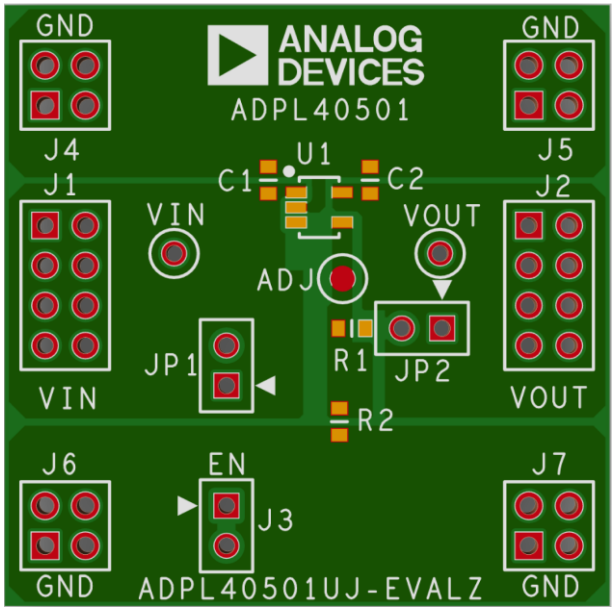

Figure 33.Example of 5-Lead TSOT PCB Layout

Light Sensitivity of WLCSPs

The WLCSP package option is essentially a silicon die with additional post-fabrication dielectric and metal processing designed to contact solder bumps on the active side of the chip. With this package type, the die is exposed to ambient light and is subject to photoelectric effects. Light sensitivity analysis of a WLCSP mounted on standard PCB material reveals that performance may be impacted when the package is illuminated directly by high-intensity light. No degradation in electrical performance is observed due to illumination by low intensity (0.1mW/cm^2) ambient light. Direct sunlight can have intensities of 50mW/cm^2, office ambient light can be as low as 0.1mW/cm^2.

When the WLCSP is assembled on the board with the bump side of the die facing the PCB, reflected light from the PCB surface is incident on active silicon circuit areas and results in the increased leakage currents. No performance degradation occurs due to illumination of the backside (substrate) of the WLCSP.

All WLCSPs are particularly sensitive to incident light with wavelengths in the near infrared range (NIR, 700nm to 1000nm). Photons in this waveband have longer wavelength and lower energy than photons in the visible (400nm to 700nm) and near ultraviolet (NUV, 200nm to 400nm) bands; therefore, they can penetrate more deeply into the active silicon.

Incident light with wavelengths greater than 1100nm has no photoelectric effect on silicon devices because silicon is transparent to wavelengths in this range.

The spectral content of conventional light sources varies considerably. Sunlight has a broad spectral range, with peak intensity in the visible band that falls off in the NUV and NIR bands; fluorescent lamps have significant peaks in the visible but not the NUV or NIR bands. Tungsten lighting has a broad peak in the longer visible wavelengths with a significant tail in the NIR.

Efforts have been made at a product level to reduce the effect of ambient light; the underbump metal (UBM) has been designed to shield the sensitive circuit areas on the active side (bump side) of the die. However, if an application encounters any light sensitivity with the WLCSP, shielding the bump side of the WLCSP package with an opaque material should eliminate this effect. Shielding can be accomplished using materials such as silica-filled liquid epoxies like those used in flip-chip underfill techniques.

OUTLINE DIMENSIONS

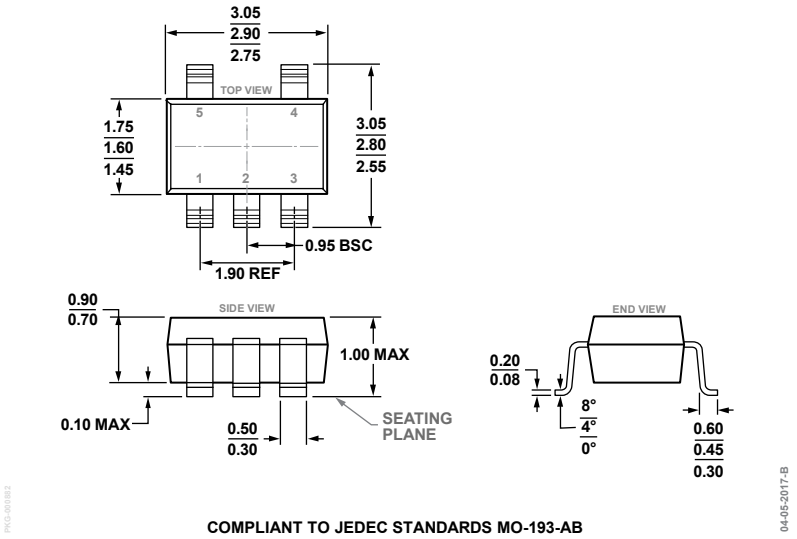

Figure 34. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5) Dimensions shown in millimeters

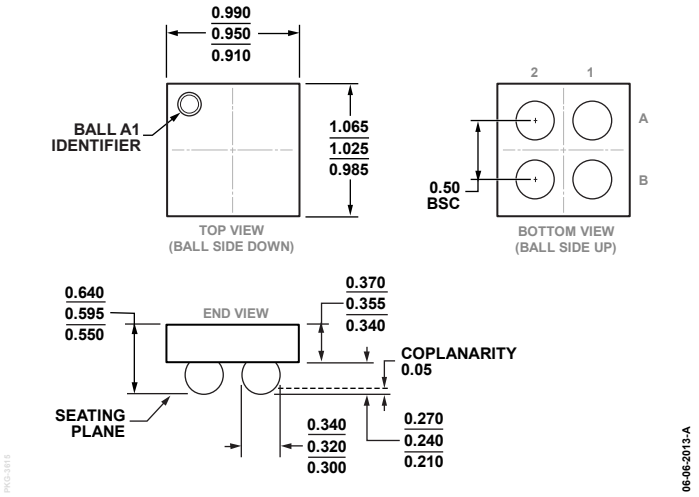

Figure 35. 4-Ball Wafer Level Chip Scale Package [WLCSP] (CB-4-4) Dimensions shown in millimeters

ORDERING GUIDE

Table 8. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	OUTPUT VOLTAGE (V)	PACKAGE DESCRIPTION	PACKAGE OPTION	BRANDING
ADPL40501ACBZ-1.2-R7	-40°C to +125°C	1.2	4-Ball WLCSP	CB-4-4	KC
ADPL40501ACBZ-1.8-R7	-40°C to +125°C	1.8	4-Ball WLCSP	CB-4-4	KB
ADPL40501ACBZ-2.8-R7	-40°C to +125°C	2.8	4-Ball WLCSP	CB-4-4	KA
ADPL40501ACBZ-3.0-R7	-40°C to +125°C	3.0	4-Ball WLCSP	CB-4-4	K9
ADPL40501ACBZ-3.3-R7	-40°C to +125°C	3.3	4-Ball WLCSP	CB-4-4	K8
ADPL40501AUJZ-1.2-R7	-40°C to +125°C	1.2	5-Lead TSOT	UJ-5	KN
ADPL40501AUJZ-1.8-R7	-40°C to +125°C	1.8	5-Lead TSOT	UJ-5	KP
ADPL40501AUJZ-2.3-R7	-40°C to +125°C	2.3	5-Lead TSOT	UJ-5	KQ
ADPL40501AUJZ-2.5-R7	-40°C to +125°C	2.5	5-Lead TSOT	UJ-5	KR
ADPL40501AUJZ-3.3-R7	-40°C to +125°C	3.3	5-Lead TSOT	UJ-5	KS
ADPL40501AUJZ-R7	-40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	KT
ADPL40501UJ-EVALZ			5-Lead TSOT Evaluation Board		

[1] Z = RoHS-Compliant Part.