ADPL31613

Dual 1.3A, 1.2MHz Boost/Inverter in 3mm × 3mm DFN

FEATURES

- 1.2MHz Switching Frequency
- Low V_{CESAT} Switches: 380mV at 1.3A
- High Output Voltage: Up to 38V
- Wide Input Range: 2.4V to 16V
- Inverting Capability
- 5V at 630mA from 3.3V Input
- 12V at 320mA from 5V Input
- –12V at 200mA from 5V Input
- Uses Tiny Surface-Mount Components
- Low Shutdown Current: <2µA
- Low Profile (0.75mm) 10-Lead 3mm × 3mm Dual Flat No-Lead (DFN) Package

APPLICATIONS

- Organic Light Emitting Diode (LED) Power Supply
- Digital Cameras
- White LED Power Supply
- Cellular Phones
- Medical Diagnostic Equipment
- Convertible ±5V or ±12V Supply
- Thin-Film Transistor (TFT)– Liquid-Crystal Display (LCD) Bias Supply
- X Digital Subscriber Line (xDSL) Power Supply

GENERAL DESCRIPTION

The **ADPL31613** dual switching regulator combines two 38V, 1.3A switches with error amplifiers that can sense to ground, providing boost and inverting capability. The low-V_{CESAT} bipolar switches enable the device to deliver high-current outputs in a small footprint. The ADPL31613 switches at 1.2MHz, enabling the use of tiny, low-cost, low-profile inductors and capacitors. High inrush current at start-up is eliminated by the programmable soft-start function, in which an external resistor-capacitor (RC) sets the current ramp rate. A constant-frequency current-mode pulse width modulation (PWM) architecture results in low, predictable output noise that is easy to filter.

The ADPL31613 switches are rated at 40V, making the device ideal for boost converters up to ±38V, and for SEPIC and flyback designs. Each channel can generate 5V at up to 630mA from a 3.3V supply, or 5V at 510mA from four alkaline cells in a single-ended primary inductor converter (SEPIC) design. The device can be configured as two boosts, a boost and inverter, or two inverters.

The ADPL31613 is available in a low-profile (0.75mm) 10-lead 3mm × 3mm DFN package.

TYPICAL APPLICATION

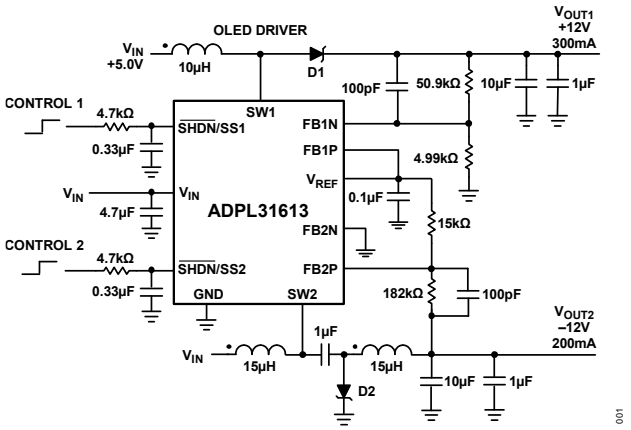

Figure 1. Organic Light-Emitting Diode (OLED) Driver

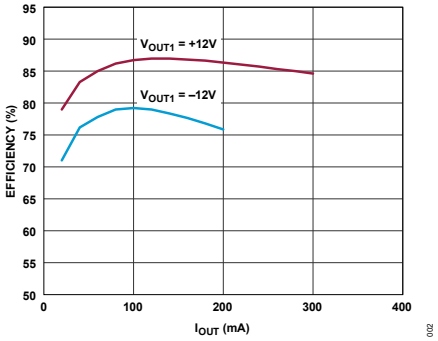

Figure 2. OLED Driver Efficiency

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/26	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C. V_{IN} = $V_{\overline{SHDN}}$ = 3V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Operating Voltage			2.1	2.4	V
Reference Voltage	-40°C ≤ T_J ≤ 85°C	0.987	1.000	1.013	V
Reference Voltage Current Limit	(Note 3)	1.2	1.68		mA
Reference Voltage Load Regulation	0mA ≤ I_{REF} ≤ 100µA[3]		0.12	0.25	%/100µA
Reference Voltage Line Regulation	2.6V ≤ V_{IN} ≤ 16V		0.04	0.09	%V
Error Amplifier Offset	Transition from not switching to switching, V_{FBP} = V_{FBN} = 1V		2.4	3.5	mV
FB Pin Bias Current	V_{FB} = 1V[3], 40°C ≤ T_J ≤ 85°C		70	115	nA
Quiescent Current	$V_{\overline{SHDN}}$ = 1.8V, Not switching		2.5	6	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0.3V, V_{IN} = 3V		0.01	2	µA
Switching Frequency	-40°C ≤ T_J ≤ 85°C	1	1.3	1.4	MHz
Maximum Duty Cycle	-40°C ≤ T_J ≤ 85°C	90 86	94		% %
Minimum Duty Cycle	-40°C ≤ T_J ≤ 85°C		15		%
Switch Current Limit	At minimum duty cycle At maximum duty cycle[4] -40°C ≤ T_J ≤ 85°C	1.5 0.9	2.05 1.45	2.6 2.0	A A
Switch V_{CESAT}	I_{SW} = 0.5A[5]		170	290	mV
Switch Leakage Current	V_{SW} = 5V		0.015	1.3	µA
$\overline{SHDN}$/SS Input Voltage High		1.8			V
$\overline{SHDN}$/SS Input Voltage Low	Quiescent current ≤ 1µA			0.3	V
$\overline{SHDN}$/SS Pin Bias Current	$V_{\overline{SHDN}}$ = 3V, V_{IN} = 4V $V_{\overline{SHDN}}$ = 0V		24 0.1	46 0.2	µA µA

1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

2 The ADPL31613 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over –40°C to 85°C operating temperature range are assured by design, characterization, and correlation with statistical process controls.

[3] Current flows out of the pin.

[4] See the *Typical Performance Characteristics* for guaranteed current limit vs. duty cycle.

[5] V_{CESAT} is 100% tested at wafer level only.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} Voltage	16V
SW1, SW2 Voltage	-0.4V to 40V
FB1N, FB1P, FB2N, FB2P Voltage	12 or V_{IN}–1.5V
$\overline{SHDN}$/SS1, $\overline{SHDN}$/SS2 Voltage	16V
V_{REF} Voltage	1.5V
Maximum Junction Temperature	125°C
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 125°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

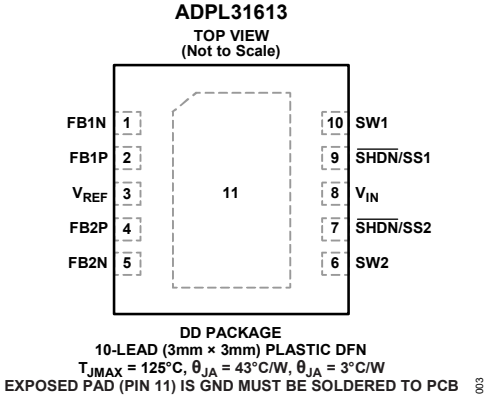


Figure 3. ADPL31613 Pin Configuration

Pin Descriptions

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	FB1N	Negative Feedback Pin for Switcher 1. Connect resistive divider tap here. Minimize trace area at FB1N. Set $V_{OUT} = V_{FB1P}(1 + R1/R2)$, or connect to ground for inverting topologies.
2	FB1P	Positive Feedback Pin for Switcher 1. Connect either to V_{REF} or a divided-down version of V_{REF}, or connect to a resistive divider tap for inverting topologies.
3	V_{REF}	1V Reference Pin. Can supply up to 1mA of current. Do not pull this pin high. The pin must be locally bypassed with a capacitor of 0.01µF or more, but no more than 1µF. A 0.1µF ceramic capacitor is recommended. Use this pin as the positive feedback reference, or connect a resistor divider here to obtain a smaller reference voltage.
4	FB2P	Same as FB1P but for Switcher 2.
5	FB2N	Same as FB1N but for Switcher 2.
6	SW2	Switch Pin for Switcher 2 (Collector of internal negative-positive-negative (NPN) power switch). Connect the inductor/diode here and minimize the metal trace area connected to this pin to minimize electromagnetic interference (EMI).
7	$\overline{SHDN}$/SS2	Shutdown and Soft-Start Pin. Tie to 1.8V or more to enable the device. Ground to shut down. The soft-start function is enabled when the voltage at this pin is ramped slowly to 1.8V using an external resistor–capacitor (RC) circuit.
8	V_{IN}	Input Supply. Must be locally bypassed.
9	$\overline{SHDN}$/SS1	Same as $\overline{SHDN}$/SS2 but for Switcher 1. Note: Driving either the $\overline{SHDN}$/SS pin high enables the device. Each switching regulator can be enabled independently through its corresponding $\overline{SHDN}$/SS pin.
10	SW1	Same as SW2 but for Switcher 1.
11	Exposed Pad	Ground. Connect the pin directly to the local ground plane. This ground plane also serves as a heatsink for optimal thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

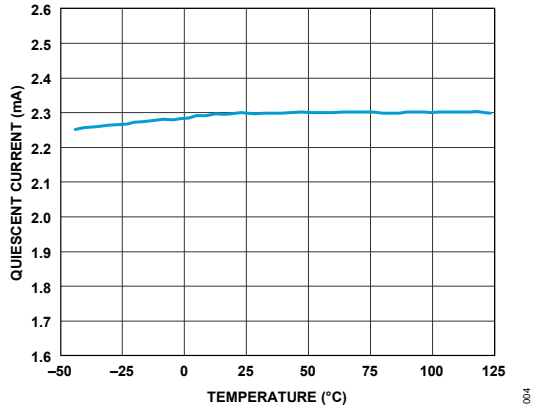


Figure 4. Quiescent Current vs. Temperature

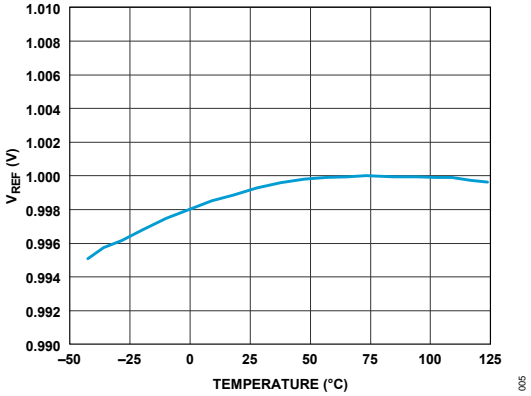


Figure 5. V_{REF} vs. Temperature

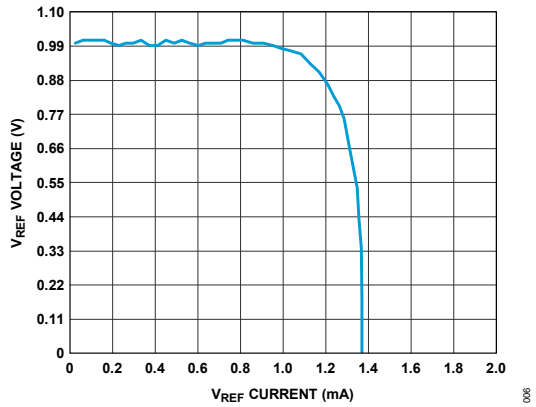


Figure 6. V_{REF} Voltage vs. V_{REF} Current

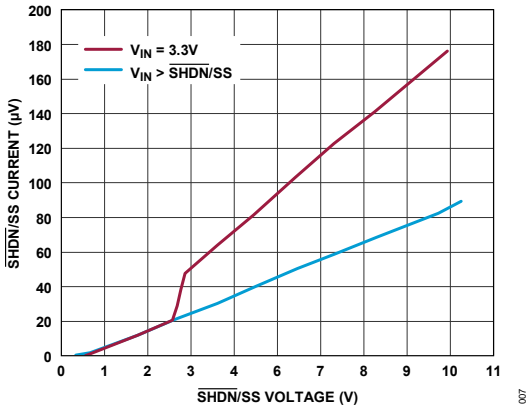


Figure 7. $\overline{SHDN}$/SS Current vs. $\overline{SHDN}$/SS Voltage

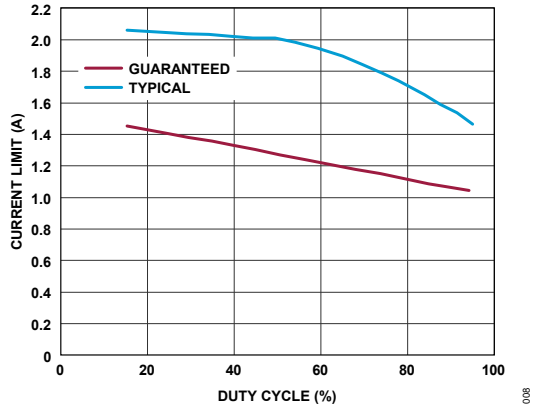


Figure 8. Current Limit vs. Duty Cycle

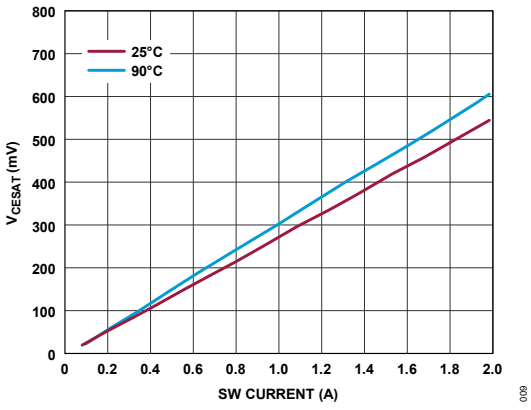


Figure 9. Switch Saturation Voltage vs. Switch Current

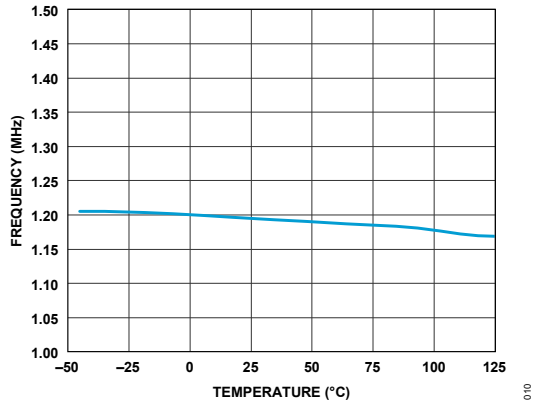


Figure 10. Oscillator Frequency vs. Temperature

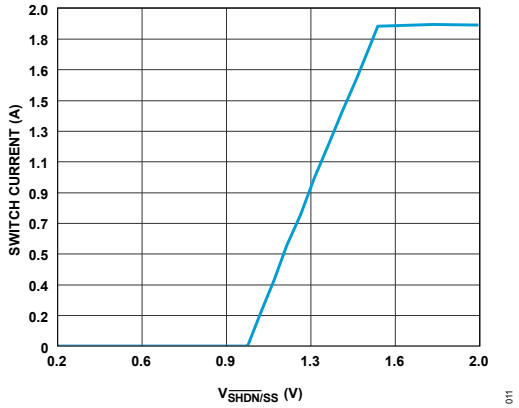


Figure 11. Peak Switch Current vs. $\overline{SHDN}$/SS Voltage

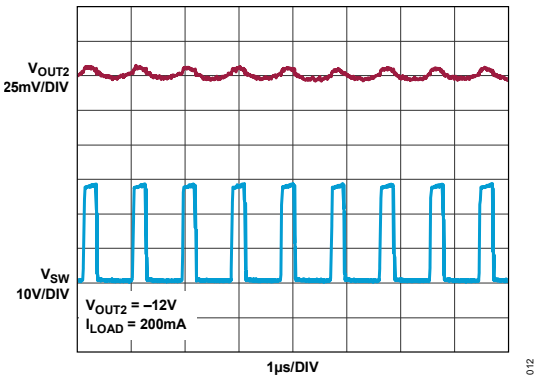


Figure 12. Switching Waveform

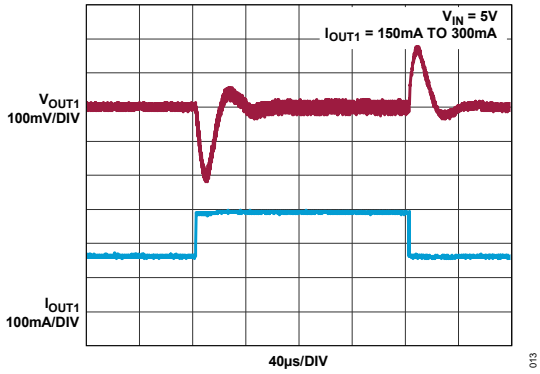


Figure 13. Transient Response

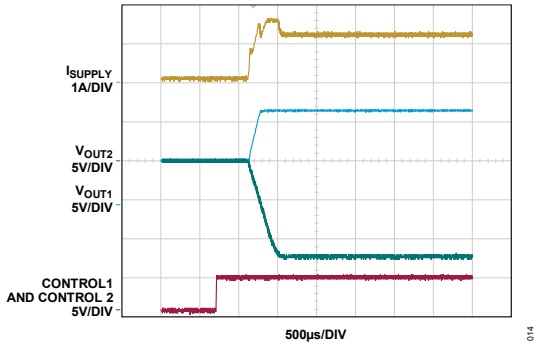


Figure 14. Start-up Waveform

THEORY OF OPERATION

Block Diagram

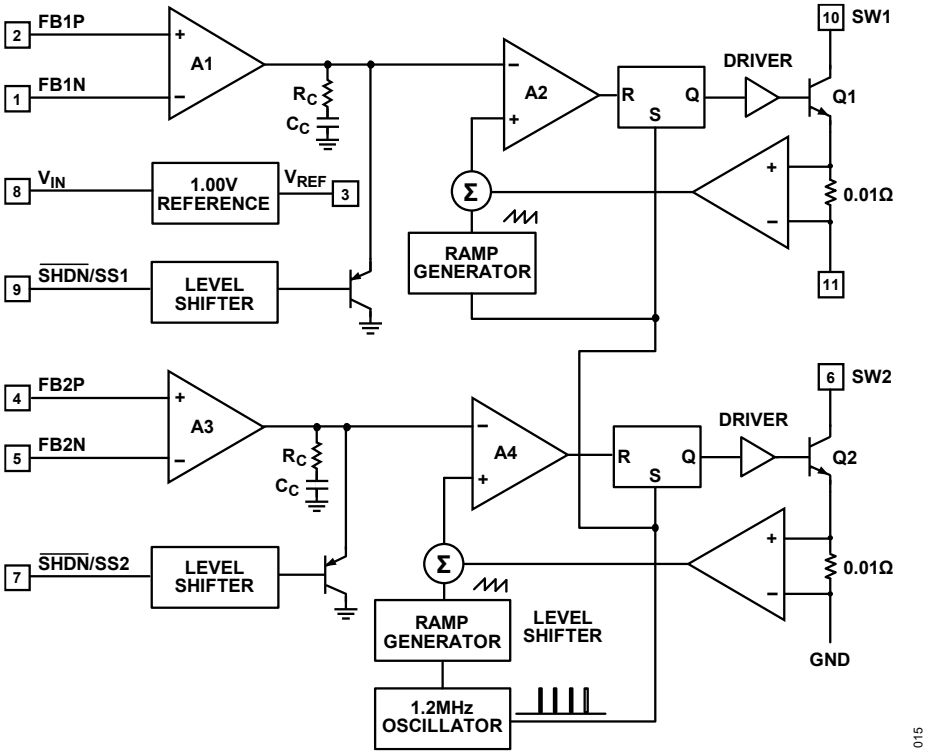


Figure 15. ADPL31613 Block Diagram

Operation

The ADPL31613 uses a constant-frequency, current-mode control scheme to provide excellent line and load regulation. See the *Figure 15* (Block Diagram) for more details. At the start of each oscillator cycle, the set-reset (SR) latch is set, which turns on the power switch, Q1 (Q2). A voltage proportional to the switch current is added to a stabilizing ramp, and the resulting sum is fed into the positive terminal of the PWM comparator A2 (A4). When this voltage exceeds the threshold at the inverting input of A2 (A4), the SR latch resets, turning off power switch Q1 (Q2). The threshold at the inverting input of A2 (A4) is established by error amplifier A1 (A3) and represents an amplified version of the difference between the feedback voltage and the reference voltage, typically V_{REG}. This control loop adjusts the peak current as required to maintain output voltage regulation. If the error amplifier's output increases, more current is delivered to the output. Similarly, if the error decreases, less current is delivered. Each switcher functions independently, but they share the same oscillator, so they are always in phase. Enabling the device is done by taking either the $\overline{SHDN}$/SS pin above 1.8V.

The device is disabled when both $\overline{SHDN}$/SS pins are held low. The soft-start feature of the ADPL31613 enables clean start-up by limiting the output voltage rise of comparators A1 and A2, which in turn limits the peak switching current. The soft-start feature for each switcher is enabled by slowly ramping that switcher's $\overline{SHDN}$/SS2 pin, using an RC network. For example, typical resistor and capacitor values are 0.33µF and 4.7kΩ, allowing for a start-up time on the order of milliseconds. The ADPL31613 has a current-limit circuit that is not shown in the *Figure 15* (Block Diagram).

The switch current is continuously monitored and must not exceed the maximum switch current (typically 1.6A). If the switch current reaches this value, the SR latch is reset regardless of the state of the comparator A2 (A4). The thermal shutdown circuit is also not shown in *Figure 15* (Block Diagram). If the device temperature exceeds approximately 160°C, both latches are reset regardless of the state of comparators A2 and A4. The current-limit and thermal-shutdown circuits protect the power switch and the external components connected to the ADPL31613.

APPLICATIONS INFORMATION

Duty Cycle

The typical maximum duty cycle of the ADPL31613 is 94%. The duty cycle for a given application is given by:

$$DC = \frac{|V_{OUT}| + |V_D| - |V_{IN}|}{|V_{OUT}| + |V_D| - |V_{CESAT}|}$$

where V_D is the diode forward voltage drop, and V_{CESAT} is 380mV maximum at a load current of 1.3A.

The ADPL31613 can be used at higher duty cycles, but it must be operated in discontinuous conduction mode so that the actual duty cycle is reduced.

Setting Output Voltage

Setting the output voltage depends on the topology used. Use the following equation for typical non-inverting boost regulator topologies:

$$V_{OUT} = V_{FBP}\left(1 + \frac{R_1}{R_2}\right)$$

where V_{FBN} is connected between R1 and R2 (See the *Typical Applications* section for application examples). Select the values of R1 and R2 according to the following equation:

$$R_1 = R_2\left[\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right]$$

An ideal value for R2 is 15kΩ, which sets the current in the resistor divider chain to 1.00V/15kΩ = 67µA. V_{FBP} is usually connected to V_{REF} = 1V, but V_{FBP} can also be connected to a divided-down version of V_{REF} or another voltage as long as the absolute maximum ratings for the feedback pins are not exceeded (see the *Absolute Maximum Ratings* for more details).

For inverting topologies, V_{FBN} is connected to ground, and V_{FBP} is connected between R1 and R2. R2 is between V_{FBP} and V_{REF}, and R1 is between V_{FBP} and V_{OUT} (see the *Applications* section for examples). In this case:

$$V_{OUT} = V_{REF}\left(\frac{R_1}{R_2}\right)$$

Select the values of R1 and R2 according to the following equation:

$$R_1 = R_2\left[\left(\frac{V_{OUT}}{V_{REF}}\right)\right]$$

An ideal value for R2 is 15kΩ, which sets the current in the resistor divider chain to 1V/15kΩ = 67µA.

Switching Frequency and Inductor Selection

The ADPL31613 switches at 1.2 MHz, allowing compact, low-value inductors to be used. 4.7µH or 10µH will usually suffice. Select an inductor that can handle at least 1.4A without saturating, and ensure it has a low DCR (copper-wire resistance) to minimize I^2R power losses. Note that in some applications, the inductor's current handling requirements can be lower, such as in the SEPIC topology, where each inductor carries only half of the total switch current. For better efficiency, use similar-valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers. Choose a core material with low losses at 1.2 MHz, such as a ferrite core.

Table 4. Inductor Manufacturers

MANUFACTURER	PHONE	WEBSITE
Sumida	(847) 956-0666	www.sumida.com
TDK	(847) 803-6100	www.tdk.com
Murata	(714) 852-2001	www.murata.com

Soft-Start and Shutdown Features

To shut down the part, ground both $\overline{SHDN}$/SS pins. To disable one switcher while leaving the other operational, pull the corresponding $\overline{SHDN}$/SS pin low (connect it to ground). The soft-start feature helps limit the inrush current drawn from the supply at start-up. To use the soft-start feature for either switcher, slowly ramp up that switcher's $\overline{SHDN}$/SS pin. The rate of voltage rise at the output of the switcher's comparator (A1 or A3 for switcher 1 or switcher 2, respectively) tracks the rate of voltage rise at the $\overline{SHDN}$/SS pin once the $\overline{SHDN}$/SS pin has reached about 1.1V. The soft-start function will be disabled once the voltage at the $\overline{SHDN}$/SS pin exceeds 1.8V. See the Peak Switch Current vs. $\overline{SHDN}$/SS Voltage graph (*Figure 11*) in the *Typical Performance Characteristics* section.

The rate of voltage rise at the $\overline{SHDN}$/SS pin can easily be controlled with a simple RC network connected between the control signal and the $\overline{SHDN}$/SS pin. Typical values for the RC network are 4.7kΩ and 0.33µF, yielding start-up times on the order of milliseconds. This RC time constant can be adjusted to give different start-up times. If different values of resistance are to be used, see the $\overline{SHDN}$/SS Current vs. $\overline{SHDN}$/SS Voltage graph (*Figure 7*) and the Peak Switch Current vs. $\overline{SHDN}$/SS Voltage graph (*Figure 11*) in the *Typical Performance Characteristics* section. The impedance looking into the $\overline{SHDN}$/SS pin depends on whether the $\overline{SHDN}$/SS is above or below V_{IN}. Typically, the $\overline{SHDN}$/SS pin will not be driven above V_{IN}, so the impedance appears as 100kΩ in series with a diode. If the $\overline{SHDN}$/SS pin voltage is above V_{IN}, the impedance appears more like 50kΩ in series with a diode. A 100kΩ or 50kΩ impedance can increase the start-up time if an excessively large resistor is selected for the RC soft-start network. Another consideration is selecting the soft-start time so that the soft-start feature is dominated by the RC network rather than by the capacitor on V_{REF}. (See the *VREG Voltage Reference* section in the *Applications Information* for more details.)

The soft-start feature is essential in applications where the switch will see voltages of 30V or higher. In these applications, the simultaneous presence of high current and voltage during start-up may cause overstress on the switch. Therefore, depending on the input and output voltage conditions, higher RC time constants may be necessary to improve the design's ruggedness.

Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have extremely low ESR and are available in very small packages. X5R dielectrics are preferred, followed by X7R, as these materials retain the capacitance over wide voltage and temperature ranges. A 4.7µF to 15µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than ceramic and will have a higher ESR. Always use a capacitor with a sufficient voltage rating.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as close as possible to the ADPL31613. A 4.7µF to 10µF input capacitor is sufficient for most applications. *Table 5* lists several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 5. Ceramic Capacitor Manufacturers

MANUFACTURER	PHONE	WEBSITE
Taiyo Yuden	(408) 573-4150	www.t-yuden.com
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com

The choice between low-ESR (ceramic) and higher-ESR (tantalum or OS-CON) capacitors can affect the overall system's stability. The ESR of any capacitor, along with its capacitance, contributes a zero to the system. For the tantalum and OS-CON capacitors, the zero occurs at a lower frequency due to their higher ESR. In contrast, the ceramic capacitor's zero occurs at a much higher frequency and can generally be ignored.

A phase lead zero can be intentionally introduced by placing a capacitor (CPL) in parallel with resistor (R4) between V_{OUT} and V_{FB}, as shown in *Figure 16*. The frequency of the zero is determined by the following equation.

$$f_Z = \frac{1}{2\pi \times R_3 \times C_{PL}}$$

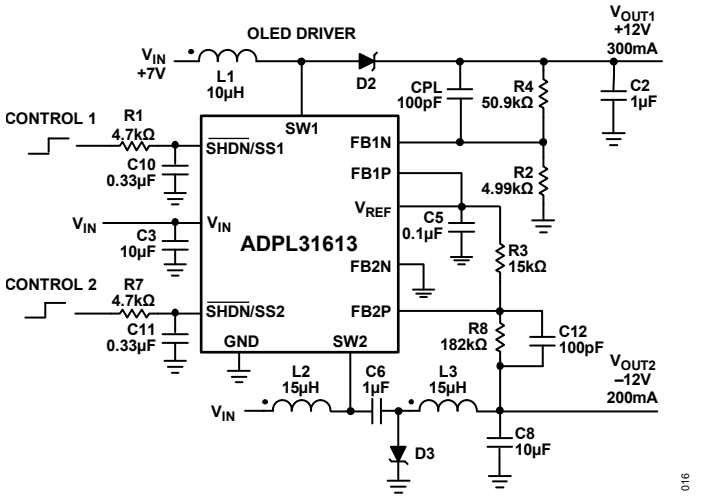


Figure 16. Lithium-Ion OLED Driver

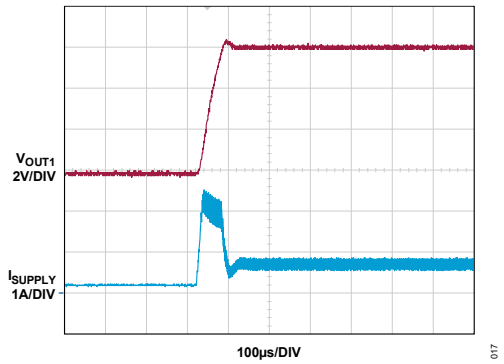


Figure 17. Supply Current of Lithium-Ion OLED Driver (Figure 16) during Start-Up without Soft-Start Network

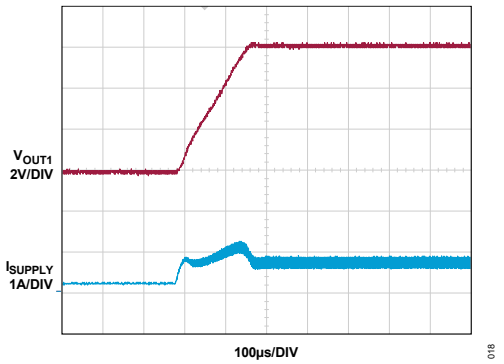


Figure 18. Supply Current of Lithium-Ion OLED Driver (Figure 16) during Start-Up with Soft-Start Network

By choosing appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the overall converter's phase margin. The typical target value for the zero frequency is between 35kHz and 55kHz. *Figure 19* shows the transient response of the step-up converter from *Figure 16* without the phase lead capacitor CPL. Although adequate for many applications, phase margin is not ideal, as evidenced by 2 to 3 bumps in both the output voltage and inductor current. A 100pF capacitor for CPL results in an ideal phase margin, as shown in *Figure 20*, with a more damped response and less overshoot.

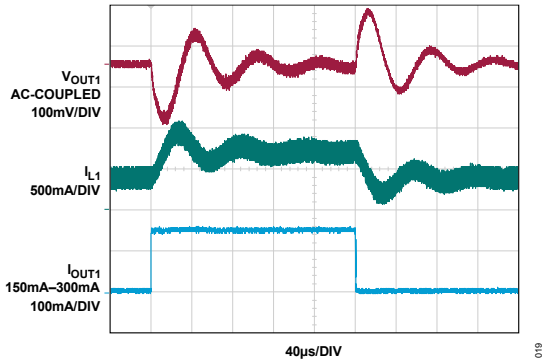


Figure 19. Transient Response of Lithium-Ion OLED Driver's (Figure 16) Step-Up Converter without Phase Lead Capacitor

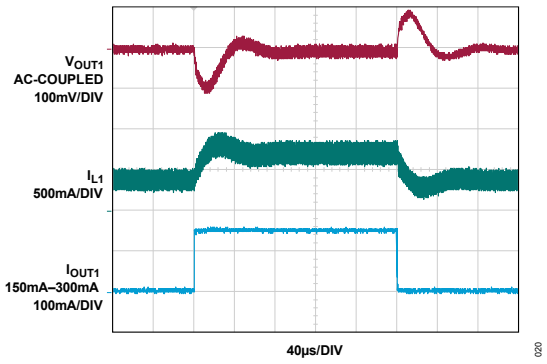


Figure 20. Transient Response of Lithium-Ion OLED Driver's (Figure 16) Step-Up Converter with 100pF Phase Lead Capacitor

V_{REG} Voltage Reference

Pin 3 of the ADPL31613 is a bandgap voltage reference that has been divided down to 1V and buffered for external use. Bypass this pin with a capacitor ranging from 0.01µF to 1µF. This will ensure stability and reduce noise on this pin. The buffer has a built-in current limit of at least 1mA (typically 1.4mA). Use this pin as an external reference for supplemental circuitry, and note that a soft-start feature is possible if this pin is used as one of the error amplifier's feedback pins. Typically, the soft-start time will be dominated by the RC time constant discussed in the soft-start and shutdown section. However, because the V_{REG} pin buffer has limited output current, the bypass capacitor charges gradually. During this time, the V_{REG} voltage ramps up, providing an alternative means of soft-starting the device. If the largest recommended bypass capacitor is used, 1µF, the worst-case (longest) soft-start function that would be provided from the V_{REF} pin is shown in the following equation:

$$\frac{1\mu F \text{ x} 1V}{1.0mA} = 1.0ms$$

Select the RC network such that its soft-start interval exceeds the charging time of the V_{REF} bypass capacitor. Alternatively, a smaller V_{REF} bypass capacitor value (greater than 0.01µF) can be used to ensure that the RC network determines the soft-start characteristics of the ADPL31613. The voltage at the V_{REF} pin can also be divided down and used for one of the feedback pins for the error amplifier. This is especially useful in light-emitting diode (LED) driver applications, where the current through the LEDs is set using the voltage reference across a sense resistor in the LED chain. Using a smaller or divided-down reference reduces power wasted in the sense resistor. See the Typical Applications section for examples of LED-driving applications.

Diode Selection

A Schottky diode is recommended for use with the ADPL31613. For optimum efficiency, select a diode with low forward voltage and good thermal performance at high currents, such as the onsemi MBRM120 (20V rated). For applications where the switch voltage exceeds 20V, use the On Semiconductor MBRM140, which is rated for 40V operation. These diodes are rated to handle an average forward current of 1.0A. In applications in which the average forward current of the diode is less than 0.5A, use the Philips PMEG 2005, 3005, or 4005 (a 20V, 30V or 40V diode, respectively).

Printed Circuit Board (PCB) Guidelines

The ADPL31613 high switching frequency necessitates careful PCB layout. Recommended component placement is shown in *Figure 21*.

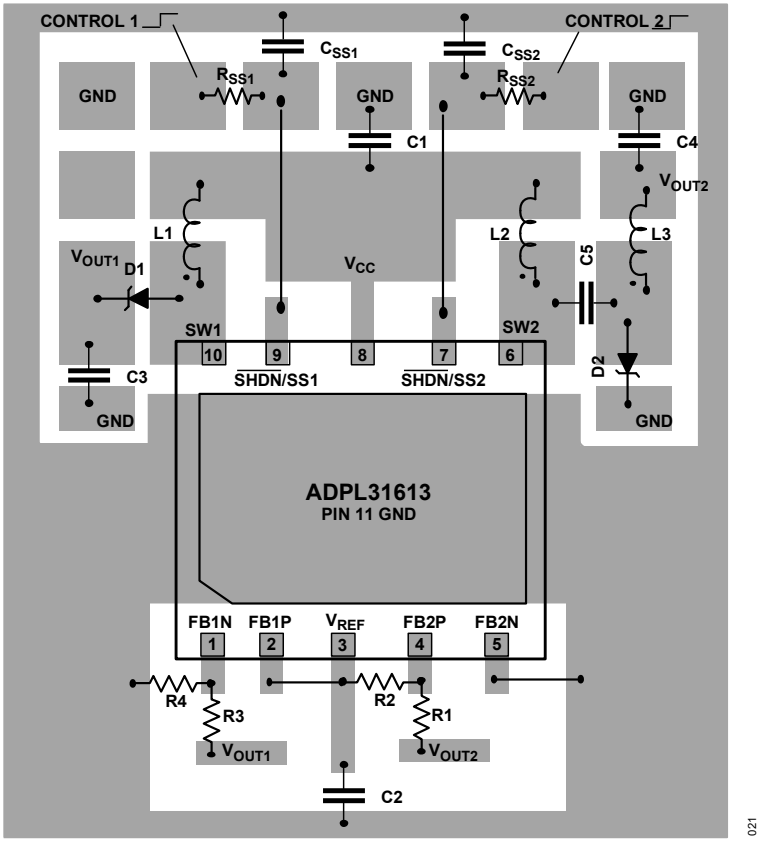


Figure 21. Suggested Layout showing a Boost on SW1 and an Inverter on SW2

Compensation—Theory

As with all current-mode switching regulators, the ADPL31613 requires loop compensation to ensure stable and efficient operation. The ADPL31613 employs two feedback loops: a fast current-control loop that requires no compensation and a slower voltage-control loop that requires compensation. Standard Bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. *Figure 22* shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor, and diode have been replaced by the equivalent transconductance amplifier g_{mp}. g_{mp} acts as a current source, with the output current proportional to the V_C voltage. Note that the maximum output current of the g_{mp} is finite due to the device's current limit.

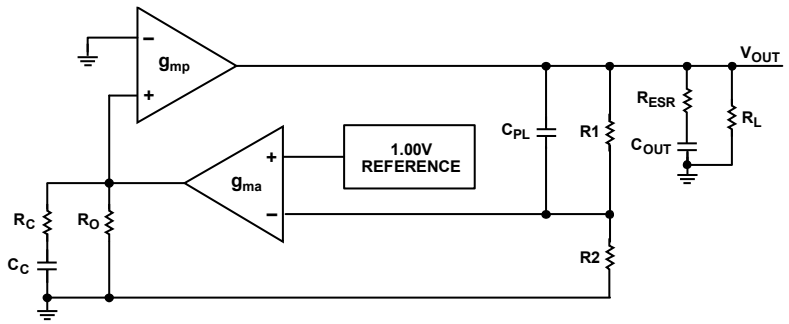
For the Boost Converter Equivalent Model (*Figure 22*), the DC gain, poles, and zeros can be calculated using the following equations:

Output pole:

$$P1 = \frac{2}{2 \times \pi \times R_L \times C_{OUT}}$$

Error amplifier pole:

$$P2 = \frac{1}{2 \times \pi \times R_O \times C_C}$$



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
g_{ma}: TRANSCUNDUCTANCE AMPLIFIER INSIDE IC
g_{mp}: POWER STANGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS VOUT DIVIDED BY $I_{LOAD(MAX)}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R1, R2: FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR

Figure 22. Boost Converter Equivalent Model

Error amplifier zero:

$$Z1 = \frac{1}{2 \times \pi \times R_C \times C_C}$$

DC gain:

$$A = \frac{V_{REF}}{V_{OUT}} \times g_{ma} \times R_O \times g_{mp} \times R_L \times \frac{1}{2}$$

ESR zero:

$$Z2 = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

Right-half-plane (RHP) zero:

$$Z3 = \frac{V_{IN}^2 \times R_L}{2 \times \pi \times V_{OUT}^2 \times L}$$

High-frequency pole:

$$P3 > \frac{f_s}{3}$$

Phase-lead zero:

$$Z4 = \frac{1}{2 \times \pi \times R_1 \times C_{PL}}$$

Phase-lead pole:

$$P4 = \frac{1}{2 \text{ x } \pi \text{ x } C_{PL} \text{ x } \frac{R_1 \text{ x } R_2}{R_1 + R_2}}$$

Current-mode control is a right-half-plane (RHP) zero that can complicate feedback control design; however, stable operation can be achieved through proper selection of external components.

Using the circuit shown in Typical Application (*Figure 1*) as an example, the parameters listed in *Table 6* were used to generate the Bode plot shown in *Figure 23*.

Table 6. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	40	Ω	Application Specific
C_{OUT}	10	µF	Application Specific
R_{ESR}	4.05	mΩ	Application Specific
R_O	0.9	MΩ	Not Adjustable
C_C	90	pF	Not Adjustable
CPL	100	pF	Adjustable
R_C	55	kΩ	Not Adjustable
R1	54.9	kΩ	Adjustable
R2	4.99	kΩ	Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	7	V	Application Specific
g_{ma}	50	µmho	Not Adjustable
g_{mp}	9.3	mho	Not Adjustable
L	10	µH	Application Specific
f_S	1.2	MHz	Not Adjustable

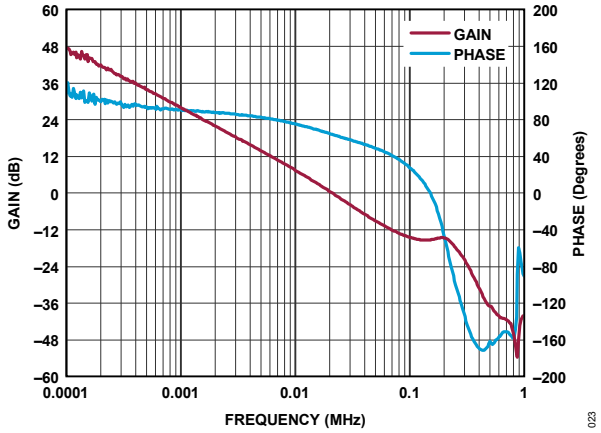


Figure 23. Bode Plot of 7V to 12V Application

As shown in *Figure 23*, the phase at the 0 dB crossover frequency is −115°, yielding a phase margin of 65°, providing ample stability. The crossover frequency is approximately 21kHz.

TYPICAL APPLICATIONS

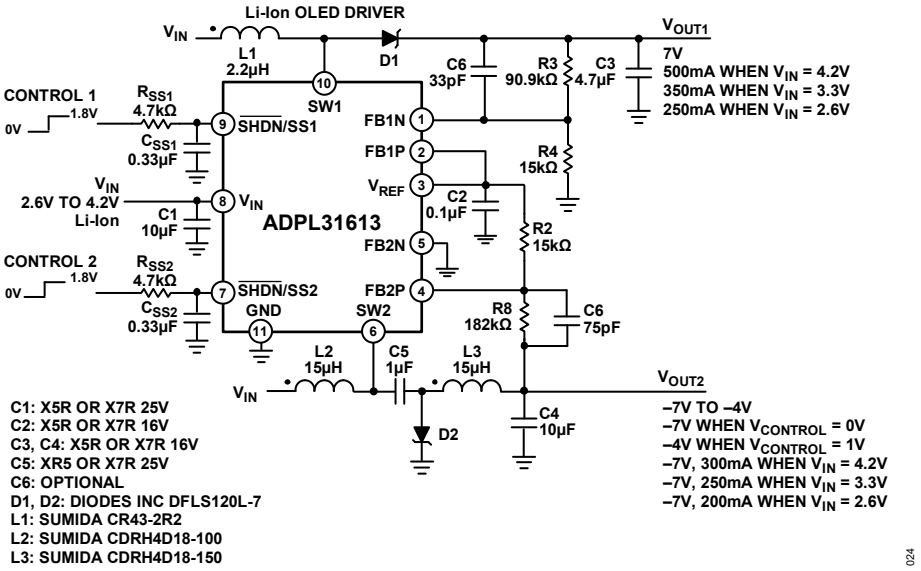


Figure 24. Lithium-Ion OLED Driver (±7V)

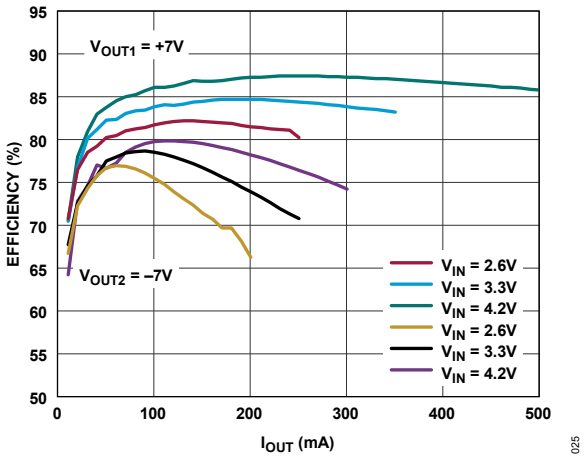


Figure 25. Lithium-Ion OLED Driver Efficiency

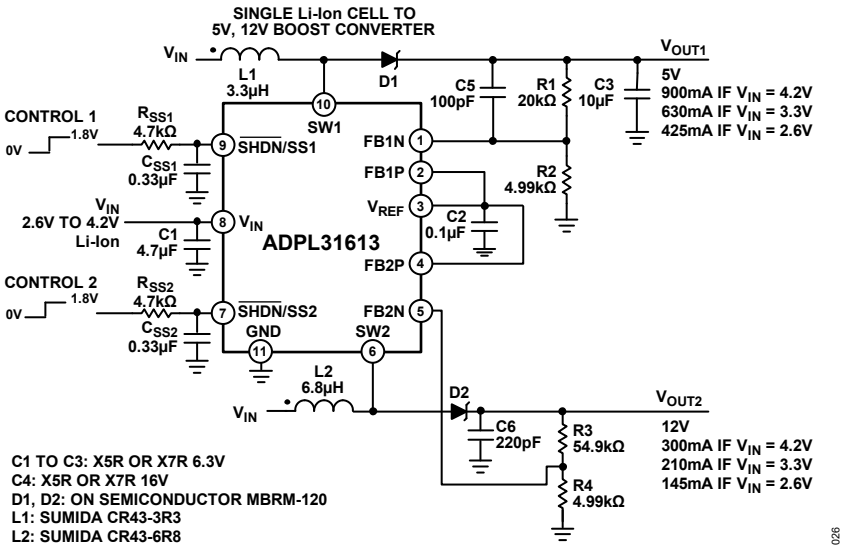


Figure 26. Single Lithium-Ion Cell to 5V, 12V Boost Converter

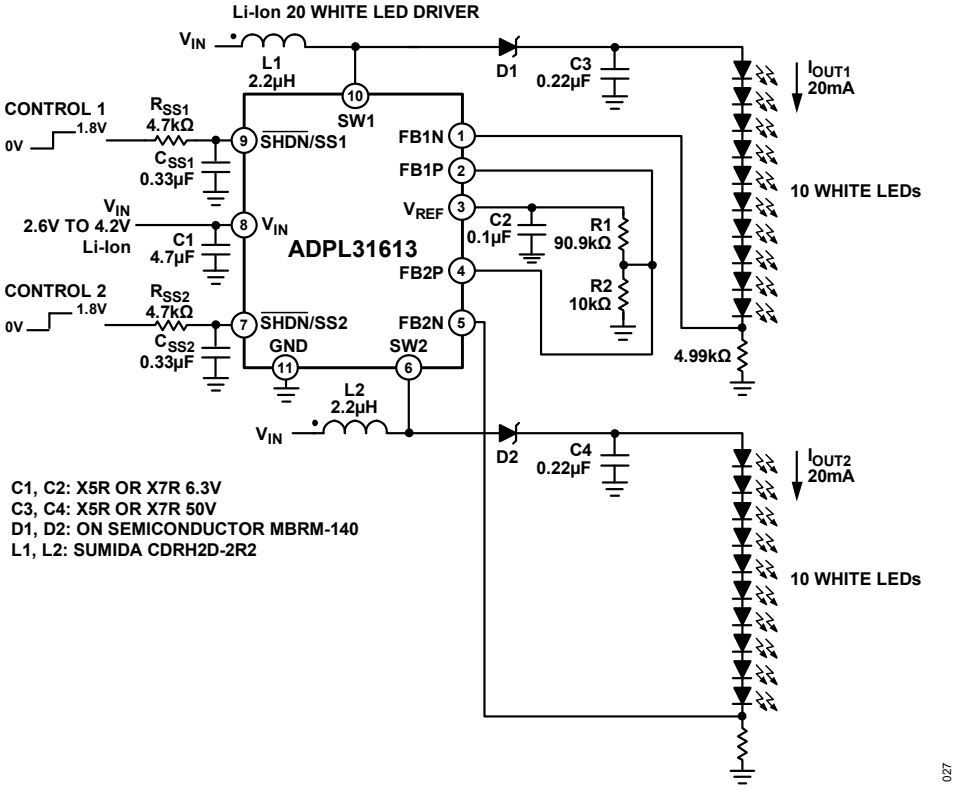


Figure 27. Lithium-Ion White LED Driver

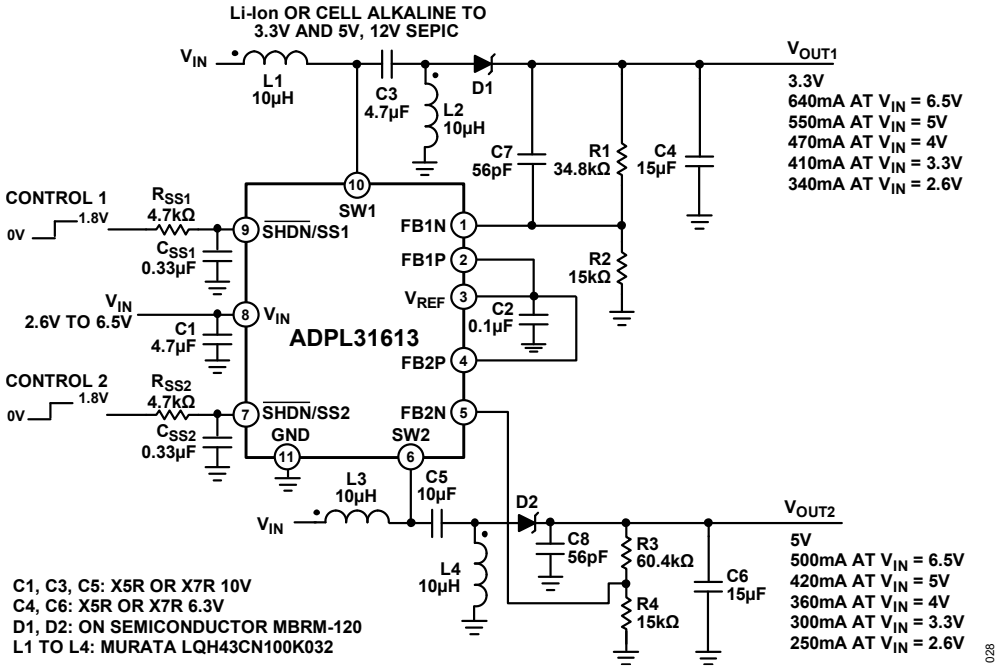
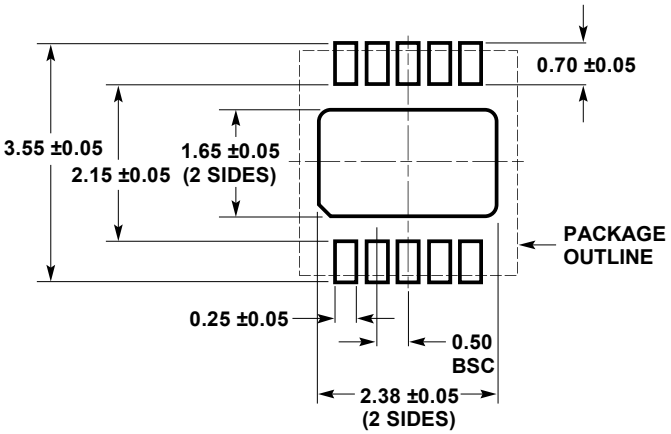
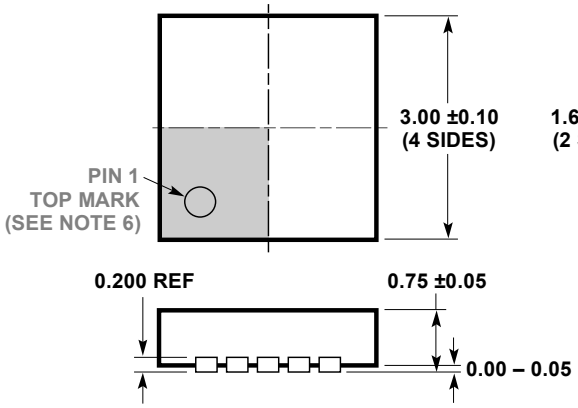


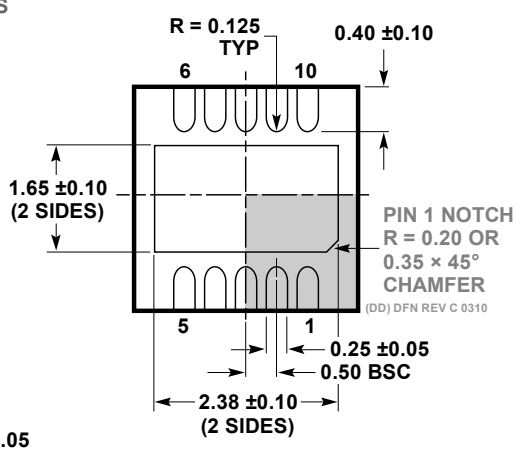
Figure 28. Lithium-Ion or 4-Cell Alkaline to 3.3V and 5V SEPIC

PACKAGE DESCRIPTION



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

ORDERING GUIDE

Table 7. Ordering Guide

TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
ADPL31613CPZ-RL	LBHM	10-Lead (3mm × 3mm) Plastic	–40°C to 85°C

Table 8. Evaluation Boards

PART NUMBER	DESCRIPTION
EVAL-ADPL31613-AZ	Evaluates ADPL31613 in a ±12V Output Voltage Application.