20V, 8A/10A Fully Integrated Buck Converter with 20µA Quiescent Current and Dual-Phase Capability

ADPL12008/ADPL12010

General Description

The ADPL12008/ADPL12010 ICs are highly integrated synchronous buck converters with internal high-side and low-side switches. The ICs are designed to deliver up to 8A/10A with an input voltage from 3V to 20V. The voltage quality can be monitored by the PGOOD signal. The ICs can operate in dropout mode by running at a very high duty cycle, making them ideal for factory automation applications.

The ADPL12008/ADPL12010 ICs offer programmable output-voltage options. High switching frequency at 1.5MHz and 400kHz options allow for small external components and reduced output ripple. SYNC input programmability enables three modes for optimized performance: Forced–Pulse-width modulation (PWM) mode, skip mode with ultra-low quiescent current, and synchronization to an external clock.

The ADPL12008/ADPL12010 ICs also feature dual-phase capability, which allows up to 20A designs. Two ICs can be configured as a controller and target with dynamic current sharing and 180º out-of-phase operation.

The ADPL12008/ADPL12010 ICs are available in a small, 3.5mm x 3.75mm, 17-pin flip-chip quad flat no-lead (FC2QFN) package. They are pin-to-pin compatible with the ADPL12005/ADPL12006 (5A to 6A) family of products.

Applications

- Factory Automation
- Point-of-Load
- Distributed DC Power Systems
- Communication Infrastructure
- Test and Measurement

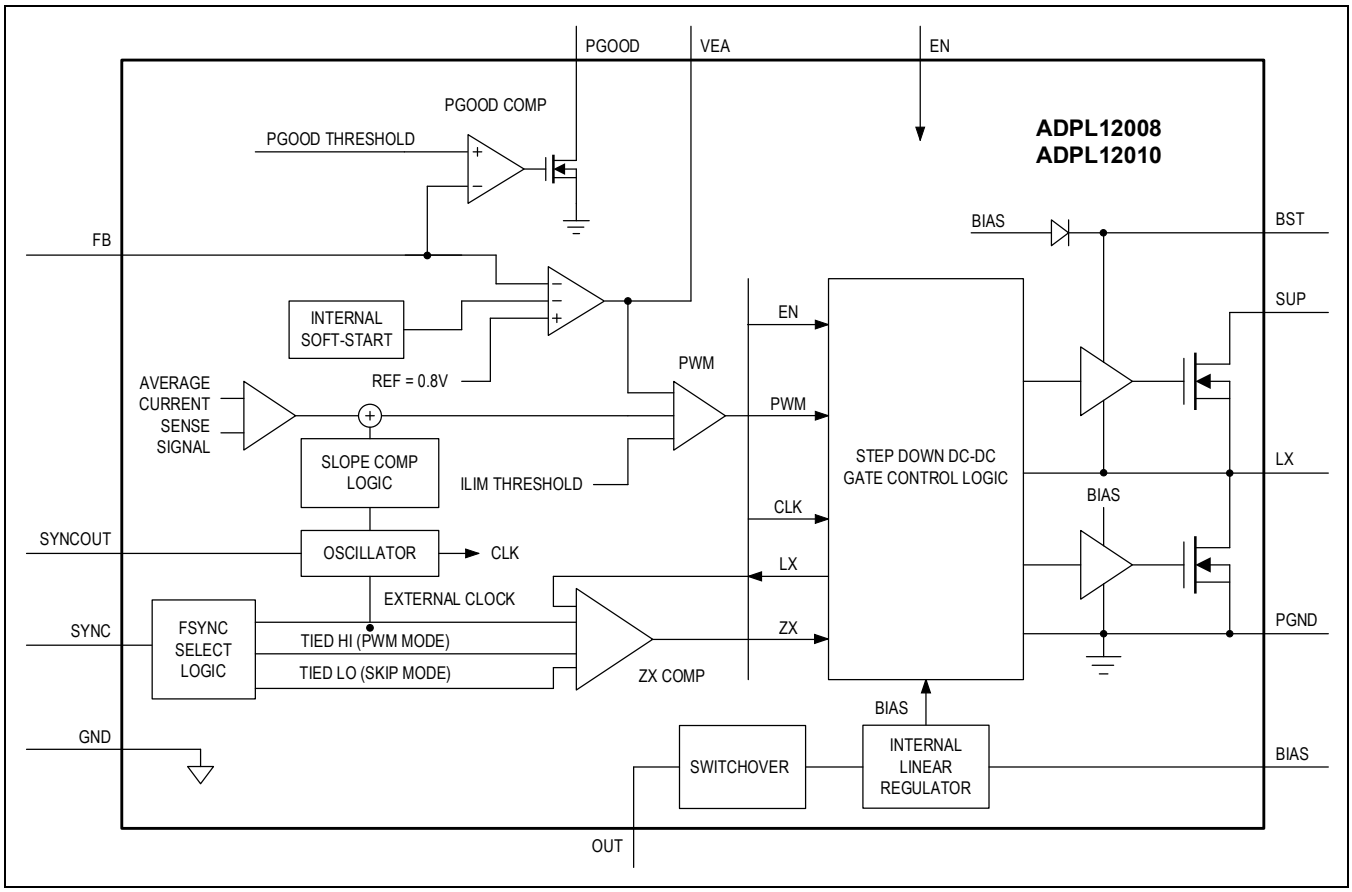
Benefits and Features

- High-Power DC/DC Converter in Small Solution Size
  - Operating V_{IN} range of 3V to 20V
  - Synchronous DC-DC Converter with Integrated FETs
  - 8A/10A Maximum Output Current
  - 400kHz and 1.5MHz Fixed Frequency Options
  - Fixed Soft-Start Time
    - 2.5ms for 400kHz
    - 3.5ms for 1.5MHz
  - 36ns Minimum On-Time
  - Programmable Output Voltage
    - 0.8V to 10V for 400kHz
    - 0.8V to 6V for 1.5MHz
  - Symmetric and Balanced SUP and PGND Pinout Placement for Better Electromagnetic Interference (EMI) Performance
  - Thermally-Enhanced 3.5mm x 3.75mm, 17-Pin FC2QFN Package
- High Efficiency at All Load Ranges
  - 20µA Quiescent Current in Skip Mode
  - Up to 95.6% Eff. at $12V_{IN}/3.3V_{OUT}$/400kHz
  - Up to 93.9% Eff. at $12V_{IN}/3.3V_{OUT}$/1.5MHz
- Dual-Phase Operation up to 20A Load Capability
  - Frequency Synchronization Input/Output
  - 180º Out-of-Phase Between Controller and Target
  - Dynamic Current Sharing
- Forced-PWM and Skip-Mode Operation
- Low Dropout Operation
- Power Good Indicator
- Overtemperature and Short-Circuit Protection
- -40°C to +150°C Operating Junction Temperature Range
- Scalable Power Solution
  - Footprint Compatible with ADPL12005/ADPL12006

Ordering Information ***appears at end of data sheet.***

19-102012; Rev 0; 5/25

Simplified Block Diagram



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Absolute Maximum Ratings

SUP, EN to PGND ..... -0.3V to +22V
BST to LX ..... -0.3V to +2.2V
BST to BIAS ..... -0.3V to 22V
BST to PGND ..... -0.3V to +24V
LX to PGND ..... -0.3V to SUP + 0.3V
SYNC, SYNCOUT, PGOOD to GND ..... -0.3V to 6V
FB, VEA to GND ..... -0.3V to BIAS + 0.3V
OUT to GND ..... -0.3V to 16V
PGND to GND ..... -0.3V to 0.3V
BIAS to GND ..... -0.3V to +2.2V
LX Continuous RMS Current 10A
SUP Continuous RMS Current 5A
ESD Protection Human Body Model ..... ±2kV
Continuous Power Dissipation (T_A = +70°C, derate 37mW/°C above +70°C) 2963mW
Operating Junction Temperature ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	F173A3F+1F
Outline Number	*21-100699*
Land Pattern Number	*90-100239*
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	38.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	7.7°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	27°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted (See Note 1, Note 2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3		20	V
Supply Current	I_{SUP_SHDN}	V_{EN} = 0, T_A = +25°C		4	6	µA
	I_{SUP}	V_{EN} = high, V_{OUT} = 3.3V, no load, switching		20		
SUP Undervoltage Lockout		Rising	2.9	3.0	3.2	V
		Falling	2.6	2.7	2.9	
BIAS Voltage		+2.5V ≤ V_{SUP} ≤ +20V		1.8		V
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	Rising	1.58	1.63	1.68	V
	$V_{BIAS\_UVLO\_HYS}$	Hysteresis		50		mV
BUCK CONVERTER						
Adjustable Output-Voltage Range		f_{SW} = 1.5MHz	0.8		6	V
		f_{SW} = 400kHz	0.8		10	
FB Voltage Accuracy	V_{FB_PWM}	PWM mode, no load	0.788	0.800	0.812	V
FB Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C			100	nA
High-Side Switch On Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 5A		26	53	mΩ
Low-Side Switch On Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 5A		13	26	mΩ
High-Side Switch Current-Limit Threshold	I_{LIM}	ADPL12008	10	12	14	A
		ADPL12010	11.9	14	16	
Low-Side Switch Negative Current-Limit Threshold	I_{NEG}			-4		A
LX Leakage Current	I_{LX_LKG}	V_{SUP} = 20V, V_{LX} = 0V or V_{LX} = 20V, T_A = +25°C	-5		5	µA
Soft-Start Ramp Time	t_{SS}	f_{SW} = 1.5MHz		3.5		ms
		f_{SW} = 400kHz		2.5		
Minimum On-Time	T_{ON}	(See Note 3)		36	65	ns
Maximum Duty Cycle		Dropout mode	96			%
SWITCHING FREQUENCY						
PWM Switching Frequency	f_{SW}	f_{SW} = 1.5MHz	1.375	1.500	1.625	MHz
		f_{SW} = 400kHz	360	400	440	kHz
SYNC External Clock Frequency	f_{SYNC}	f_{SW} = 1.5MHz	1.215		1.845	MHz
		f_{SW} = 400kHz	360		600	kHz
PGOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_R}	Percentage of V_{OUT}, rising	92	94	96	%
	V_{GOOD_F}	Percentage of V_{OUT}, falling	91	93	95	
PGOOD Debounce	T_{DEB}	PWM mode, falling, f_{SW} = 1.5MHz		70		µs
		PWM mode, falling, f_{SW} = 400kHz		50		
		PWM mode, rising, f_{SW} = 1.5MHz		140		µs

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted (See Note 1, Note 2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		f_{SW} = 400kHz		100		
PGOOD High-Leakage Current	I_{PGOOD_LKG}	T_A = +25°C			1	µA
PGOOD Low-Voltage Level	V_{PGOOD_LOW}	Sinking 1mA			0.4	V
LOGIC LEVELS						
EN High-Voltage Level	V_{EN_HIGH}		1.2			V
EN Low-Voltage Level	V_{EN_LOW}				0.5	V
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 20V, T_A = +25°C			1	µA
SYNC High-Voltage Level	V_{SYNC_HIGH}		1.4			V
SYNC Low-Voltage Level	V_{SYNC_LOW}				0.4	V
SYNC Input Current	$I_{IN,SYNC}$	T_A = +25°C			1	µA
SYNCOUT Output-Voltage Level	$V_{SYNCOUT}$	No load	2.6	3.3	3.9	V
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			20		°C

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design and characterization.

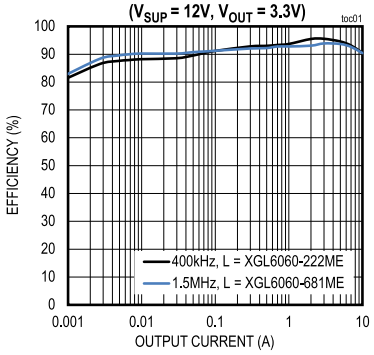
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5000 hours.

Note 3: Guaranteed by design, not production tested.

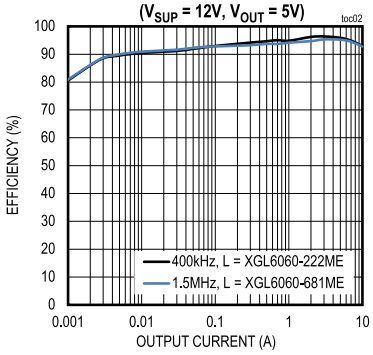
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

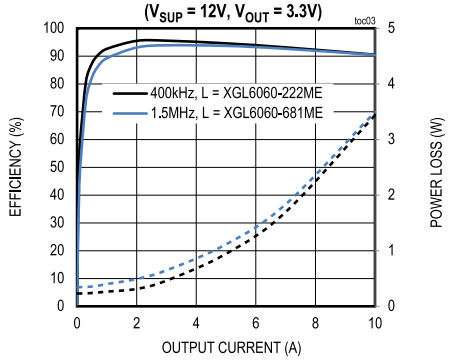
EFFICIENCY vs. OUTPUT CURRENT
SKIP MODE
(V_{SUP} = 12V, V_{OUT} = 3.3V)



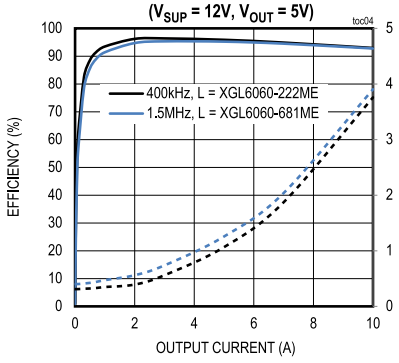
EFFICIENCY vs. OUTPUT CURRENT
SKIP MODE
(V_{SUP} = 12V, V_{OUT} = 5V)



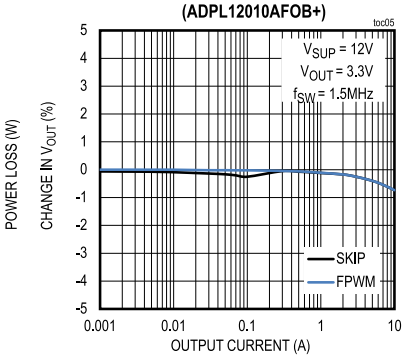
EFFICIENCY AND POWER LOSS
vs. OUTPUT CURRENT, FPWM MODE
(V_{SUP} = 12V, V_{OUT} = 3.3V)



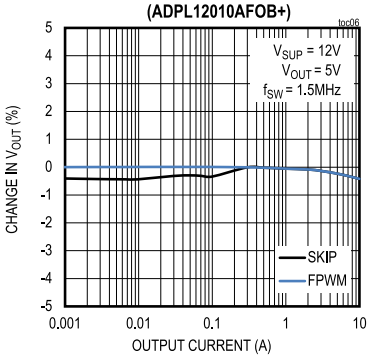
EFFICIENCY AND POWER LOSS
vs. OUTPUT CURRENT, FPWM MODE
(V_{SUP} = 12V, V_{OUT} = 5V)



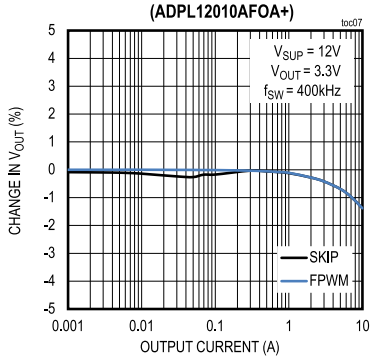
OUTPUT LOAD REGULATION
(ADPL12010AFOB+)



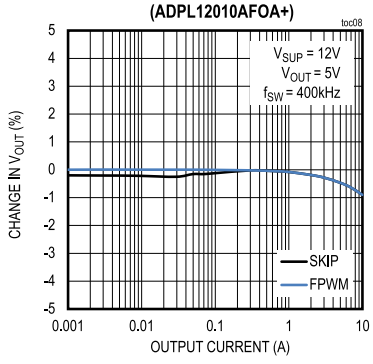
OUTPUT LOAD REGULATION
(ADPL12010AFOB+)



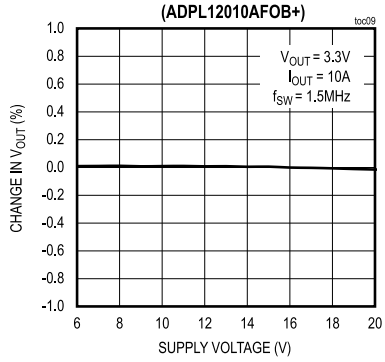
OUTPUT LOAD REGULATION
(ADPL12010AFOA+)



OUTPUT LOAD REGULATION
(ADPL12010AFOA+)

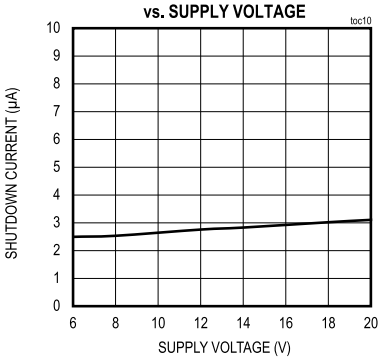


OUTPUT LINE REGULATION
(ADPL12010AFOB+)

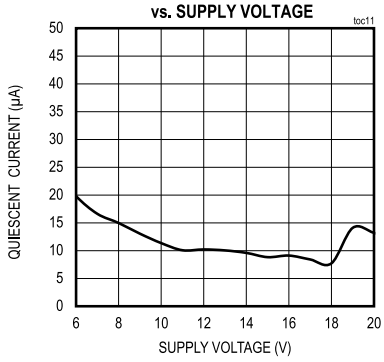


(T_A = +25°C, unless otherwise noted.)

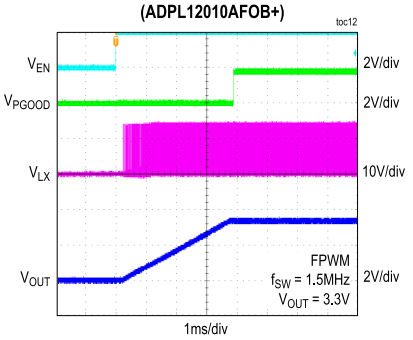
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



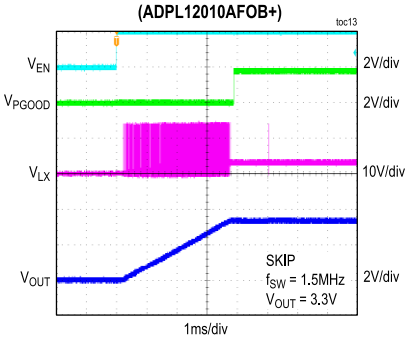
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



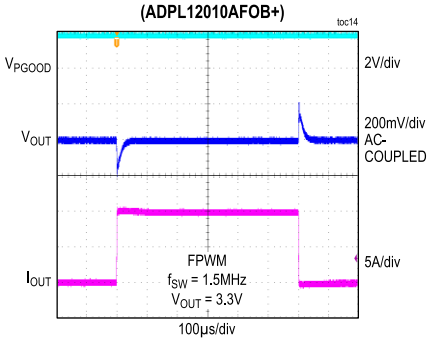
STARTUP INTO NO LOAD (ADPL12010AFOB+)



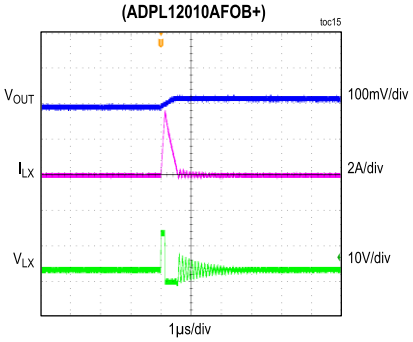
STARTUP INTO NO LOAD (ADPL12010AFOB+)



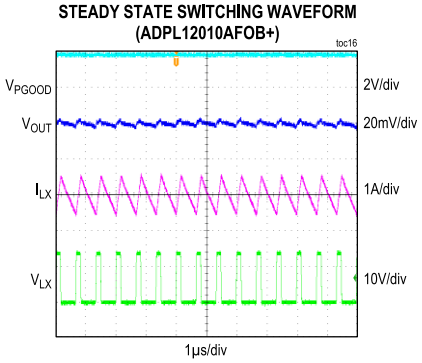
LOAD TRANSIENT RESPONSE (ADPL12010AFOB+)



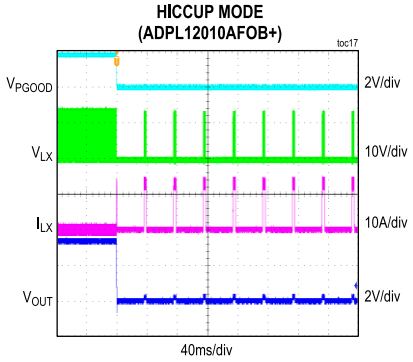
SKIP-MODE OPERATION (ADPL12010AFOB+)



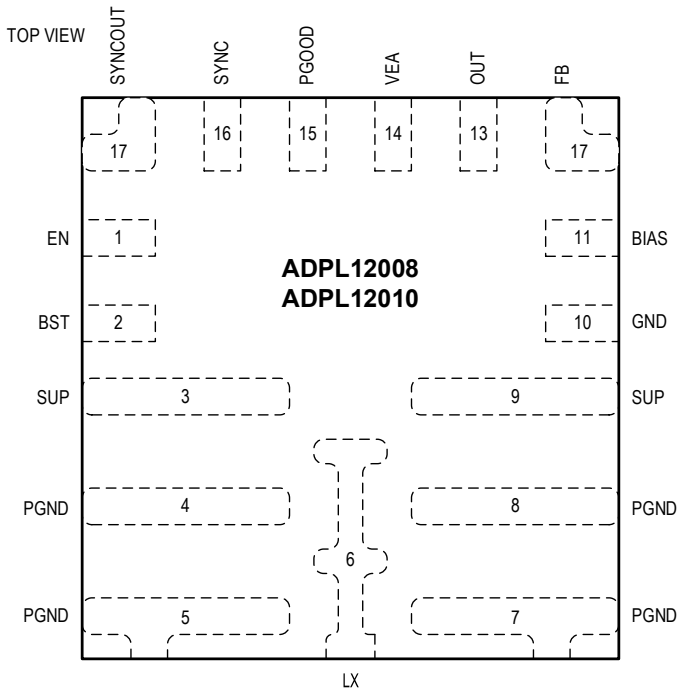
STEADY STATE SWITCHING WAVEFORM (ADPL12010AFOB+)



HICCUP MODE (ADPL12010AFOB+)



Pin Configurations



17 FC2QFN
(3.5mm x 3.75mm)

Pin Descriptions

PIN	NAME	FUNCTION
1	EN	High-Voltage Compatible Enable Input. Drive EN high to enable the buck converter.
2	BST	High-Side Gate Driver Supply. Connect a 0.1µF ceramic capacitor between BST and LX.
3	SUP	IC Supply Input and Internal High-Side Switch Supply Input. Bypass SUP to PGND with 0.1µF and 4.7µF ceramic capacitors as close as possible. Both SUP pins are internally connected.
4, 5	PGND	Power Ground. Connect all PGND pins together.
6	LX	Buck Inductor Connection. Connect an inductor from LX to the buck output. LX is high impedance when the IC is disabled.
7, 8	PGND	Power Ground. Connect all PGND pins together.
9	SUP	IC Supply Input and Internal High-Side Switch Supply Input. Bypass SUP to PGND with 0.1µF and 4.7µF ceramic capacitors as close as possible. Both SUP pins are internally connected.
10	GND	Analog Ground. Connect GND and PGND through the start connection to the PCB ground plane.
11	BIAS	1.8V Internal Linear Regulator Output. Connect BIAS to ground with a minimum of 2.2µF ceramic capacitor.
12	FB	Feedback Input. Connect FB to a resistor-divider between OUT and GND to adjust the output voltage between 0.8V and 10V.
13	OUT	Output Voltage Sense Input. The buck converter uses OUT to sense output voltage.
14	VEA	Internal Voltage Loop Error Amplifier Output. Connect the VEA of the controller and target together in dual-phase operation. Leave VEA open for single-phase operation.
15	PGOOD	Open-Drain Power Good Output. The PGOOD is low if the buck output voltage falls below 93% (typ) of the regulation voltage. The PGOOD becomes high impedance when the buck output voltage rises above 94% (typ) of its regulation voltage. The PGOOD asserts low during soft-start. Connect PGOOD to BIAS or a positive voltage lower than 5.5V with a pull-up resistor to indicate buck output status.
16	SYNC	External Clock Synchronization Input. Connect SYNC low to enable skip-mode operation. Connect SYNC high for forced PWM operation. Connect a valid external clock signal to SYNC to enable external clock synchronization.
17	SYNCOUT	180° Out-of-Phase Clock Output. In dual-phase operation, connect SYNCOUT to BIAS to configure the IC as a target, and connect the SYNCOUT of the controller to the SYNC of the target. Leave SYNC open in single-phase operation.

Detailed Description

The ADPL12008/ADPL12010 ICs are highly integrated synchronous buck converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 8A/10A current with input voltages from 3V to 20V while using only 20µA quiescent current at no load condition. The voltage quality can be monitored by the PGOOD signal. The ICs can operate in dropout mode by running at a very high duty cycle, making them ideal for factory automation applications.

The ADPL12008/ADPL12010 ICs offer adjustable output voltage programmed by an external resistor-divider. The frequency is internally fixed at 1.5MHz and 400kHz options, allowing for the use of small external components and reduced output ripple. The signal at SYNC programs the ICs in skip enable, FPWM, or when synchronizing to the external clock. Average current-mode control with 36ns minimum ON time allows for large input/output step-down ratios without skipping cycles.

The ADPL12008/ADPL12010 ICs can also be configured in dual-phase mode to supply up to a 20A load. The average current-mode control provides noise immunity and accurate dynamic current sharing during transients.

The FC2QFN package lowers the package parasitic impedance and improves the thermal performance. A symmetrical pinout placement of SUP and PGND provides a balanced current loop around the ICs and further improves their EMI performance.

Linear Regulator Output (BIAS)

The devices include a 1.8V linear regulator (V_{BIAS}) that powers the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to GND. During startup, the bias regulator draws power from the input and switches over to the output after the startup is completed (if V_{OUT} > 2.5V).

Synchronization Input (SYNC)

The ADPL12008/ADPL12010 ICs provide an internal oscillator with 400kHz and 1.5MHz options. Drive SYNC high for FPWM operation with 400kHz or 1.5MHz switching frequency. Drive SYNC low to enable skip-mode for better efficiency improvement at light load. The ICs can be synchronized to the external clock with a valid external clock present at SYNC.

Enable Input (EN)

An Enable Input (EN) enables the ICs from shutdown mode. Drive EN high to enable the ICs. Drive EN low to disable the ICs into shutdown mode. The quiescent current is reduced to 4µA (typ) during shutdown.

Soft-Start

Drive EN high to enable the ICs. The soft-start circuitry gradually ramps up the reference voltage during the soft-start time (2.5ms at 400kHz or 3.5ms at 1.5MHz, typ) to reduce the input inrush currents during startup.

Short-Circuit Protection

The ICs feature a cycle-by-cycle current limit and hiccup mode to protect against short-circuit or overload conditions. In overload conditions, the high-side FET remains on until the inductor current reaches the current limit threshold, I_{LIM}. Then, the converter turns off the high-side FET and turns on the low-side FET, allowing the inductor current to ramp down. Once the inductor current decreases to the valley current limit, the converter turns on the high-side FET again. This cycle repeats until the overload condition is removed.

A short-circuit is detected when the output voltage falls below the preset threshold voltage while the inductor current hits the current limit. The threshold voltage is 25% of output regulation voltage. During hiccup-mode, the ICs turn off the buck converter for 35ms (10x soft-start time, f_{SW} = 1.5MHz), and then restart it if the overcurrent or short-circuit condition is removed. The hiccup repeats when the short-circuit is continuously present.

Power Good Indicator (PGOOD)

The ICs feature an open-drain Power Good (PGOOD) output to indicate the output voltage status. The PGOOD goes low to high impedance when the converter output voltage rises above 94% (typ) of its nominal regulation voltage. The PGOOD goes low when the output voltage drops below 93% (typ) of the nominal regulation voltage. Connect PGOOD to the converter output or BIAS voltage through a pull-up resistor. The PGOOD asserts low during soft-start.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the ICs. When the junction temperature exceeds +175°C, an internal sensor shuts down the ICs, allowing them to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 20°C.

Dual-Phase Operation

Two ADPL12008/ADPL12010 ICs can be configured in dual-phase to provide higher output current up to 20A. To operate in dual-phase mode, one IC is programmed as a target by connecting its SYNCOUT to BIAS, and the other IC is treated as the controller. The SYNCOUT of the controller is connected to the SYNC of the target, allowing both ICs to switch in 180° out-of-phase. Therefore, with the present SYNCOUT signal from the controller, FPWM is recommended for dual-phase operation.

The VEA nodes of the controller and target are connected to ensure balanced current sharing between the two phases. Also, by doing this, the controller's voltage control loop is shared with the target. Instead of connecting FB nodes together, use separate resistor-dividers for each phase.

To set the output voltage to a value, connect a resistor-divider between the buck output, FB, and GND as shown in *Figure 1*. Use an identical but separate resistor-divider for the controller and the target.

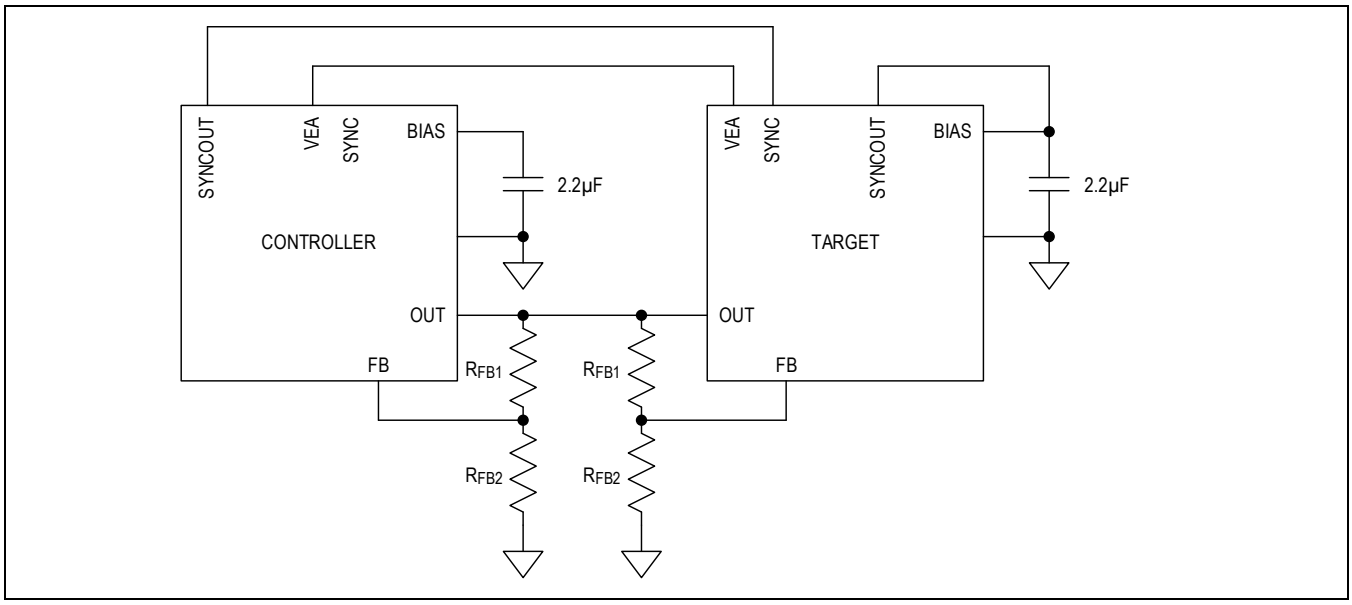


Figure 1. Typical Application Circuit for Dual-Phase Configuration with External Resistor-Divider

Low-I_Q Operation in Dual-Phase

The ADPL12008/ADPL12010 ICs feature dual-phase capability, allowing each IC to be configured as either a controller or a target. The SYNCOUT pin of the controller outputs a 180° out-of-phase clock when SYNC is tied high (FPWM mode). For low-I_Q mode, pull the SYNC pin of the controller low (skip-mode). In this mode, there is no clock present on the SYNCOUT pin of the controller, and the controller IC enters the skip-mode. The internal circuit of the target IC remains ON during this time and actively looks for the SYNCOUT signal from the controller. As the target IC is ON, the quiescent current is slightly higher, even though both the ICs skip pulses.

To improve the light-load efficiency and further reduce the I_Q, pull the target EN low. This disables the target and its internal circuits, which further reduces the I_Q. *Table 1* summarizes the truth table for low-I_Q operation.

Table 1. Configurations for Low-I_Q Operation

CONTROLLER	TARGET	MODE
EN = High, SYNC = BIAS	EN = High	FPWM (high I_Q)
EN = High, SYNC = Low	EN = High	Skip-mode (low I_Q)
EN = High, SYNC = Low	EN = Low	Standby-mode (ultra-low I_Q)
EN = Low	EN = High	Not allowed

Applications Information

Setting the Output Voltage

To externally program the output voltage between 0.8V and 10V for a 400kHz switching frequency, and between 0.8V and 6V for a 1.5MHz switching frequency, connect a resistor-divider from the buck converter output to FB, and then to GND. Select R_{FB2} between FB and GND in *Typical Application Circuits* less than 20kΩ. Calculate R_{FB1} between the buck output and FB with the following equation:

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

Where, V_{FB} = 0.8V, and R_{FB2} is less than 20 kΩ.

Table 2 provides component selection recommendations for each output range (C_{FF} is recommended based on R_{FB1} = 50kΩ).

Table 2. Recommended Component Selection

SWITCHING FREQUENCY (kHz)	V_{OUT} (V)	INDUCTOR (µH)	OUTPUT CAPACITOR (µF)	C_{FF} (pF)
400	0.8V–1.8V	0.68µH	500µF	N/A
400	1.8V–3.3V	1µH	220µF	N/A
400	3.3V–5V	2.2µH	120µF	82pF
400	5V–7V	2.2µH	88µF	56pF
400	7V–10V	3.3µH	66µF	47pF
1500	0.8V–1.8V	0.38µH	88µF	N/A
1500	1.8V–3.3V	0.47µH	88µF	N/A
1500	3.3V–5V	0.68µH	66µF	47pF
1500	5V–6V	0.68µH	44µF	15pF

Input Capacitor

The input capacitors reduce peak current drawn from the power source and improve noise and voltage ripple on the SUP nodes caused by the buck converter switching cycles. Use two ceramic input capacitors with 0.1µF and 4.7µF capacitance in parallel at each side of the IC for proper buck operation.

Place a 0.1µF ceramic capacitor with 0402 or 0603 size next to SUP and PGND on each side of the IC to reduce input noise and improve EMI performance. A 4.7µF ceramic capacitor is required after a 0.1µF capacitor on each input side to reduce input voltage ripple. An additional buck capacitor might be required if a high impedance exists in the input supply or traces.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \left(\frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}\right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and Equivalent series resistance (ESR) required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + {}^{\Delta I_L}/_2}$$

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D\,(1 - D)}{\Delta V_Q \times f_{SW}}$$

Where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

and $I_{LOAD(MAX)}$ is the maximum output current, ΔI_L is the peak-to-peak inductor current, f_{SW} is the switching frequency, and D is the duty cycle.

Selecting the Inductor

Inductor selection is a compromise between component size, efficiency, control loop bandwidth, and loop stability. Insufficient inductance increases the inductor current ripple, conduction losses, and output voltage ripple, and causes loop instability in the worst case. A large inductor reduces the inductor current ripple by sacrificing component size and slow response. For recommended inductor values, see *Table 2* for more details.

Output Capacitor

The output capacitor is a critical component for switching regulators. It is selected to meet the requirements for output voltage ripple, load transient response, and loop stability.

The output voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low ESR ceramic capacitors. Assume the contribution to the output ripple voltage from ESR and the capacitor discharge to be equal. Use the following equations for the output capacitance and ESR for a specified output voltage ripple.

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

$$\Delta I_{P-P} = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

$$V_{OUTRIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

Where, ΔI_{P-P} is the peak-to-peak inductor current, and f_{SW} is the switching frequency.

During a load step, the output capacitors supply the load current before the converter loop responds with a higher duty cycle, which causes the output voltage to undershoot. To keep the maximum output voltage deviations below the tolerable limits of the electronics being powered, calculate the output capacitance with the following equation:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{\Delta V \times 2\pi \times f_C}$$

Where, ΔI is the load step, ΔV is the allowed output voltage undershoot, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. The calculated C_{OUT} is the capacitance after considering capacitance tolerance, temperature effect, and voltage derating. *Table 2* shows the recommended values of output capacitance based on frequency and output voltage.

PCB Layout Guidelines

1. Careful Printed circuit board (PCB) layout is critical to achieve low switching losses, low EMI, and clean, stable operation. For example, see *Figure 2* for more details.
2. Place the input bypass capacitors C_{BP} and C_{IN} as close as possible to each SUP and PGND on both sides of the IC. C_{BP} should be placed right next to the SUP and PGND node on the same layer to provide the best EMI rejection and minimize the input noise on the SUP. The symmetrical C_{IN} and CBP arrangements generate SUP loops with opposite orientations to cancel the magnetic fields and aid in EMI mitigation.
3. Minimize the connection from the buck output capacitor's ground terminal to the input capacitor's ground terminal. Keep the buck high-current path, and power traces wide and short. Minimize the traces from the LX node to the inductor and then to the output capacitors. This minimizes the buck current loop area and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency.
4. Place the bootstrap capacitor C_{BST} close to the IC. Use short and wide traces from BST and LX, and minimize the routing parasitic impedance. High parasitic impedance from BST to LX impacts the switching speed, further increases switching losses, and high dV/dt noise. For the BST to LX routing, see *Figure 2*.
5. Place the BIAS capacitor as close to the BIAS node as possible. Noise coupling into BIAS can disturb the reference and bias circuitry if this capacitor is installed away from the IC.
6. Keep the sensitive analog signals (FB/VEA) away from noisy switching nodes (LX and BST) and high current loops.
7. Ground is the return path for the full-load currents flowing into and out of the IC. It is also the common reference voltage for all analog circuits. Improper ground routing can bring extra resistance and inductance into the current loop, causing different voltage references and worsening voltage ringing or spikes. Place a solid ground plane layer under the power loop components layer to shield the switching noise from other sensitive traces. Connect the analog ground GND and power grounds PGND together at a single point in a star ground connection.
8. The PCB layout also plays an important role in power dissipation and thermal performance. The PGND nodes are the main power connection area between the IC and the outside of the IC. Place the ground copper area as much as possible around the PGND area to ensure efficient heat transfer. Place vias as many as possible around the PGND nodes to further transfer heat down the internal ground plane and other layers, thereby improving the thermal resistance from the IC package to the ambient.

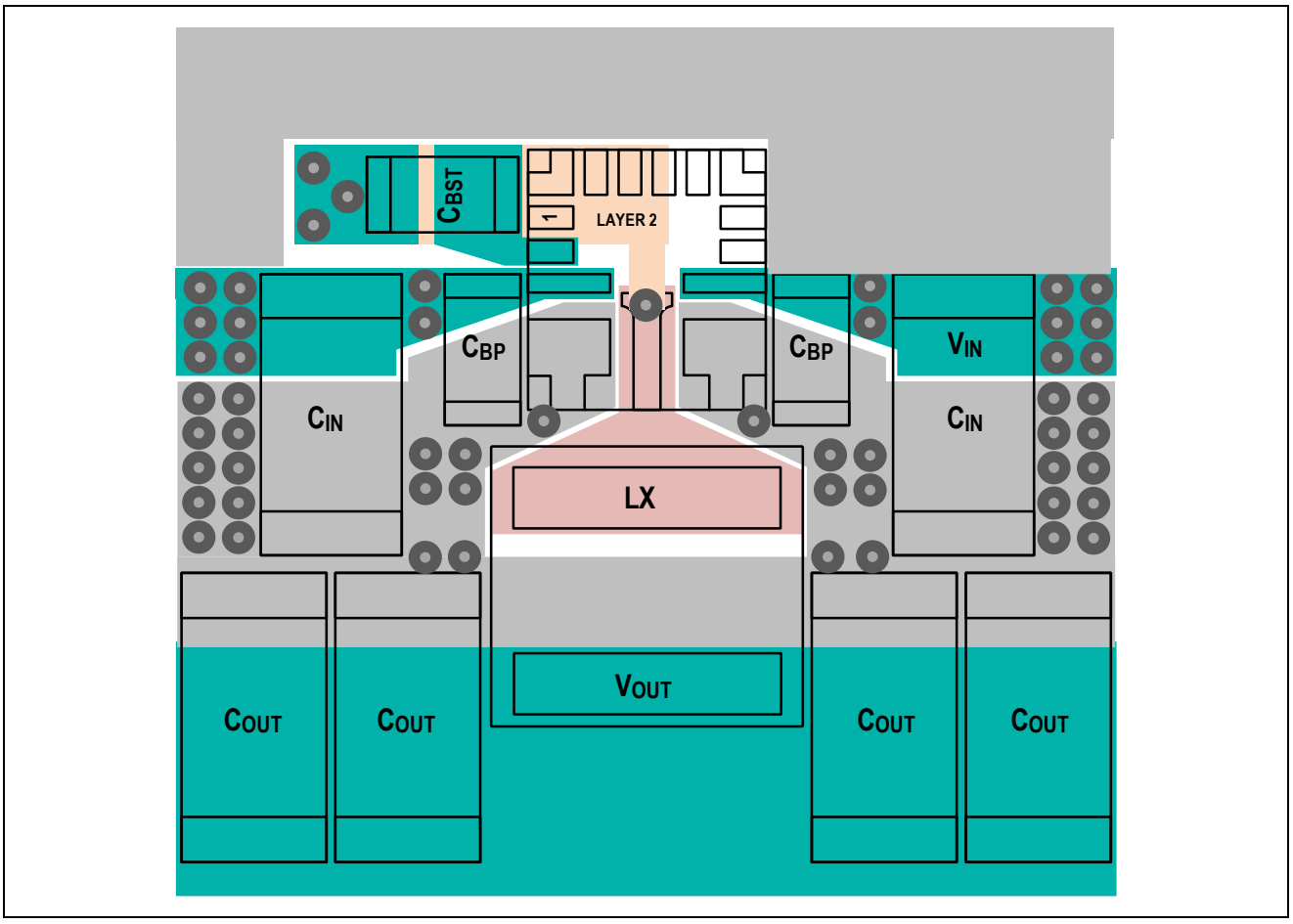
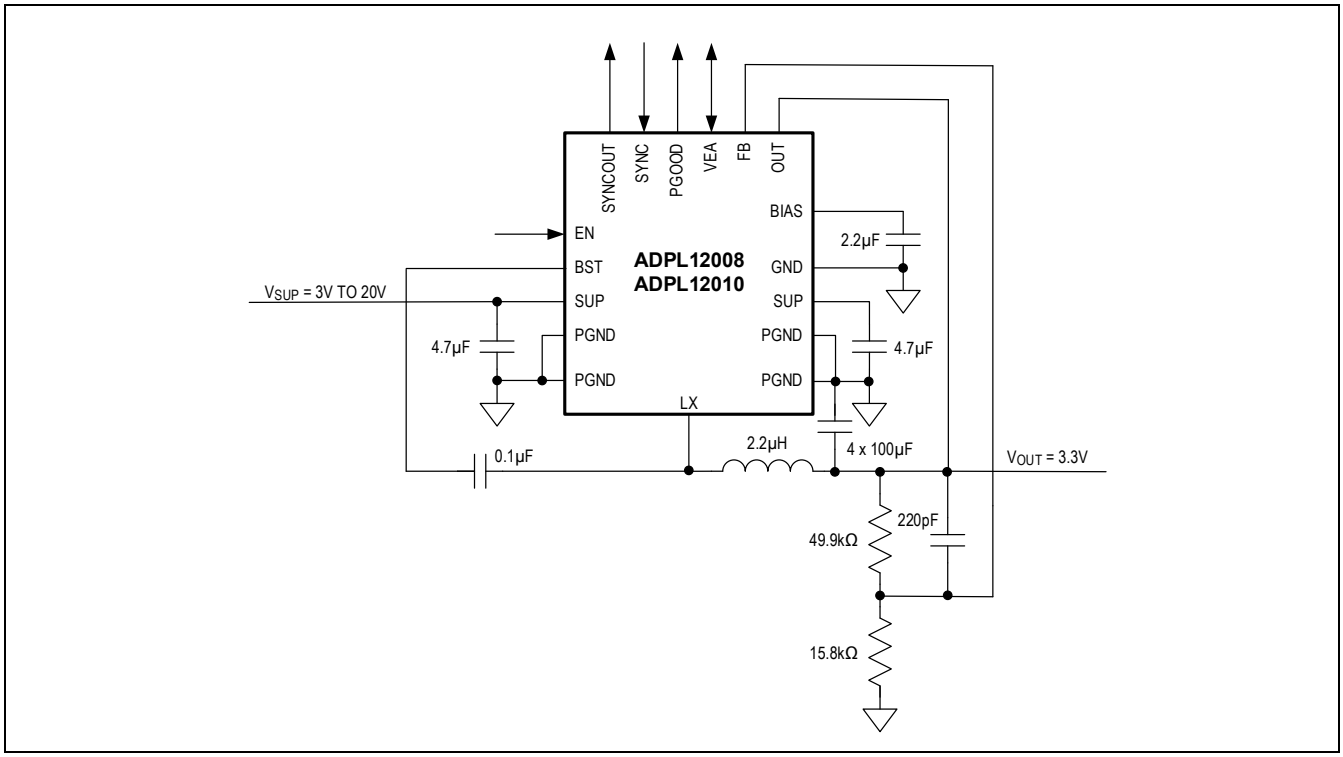


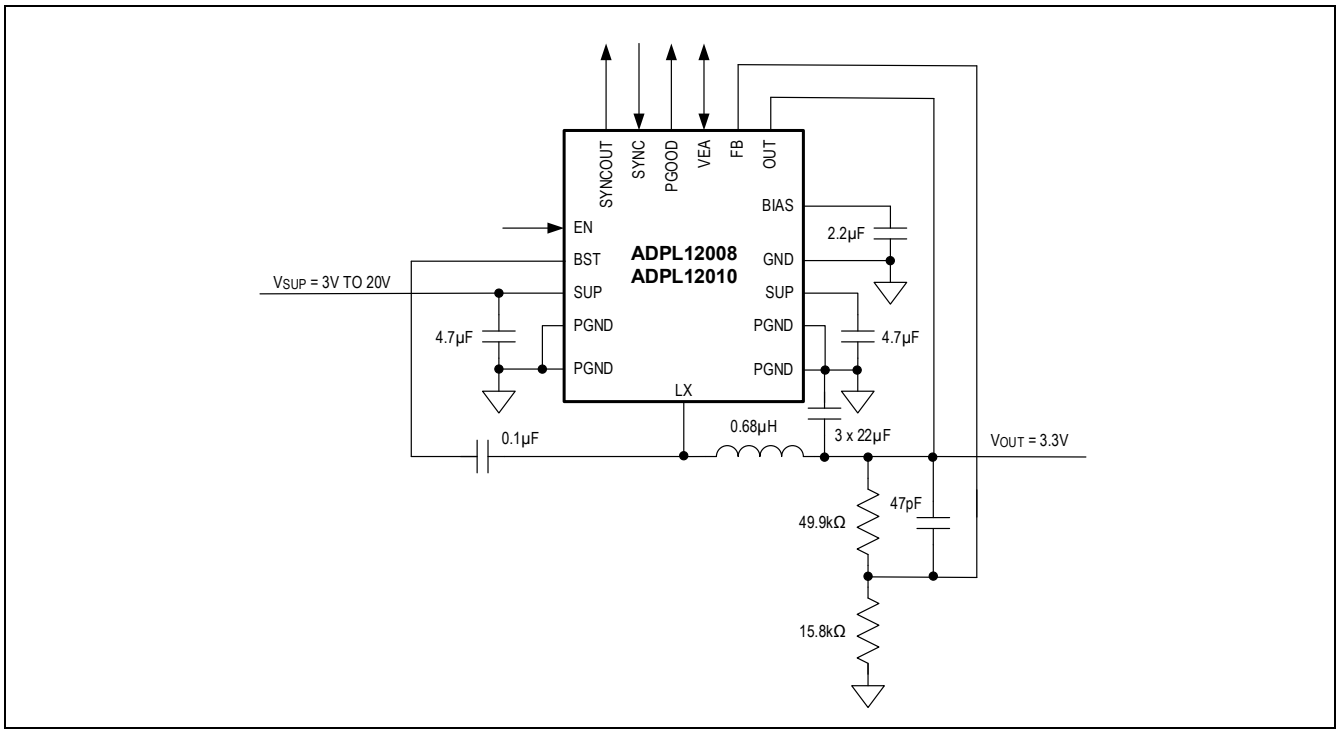
Figure 2. PCB Layout Example

Typical Application Circuits

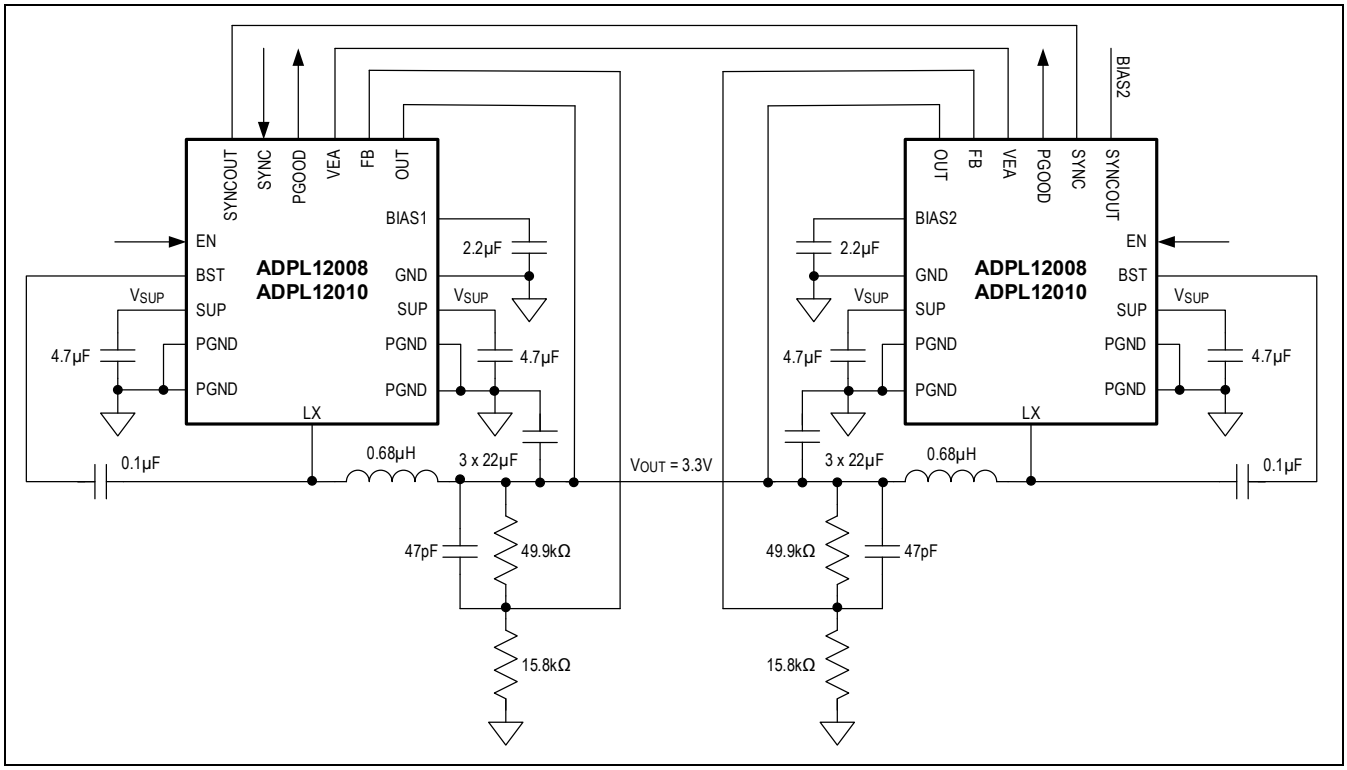
Single-Phase Operation (400kHz)



Single-Phase Operation (1.5MHz)



Dual-Phase Operation (1.5MHz)



Ordering Information

PART NUMBER	V_{OUT} (V)	MAXIMUM OPERATING CURRENT (A)	FREQUENCY
ADPL12008AFOA+T	Adjustable 0.8V to 10V	8A	400kHz
ADPL12008AFOB+T	Adjustable 0.8V to 6V	8A	1.5MHz
ADPL12010AFOA+T	Adjustable 0.8V to 10V	10A	400kHz
ADPL12010AFOB+T	Adjustable 0.8V to 6V	10A	1.5MHz

+ denotes a lead(Pb)-free/RoHS-compliant package.

T denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/25	Initial release	—