20V, 5A/6A Fully Integrated Synchronous Buck Converters

ADPL12005/ADPL12006

General Description

The ADPL12005/ADPL12006 ICs are small, synchronous buck converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 6A with wide input voltages ranging from 3V to 20V. Voltage quality can be monitored by observing the PGOOD signal. The ICs can operate in dropout by running at a very high duty cycle, making it ideal for factory automation applications.

The ADPL12005/ADPL12006 ICs offer programmable output voltage. The frequency is internally fixed at 400kHz and 1.5MHz, allowing for small external components and reduced output ripple. The ICs automatically enter skip mode at light loads with ultra-low quiescent current of 20µA at no load. This family of products (including the ADPL12008/ADPL12010) offers a pin-to-pin compatible offering from 5A to 10A in a single-phase configuration, and up to 20A in a dual-phase configuration. These devices are also optimized for dual-phase operation with very high current-sharing accuracy.

The ADPL12005/ADPL12006 ICs are available in a small 3.5mm x 3.75mm, 17-pin flip-chip quad flat no-lead (FC2QFN) package, utilizing very few external components.

Applications

- Factory Automation
- Point-of-Load
- Distributed DC Power Systems
- Communication Infrastructure
- Test and Measurement

Benefits and Features

- Multiple Functions for Small Size
  - Operating V_{IN} Range of 3V to 20V
  - 20µA Quiescent Current in Skip Mode
  - Synchronous DC-DC Converter with Integrated Field-Effect Transistors (FETs)
  - 400kHz and 1.5MHz Fixed-Frequency Options
  - Internal Soft-Start
    - 2.5ms for 400kHz
    - 3.5ms for 1.5MHz
  - Programmable Output Voltage
    - 0.8V to 12V for 400kHz
    - 0.8V to 10V for 1.5MHz
  - 3.5mm x 3.75mm, 17-Pin FC2QFN
  - Symmetrical Package Offers Superior Electromagnetic Interference (EMI) Performance
- Dual Phase Capability
  - Can be used in Dual-Phase Configuration for High-Power Design
  - Dynamic Current Sharing through Shared VEA Pin
  - Low-I_Q Operation Capability in Dual Phase
- Precise Output Voltage Monitoring with PGOOD
- Forced–Pulse-Width Modulation (PWM) and Skip-Mode Operation
- Low Dropout Operation
- Overtemperature and Short-Circuit Protection
- -40°C to +150°C Operating Junction Temperature Range

Ordering Information **appears at end of data sheet.**

19-102008; Rev 0; 5/25

Simplified Block Diagram

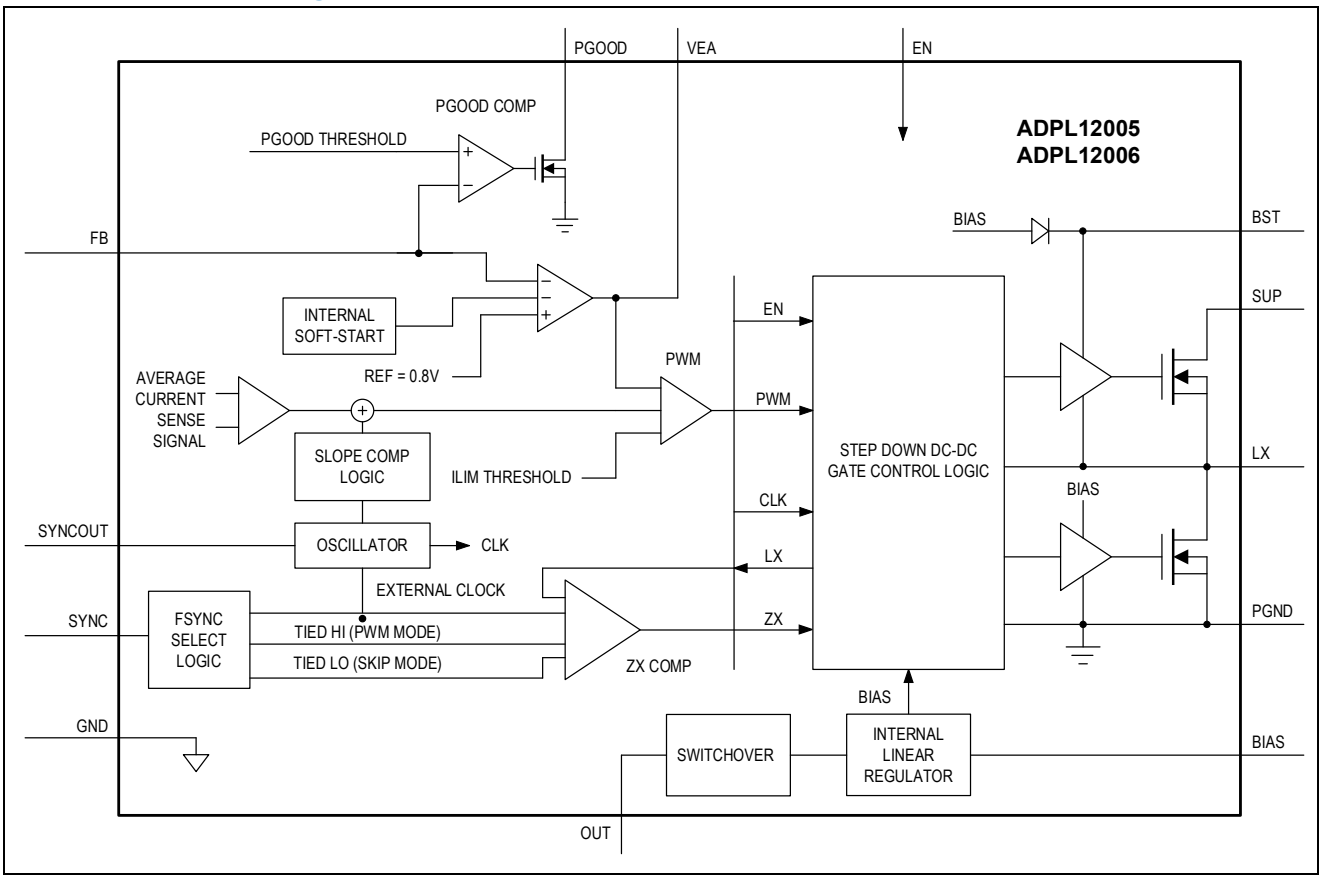


TABLE OF CONTENTS

Absolute Maximum Ratings

SUP ..... -0.3V to +22V
EN ..... -0.3V to +22V
BST to LX ..... -0.3V to +2.2V
BST ..... -0.3V to +24V
LX ..... -0.3V to SUP+0.3V
SYNCOUT ..... -0.3V to +6V
SYNC ..... -0.3V to +6V
VEA ..... -0.3V to BIAS+0.3V
FB ..... -0.3V to BIAS+0.3V
OUT ..... -0.3V to +16V
PGOOD ..... -0.3V to +6V
BIAS ..... -0.3V to +2.2V
PGND to AGND ..... -0.3V to +0.3V
LX Continuous RMS Current 6A
ESD Protection
Human Body Model ..... ±2kV
Charged Device Model ..... ±750V
Continuous Power Dissipation (T_A = +70°C, derate 34.48 mW/°C above +70°C.) 2758mW
Operating Junction Temperature ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (Soldering 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	F173A3F+2F
Outline Number	*21-100700*
Land Pattern Number	*90-100240*
Thermal Resistance, JEDEC Board	
Junction to Ambient (θ_{JA})	38.41°C/W
Junction to Case (θ_{JC})	10.35°C/W
Thermal Resistance, Four-Layer EV Kit Board	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	10.51°C/W

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using both the four-layer EV kit as well as the method described in JEDEC specification JESD51-7. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted. (See *Note 1*, *Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3		20	V
Supply Current	I_{SUP_SHDN}	V_{EN} = 0V, T_A = +25°C		4	6	μA
	I_{SUP}	V_{EN} = high, V_{OUT} = 3.3V, no load, switching		20		
SUP Undervoltage Lockout	$V_{SUP\_UVLO\_RISE}$	SUP voltage rising	2.945	3.025	3.175	V
	$V_{SUP\_UVLO\_FALL}$	SUP voltage falling	2.655	2.725	2.870	
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	BIAS voltage falling	1.53	1.58	1.63	V
BIAS Undervoltage Lock	$V_{BIAS\_UVLO\_HYS}$	BIAS UVLO hysteresis		50		mV
BIAS Voltage	V_{BIAS}			1.8		V
BUCK CONVERTER						
Output Voltage Adjustable Range	V_{OUT}	f_{SW} = 400kHz	0.8		12	V
		f_{SW} = 1.5MHz	0.8		10	
Feedback Voltage Accuracy	V_{FB_PWM}	PWM mode, no load	0.787	0.800	0.813	V
Feedback Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C			100	nA
High-Side Double diffusion metal oxide semiconductor field-effect (DMOS) On-Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 2A		46	95	mΩ
Low-Side DMOS On-Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 2A		23	47	mΩ
High-Side DMOS Current-Limit Threshold	I_{LIM}	ADPL12005	6.5	7.5	8.5	A
		ADPL12006	7.5	8.75	10	
Low-Side DMOS Negative Current-Limit Threshold	I_{NEG}	ADPL12005		-3		A
		ADPL12006		-3.5		
LX Leakage	I_{LX_LKG}	V_{SUP} = 20V, V_{LX} = 0V, or V_{LX} = 20V, T_A = +25°C			1	μA
Soft-Start Ramp Time	t_{SS}	f_{SW} = 400kHz		2.5		ms
		f_{SW} = 1.5MHz		3.5		
Minimum On-Time	t_{ON}	(See *Note 3*)		36	65	ns
Maximum Duty Cycle	D_{MAX}	Dropout Mode	96			%
SWITCHING FREQUENCY						
PWM Switching Frequency	f_{SW}	f_{SW} = 400kHz	360	400	440	kHz
		f_{SW} = 1.5MHz	1.375	1.500	1.625	MHz
SYNC External Clock Frequency	f_{SYNC}	f_{SW} = 400kHz	360		600	kHz
		f_{SW} = 1.5MHz	1.215		1.845	MHz
PGOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_THR}	V_{OUT} rising	92	94	96	%

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted. (See Note 1, Note 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{PGOOD_THF}	V_{OUT} falling		91	93	95	
PGOOD Debounce Time	t_{DEB}	Rising	f_{SW} = 400kHz		100		µs
			f_{SW} = 1.5MHz		140		
		Falling	f_{SW} = 400kHz		50		
			f_{SW} = 1.5MHz		70		
PGOOD Leakage Current	I_{PGOOD_LKG}	T_A = +25°C				1	µA
PGOOD Low Voltage Level	V_{PGOOD_LOW}	Sinking 1mA				0.4	V
LOGIC LEVELS							
EN High Voltage Level	V_{EN_HIGH}			1.2			V
EN Low Voltage Level	V_{EN_LOW}					0.5	V
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 20V, T_A = +25°C				1	µA
SYNC High Voltage Level	V_{SYNC_HIGH}			1.4			V
SYNC Low Voltage Level	V_{SYNC_LOW}					0.4	V
SYNCOUT Output Voltage Level	$V_{SYNCOUT}$	No load		2.6	3.3	3.9	V
THERMAL PROTECTION							
Thermal Shutdown	T_{SHDN}				175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}				20		°C

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

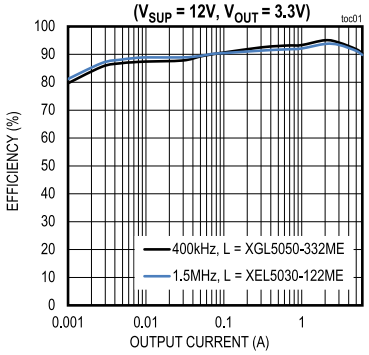
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 3: Guaranteed by design; not production tested.

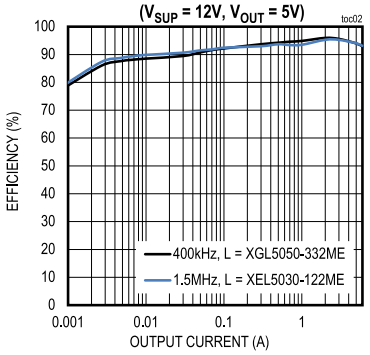
Typical Operating Characteristics

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

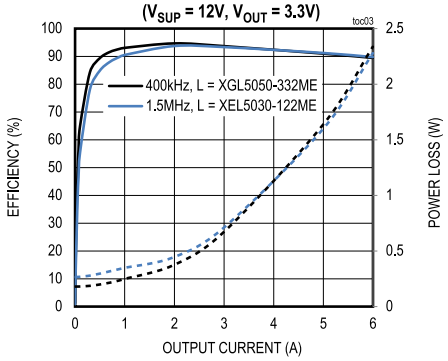
EFFICIENCY vs. OUTPUT CURRENT
SKIP MODE
(V_{SUP} = 12V, V_{OUT} = 3.3V)



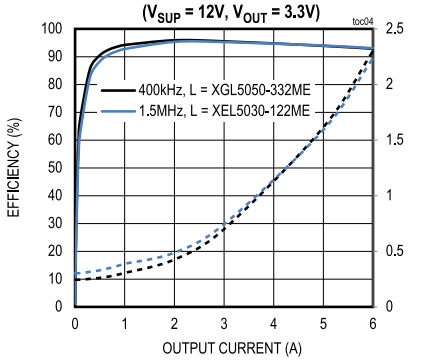
EFFICIENCY vs. OUTPUT CURRENT
SKIP MODE
(V_{SUP} = 12V, V_{OUT} = 5V)



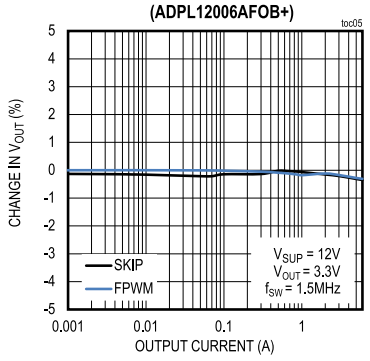
EFFICIENCY AND POWER LOSS
vs. OUTPUT CURRENT, FPWM MODE
(V_{SUP} = 12V, V_{OUT} = 3.3V)



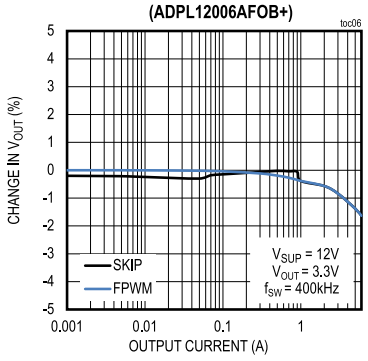
EFFICIENCY AND POWER LOSS
vs. OUTPUT CURRENT, FPWM MODE
(V_{SUP} = 12V, V_{OUT} = 3.3V)



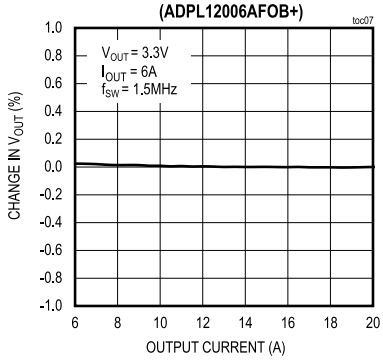
OUTPUT LOAD REGULATION
(ADPL12006AFOB+)



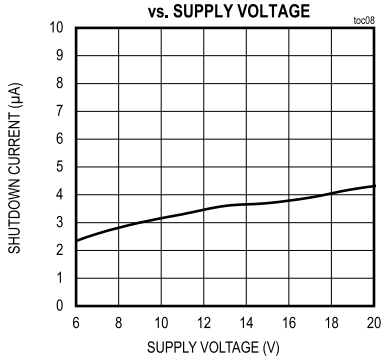
OUTPUT LOAD REGULATION
(ADPL12006AFOB+)



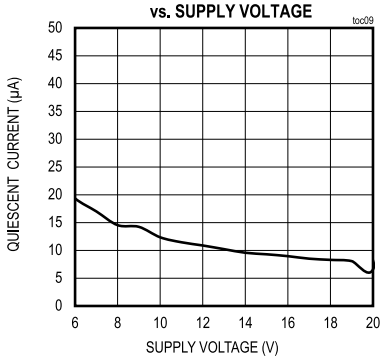
OUTPUT LINE REGULATION
(ADPL12006AFOB+)



SHUTDOWN CURRENT
vs. SUPPLY VOLTAGE

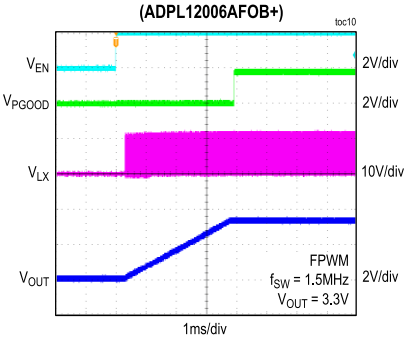


QUIESCENT CURRENT
vs. SUPPLY VOLTAGE

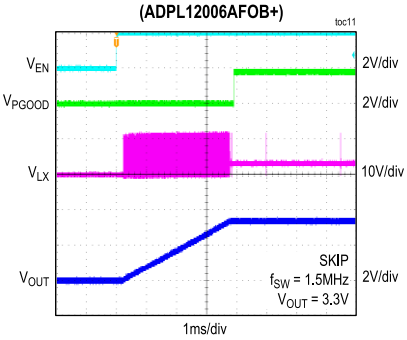


(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

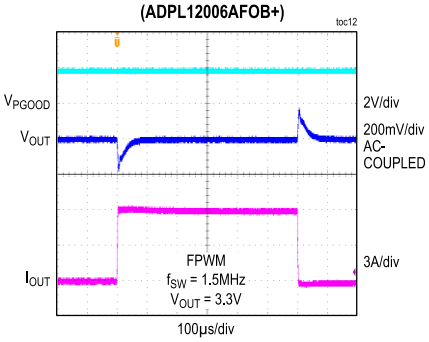
STARTUP INTO NO LOAD
(ADPL12006AFOB+)



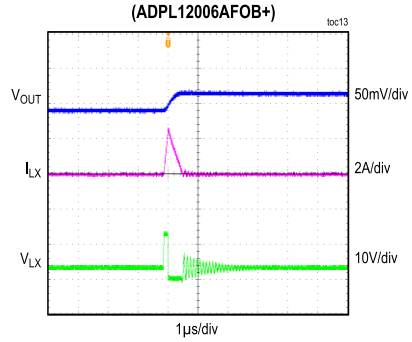
STARTUP INTO NO LOAD
(ADPL12006AFOB+)



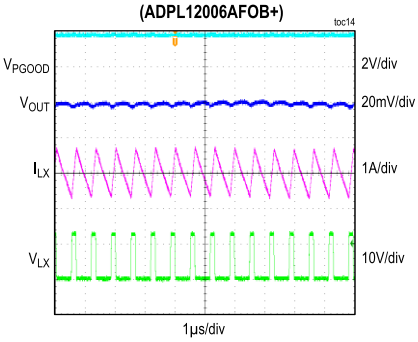
LOAD TRANSIENT RESPONSE
(ADPL12006AFOB+)



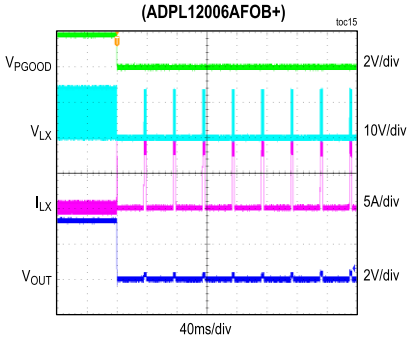
SKIP MODE OPERATION
(ADPL12006AFOB+)



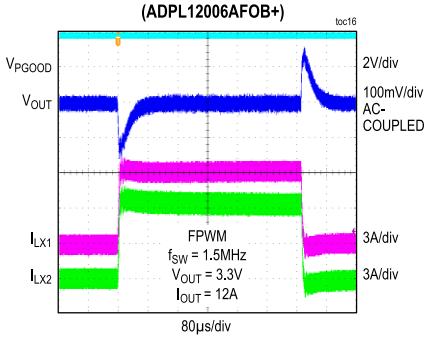
STEADY STATE SWITCHING WAVEFORM
(ADPL12006AFOB+)



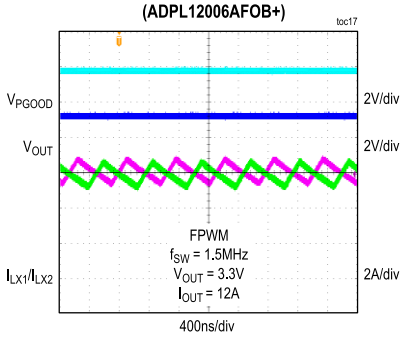
HICCUP MODE
(ADPL12006AFOB+)



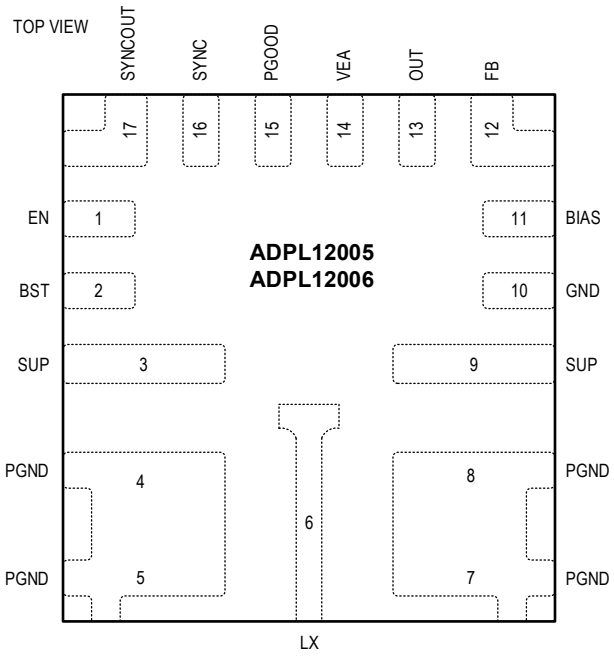
DUAL-PHASE LOAD TRANSIENT
(ADPL12006AFOB+)



DUAL-PHASE CURRENT SHARING
(ADPL12006AFOB+)



Pin Configurations



17 FC2QFN
(3.5mm x 3.75mm)

Pin Descriptions

PIN	NAME	FUNCTION
1	EN	High-Voltage-Compatible Input for Circuit Activation. If this pin is low, the part is off.
2	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
3, 9	SUP	IC Supply Input. Connect a 1µF or larger ceramic capacitor in parallel with a 4.7µF cap from SUP to PGND.
4, 5, 7, 8	PGND	Power Ground. Connect all PGND pins together.
6	LX	BUCK Switching Node. High impedance when the part is off. Connect LX to the switched side of the appropriate inductor.
10	GND	Analog Ground
11	BIAS	1.8V Internal BIAS Supply. Connect a minimum of 2µF ceramic capacitor to PGND.
12	FB	Feedback Pin. Connect a resistor divider from OUT to FB to GND to set the output voltage.
13	OUT	Buck Regulator Output Voltage-Sense Input.
14	VEA	Internal Voltage Loop Error-Amplifier Output. Connect to VEA of the target for dual-phase operation. Leave unconnected for single-phase operation.
15	PGOOD	Open-Drain Reset Output. External pull-up is required.
16	SYNC	SYNC. If connected to GND, Skip-mode operation is enabled under light loads. If connected to BIAS, forced-PWM mode is enabled.
17	SYNCOUT	180° Out-of-Phase Clock Output for Multiphase Operation. Leave SYNCOUT open for single-phase operation.

Detailed Description

The ADPL12005/ADPL12006 ICs are small, synchronous buck converters with integrated high-side and low-side switches. These ICs are designed to deliver up to 6A with input voltages from 3V to 20V while using only 20µA quiescent current at no load (V_{SUP} = 12V, V_{OUT} = 3.3V). Voltage quality can be monitored by observing the PGOOD signal. The ICs can operate in dropout mode by running at a very high-duty cycle, making them ideal for factory automation applications.

The ADPL12005/ADPL12006 ICs offer an adjustable output voltage using an external resistor-divider. The frequency is internally fixed at 400kHz and 1.5MHz, allowing for small external components and reduced output ripple. The device automatically enters skip mode (SYNC pin pulled low) at light loads with an ultra-low-quiescent current of 20µA at no load. The architecture is an average current-mode control that allows much better noise rejection of the current loop. The ICs have a small minimum ON time of 36ns to allow for large step-down ratios in a single stage without skipping cycles.
The devices can also be used in a dual-phase configuration with the help of SYNCOUT and VEA. An innovative average current-mode control architecture provides noise immunity and accurate dynamic current sharing during transients. High-power designs with up to 12A of output current can be enabled with integrated switches using the IC's dual-phase capability. FC2QFN provides improved thermal and EMI performance. A symmetrical pinout across V_{IN} and PGND further improves the EMI performance, enabling low-noise designs.

Linear Regulator Output (BIAS)

The devices include a 1.8V linear regulator (V_{BIAS}) that powers the internal circuit blocks. Connect a 2.2µF ceramic capacitor from BIAS to GND. During startup, the bias regulator draws power from the input and switches over to the output after the startup is complete (if V_{OUT} > 2.5V). For output voltages less than 1.8V, the bias regulator is always connected to the input.

System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with input levels down to 4.5V. EN turns on the internal linear (BIAS) regulator. Once V_{BIAS} exceeds the internal lockout threshold (V_{UVBIAS} = 1.63V (typ)), the converter activates, and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During the shutdown, the BIAS regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 4µA (typ). Drive EN high to bring the device out of shutdown.

Synchronization Input (SYNC)

The ADPL12005/ADPL12006 include a SYNC pin, which is a logic-level input used for operating-mode selection and frequency control. Connecting SYNC to BIAS or to an external clock enables forced fixed-frequency (FPWM) operation. Connecting SYNC to GND enables automatic skip-mode operation for better light-load efficiency. The ICs synchronize to an external clock at the rising edge applied at the SYNC pin. The devices synchronize to the external clock in two cycles. When the external clock signal at SYNC is absent for more than two clock cycles, the devices use the internal clock.

Soft-Start

The devices include an internal 2.5ms (400kHz) and 3.5ms (1.5MHz) soft-start. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Short-Circuit Protection

The devices feature a current limit that protects them against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the specified LX current-limit threshold. The converter then turns the high-side MOSFET off and the low-side MOSFET on, allowing the inductor current to ramp down. Once the inductor current crosses below the current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

A hard short is detected when the output voltage falls below 25% of the target while in the current limit. If this occurs, hiccup mode activates, and the output turns off for 35ms at 1.5MHz and 25ms at 400kHz. The output then enters soft-start and powers back up. This repeats indefinitely while the short circuit is present. Hiccup mode is disabled during soft-start.

Thermal Shutdown

Thermal shutdown protects the devices from excessive operating temperature. When the junction temperature exceeds +175°C, an internal sensor shuts down the step-down converter, allowing the IC to cool. The sensor turns the IC on again after the junction temperature cools by 15°C.

Multiphase Operation

The ADPL12005/ADPL12006 ICs are capable of dual-phase operation for high-current applications, and each IC can be configured as a controller or a target. The multiphase operation is intended for forced-PWM mode only. SYNCOUT will be 180 degrees out of phase with the controller clock. If the device is in Skip mode, then no clock will be present on SYNCOUT. To enable low-I_Q operation in dual-phase configuration, disable the EN of the target to turn OFF the IC and save quiescent current.

For a target, connect SYNCOUT to BIAS. When EN is high, there will be a procedure to detect if the IC is a controller (SYNCOUT is not connected to BIAS) or a target. The VEA pin will be the voltage-error amplifier output for the controller or the current-error amplifier input for the target. Connect the VEA pin of the controller to the VEA pin of the target to ensure balanced current sharing between the two phases. Use two separate resistor-dividers for each IC to avoid the FB pins of the controller and target being connected at the same point. Since the target IC uses the outer voltage loop of the controller (through the VEA pin), any mismatch in the output voltage is avoided. See *Figure 1* for a dual-phase configuration setup using the ADPL12005/ADPL12006.

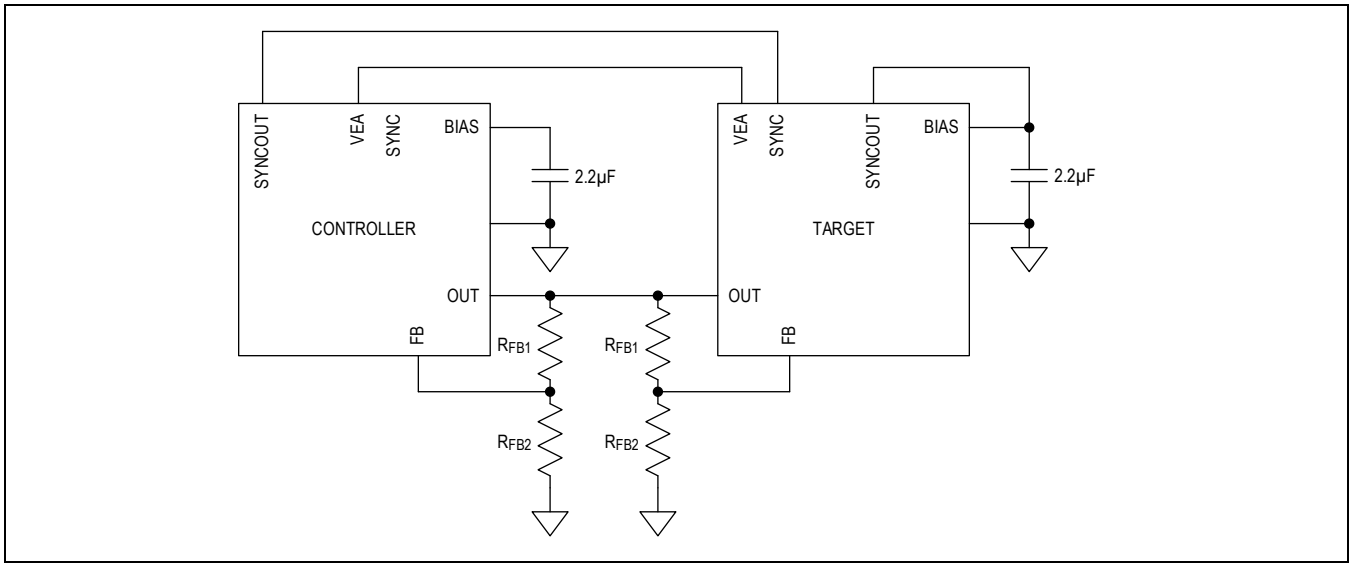


Figure 1. Typical Dual-Phase Configuration Setup

Applications Information

Setting the Output Voltage

To program the output voltage, connect a resistor-divider from the output (OUT) to GND (See *Figure 2*). Select R_{FB2} (FB to GND resistor) less than or equal to 50kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

Equation 1:

$$R_{FB1} = R_{FB2} \times (\frac{V_{OUT}}{V_{FB}} - 1)$$

Where, V_{FB} is the feedback regulation voltage. See the *Electrical Characteristics* table for more details.

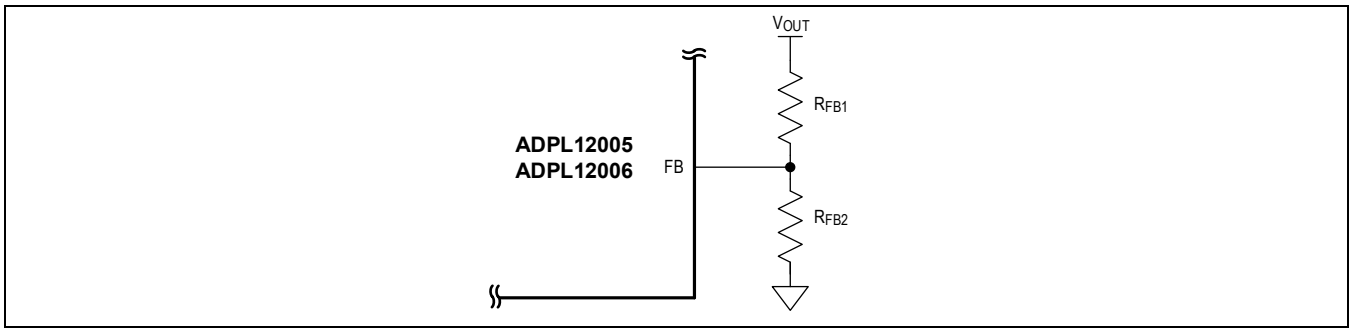


Figure 2. Output Voltage Setting using External Resistor-Divider

Table 1 provides component selection recommendations for each output range for the adjustable-output configuration. Recommendations can be further optimized for specific applications. The C_{FF} values listed in *Table 1* are recommended based on R_{FB1} = 50kΩ. The C_{FF} recommendation changes with the R_{FB1} selection.

Table 1. Recommended Components

SWITCHING FREQUENCY (kHz)	V_{OUT} (V)	INDUCTOR (µH)	EFFECTIVE C_{OUT} (µF)	C_{FF} (pF)
400	0.8V–1.8V	1.5	440	100
	1.8V–3V	3.3	440	100
	3V–5V	3.3	150	47
	5V–10V	4.7	90	100
	10V–12V	6.8	90	100
1500	0.8V–1.8V	0.47	240	10
	1.8V–3V	0.56	100	33
	3V–5V	1.2	66	33
	5V–10V	2.2	44	82

Inductor Selection

Inductor design is a compromise between the size, efficiency, control-loop bandwidth, and stability of the converter. Insufficient inductance value would increase the inductor current ripple, causing higher conduction losses and higher output voltage ripple. Since the slope compensation is fixed internally for the ADPL12005/ADPL12006, it might also cause current-mode-control instability to appear. A large inductor reduces the ripple, but increases the size and cost of the solution and slows the response. The nominal standard value selected should be within ±30% of the specified inductance. See *Table 1* for recommended inductor values.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The ADPL12005/ADPL12006 incorporates a symmetrical pinout that can be leveraged for better EMI performance. Connect two high-frequency 0603 or smaller capacitors on two SUP pins on either side of the package for good EMI performance. Connect a high-quality, 4.7µF (or larger) low-ESR ceramic capacitor on the SUP pin for low-input voltage ripple.

A bulk capacitor with higher Equivalent series resistance (ESR), such as an electrolytic capacitor, is normally required as well to lower the Q of the front-end circuit and provide the remaining capacitance needed to minimize input-voltage ripple. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

Equation 6:

$$I_{RMS} = I_{LOADMAX} \times \left(\frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}} \right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple consists of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

Equation 7:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + {}^{\Delta I_L}/_2}$$

Where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

where:

I_{OUT} = maximum output current

D = duty cycle

Output Capacitor

Output capacitance is selected to satisfy the output load-transient, output voltage ripple, and closed-loop stability requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. For a buck converter controlled by inductor current, as employed in the ADPL12005/ADPL12006, output capacitance also affects the control-loop stability.

The output ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 8 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output-ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 8:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

Where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated in equation 8, and f_{SW} is the converter's switching frequency.

The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 9:

$$C_{OUT} = \frac{\Delta I}{\Delta V \times 2\pi \times f_C}$$

Where ΔI is the load change, ΔV is the allowed voltage droop, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. Any calculations involving C_{OUT} should consider capacitance tolerance, temperature, and voltage derating. *Table 1* shows the recommended output capacitor values according to switching frequency and output voltage.

Dual-Phase Operation

Low-I_Q Operation in Dual Phase

The ADPL12005/ADPL12006 features dual-phase capability, allowing each IC to be configured as either a controller or a target. The SYNCOUT pin of the controller outputs a 180-degree out-of-phase clock when SYNC is tied high (FPWM mode). For low-I_Q mode, the SYNC pin of the controller should be pulled low (Skip mode). In this mode, there is no clock present on the SYNCOUT pin of the controller, and the controller IC enters Skip mode. The internal circuit of the target IC remains ON during this time and actively looks for the SYNCOUT signal from the controller. Since the target IC is ON, the quiescent current is slightly higher, even though both of the ICs skip pulses.

To improve the light-load efficiency and further reduce the I_Q, the target EN should be pulled low. This disables the target and its internal circuits, further reducing the I_Q. *Table 2* summarizes the truth table for low-I_Q operations.

Table 2. Configurations for Low-I_Q Operation

CONTROLLER	TARGET	MODE
EN = High, SYNC = BIAS	EN = High	FPWM (high I_Q)
EN = High, SYNC = Low	EN = High	Skip mode (low I_Q)
EN = High, SYNC = Low	EN = Low	Standby mode (ultra-low I_Q)
EN = Low	EN = High	Not allowed

Setting Output Voltage

For setting the output voltage to a value, connect a resistor-divider between OUT, FB, and GND as shown in *Figure 1*. An identical but separate resistor-divider for controller and target is recommended.

PCB Layout Guidelines

Careful Printed circuit board (PCB) layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. See *Figure 3* and the following guidelines for a good PCB layout:

1) Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.
2) Place the ceramic input-bypass capacitors, C_{BP} and C_{IN}, as close as possible to the SUP and PGND pins on both sides of the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. C_{BP} should be located closest to the IC and should have very good high-frequency performance (small package size and high capacitance). This will provide the best EMI rejection and minimize internal noise on the device, which can degrade performance.
3) Place the inductor (L), output capacitors (C_{OUT}), bootstrap capacitor (C_{BST}), and BIAS capacitor (C_{BIAS}) in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors (C_{OUT}) near the inductor so that the ground side of C_{OUT} is near the CIN ground connection to minimize the current-loop area. Place the BIAS capacitor (C_{BIAS}) next to the BIAS pin.
4) Place the bootstrap capacitor C_{BST} close to the IC and use short, wide traces to minimize the loop area to minimize the parasitic inductance. Use the nearest layer for return trace (C_{BST} to LX) to minimize the inductance further. High parasitic inductance can impact switching speed (increase switching losses) and cause high dv/dt noise.
5) Use a continuous copper GND plane on the layer next to the IC to shield the entire circuit. GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias at the GND terminals of the IC and input/output/ bypass capacitors. Do not separate or isolate PGND and GND connections with separate planes or areas.
6) Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor, LX node and other noisy signals.

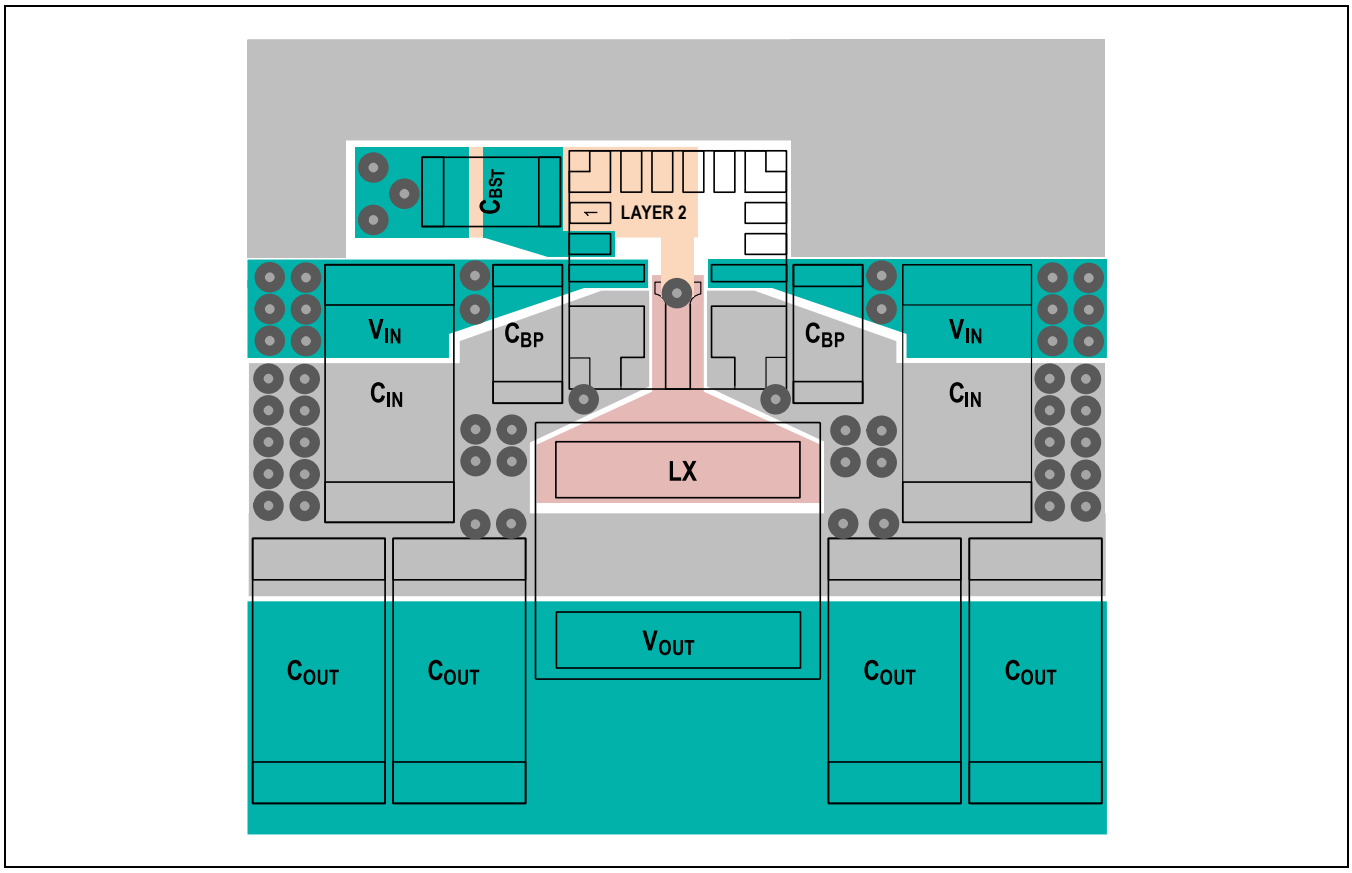
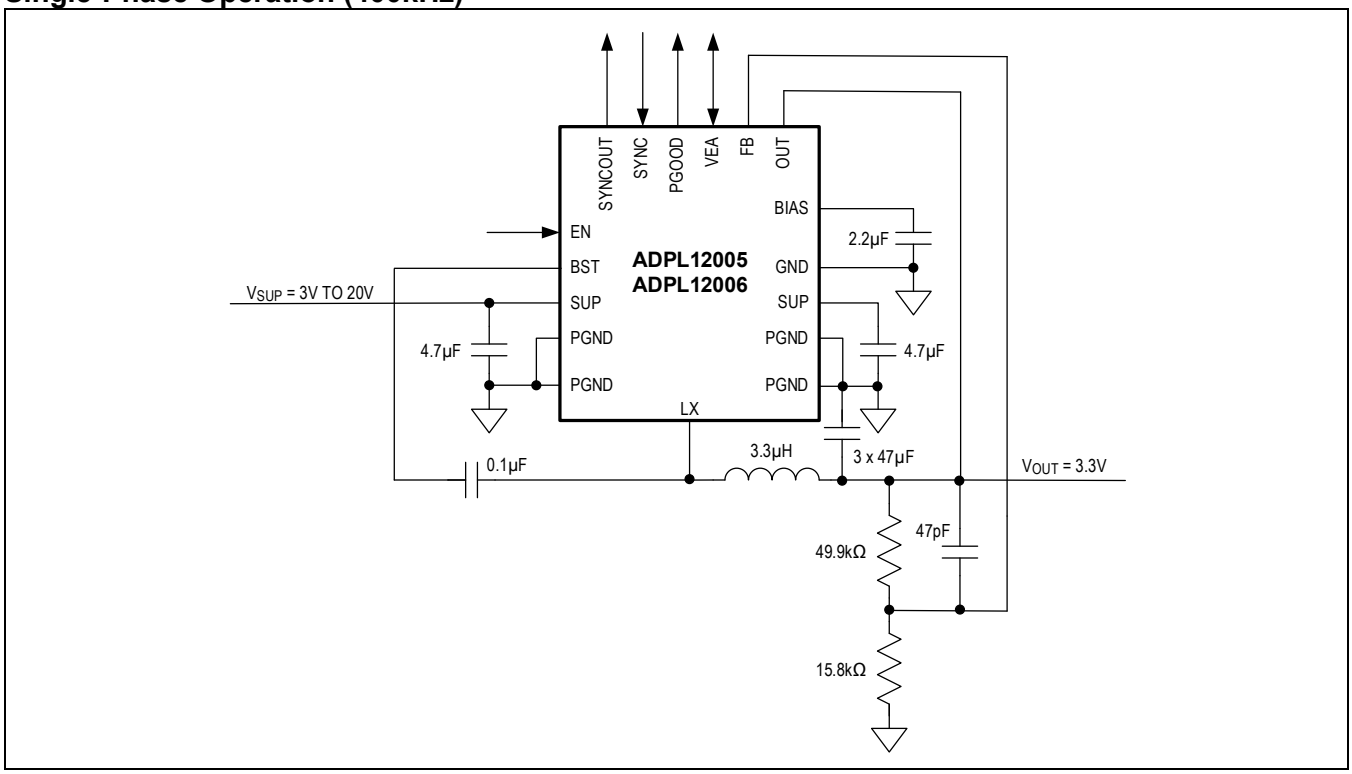


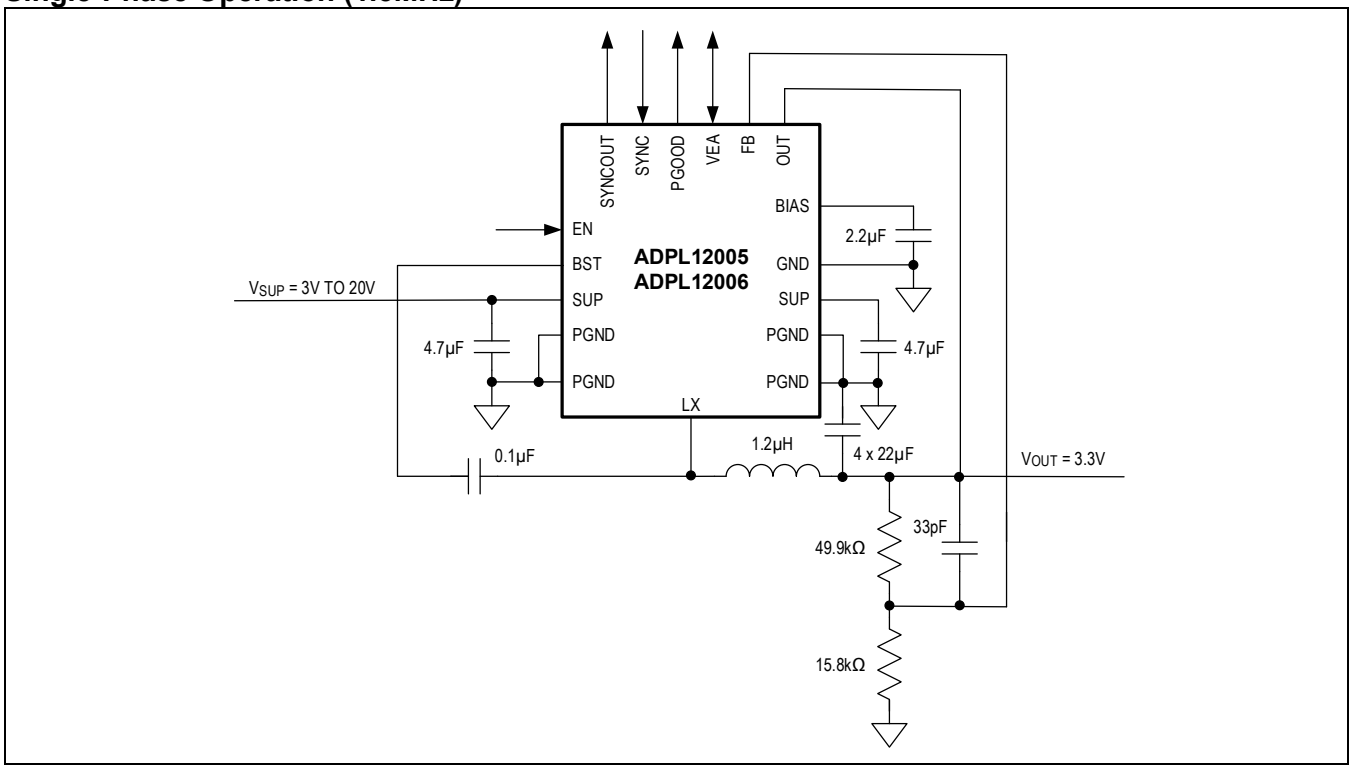
Figure 3. PCB Layout Example

Typical Application Circuits

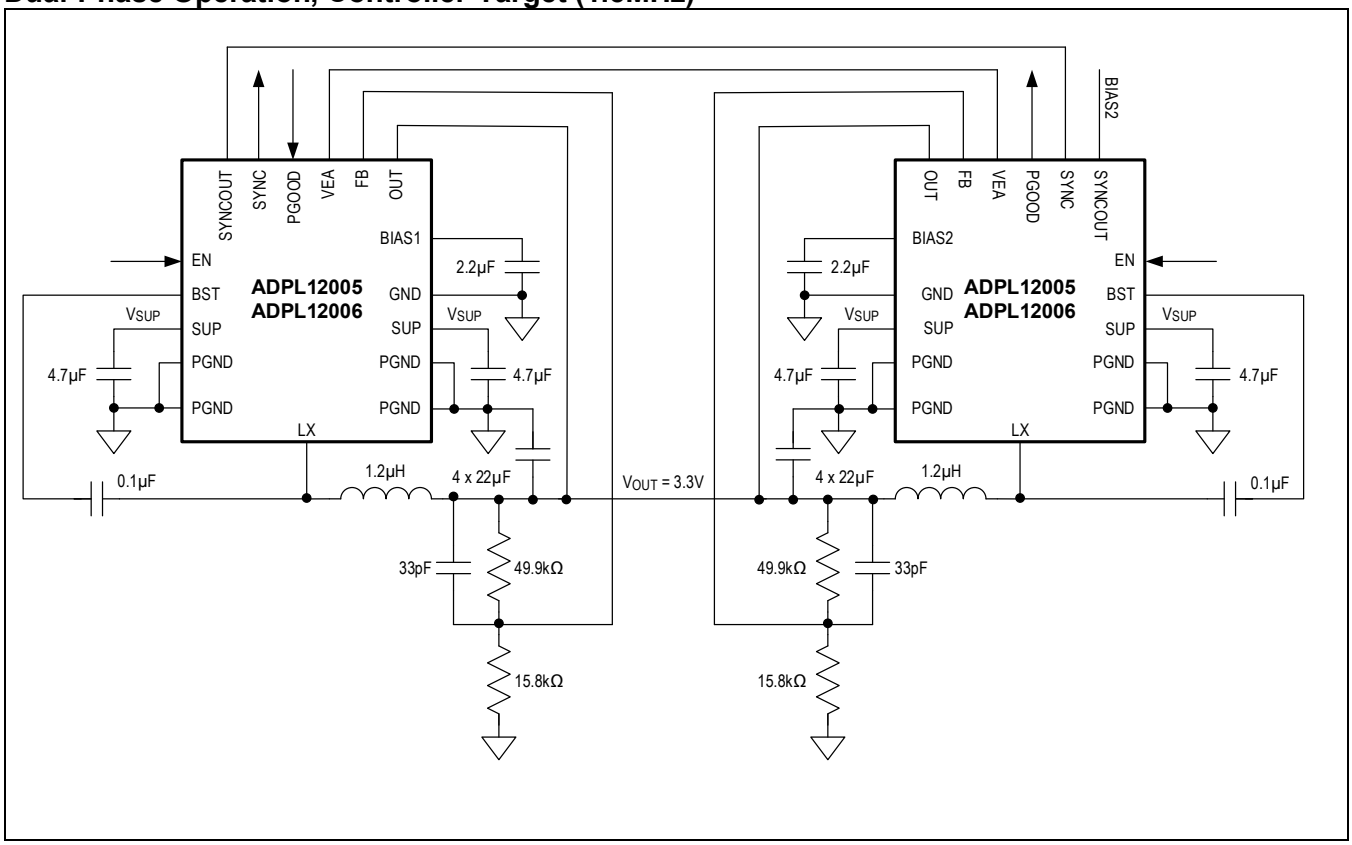
Single-Phase Operation (400kHz)



Single-Phase Operation (1.5MHz)



Dual-Phase Operation, Controller-Target (1.5MHz)



Ordering Information

PART NUMBER	V_{OUT} (V)	MAXIMUM LOAD CURRENT (A)	SWITCHING FREQUENCY
ADPL12005AFOA+T	Adjustable 0.8V to 12V	5A	400kHz
ADPL12005AFOB+T	Adjustable 0.8V to 10V	5A	1.5MHz
ADPL12006AFOA+T	Adjustable 0.8V to 12V	6A	400kHz
ADPL12006AFOB+T	Adjustable 0.8V to 10V	6A	1.5MHz

+ Denotes a lead (Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/25	Initial release	—