# ADPA9005

1GHz to 28GHz, 37.5dBm, GaN Power Amplifier

## FEATURES

- Frequency range: 1GHz to 28GHz
- Internally matched and AC-coupled input and output
- Integrated temperature-compensated RF power detector
- Power gain: 9.5dB typical with $P_{IN}$ = 28.0dBm from 6GHz to 25GHz
- $P_{OUT:}$ 37.5dBm typical with $P_{IN}$ = 28.0dBm from 6GHz to 25GHz
- Small signal gain: 20.5dB typical from 6GHz to 25GHz
- OIP3: 39.5dBm typical from 6GHz to 25GHz
- $V_{DD}$: 20V typical
- $I_{DQ}$: 560mA
- **14-terminal, 7mm × 7mm, LCC_HS package**

## APPLICATIONS

- Electronic warfare
- Test and measurement equipment

## FUNCTIONAL BLOCK DIAGRAM

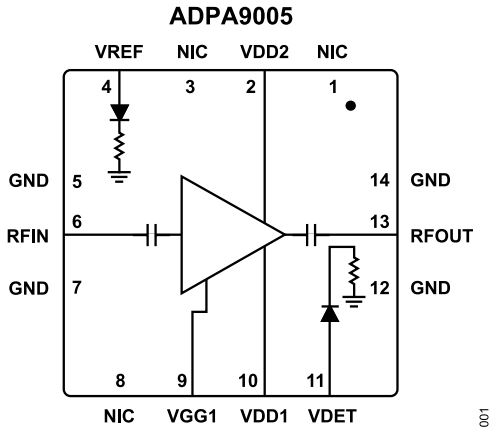



*Figure 1. Functional Block Diagram*

## GENERAL DESCRIPTION

The ADPA9005 is a 1GHz to 28GHz, wideband power amplifier with a saturated output power ($P_{OUT}$) of 37.5dBm typical, a power-added efficiency (PAE) of 15.5% typical, and a power gain of 9.5dB typical from 6GHz to 25GHz at an input power ($P_{IN}$) of 28.0dBm. The RF input and RF output are internally matched and AC-coupled. A drain bias voltage ($V_{DD}$) of 20V typical is applied to the VDD1 and VDD2 pins, which have integrated bias inductors. The drain current is set by applying a negative voltage to the VGG1 pin. A temperature-compensated RF detector is integrated, which allows monitoring of the RFOUT power.

The ADPA9005 is fabricated on a gallium nitride (GaN) process, is housed in a 14-terminal, ceramic, leadless chip carrier with a heatsink, and is specified for operation from −40°C to +85°C.


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# REVISION HISTORY

**10/2026—Revision 0: Initial Version**

# ELECTRICAL SPECIFICATIONS

## 1GHz to 6GHz Frequency Range

$T_{CASE}$ = 25°C, $V_{DD}$ = 20V, target quiescent current ($I_{DQ}$) = 560mA, and frequency range = 1GHz to 6GHz, unless otherwise stated.

**Table 1. 1GHz to 6GHz Frequency Range**

| PARAMETER | SYMBOL | TEST CONDITIONS/COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **FREQUENCY RANGE** | | | 1 | | 6 | GHz |
| **GAIN** | | | | | | |
| Small Signal Gain | S21 | | | 19 | | dB |
| Gain Flatness | | | | ±1.8 | | dB |
| Gain Variation Over Temperature | | | | 0.06 | | dB/°C |
| **RETURN LOSS** | | | | | | |
| Input | S11 | | | 12.5 | | dB |
| Output | S22 | | | 15 | | dB |
| **POWER** | | $P_{IN}$ = 28.0dBm | | | | |
| Output | $P_{OUT}$ | | 36 | 38 | | dBm |
| Gain | | | 8 | 10 | | dB |
| Power-Added Efficiency | PAE | | | 19.5 | | % |
| Output Third-Order Intercept | OIP3 | $P_{OUT}$ per tone = 28.0dBm with 1MHz spacing | | 39.5 | | dBm |
| Output Second-Order Intercept | OIP2 | $P_{OUT}$ per tone = 28.0dBm with 1MHz spacing | | 47 | | dBm |
| **SUPPLY** | | | | | | |
| Drain Bias Voltage | $V_{DD}$ | | | 20 | 24 | V |
| Quiescent Current | $I_{DQ}$ | Adjust the gate control voltage ($V_{GG1}$) between −3V and −1V to achieve an $I_{DQ}$ = 560mA typical | | 560 | | mA |

# ELECTRICAL SPECIFICATIONS

## 6GHz to 25GHz Frequency Range

$T_{CASE}$ = 25°C, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA, and frequency range = 6GHz to 25GHz, unless otherwise stated.

**Table 2. 6GHz to 25GHz Frequency Range**

| PARAMETER | SYMBOL | TEST CONDITIONS/COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **FREQUENCY RANGE** | | | 6 | | 25 | GHz |
| **GAIN** | | | | | | |
| Small Signal Gain | S21 | | | 20.5 | | dB |
| Gain Flatness | | | | ±1.3 | | dB |
| Gain Variation Over Temperature | | | | 0.07 | | dB/°C |
| **RETURN LOSS** | | | | | | |
| Input | S11 | | | 16 | | dB |
| Output | S22 | | | 14 | | dB |
| **POWER** | | $P_{IN}$ = 28.0dBm | | | | |
| Output | $P_{OUT}$ | | 35.5 | 37.5 | | dBm |
| Gain | | | 7.5 | 9.5 | | dB |
| Power-Added Efficiency | PAE | | | 15.5 | | % |
| Output Third-Order Intercept | OIP3 | $P_{OUT}$ per tone = 28.0dBm with 1MHz spacing | | 39.5 | | dBm |
| Output Second-Order Intercept | OIP2 | $P_{OUT}$ per tone = 28.0dBm with 1MHz spacing | | 56 | | dBm |
| **SUPPLY** | | | | | | |
| Drain Bias Voltage | $V_{DD}$ | | | 20 | 24 | V |
| Quiescent Current | $I_{DQ}$ | Adjust $V_{GG1}$ between −3V and −1V to achieve an $I_{DQ}$ = 560mA typical | | 560 | | mA |

# ELECTRICAL SPECIFICATIONS

## 25GHz to 28GHz Frequency Range

$T_{CASE}$ = 25°C, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA, and frequency range = 25GHz to 28GHz, unless otherwise stated.

**Table 3. 25GHz to 28GHz Frequency Range**

| PARAMETER | SYMBOL | TEST CONDITIONS/COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **FREQUENCY RANGE** | | | 25 | | 28 | GHz |
| **GAIN** | | | | | | |
| Small Signal Gain | S21 | | | 17.5 | | dB |
| Gain Flatness | | | | ±3.5 | | dB |
| Gain Variation Over Temperature | | | | 0.12 | | dB/°C |
| **RETURN LOSS** | | | | | | |
| Input | S11 | | | 13 | | dB |
| Output | S22 | | | 11 | | dB |
| **POWER** | | $P_{IN}$ = 28.0dBm | | | | |
| Output | $P_{OUT}$ | | | 35 | | dBm |
| Gain | | | | 7.5 | | dB |
| Power-Added Efficiency | PAE | | | 10 | | % |
| Output Third-Order Intercept | OIP3 | $P_{OUT}$ per tone = 28.0dBm with 1MHz spacing | | 39 | | dBm |
| **SUPPLY** | | | | | | |
| Drain Bias Voltage | $V_{DD}$ | | | 20 | 24 | V |
| Quiescent Current | $I_{DQ}$ | Adjust $V_{GG1}$ between −3V and −1V to achieve an $I_{DQ}$ = 560mA typical | | 560 | | mA |

# ABSOLUTE MAXIMUM RATINGS

**Table 4. Absolute Maximum Ratings**

| PARAMETER | RATING |
|---|---|
| Bias Voltage | |
| Drain ($V_{DD}$) | 28V |
| Gate ($V_{GG1}$) | −5V DC to 0V DC |
| Bias Current | |
| Gate Current ($I_{GG1}$) at 85°C | 4.3mA (see **Figure 53**) |
| RF Input Power (RFIN) | 33dBm |
| Continuous Power Dissipation ($P_{DISS}$), $T_{CASE}$ = 85°C, Derate 244.5mW/°C Above 85°C | 34.2W |
| Temperature | |
| Storage Range | −65°C to +150°C |
| Operating Range | −40°C to +85°C |
| Maximum Channel | 225°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the channel to case thermal resistance where the case is the bottom of the package base.

**Table 5. Thermal Resistance**

| PACKAGE TYPE | $\theta_{JC}$[1] | UNIT |
|---|---|---|
| EH-14-1 | 4.09 | °C/W |

[1] $\theta_{JC}$ was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the package base to the heatsink. The bottom of the package base is held constant at the operating temperature of 85°C.

## Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

### ESD Ratings for ADPA9005

**Table 6. ADPA9005, 14-Terminal LCC_HS**

| ESD MODEL | WITHSTAND THRESHOLD (V) | CLASS |
|---|---|---|
| HBM | ±250 | 1B |

## ESD Caution



**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

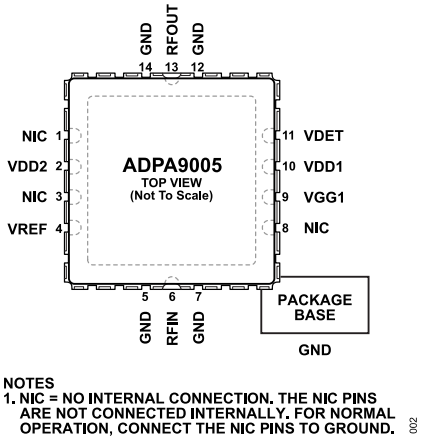



*Figure 2. Pin Configuration*

**Table 7. Pin Function Descriptions**

| PIN NO. | MNEMONIC | DESCRIPTION |
|---|---|---|
| 1, 3, 8 | NIC | No Internal Connection. The NIC pins are not connected internally. For normal operation, connect the NIC pins to ground. |
| 2 | VDD2 | Drain Bias for the Second Gain Stage. Capacitively bypass as shown in the typical application circuit (see **Figure 66**). See **Figure 3** for the interface schematic. |
| 4 | VREF | Reference Diode for Temperature Compensation of the VDET RF Output Power Measurements. Connect a 40.2kΩ resistor between the VREF pin and 5V to provide DC bias. See **Figure 4** for the interface schematic. |
| 5, 7, 12, 14 | GND | Ground. The GND pins must be connected to the RF and DC ground. See **Figure 5** for the interface schematic. |
| 6 | RFIN | RF Input. The RFIN pin is AC-coupled and matched to 50Ω. See **Figure 6** for the interface schematic. |
| 9 | VGG1 | Gate Bias for the First and Second Gain Stages. Adjust the negative voltage on the VGG1 pin to set $I_{DQ}$ to the desired level. See **Figure 7** for the interface schematic. |
| 10 | VDD1 | Drain Bias for the First Gain Stage. Capacitively bypass as shown in the typical application circuit (see **Figure 66**). See **Figure 8** for the interface schematic. |
| 11 | VDET | Detector Diode for RF Output Power Measurements. Used in combination with the VREF pin. The difference in voltage (VREF voltage ($V_{REF}$) − VDET voltage ($V_{DET}$)) is a temperature-compensated DC voltage that is proportional to the RF output power. Connect a 40.2kΩ resistor between the VDET pin and 5V to provide the DC bias. See **Figure 3** for the interface schematic. |
| 13 | RFOUT | RF Output. The RFOUT pin is AC-coupled and matched to 50Ω. See **Figure 3** for the interface schematic. |
| Package Base | GND | The package base must be connected to the RF and the DC ground. See **Figure 5** for the interface schematic. |

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

## Interface Schematics

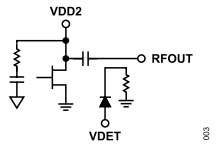



*Figure 3. VDD2, VDET, and RFOUT Interface Schematic*




*Figure 4. VREF Interface Schematic*




*Figure 5. GND Interface Schematic*

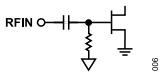



*Figure 6. RFIN Interface Schematic*

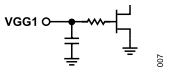



*Figure 7. VGG1 Interface Schematic*

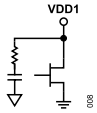



*Figure 8. VDD1 Interface Schematic*

## TYPICAL PERFORMANCE CHARACTERISTICS

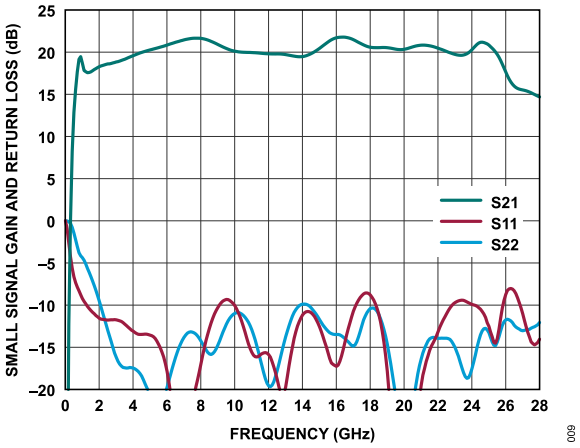



Figure 9. Small Signal Gain and Return Loss vs. Frequency, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

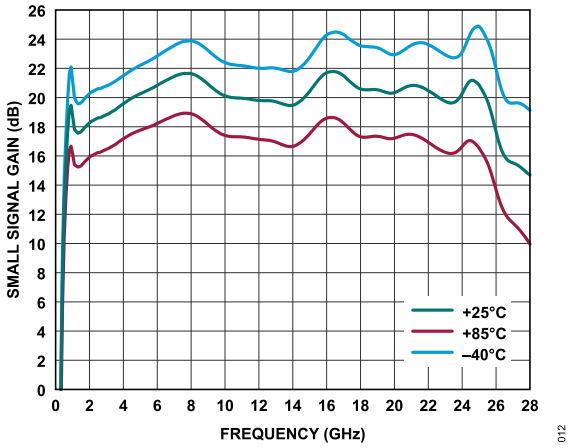



Figure 12. Small Signal Gain vs. Frequency for Various Temperatures, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

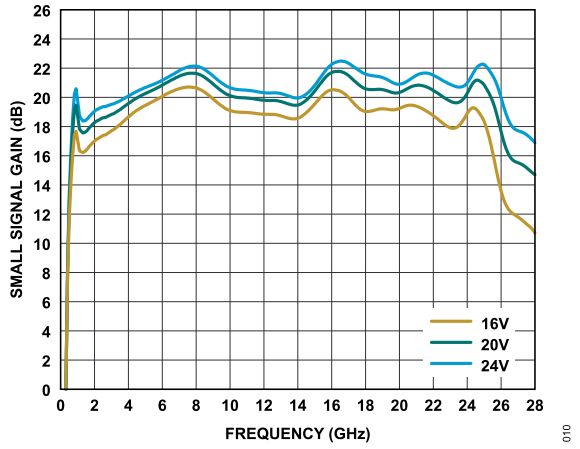



Figure 10. Small Signal Gain vs. Frequency for Various Supply Voltages, $I_{DQ}$ = 560mA

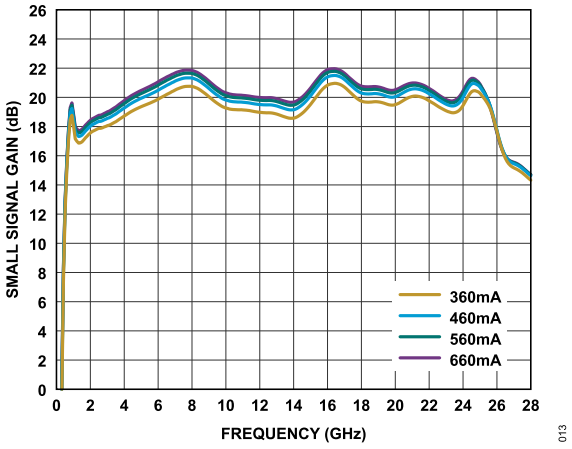



Figure 13. Small Signal Gain vs. Frequency for Various Supply Currents, $V_{DD}$ = 20V

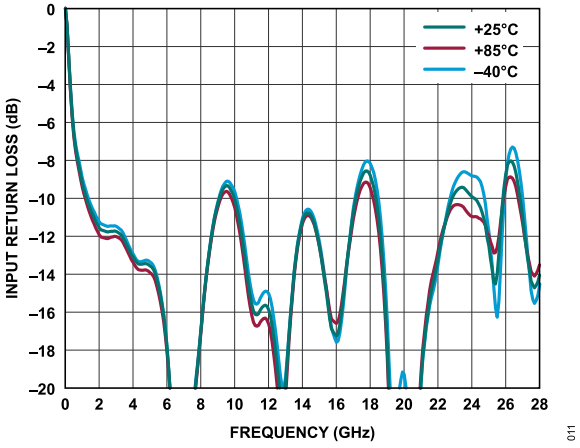



Figure 11. Input Return Loss vs. Frequency for Various Temperatures, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

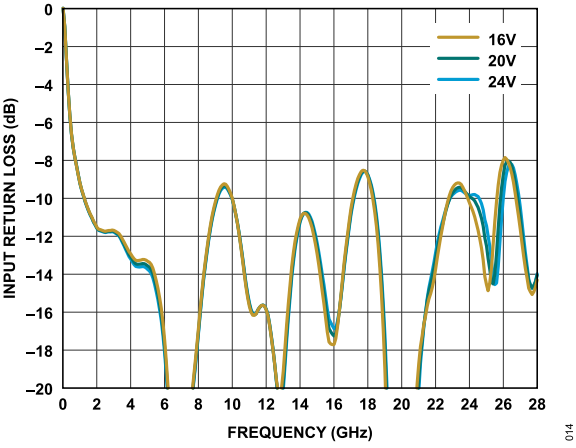



Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages, $I_{DQ}$ = 560mA

## TYPICAL PERFORMANCE CHARACTERISTICS

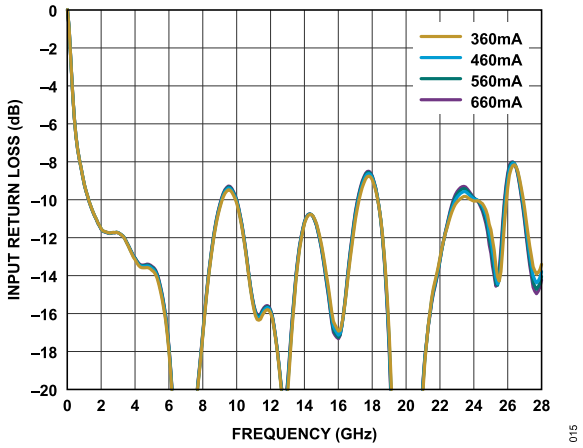



*Figure 15. Input Return Loss vs. Frequency for Various Supply Currents, $V_{DD}$ = 20V*

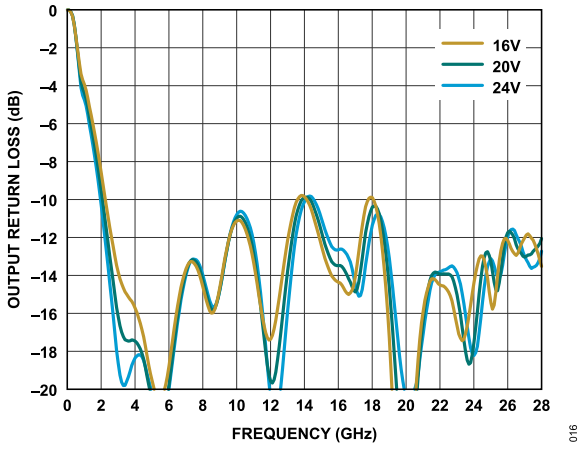



*Figure 16. Output Return Loss vs. Frequency for Various Supply Voltages, $I_{DQ}$ = 560mA*

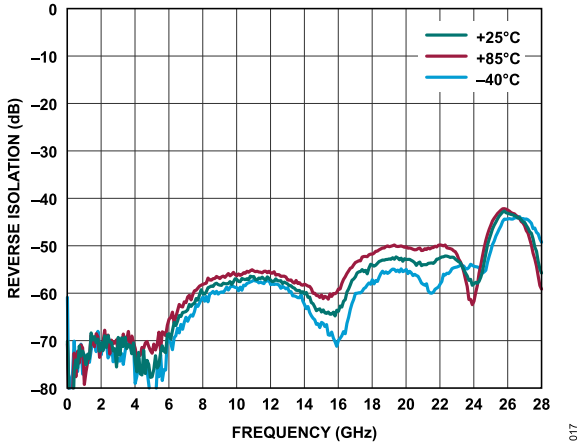



*Figure 17. Reverse Isolation vs. Frequency for Various Temperatures, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

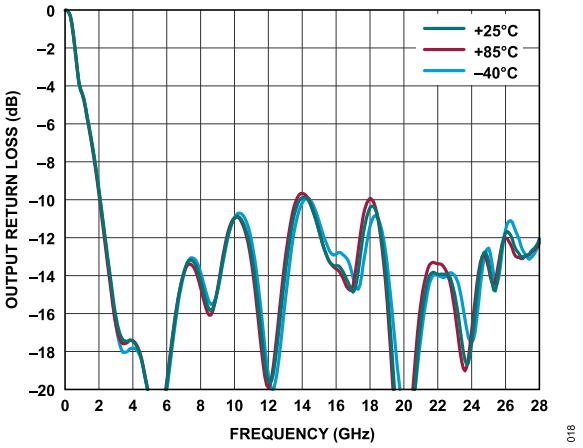



*Figure 18. Output Return Loss vs. Frequency for Various Temperatures, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

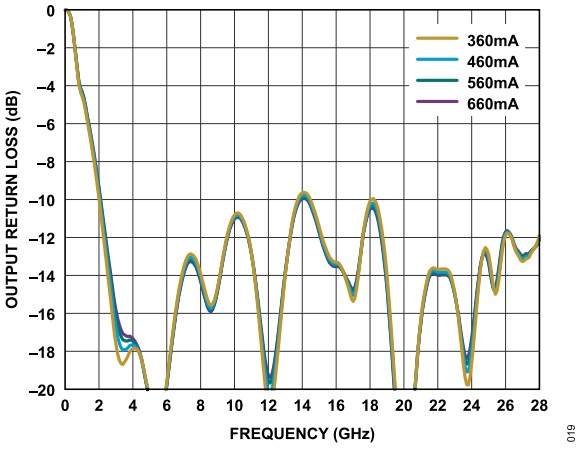



*Figure 19. Output Return Loss vs. Frequency for Various Supply Currents, $V_{DD}$ = 20V*

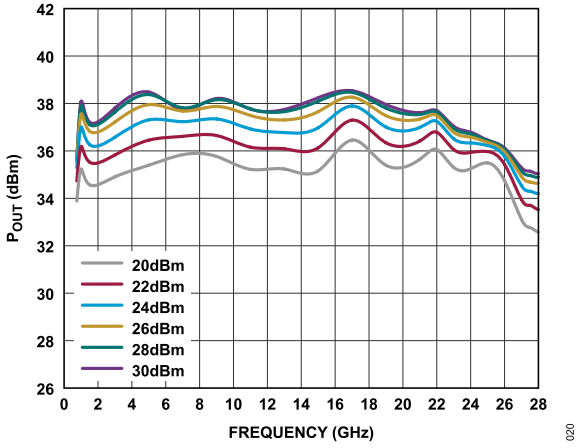



*Figure 20. $P_{OUT}$ vs. Frequency for Various $P_{IN}$ Levels, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

## TYPICAL PERFORMANCE CHARACTERISTICS

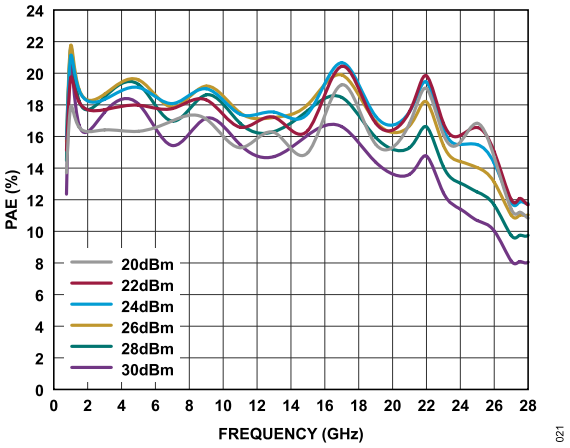



Figure 21. PAE vs. Frequency for Various $P_{IN}$ Levels, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

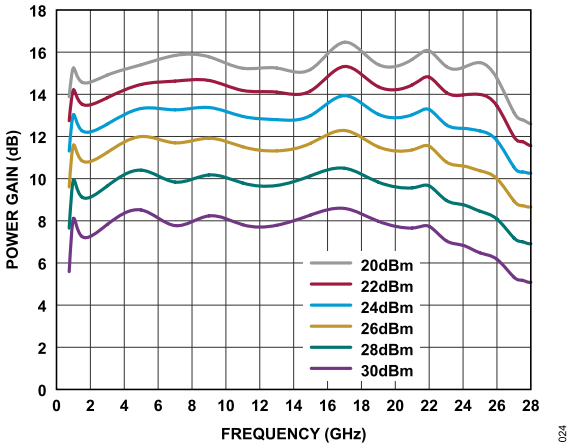



Figure 24. Power Gain vs. Frequency for Various $P_{IN}$ Levels, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

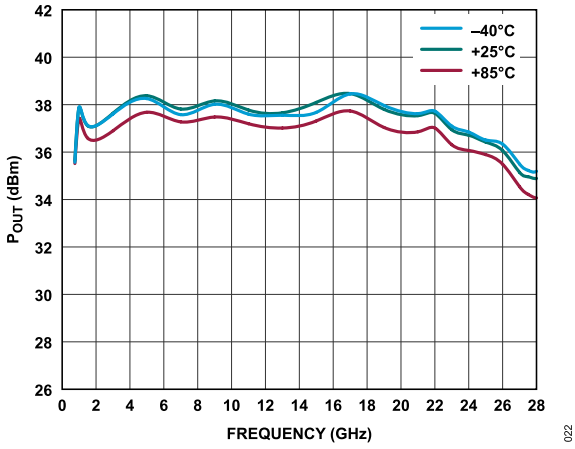



Figure 22. $P_{OUT}$ vs. Frequency at Various Temperatures for $P_{IN}$ = 28dBm, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

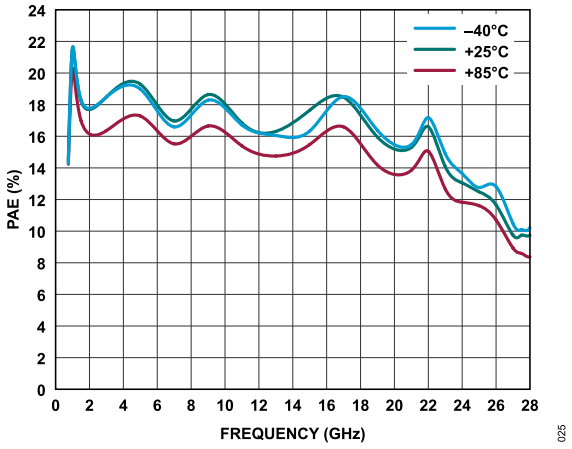



Figure 25. PAE vs. Frequency at Various Temperatures for $P_{IN}$ = 28dBm, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

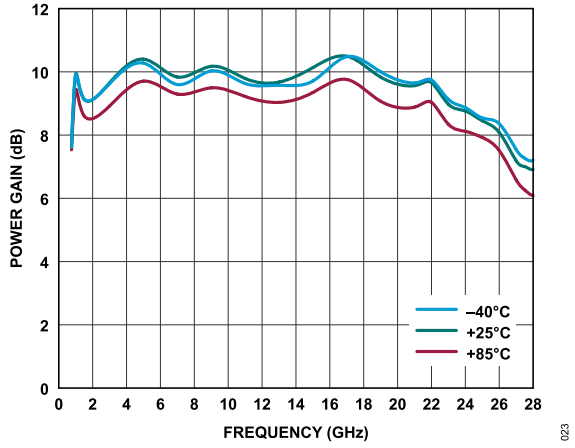



Figure 23. Power Gain vs. Frequency at Various Temperatures for $P_{IN}$ = 28dBm, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

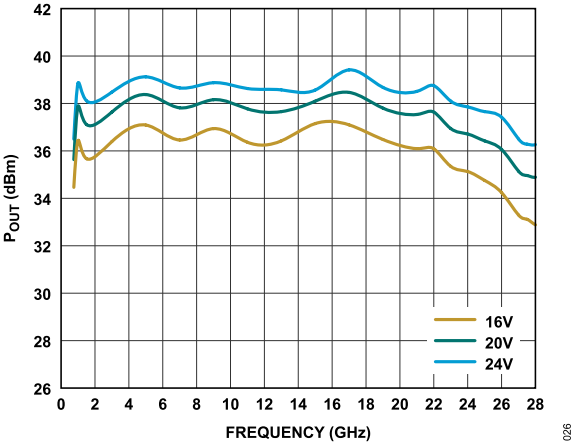



Figure 26. $P_{OUT}$ vs. Frequency for Various Supply Voltages at $P_{IN}$ = 28dBm, $I_{DQ}$ = 560mA

## TYPICAL PERFORMANCE CHARACTERISTICS

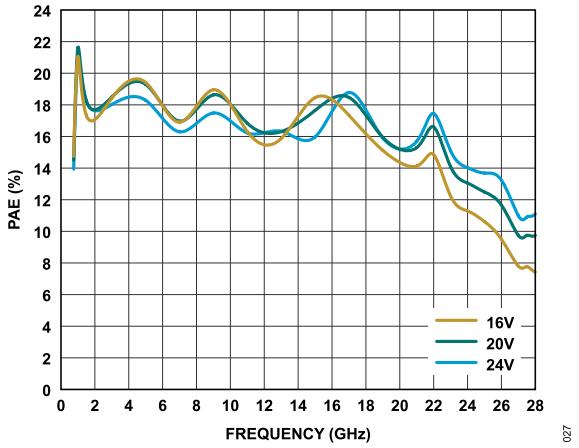



Figure 27. PAE vs. Frequency for Various Supply Voltages at $P_{IN}$ = 28dBm, $I_{DQ}$ = 560mA

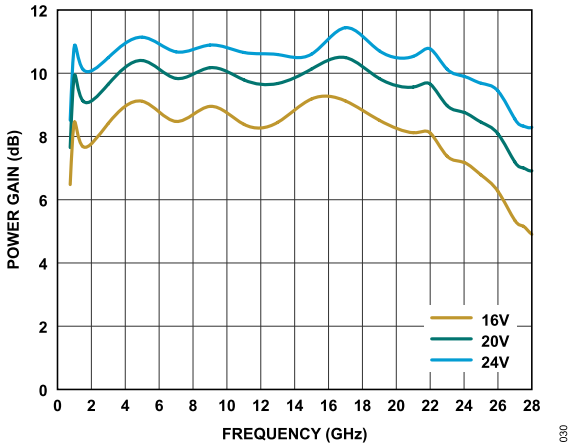



Figure 30. Power Gain vs. Frequency for Various Supply Voltages at $P_{IN}$ = 28dBm, $I_{DQ}$ = 560mA

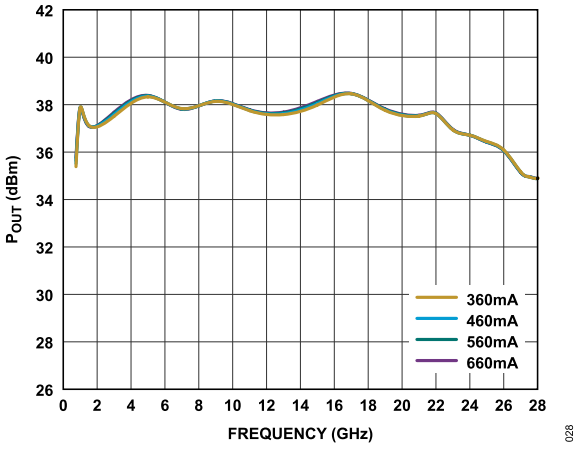



Figure 28. $P_{OUT}$ vs. Frequency for Various Supply Currents at $P_{IN}$ = 28dBm, $V_{DD}$ = 20V

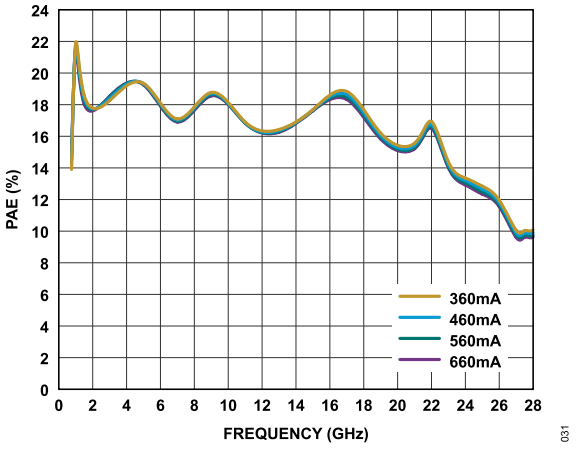



Figure 31. PAE vs. Frequency for Various Supply Currents at $P_{IN}$ = 28dBm, $V_{DD}$ = 20V

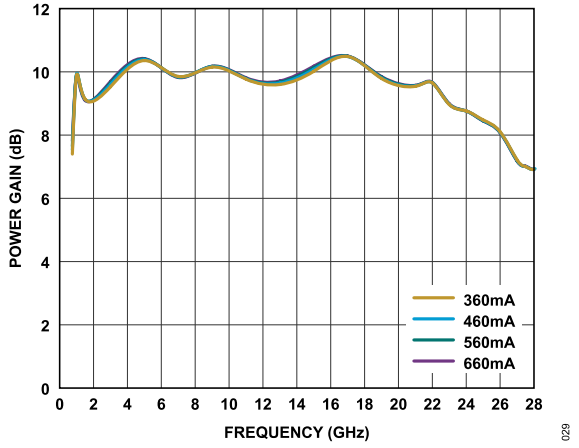



Figure 29. Power Gain vs. Frequency for Various Supply Currents at $P_{IN}$ = 28dBm, $V_{DD}$ = 20V

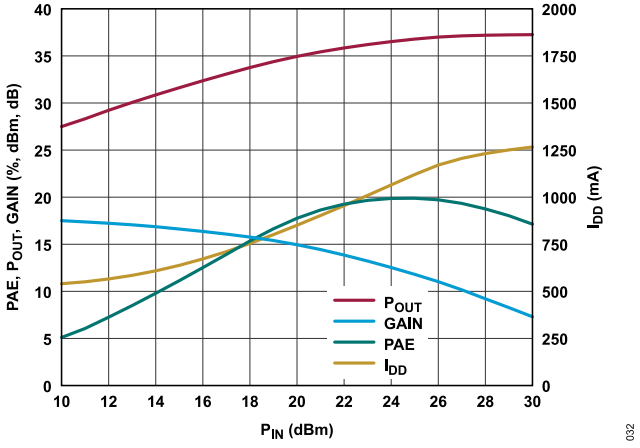



Figure 32. PAE, $P_{OUT}$, Gain, and Supply Current ($I_{DD}$) vs. $P_{IN}$ at 2GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

## TYPICAL PERFORMANCE CHARACTERISTICS

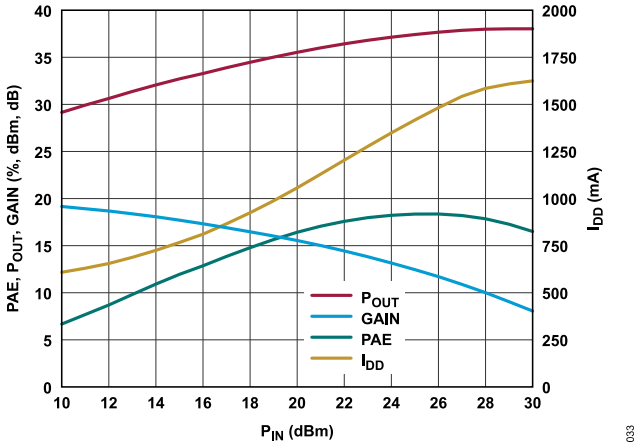



Figure 33. PAE, $P_{OUT}$, Gain, and $I_{DD}$ vs. $P_{IN}$ at 6GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

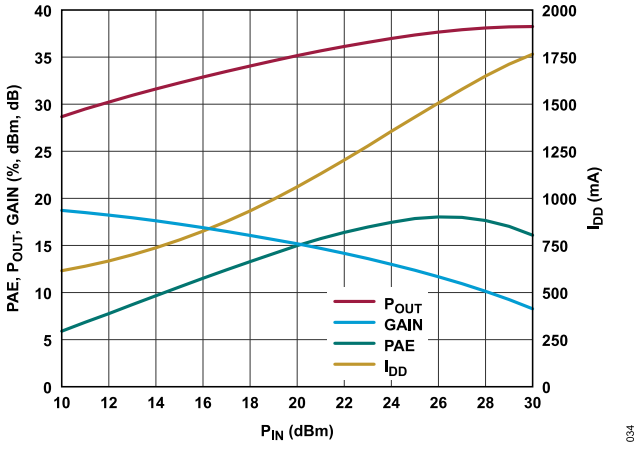



Figure 34. PAE, $P_{OUT}$, Gain, and $I_{DD}$ vs. $P_{IN}$ at 15GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

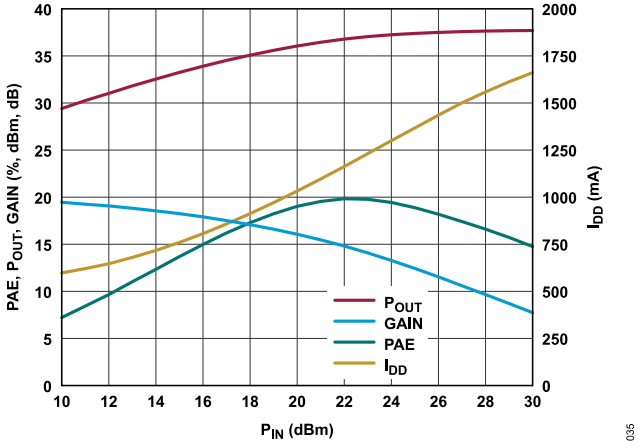



Figure 35. PAE, $P_{OUT}$, Gain, and $I_{DD}$ vs. $P_{IN}$ at 22GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

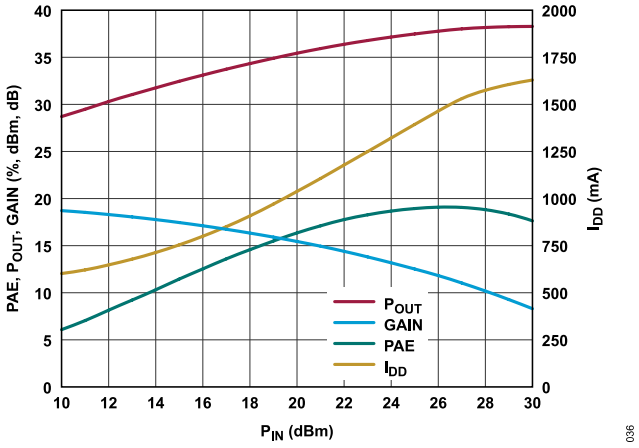



Figure 36. PAE, $P_{OUT}$, Gain, and $I_{DD}$ vs. $P_{IN}$ at 10GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

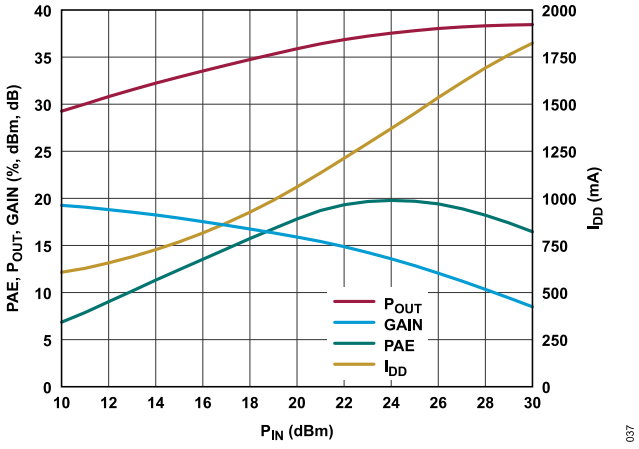



Figure 37. PAE, $P_{OUT}$, Gain, and $I_{DD}$ vs. $P_{IN}$ at 18GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

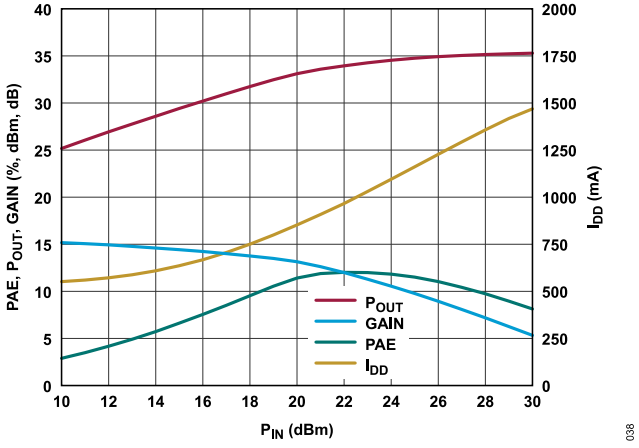



Figure 38. PAE, $P_{OUT}$, Gain, and $I_{DD}$ vs. $P_{IN}$ at 27GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

## TYPICAL PERFORMANCE CHARACTERISTICS

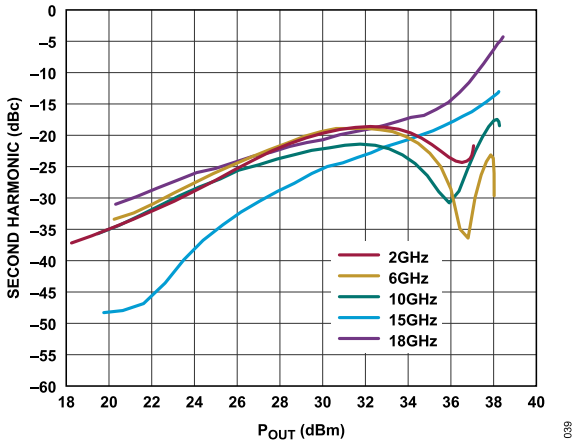



*Figure 39. Second Harmonic vs. $P_{OUT}$ for Various Frequencies, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

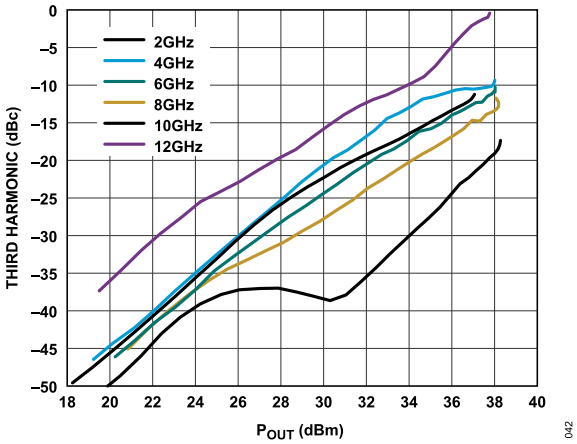



*Figure 42. Third Harmonic vs. $P_{OUT}$ for Various Frequencies, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

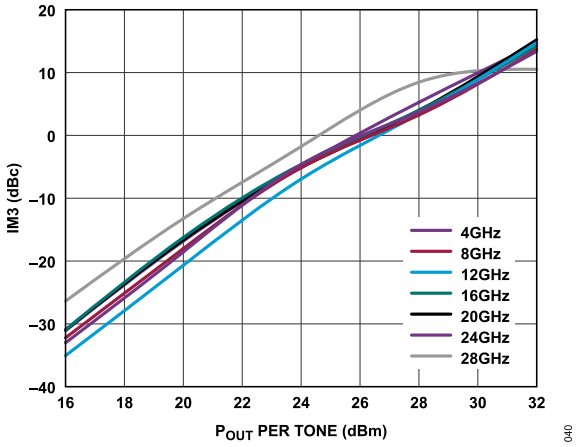



*Figure 40. Third-Order Intermodulation (IM3) vs. $P_{OUT}$ per Tone for Various Frequencies, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

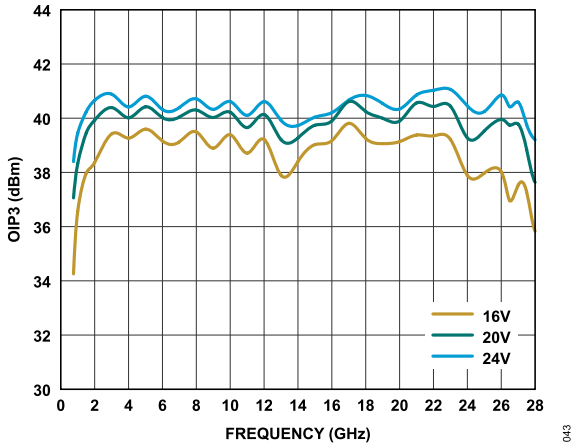



*Figure 43. OIP3 vs. Frequency for Various Supply Voltages at $P_{OUT}$ per Tone = 28dBm, $I_{DQ}$ = 560mA*

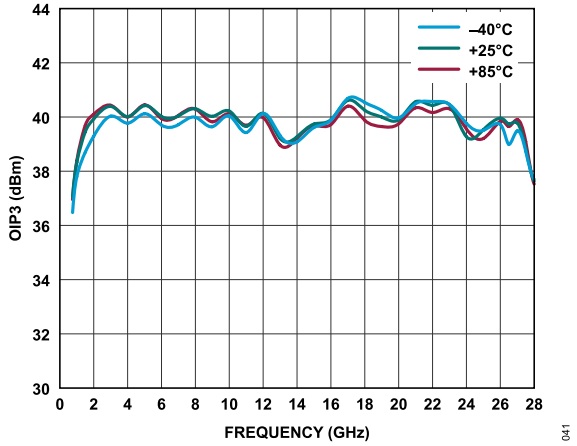



*Figure 41. OIP3 vs. Frequency for Various Temperatures at $P_{OUT}$ per Tone = 28dBm, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

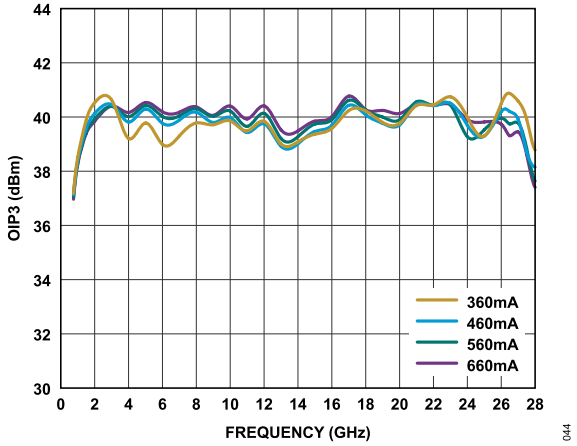



*Figure 44. OIP3 vs. Frequency for Various Supply Currents at $P_{OUT}$ per Tone = 28dBm, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

## TYPICAL PERFORMANCE CHARACTERISTICS

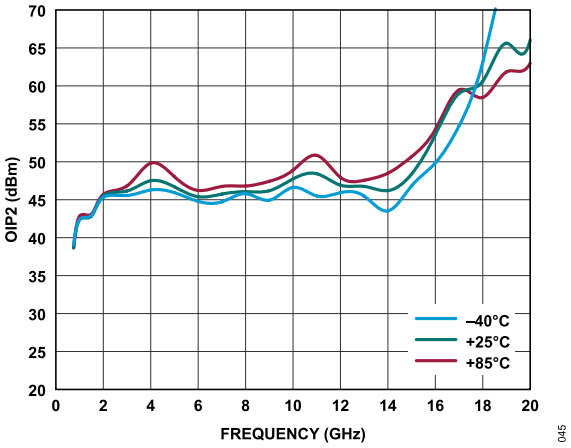



*Figure 45. OIP2 vs. Frequency for Various Temperatures at $P_{OUT}$ per Tone = 28dBm, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

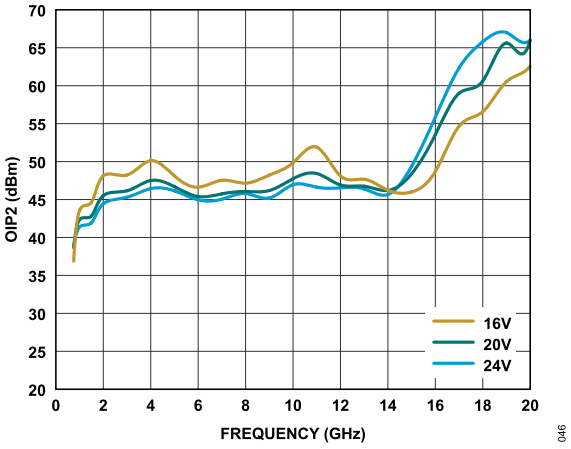



*Figure 46. OIP2 vs. Frequency for Various Supply Voltages at $P_{OUT}$ per Tone = 28dBm, $I_{DQ}$ = 560mA*

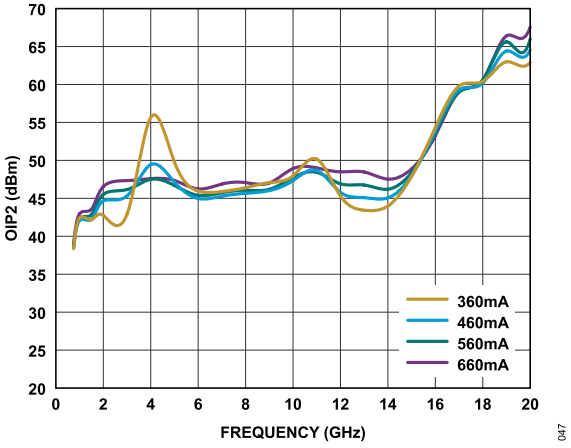



*Figure 47. OIP2 vs. Frequency for Various Supply Currents at $P_{OUT}$ per Tone = 28dBm, $V_{DD}$ = 20V*

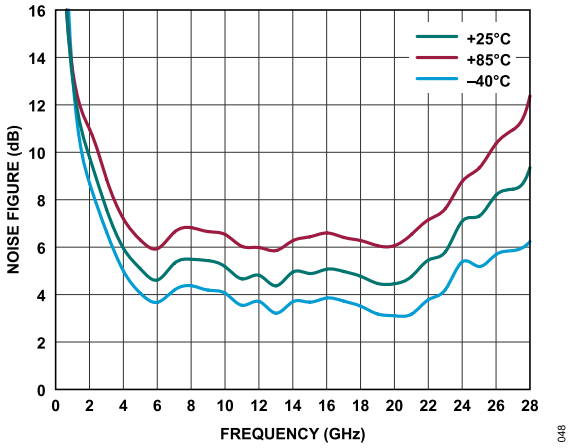



*Figure 48. Noise Figure vs. Frequency for Various Temperatures, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

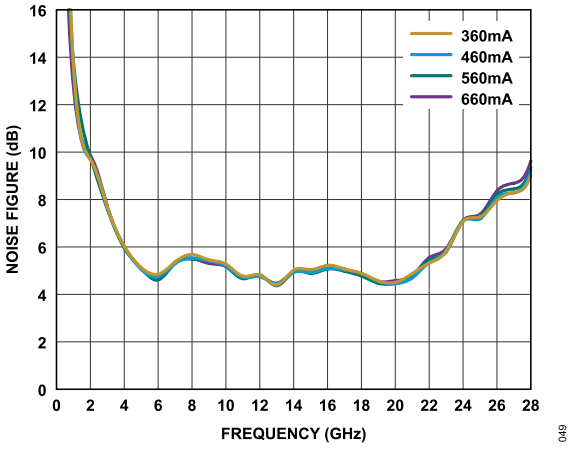



*Figure 49. Noise Figure vs. Frequency for Various Supply Currents, $V_{DD}$ = 20V*

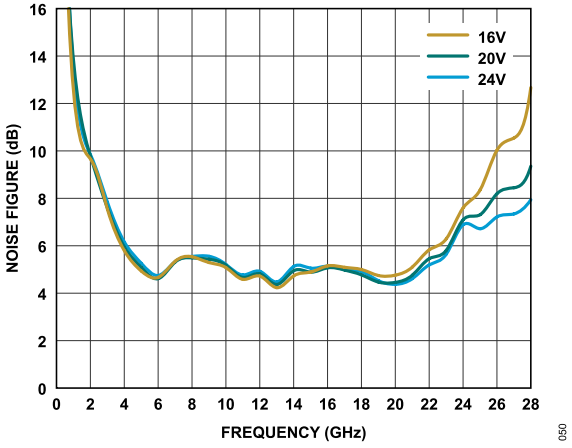



*Figure 50. Noise Figure vs. Frequency for Various Supply Voltages, $I_{DQ}$ = 560mA*

## TYPICAL PERFORMANCE CHARACTERISTICS

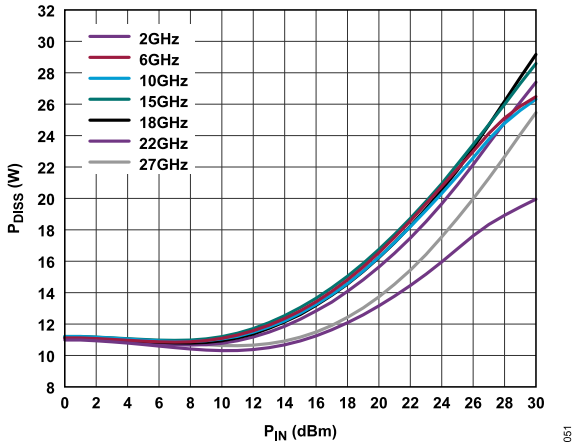



Figure 51. $P_{DISS}$ vs. $P_{IN}$ for Various Frequencies at $T_{CASE}$ = 85°C, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

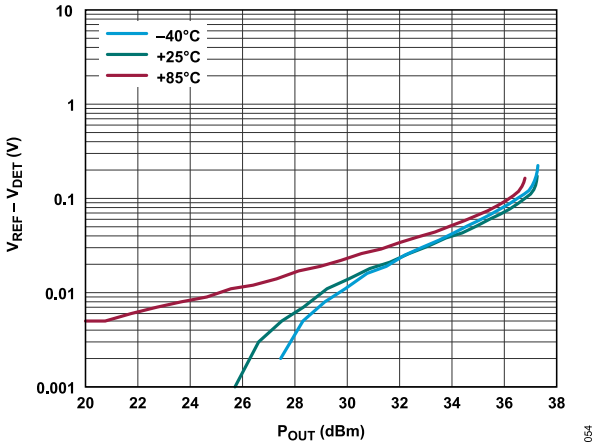



Figure 54. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 2GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

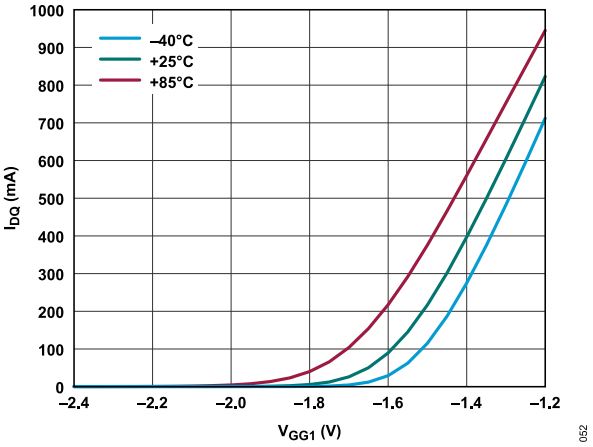



Figure 52. $I_{DQ}$ vs. $V_{GG1}$ for Various Temperatures, $V_{DD}$ = 20V

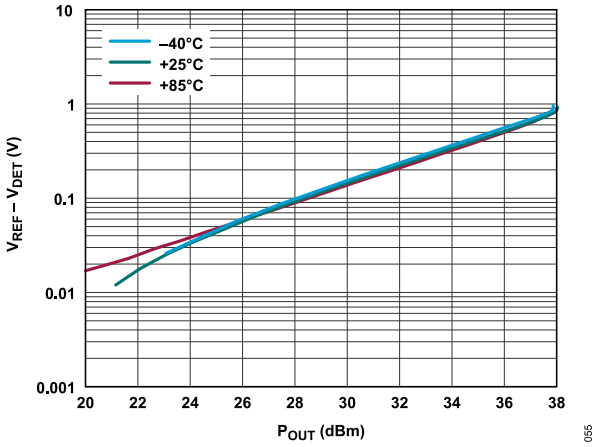



Figure 55. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 6GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

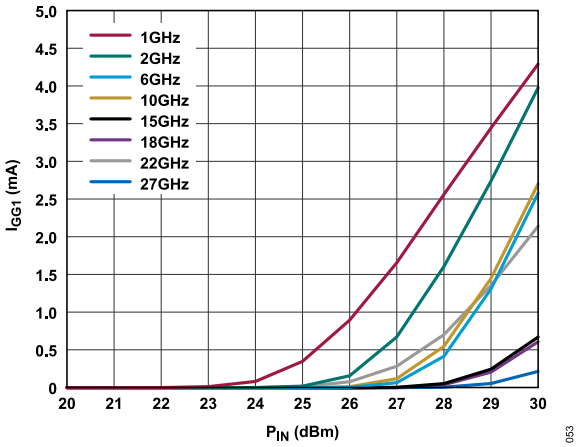



Figure 53. $I_{GG1}$ vs. $P_{IN}$ for Various Frequencies at $T_{CASE}$ = 85°C, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

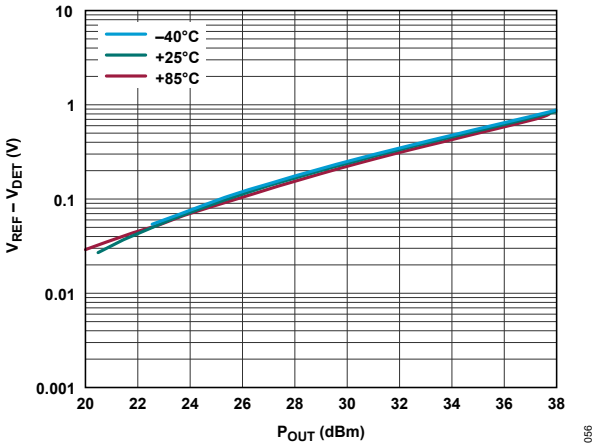



Figure 56. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 10GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

## TYPICAL PERFORMANCE CHARACTERISTICS

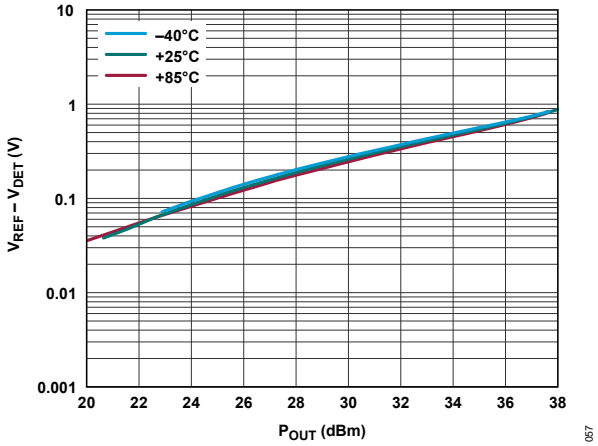



Figure 57. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 15GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

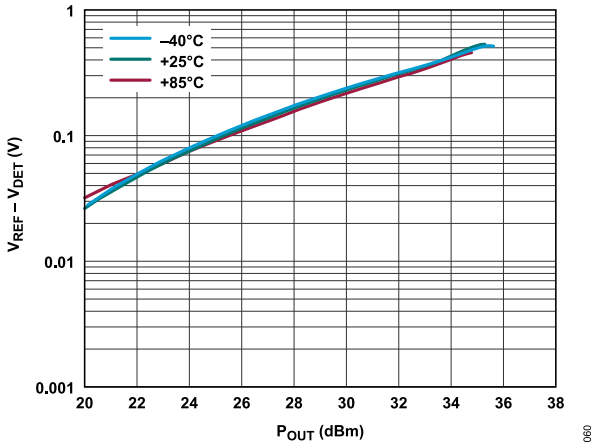



Figure 60. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 27GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

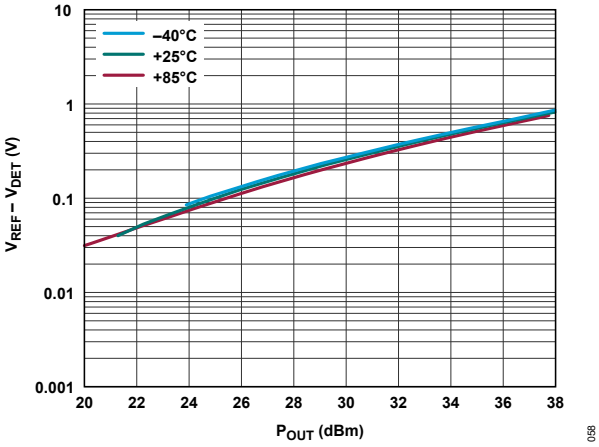



Figure 58. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 18GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

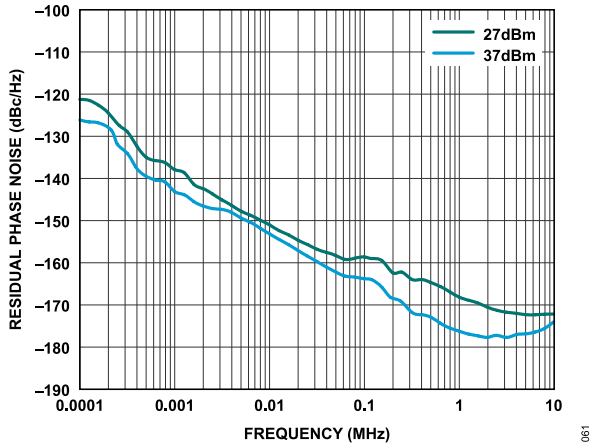



Figure 61. Residual Phase Noise vs. Frequency for Various $P_{OUT}$ Levels at 2GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

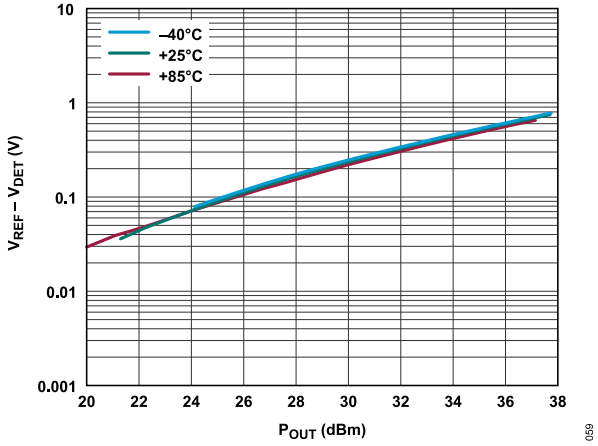



Figure 59. $V_{REF} - V_{DET}$ vs. $P_{OUT}$ for Various Temperature at 22GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

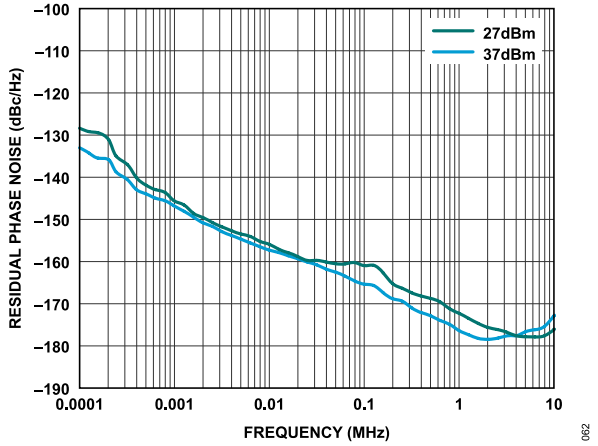



Figure 62. Residual Phase Noise vs. Frequency for Various $P_{OUT}$ Levels at 5GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA

## TYPICAL PERFORMANCE CHARACTERISTICS

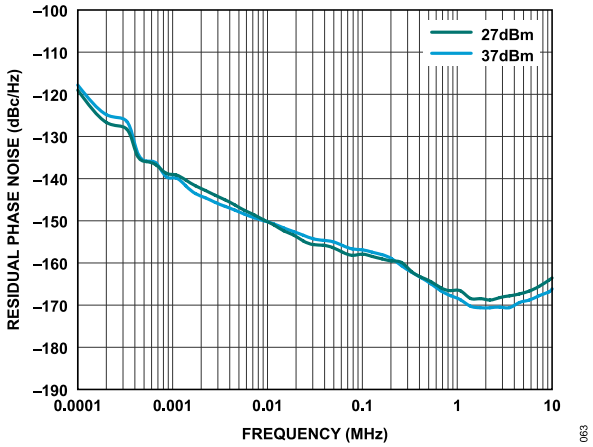



*Figure 63. Residual Phase Noise vs. Frequency for Various $P_{OUT}$ Levels at 15GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

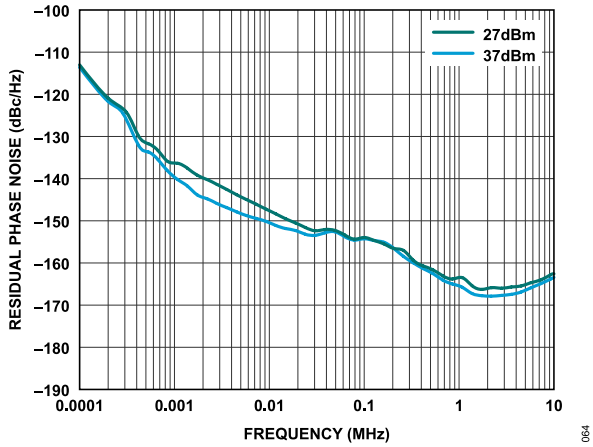



*Figure 64. Residual Phase Noise vs. Frequency for Various $P_{OUT}$ Levels at 20GHz, $V_{DD}$ = 20V, $I_{DQ}$ = 560mA*

## THEORY OF OPERATION

The ADPA9005 is a GaN power amplifier with cascaded gain stages that are biased by a positive drain bias voltage ($V_{DD}$) and an externally applied negative gate voltage ($V_{GG1}$). A nominal 20V is applied to the first and second stage drains (the VDD1 and VDD2 pins), and a negative voltage is applied to the VGG1 pin to set the total $I_{DQ}$ to 560mA nominal.

When biased as described, the ADPA9005 operates in Class AB, resulting in the maximum PAE at saturation. The ADPA9005 features integrated RF chokes for each drain plus on-chip DC blocking of the RFIN and RFOUT ports.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is DC biased, the diode rectifies the coupled RF output power and makes it available for measurement as a DC voltage at the VDET pin. To allow temperature compensation of the VDET pin, an identical and symmetrically located circuit without the coupled RF output power is available through the VREF pin. Taking the difference of $V_{REF} - V_{DET}$ provides a temperature-compensated signal that is proportional to the RF output power.

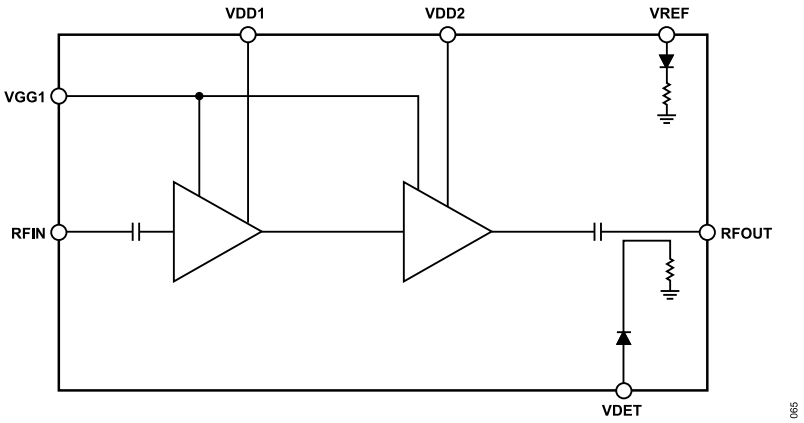



*Figure 65. Basic Block Diagram*

# APPLICATIONS INFORMATION

## Basic Connections

The basic connections to operate the ADPA9005 are shown in Figure 66. Decouple the VDD1, VDD2, and VGG1 pins as shown in Figure 66. The gate voltage for all stages (−3.0V to −1.0V for biased operation and −4.0V for pinch off) is applied to the VGG1 pin. A $V_{DD}$ of 20V nominal is applied to the VDD1 and VDD2 pins. Pin 1, Pin 3, and Pin 8 are designated as NIC pins. Although these NIC pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

To turn on the ADPA9005, take the following steps:

1. Connect the power supply grounds to GND.
2. Set VGG1 to −4V.
3. Set VDD1 and VDD2 to 20V.
4. Adjust VGG1 between −3V to −1V to achieve a $I_{DQ}$ of 560mA.
5. Apply the RF signal.

To turn off the ADPA9005, take the following steps:

1. Turn off the RF signal.
2. Set VGG1 to −4V to achieve an $I_{DQ}$ of 0mA.
3. Set VDD to 0V.
4. Increase VGG1 to 0V.

## Typical Application Circuit

Figure 66 shows the typical application circuit.

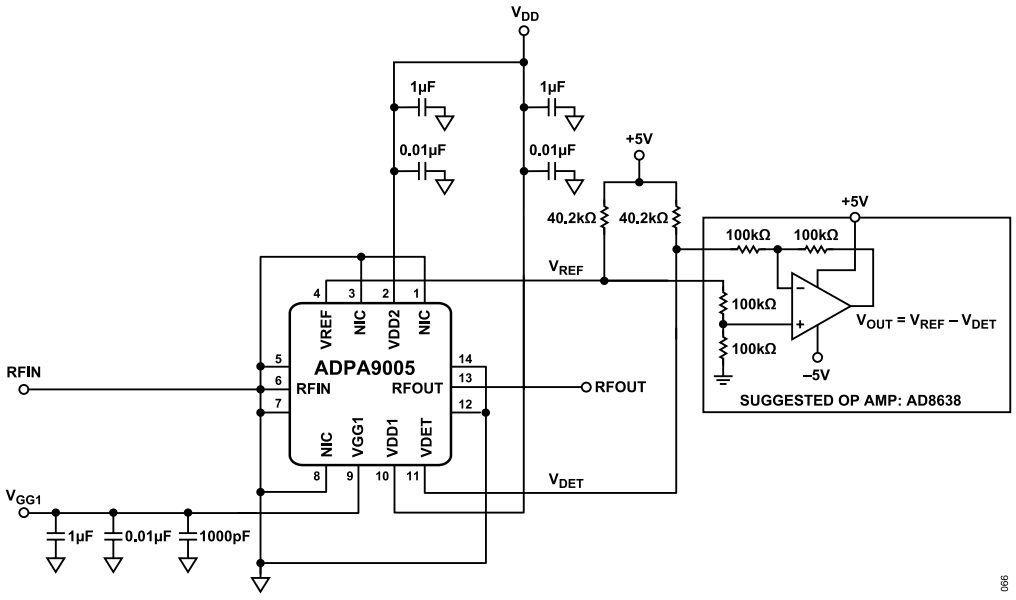



*Figure 66. Typical Application Circuit*

## OUTLINE DIMENSIONS

| PACKAGE DRAWING OPTION | PACKAGE TYPE | PACKAGE DESCRIPTION |
|---|---|---|
| EH-14-1 | LCC_HS | 14-Terminal, Ceramic, Leadless Chip Carrier with Heatsink |

For the latest package outline information and land patterns (footprints), go to **Package Index**.

## Ordering Guide

| MODEL[1] | TEMPERATURE RANGE | PACKAGE DESCRIPTION | PACKING QUANTITY | PACKAGE OPTION |
|---|---|---|---|---|
| ADPA9005AEHZ | −40°C to +85°C | 14-Terminal, Ceramic, Leadless Chip Carrier with Heatsink [LCC_HS] | Tape, 1 | EH-14-1 |
| ADPA9005AEHZ-R7 | −40°C to +85°C | 14-Terminal, Ceramic, Leadless Chip Carrier with Heatsink [LCC_HS] | Reel, 500 | EH-14-1 |

[1] Z = RoHS Compliant Part.

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