20 GHz to 54 GHz, GaAs, pHEMT, MMIC, 29 dBm (0.5 W) Power Amplifier

FEATURES
Output P1dB: 28.5 dBm typical at 24 GHz to 36 GHz
PSAT: 29 dBm typical at 24 GHz to 36 GHz
Gain: 19.5 dB typical at 24 GHz to 36 GHz
Input return loss: 17.5 dB typical at 24 GHz to 36 GHz
Output return loss: 22.0 dB typical at 24 GHz to 36 GHz
Output IP3: 35 dBm typical at 24 GHz to 36 GHz
Supply voltage: 5 V typical at 750 mA
50 Ω matched input and output
Die size: 2.750 mm × 1.845 mm × 0.102 mm

APPLICATIONS
Military and space
Test instrumentation
Satellite communications

GENERAL DESCRIPTION
The ADPA7009CHIP is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), 29 dBm saturated output power (0.5 W) distributed power amplifier that operates from 20 GHz to 54 GHz. The amplifier provides a gain of 19.5 dB, an output power for 1 dB compression (P1dB) of 28.5 dBm, and a typical output third-order intercept (IP3) of 35 dBm at 24 GHz to 36 GHz. The ADPA7009CHIP requires 750 mA from a 5 V supply voltage (VDD) and features inputs and outputs that are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the RFIN and RFOUT pads connected via one 0.076 mm (3 mil) ribbon bond of 0.076 mm (3 mil) minimal length.
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REVISION HISTORY

3/2021—Revision 0: Initial Version
SPECIFICATIONS

20 GHz TO 24 GHz FREQUENCY RANGE

$T_A = 25^\circ C$, supply voltage ($V_{DD}$) = 5 V, $I_{DQ} = 750$ mA, and 50 Ω matched input and output, unless otherwise noted. Adjust the gate voltage ($V_{GGx}$) from −1.5 V to 0 V to achieve $I_{DQ} = 750$ mA typical.

Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RANGE</td>
<td></td>
<td>20</td>
<td></td>
<td>24</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>14.5</td>
<td>17</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Flatness</td>
<td></td>
<td>±1.2</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td></td>
<td>0.033</td>
<td></td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>NOISE FIGURE</td>
<td></td>
<td>6.5</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>15.0</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td>20.0</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
<td>P1dB</td>
<td>25</td>
<td>27.5</td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>P_{SAT}</td>
<td>28.5</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>IP3</td>
<td>32</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_{DQ}$</td>
<td>750</td>
<td></td>
<td></td>
<td>mA</td>
<td>Adjust $V_{GGx}$ to achieve $I_{DQ} = 750$ mA typical</td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>3</td>
<td>5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

24 GHz TO 36 GHz FREQUENCY RANGE

$T_A = 25^\circ C$, $V_{DD} = 5$ V, $I_{DQ} = 750$ mA, and 50 Ω matched input and output, unless otherwise noted. Adjust $V_{GGx}$ from −1.5 V to 0 V to achieve $I_{DQ} = 750$ mA typical.

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RANGE</td>
<td></td>
<td>24</td>
<td>36</td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>17.0</td>
<td>19.5</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Flatness</td>
<td></td>
<td>±1.1</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td></td>
<td>0.023</td>
<td></td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>NOISE FIGURE</td>
<td></td>
<td>5.5</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>17.5</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td>22.0</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
<td>P1dB</td>
<td>26</td>
<td>28.5</td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>P_{SAT}</td>
<td>29</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>IP3</td>
<td>35</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_{DQ}$</td>
<td>750</td>
<td></td>
<td></td>
<td>mA</td>
<td>Adjust $V_{GGx}$ to achieve $I_{DQ} = 750$ mA typical</td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>3</td>
<td>5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### 36 GHz TO 50 GHz FREQUENCY RANGE

$T_A = 25^\circ C$, $V_{DD} = 5\, V$, $I_{DQ} = 750\, mA$, and 50 $\Omega$ matched input and output, unless otherwise noted. Adjust $V_{GGx}$ from $-1.5$ V to 0 V to achieve $I_{DQ} = 750\, mA$ typical.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RANGE</td>
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<td>36</td>
<td>36</td>
<td>50</td>
<td>50</td>
<td>GHz</td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>17.5</td>
<td>20.0</td>
<td>20.0</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Flatness</td>
<td></td>
<td>$\pm1.1$</td>
<td></td>
<td></td>
<td>dB</td>
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<tr>
<td>Gain Variation Over Temperature</td>
<td></td>
<td>0.026</td>
<td></td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>NOISE FIGURE</td>
<td></td>
<td>6.0</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
<td>$P_{1dB}$</td>
<td>22</td>
<td>25</td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>$P_{SAT}$</td>
<td>27.0</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>$IP3$</td>
<td>34.5</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_{DQ}$</td>
<td></td>
<td>750</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>3</td>
<td>5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### 50 GHz TO 54 GHz FREQUENCY RANGE

$T_A = 25^\circ C$, $V_{DD} = 5\, V$, $I_{DQ} = 750\, mA$, and 50 $\Omega$ matched input and output, unless otherwise noted. Adjust $V_{GGx}$ from $-1.5$ V to 0 V to achieve $I_{DQ} = 750\, mA$ typical.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
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<tbody>
<tr>
<td>FREQUENCY RANGE</td>
<td></td>
<td>50</td>
<td>50</td>
<td>54</td>
<td>54</td>
<td>GHz</td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>20.5</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
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<td>$\pm0.85$</td>
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<td></td>
<td></td>
<td>dB</td>
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<tr>
<td>Gain Variation Over Temperature</td>
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<td>0.027</td>
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<td></td>
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<td>dB/°C</td>
</tr>
<tr>
<td>NOISE FIGURE</td>
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<td>6.0</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>16.5</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
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<tr>
<td>Output</td>
<td></td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>OUTPUT</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
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<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>$P_{SAT}$</td>
<td>26.0</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>$IP3$</td>
<td>33</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_{DQ}$</td>
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<td>750</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>3</td>
<td>5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Adjust $V_{GGx}$ to achieve $I_{DQ} = 750\, mA$ typical.
ABSOLUTE MAXIMUM RATINGS

Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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</thead>
<tbody>
<tr>
<td>Drain Bias Voltage (VDDx)</td>
<td>6.0 V</td>
</tr>
<tr>
<td>VGGx</td>
<td>−1.6 V to 0 V</td>
</tr>
<tr>
<td>RF Input Power (RFIN)</td>
<td>20 dBm</td>
</tr>
<tr>
<td>Continuous Power Dissipation (PCONT),</td>
<td>7.7 W</td>
</tr>
<tr>
<td>Tja = 85°C (Derate 85 mW/°C Above 85°C)</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature to Maintain</td>
<td>175°C</td>
</tr>
<tr>
<td>1,000,000 Hour Mean Time to Failure (MTTF)</td>
<td></td>
</tr>
<tr>
<td>Nominal Junction Temperature (TJ = 85°C,</td>
<td>129°C</td>
</tr>
<tr>
<td>VDD = 5 V, Iq = 750 mA)</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td></td>
</tr>
<tr>
<td>Storage</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating</td>
<td>−55°C to +85°C</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the carrier or substrate on which the die is mounted. Careful attention is needed with each material used in the thermal path below the IC.

θjc is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 6. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θjc</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-10-13</td>
<td>11.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA7009CHIP

Table 7. ADPA7009CHIP, 10-Pad Die

<table>
<thead>
<tr>
<th>ESD Model</th>
<th>Withstand Threshold (V)</th>
<th>Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBM</td>
<td>±500</td>
<td>1B</td>
</tr>
</tbody>
</table>

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RFIN</td>
<td>RF Signal Input. This pad is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.</td>
</tr>
<tr>
<td>2, 10</td>
<td>VGG1, VGG2</td>
<td>Amplifier Gate Controls. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required for these pads. Adjust VGGx from −1.5 V to 0 V to achieve the desired quiescent current. See Figure 7 for the interface schematic.</td>
</tr>
<tr>
<td>3, 4, 8, 9</td>
<td>VDD1, VDD2, VDD3, VDD4</td>
<td>Drain Biases for the Amplifier. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required for these pads. See Figure 9 for the interface schematic.</td>
</tr>
<tr>
<td>5</td>
<td>VREF</td>
<td>Reference Diode Voltage. Use this pad for temperature compensation of the VDET RF output power measurements. Used in combination with VDET, this voltage provides temperature compensation to the VDET RF output power measurements. See Figure 4 for the interface schematic.</td>
</tr>
<tr>
<td>6</td>
<td>RFOUT</td>
<td>RF Signal Output. This pad is ac-coupled and matched to 50 Ω. See Figure 8 for the interface schematic.</td>
</tr>
<tr>
<td>7</td>
<td>VDET</td>
<td>Detector Diode Used for Measuring the RF Output Power. Detection via this pad requires the application of a dc bias voltage through an external series resistor. Used in combination with VREF, the difference detector voltage, VREF − VDET, is a temperature compensated dc voltage proportional to the RF output power. See Figure 5 for the interface schematic.</td>
</tr>
<tr>
<td>Die Bottom</td>
<td>GND</td>
<td>Ground. The die bottom must be connected to RF and dc ground. See Figure 3 for the interface schematic.</td>
</tr>
</tbody>
</table>
INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

Figure 4. VREF Interface Schematic

Figure 5. VDET Interface Schematic

Figure 6. RFIN Interface Schematic

Figure 7. VGG1, VGG2 Interface Schematic

Figure 8. RFOUT Interface Schematic

Figure 9. VDD1 to VDD4 Interface Schematic
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 10. Gain and Return Loss vs. Frequency, $V_{DD} = 5\ V$, $I_{Q} = 750\ mA$

Figure 11. Gain vs. Frequency for Various Supply Voltages, $I_{Q} = 750\ mA$

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, $V_{DD} = 5\ V$, $I_{Q} = 750\ mA$

Figure 13. Gain vs. Frequency for Various Temperatures, $V_{DD} = 5\ V$, $I_{Q} = 750\ mA$

Figure 14. Gain vs. Frequency for Various $I_{Q}$ Currents, $V_{DD} = 5\ V$

Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, $I_{Q} = 750\ mA$
Figure 16. Input Return Loss vs. Frequency for Various IOQ Currents, $V_{DD} = 5$ V

Figure 17. Output Return Loss vs. Frequency for Various Supply Voltages, $I_{OQ} = 750$ mA

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, $V_{DD} = 5$ V, $I_{OQ} = 750$ mA

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, $V_{DD} = 5$, $I_{OQ} = 750$ mA

Figure 20. Output Return Loss vs. Frequency for Various $I_{OQ}$ Currents, $V_{DD} = 5$ V

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Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 44 GHz, V_{DD} = 5 V, I_{DDQ} = 750 mA

Figure 36. P_{Diss} vs. Input Power for Various Frequencies at T_{A} = 85°C, V_{DD} = 5 V, I_{DDQ} = 750 mA

Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 40 GHz, V_{DD} = 5 V, I_{DDQ} = 750 mA

Figure 38. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 50 GHz, V_{DD} = 5 V, I_{DDQ} = 750 mA

Figure 39. Output IP3 vs. Frequency at −20°C, −40°C, and −55°C, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DDQ} = 750 mA
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P_{out per Tone} = 14 dBm, V_{DD} = 5 V, I_{DQ} = 750 mA

Figure 41. Output IP3 vs. Frequency for Various I_{DQ} Currents,
P_{out per Tone} = 14 dBm, V_{DD} = 5 V

Figure 42. Third-Order Intermodulation Distortion (IM3) vs. P_{out per Tone},
V_{DD} = 4 V, I_{DQ} = 750 mA

Figure 43. Drain Supply Current vs. Input Power at Various Frequencies,
V_{DD} = 5 V, I_{DQ} = 750 mA

Figure 44. Output IP3 vs. Frequency for Various Supply Voltages,
P_{out per Tone} = 14 dBm, I_{DQ} = 750 mA

Figure 45. IM3 vs. P_{out per Tone}, V_{DD} = 5 V, I_{DQ} = 750 mA
Figure 46. Drain Supply Current vs. Input Power at Various Temperature, 36 GHz, VDD = 5 V, IDV = 750 mA

Figure 47. Drain Supply Current vs. Gate Voltage at Various Temperature

Figure 48. Detector Voltage (VREF – VDET) vs. Output Power for Various Temperatures at 36 GHz

Figure 49. Detector Voltage (VREF – VDET) vs. Output Power for Various Frequencies

Figure 50. Detector Voltage (VREF – VDET) vs. Frequency for Various Output Powers
LOWER BIAS OPERATION

Figure 51. Gain vs. Frequency for Various $I_{DD}$ Currents, $V_{DD} = 3 \, V$

Figure 52. Input Return Loss vs. Frequency for Various $I_{DD}$ Currents, $V_{DD} = 3 \, V$

Figure 53. Output Return Loss vs. Frequency for Various $I_{DD}$ Currents, $V_{DD} = 3 \, V$

Figure 54. Gain vs. Frequency for Various $I_{DD}$ Currents, $V_{DD} = 4 \, V$

Figure 55. Input Return Loss vs. Frequency for Various $I_{DD}$ Currents, $V_{DD} = 4 \, V$

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**Figure 57.** Output $P_{1dB}$ vs. Frequency for Various $I_{DQ}$ Currents, $V_{DD} = 3\, \text{V}$

**Figure 58.** $P_{SAT}$ vs. Frequency for Various $I_{DQ}$ Currents, $V_{DD} = 3\, \text{V}$

**Figure 59.** Noise Figure vs. Frequency for Various $I_{DQ}$ Currents, $V_{DD} = 3\, \text{V}$

**Figure 60.** Output $P_{1dB}$ vs. Frequency for Various $I_{DQ}$ Currents, $V_{DD} = 4\, \text{V}$

**Figure 61.** $P_{SAT}$ vs. Frequency for Various $I_{DQ}$ Currents, $V_{DD} = 4\, \text{V}$

**Figure 62.** Noise Figure vs. Frequency for Various $I_{DQ}$ Currents, $V_{DD} = 4\, \text{V}$
Figure 63. Output IP3 vs. Frequency for Various IQ0 Currents, P_{out} per Tone = 14 dBm, V_{DD} = 3 V

Figure 64. Output IP3 vs. Frequency for Various IQ0 Currents, P_{out} per Tone = 14 dBm, V_{DD} = 4 V
THEORY OF OPERATION

The architecture of the ADPA7009CHIP, a medium power amplifier, is shown in Figure 65. The ADPA7009CHIP uses a cascaded, four-stage amplifier operating in quadrature between two 90° hybrids.

The input signal is divided evenly in two. Each path is amplified through four independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 19.5 dB and a $P_{\text{SAT}}$ value of 29 dBm. The gate pins are internally connected and can be biased from either north or south of the circuit.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output (see Figure 65).

![Figure 65. ADPA7009CHIP Architecture](image-url)
The ADPA7009CHIP is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for all primary and alternate VGGx and VDDx pads. VGG1 and VGG2 are the gate bias pads for the amplifier. VDD1, VDD2, VDD3, and VDD4 are the drain bias pads for the amplifier.

All measurements for this device were taken using the primary application circuit (see Figure 66) and were configured as shown in the assembly diagram (see Figure 79).

The recommended bias sequence during power-up is as follows:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, VGG1 and VGG2, to −1.5 V.
3. Set all the drain bias voltages, VDDx, to 5 V.
4. Increase the gate bias voltages, VGG1 and VGG2, to achieve an IDQ of 750 mA.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the primary gate bias voltages, VGG1 and VGG2, to −1.5 V to achieve IDQ = 0 mA (approximately).
3. Decrease all the drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

The VDD = 5 V and IDQ = 750 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7009CHIP at different bias conditions may provide performance that differs from what is shown in Table 1 to Table 4. Biasing the ADPA7009CHIP for higher drain current typically results in higher P1dB and gain at the expense of increased power consumption (see Table 9).

**TYPICAL APPLICATION CIRCUIT**

Figure 66 shows the primary application circuit. Figure 67 shows the alternate typical application circuit.

### Table 9. Power Selection Table

<table>
<thead>
<tr>
<th>I_{DQ} (mA)</th>
<th>Gain (dB)</th>
<th>P1\text{dB} (dBm)</th>
<th>Output IP3 (dBm)</th>
<th>P_{\text{DSS}} (W) at P_{\text{SAT}}</th>
<th>V_{\text{GQX}} (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>650</td>
<td>20.33</td>
<td>27.57</td>
<td>37.07</td>
<td>3.25</td>
<td>−0.68</td>
</tr>
<tr>
<td>750</td>
<td>21.02</td>
<td>27.93</td>
<td>34.83</td>
<td>3.75</td>
<td>−0.63</td>
</tr>
<tr>
<td>850</td>
<td>21.52</td>
<td>28.17</td>
<td>32.69</td>
<td>4.25</td>
<td>−0.59</td>
</tr>
<tr>
<td>950</td>
<td>22.02</td>
<td>28.34</td>
<td>31.19</td>
<td>4.75</td>
<td>−0.54</td>
</tr>
</tbody>
</table>

1. Data taken at the following nominal bias conditions: VDD = 5 V, T_a = 25°C, and frequency = 36 GHz.
2. Adjust V_{GQX} from −1.5 V to 0 V to achieve the desired drain current.
Figure 67. Alternate Application Circuit
BIASING THE ADPA7009CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers such as the ADPA7009CHIP. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self-protection in the event of a short circuit, an internal charge pump that generates the negative voltage needed on the gate of the ADPA7008CHIP, and the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-Die.

APPLICATION CIRCUIT SETUP

Figure 69 shows an application circuit using the HMC980LP4E to control the ADPA7009CHIP. When using an external negative supply for VNEG, refer to the application circuit shown in Figure 70.

In the application circuit shown in Figure 69, the ADPA7009CHIP drain voltage, $V_{DRAIN}$, and drain current, $I_{DRAIN}$, are set by the following equations:

$$V_{DD} = V_{DRAIN} + (I_{DRAIN} \times 0.85 \, \Omega) \quad (1)$$

$$V_{DD} = 5 \, V + (0.85 \, A \times 0.85 \, \Omega) = 5.72 \, V$$

where:

- $V_{DD}$ and $V_{DRAIN}$ are in volts.
- $I_{DRAIN}$ is in amperes.

$$R10 = (150 \, \Omega \times A) + (I_{DRAIN}) \quad (2)$$

$$R10 = (150 \, \Omega \times A) + (0.85 \, A) = 176 \, \Omega$$

where:

- $R10$ is in ohms.
- $I_{DRAIN}$ is in amperes.

LIMITING VGATE FOR THE ADPA7009CHIP $V_{GGx}$ ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7009CHIP, the minimum voltages for VNEG and VGATE must be $-1.5 \, V$ to keep the voltages within the absolute maximum rating limit for the $V_{GGx}$ pad of the ADPA7009CHIP. To set the minimum voltages, set R15 and R16 to the values shown in Figure 69 and Figure 70. Refer to the AN-1363 Application Note for more information and calculations for R15 and R16.

The HMC980LP4E application circuits for biasing figures in the AN-1363 are two examples of how the HMC980LP4E is used as an active bias controller. Both application circuits within the AN-1363 show the R5 and R7 resistors, which are analogous to the R15 and R16 resistor shown in Figure 69 and Figure 70.
Figure 69. Application Circuit Using the HMC980LP4E with the ADPA7009CHIP (Internal Negative Voltage Source)

Figure 70. Application Circuit Using the HMC980LP4E with the ADPA7009CHIP (External Negative Voltage Source)
HMC980LP4E BIAS SEQUENCE

The dc supply sequence described in this section is required to prevent damage to the HMC980LP4E when using the device to control the ADPA7009CHIP.

Power-Up Sequence

The power-up sequence for the HMC980LP4E is as follows:

1. Set VDIG = 3.3 V.
2. Set S0 = 3.3 V.
3. Set VDD = 5.72 V.
4. Set VNEG = −1.5 V (this step is unnecessary if using an internally generated voltage).
5. Set EN = 3.3 V (the transition from 0 V to 3.3 V turns on VGATE and VDRAIN).

Power-Down Sequence

The power-down sequence for the HMC980LP4E is as follows:

1. Set EN = 0 V (the transition from 3.3 V to 0 V turns off VDRAIN and VGATE).
2. Set VNEG = 0 V (this step is unnecessary if using and internally generated voltage).
3. Set VDD = 0 V.
4. Set S0 = 0 V.
5. Set VDIG = 0 V.

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7009CHIP on or off by applying 3.3 V or 0 V, respectively, to the EN pad. At EN = +3.3 V, VGATE drops to −1.5 V, and VDRAIN turns on at +5 V. VGATE then rises until IDRAIN = 850 mA, and the closed control loop regulates IDRAIN at 850 mA. When EN = 0 V, VDRAIN is set to −1.5 V, and VDRAIN is set to 0 V.

CONSTANT DRAIN CURRENT BIASING vs. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses closed-loop feedback to continuously adjust VGATE to maintain a constant drain current bias over dc supply variation, temperature, and device to device variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. By comparing the constant drain current bias with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower output P1dB is seen with a constant drain current bias. This output P1dB is shown in Figure 78, where the RF performance is slightly lower than the constant gate voltage bias operation due to a lower drain current at the high input powers as the device reaches 1 dB compression.

To increase the output P1dB performance for the constant drain current bias toward the constant gate voltage bias performance, increase the set current toward the IDD value this performance reaches under the RF drive in the constant gate voltage bias condition, as shown in Figure 78. The limit of increasing IDD under the constant drain current operation is set by the thermal limitations found in Table 5 with the maximum power dissipation specification. As the IDD increase continues, the actual output P1dB does not continue to increase indefinitely and the power dissipation increases. Therefore, when using constant drain current biasing, take the trade-off between the power dissipation and the output P1dB performance into consideration.
CONSTANT $I_{DD}$ OPERATION

$T_A = 25^\circ C$, $V_{DD} = 5\, V$, $I_{DD} = 850\, mA$ for nominal operation, unless otherwise noted. Figure 71 to Figure 78 are biased with the HMC980LP4E active bias controller. See the Biasing the ADPA7009CHIP with the HMC980LP4E section for biasing details.

**Figure 71.** $P_{1dB}$ vs. Frequency for Various Temperatures, $V_{DD} = 5\, V$, Data Measured with Constant $I_{DD}$

**Figure 72.** $P_{SAT}$ vs. Frequency for Various Temperatures, $V_{DD} = 5\, V$, Data Measured with Constant $I_{DD}$

**Figure 73.** $P_{1dB}$ vs. Frequency for Various Drain Currents, $V_{DD} = 5\, V$, Data Measured with Constant $I_{DD}$

**Figure 74.** $P_{SAT}$ vs. Frequency for Various Drain Currents, $V_{DD} = 5\, V$, Data Measured with Constant $I_{DD}$

**Figure 75.** $I_{DD}$ vs. Input Power, $V_{DD} = 5\, V$, Frequency = 36\, GHz, Constant Drain Current Bias ($I_{DRAIN}$ Setpoint = 850\, mA) and Constant Gate Voltage Bias ($V_{GGX} = -0.63\, V$)

**Figure 76.** PAE vs. Input Power, $V_{DD} = 5\, V$, Frequency = 36\, GHz, Constant Drain Current Bias ($I_{DRAIN}$ Setpoint = 850\, mA) and Constant Gate Voltage Bias ($V_{GGX} = -0.63\, V$)
Figure 77. $P_{\text{OUT}}$ vs. Input Power, $V_{DD} = 5 \, \text{V}$, Frequency $= 36 \, \text{GHz}$, Constant Drain Current Bias ($I_{\text{DRAIN}}$ Setpoint $= 850 \, \text{mA}$) and Constant Gate Voltage Bias ($V_{\text{GGx}} \approx -0.63 \, \text{V}$)

Figure 78. $P_{1\text{dB}}$ vs. Frequency, $V_{DD} = 5 \, \text{V}$, Constant Drain Current Bias ($I_{\text{DRAIN}}$ Setpoint $= 850 \, \text{mA}$) and Constant Gate Voltage Bias ($V_{\text{GGx}} \approx -0.63 \, \text{V}$)
Figure 79 shows the assembly diagram for the ADPA7009CHIP.

Figure 79. Assembly Diagram with Bias Control on North Side of Die
MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either wafer- or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chips using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

MOUNTING

Before the epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

WIRE BONDING

RF bonds made with 0.076 mm × 0.0127 mm (3 mil × 0.5 mil) gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Thermosonically bonded dc bonds of 0.025 mm (1 mil) diameter are recommended. Create ball bonds with a force of 40 g to 50 g, and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31 mm (12.2 mil).

Alternatively, use short RF bonds that are ≤3 mm and made with two 1 mm wires.
OUTLINE DIMENSIONS

Figure 82. 10-Pad Bare Die [CHIP]
(C-10-13)
Dimensions shown in millimeter

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
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<td>ADPA7009CHIP</td>
<td>−55°C to +85°C</td>
<td>10-Pad Bare Die [CHIP]</td>
<td>C-10-13</td>
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<tr>
<td>ADPA7009C-KIT</td>
<td>−55°C to +85°C</td>
<td>10-Pad Bare Die [CHIP]</td>
<td>C-10-13</td>
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</tbody>
</table>

1 The ADPA7009CHIP and ADPA7009C-KIT are RoHS compliant parts.
2 Die inspected to meet MIL-STD-883 Method 2010, Condition B.