4.5W (36.5dBm), 8GHz to 12GHz, GaN Power Amplifier

FEATURES

- Internally matched and AC-coupled, 4.5W, GaN power amplifier
- Integrated temperature-compensated RF power detector
- P_{OUT}: 36.5dBm typical with P_{IN} = 1dBm from 9.5GHz to 11.5GHz
- Small signal gain: 38.5dB typical from 9.5GHz to 11.5GHz
- Power gain: 35.5dB typical with P_{IN} = 1dBm from 9.5GHz to 11.5GHz
- PAE: 47% typical with P_{IN} = 1dBm from 9.5GHz to 11.5GHz
- Supply voltage: 20V at 50mA on 10% duty cycle
- 32-lead, 5mm × 5mm, LFCSP

APPLICATIONS

- Weather radars
- Marine radars
- Military radars

GENERAL DESCRIPTION

The ADPA1120 is a 8GHz to 12GHz power amplifier with a saturated output power (P_{OUT}) of 36.5dBm, power added efficiency (PAE) of 47%, and a power gain of 35.5dB typical from 9.5GHz to 11.5GHz at an input power (P_{IN}) of 1dBm. The RF input and RF output are internally matched and AC-coupled. A drain bias voltage of 20V is applied to the VDD1-2, VDD3, and VDD4 pins. The drain current is set by applying a negative voltage to the VGG1-2 pin.

The ADPA1120 is fabricated on a gallium nitride (GaN) process, is housed in a 32-lead, 5mm × 5mm lead frame chip scale package [LFCSP] and is specified for operation from −40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM

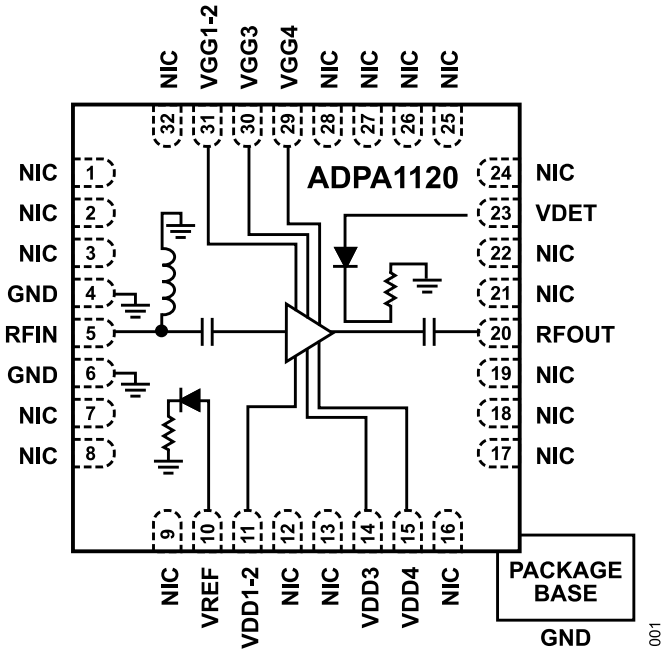

Figure 1. Functional Block Diagram

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REVISION HISTORY

10/2025—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_{CASE} = 25°C, supply current (V_{DD}) = 20V, quiescent current (I_{DQ}) = 50mA, pulse width = 100µs, 10% duty cycle, and frequency range = 8GHz to 9.5GHz, unless otherwise noted.

Table 1. 8GHz to 9.5GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8		9.5	GHz	
GAIN					
Small Signal Gain (S21)		39		dB	
Gain Flatness		±1.37		dB	
RETURN LOSS					
Input (S11)		15		dB	
Output (S22)		20		dB	
POWER					
P_{OUT}	34.5	36.5		dBm	P_{IN} = 1dBm
Gain	33.5	35.5		dB	P_{IN} = 1dBm
PAE		50		%	P_{IN} = 1dBm
I_{DQ}		50		mA	Adjust the gate control voltage (V_{GG1}) between −3V and −1V to achieve an I_{DQ} = 50mA, V_{GG1} = −2.0V typical to achieve I_{DQ} = 50mA

T_{CASE} = 25°C, V_{DD} = 20V, I_{DQ} = 50mA, pulse width = 100µs, 10% duty cycle, and frequency range = 9.5GHz to 11.5GHz, unless otherwise noted.

Table 2. 9.5GHz to 11.5GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	9.5		11.5	GHz	
GAIN					
S21		38.5		dB	
Gain Flatness		±1.13		dB	
RETURN LOSS					
S11		15		dB	
S22		11		dB	
POWER					
P_{OUT}	34.5	36.5		dBm	P_{IN} = 1dBm
Gain	33.5	35.5		dB	P_{IN} = 1dBm
PAE		47		%	P_{IN} = 1dBm
I_{DQ}		50		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 50mA, V_{GG1} = −2.0V typical to achieve I_{DQ} = 50mA

SPECIFICATIONS

T_{CASE} = 25°C, V_{DD} = 20V, I_{DQ} = 50mA, pulse width = 100µs, 10% duty cycle, and frequency range = 11.5GHz to 12GHz, unless otherwise noted.

Table 3. 11.5GHz to 12GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	11.5		12	GHz	
GAIN					
S21		35.5		dB	
Gain Flatness		±2.33		dB	
RETURN LOSS					
S11		11		dB	
S22		12		dB	
POWER					
P_{OUT}		34.5		dBm	P_{IN} = 1dBm
Gain		33.5		dB	P_{IN} = 1dBm
PAE		42		%	P_{IN} = 1dBm
I_{DQ}		50		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 50mA, V_{GG1} = −2.0V typical to achieve I_{DQ} = 50mA

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Bias Voltage	
Drain (VDD1-2, VDD3, and VDD4)	35V DC
Gate (VGG1-2, VGG3, and VGG4)	−8V DC to 0V DC
Continuous Wave RF Input Power (RFIN)	12dBm
Maximum Power Dissipation, P_{DISS}	
Drain Bias Pulse Width = 100µs at 10% Duty Cycle, T_{CASE} = 85°C	17W
Continuous Drain Bias, T_{CASE} = 85°C	14W
Temperature	
Maximum Channel	225°C
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type[1, 2]	Pulsed 10% Duty Cycle, 100µs Pulse Width, θ_{JC}	Continuous Wave θ_{JC}	Unit
CP-32-13	8.20	10	°C/W

1 θ_{JC} was determined under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

2 Drain bias pulse width = 100µs at 10% duty cycle.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1120

Table 6. ADPA1120, 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	200	0B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

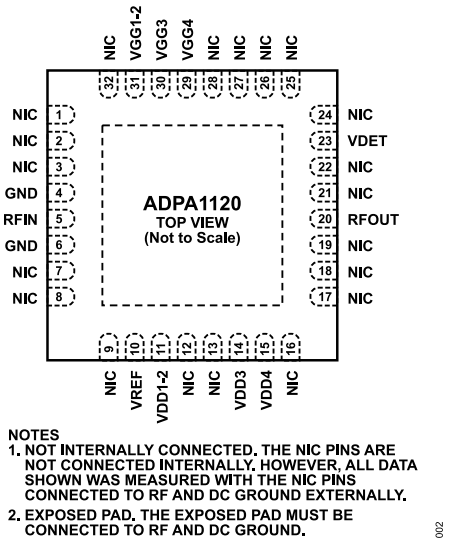

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 3, 7 to 9, 12, 13, 16 to 19, 21, 22, 24 to 28, 32	NIC	Not Internally Connected. The NIC pins are not connected internally. However, all data shown was measured with the NIC pins connected to RF and DC ground externally.
4, 6	GND	Ground. The GND pins must be connected to RF and DC ground. See Figure 3 for the interface schematic.
5	RFIN	RF Input. The RFIN pin is AC-coupled in the signal path and is matched to 50Ω. See Figure 4 for the interface schematic. If the RFIN pin is externally connected to a DC bias level other than 0 V, AC-couple the RFIN pin externally because of the internal DC path to ground.
10	VREF	Reference Diode for Temperature Compensation of VDET RF P_{OUT} Measurements. See Figure 8 for the interface schematic.
11, 14, 15	VDD1-2, VDD3, VDD4	Drain Bias Voltages. First, second, third and fourth stage drain bias. See Figure 7 for the interface schematic.
20	RFOUT	RF Output. The RFOUT pin is AC-coupled and is matched to 50Ω. See Figure 6 for the interface schematic.
23	VDET	Detector Diode to Measure RF P_{OUT}. P_{OUT} detection via the VDET pin requires the application of a DC bias voltage through an external series resistor. Used in combination with the VREF pin, the difference voltage (VREF voltage (V_{REF}) − VDET voltage (V_{DET})) is a temperature compensated DC voltage that is proportional to the RF P_{OUT}. See Figure 8 for the interface schematic.
29, 30, 31	VGG4, VGG3, VGG1-2	Gate Bias Voltages. First, second, third and fourth stage gate bias. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

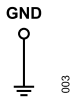

Figure 3. GND Interface Schematic

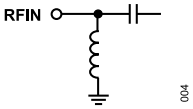

Figure 4. RFIN Interface Schematic

Figure 5. VGG1-2, VGG3, VGG4 Interface Schematic

Figure 6. RFOUT Interface Schematic

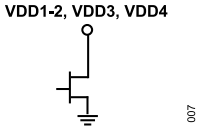

Figure 7. VDD1-2, VDD3, VDD4

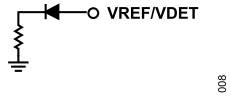

Figure 8. VREF/VDET Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 20V, I_{DQ} = 50mA, V_{DD} is pulsed at 10% duty cycle, 100µs pulse width, and T_{CASE} = 25°C, unless otherwise noted.

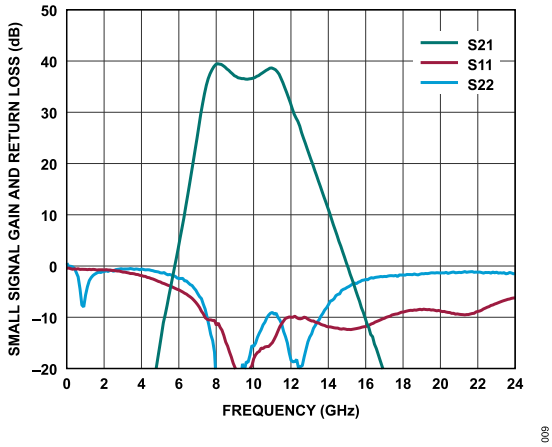

Figure 9. Small Signal Gain and Return Loss vs. Frequency

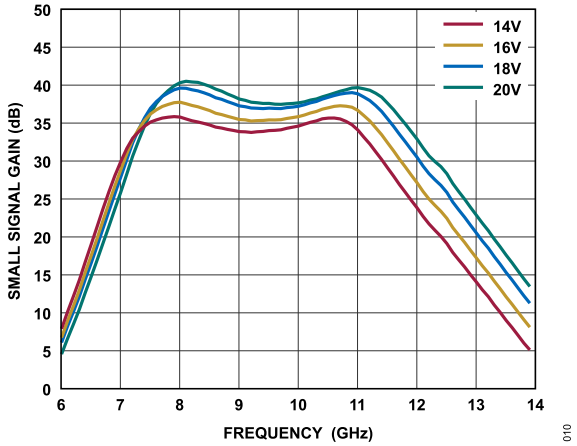

Figure 10. Small Signal Gain vs. Frequency for Various Supply Voltages

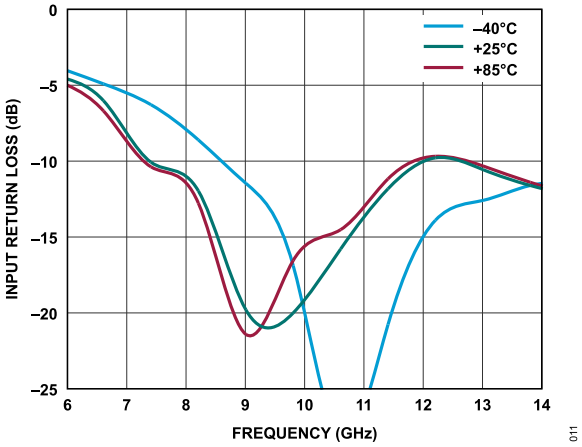

Figure 11. Input Return Loss vs. Frequency for Various Temperatures

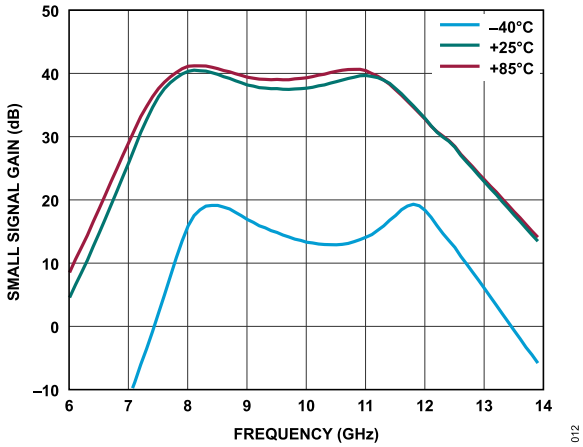

Figure 12. Small Signal Gain vs. Frequency for Various Temperatures, Small Signal Gain Varies by ±6dB, −40°C Behavior Expected, See Figure 46

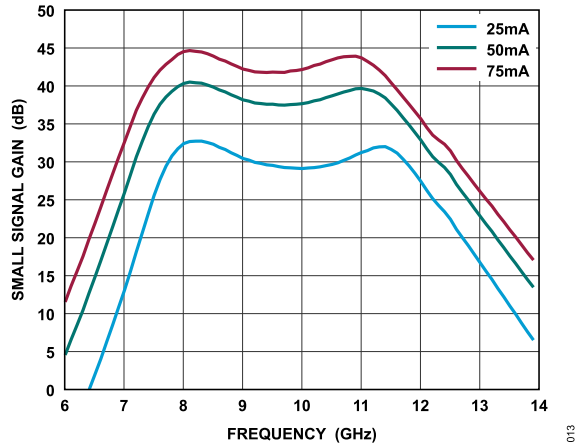

Figure 13. Small Signal Gain vs. Frequency for Various Supply Currents

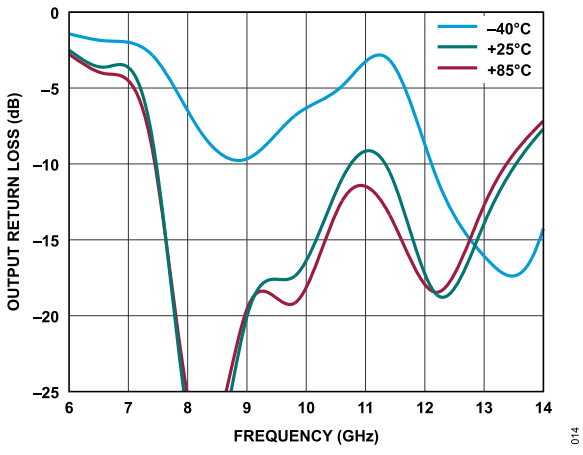

Figure 14. Output Return Loss vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

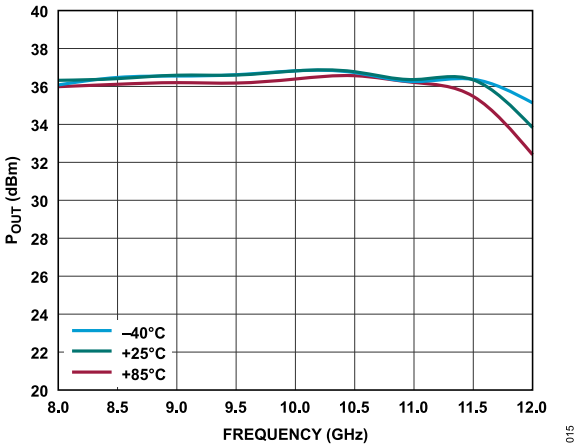

Figure 15. P_{OUT} at P_{IN} = 1dBm vs. Frequency for Various Temperatures

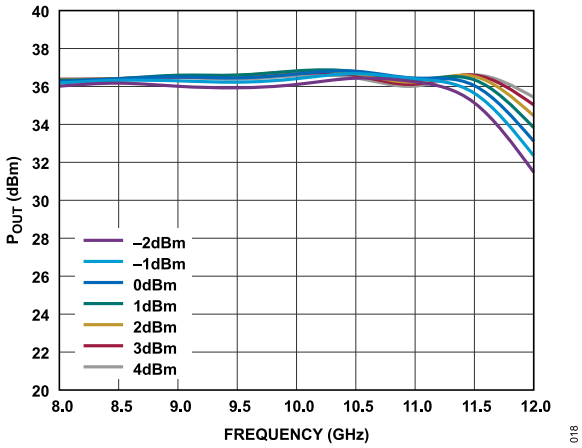

Figure 18. P_{OUT} vs. Frequency at Various P_{IN} Values

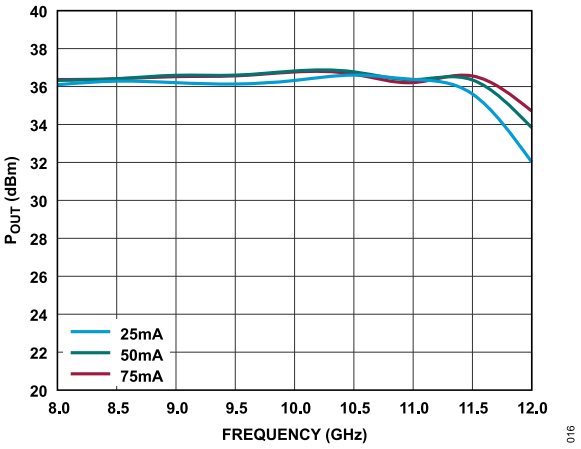

Figure 16. P_{OUT} at P_{IN} = 1dBm vs. Frequency for Various Supply Currents

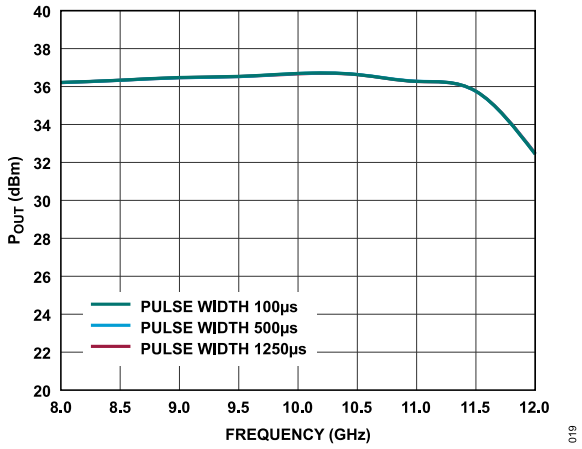

Figure 19. P_{OUT} at P_{IN} = 1dBm vs. Frequency for Various Pulse Widths at 10% Duty Cycle

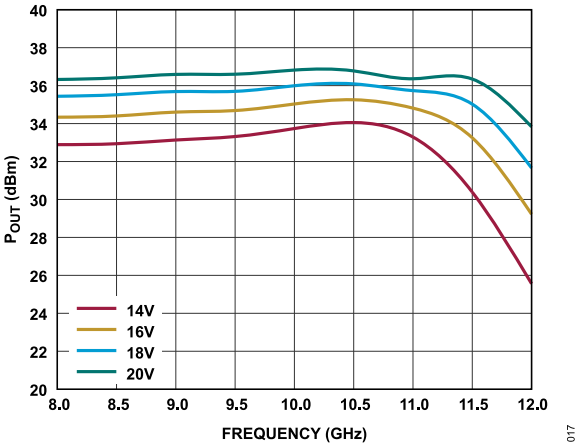

Figure 17. P_{OUT} at P_{IN} = 1dBm vs. Frequency for Various Supply Voltages

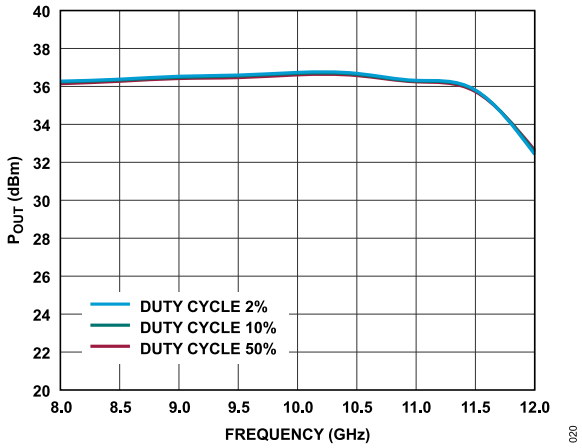

Figure 20. P_{OUT} at P_{IN} = 1dBm vs. Frequency for Various Duty Cycles at 100µs Pulse Width

TYPICAL PERFORMANCE CHARACTERISTICS

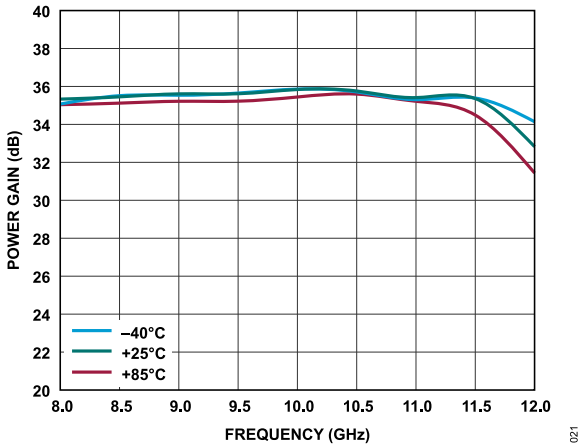

Figure 21. Power Gain at P_{IN} = 1dBm vs. Frequency for Various Temperatures

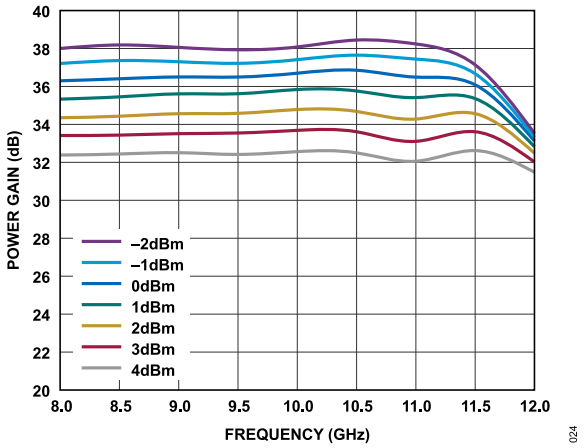

Figure 24. Power Gain vs. Frequency at Various P_{IN} Values

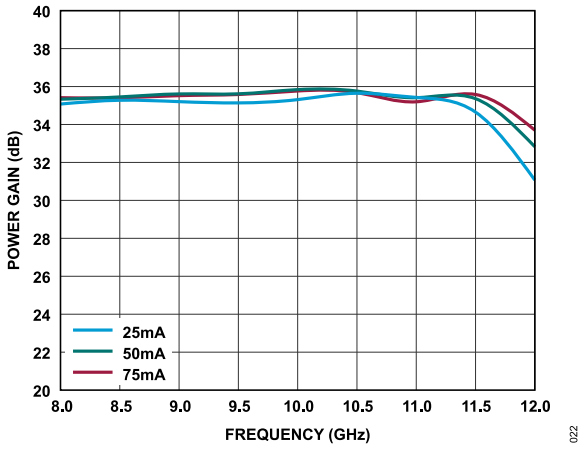

Figure 22. Power Gain at P_{IN} = 1dBm vs. Frequency for Various Supply Currents

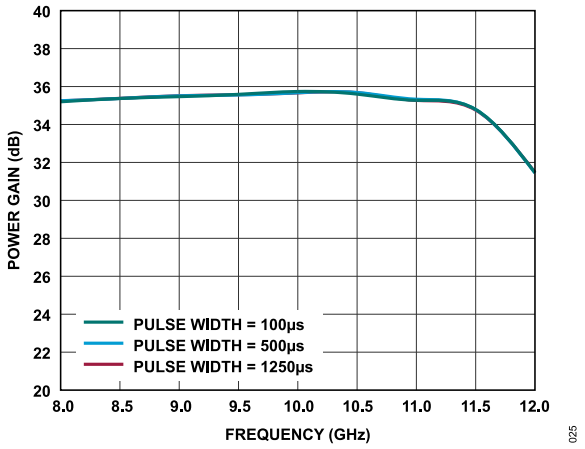

Figure 25. Power Gain at P_{IN} = 1dBm vs. Frequency for Various Pulse Widths at 10% Duty Cycle

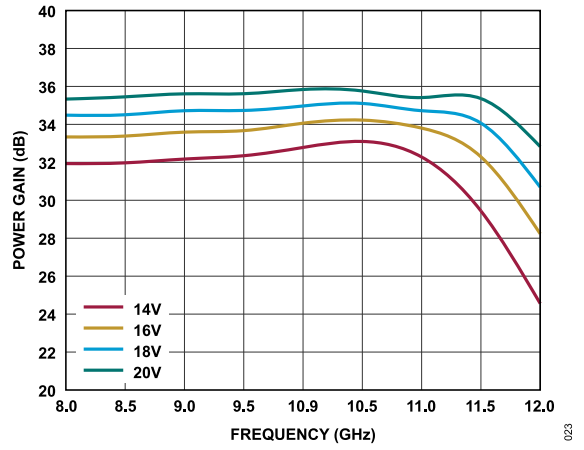

Figure 23. Power Gain at P_{IN} = 1dBm vs. Frequency for Various Supply Voltages

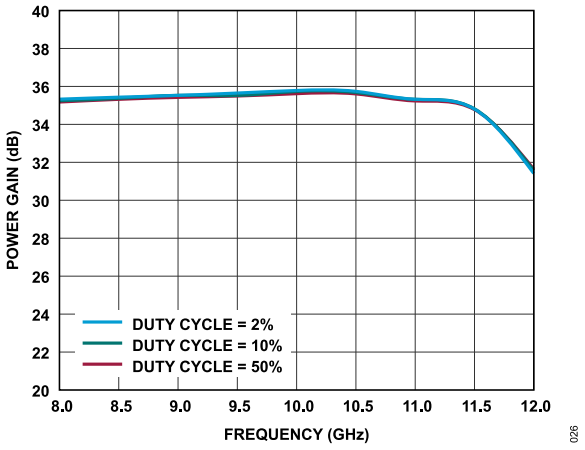

Figure 26. Power Gain at P_{IN} = 1dBm vs. Frequency for Various Duty Cycles at 100µs Pulse Width

TYPICAL PERFORMANCE CHARACTERISTICS

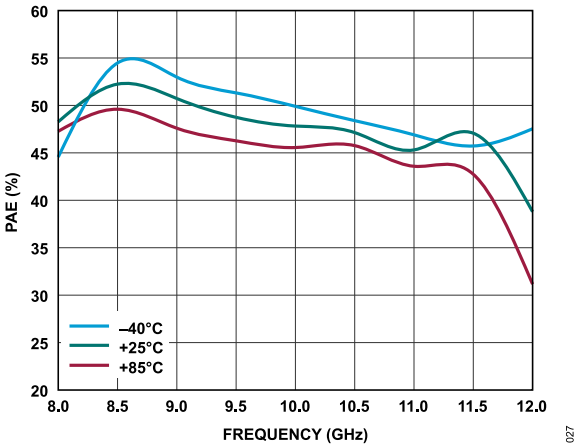

Figure 27. PAE at P_{IN} = 1dBm vs. Frequency for Various Temperatures

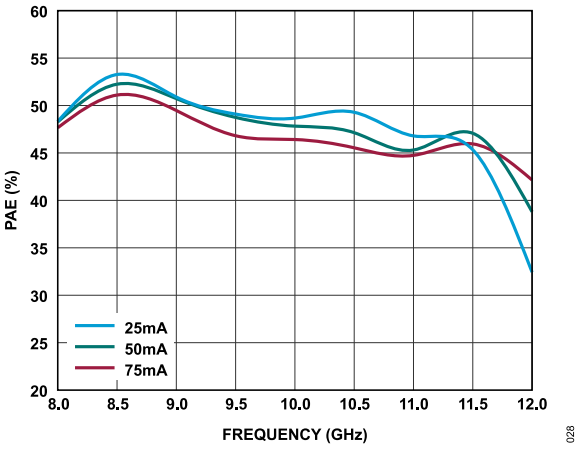

Figure 28. PAE at P_{IN} = 1dBm vs. Frequency for Various Supply Currents

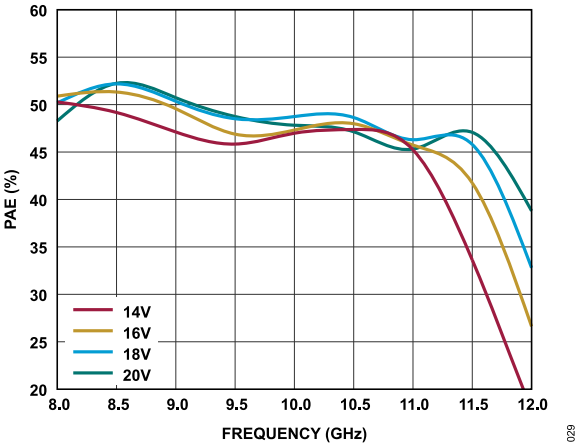

Figure 29. PAE at P_{IN} = 1dBm vs. Frequency for Various Supply Voltages

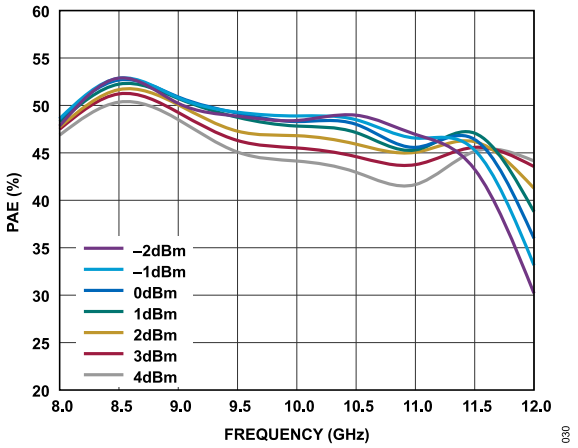

Figure 30. PAE vs. Frequency for Various P_{IN} Values

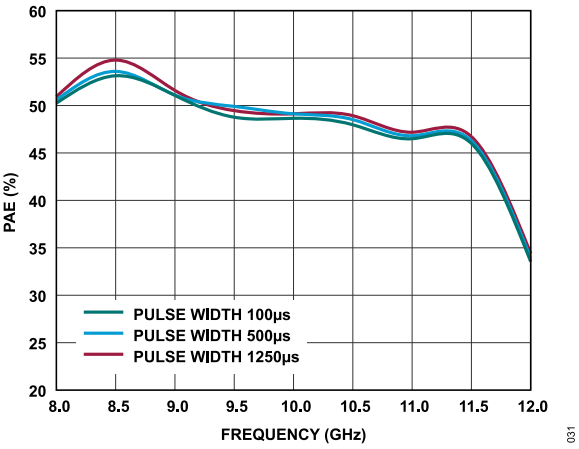

Figure 31. PAE at P_{IN} = 1dBm vs. Frequency for Various Pulse Widths at 10% Duty Cycle

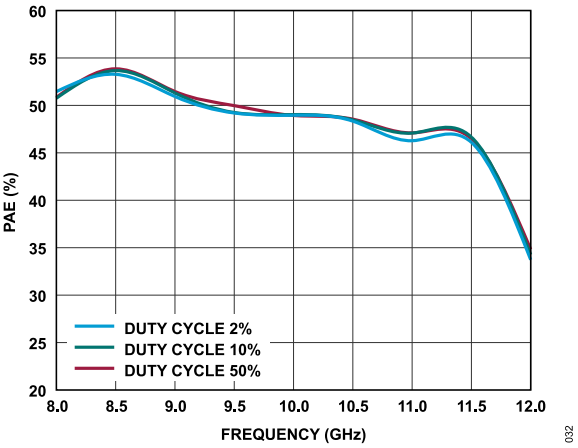

Figure 32. PAE at P_{IN} = 1dBm vs. Frequency for Various Duty Cycles at 100µs Pulse Width

TYPICAL PERFORMANCE CHARACTERISTICS

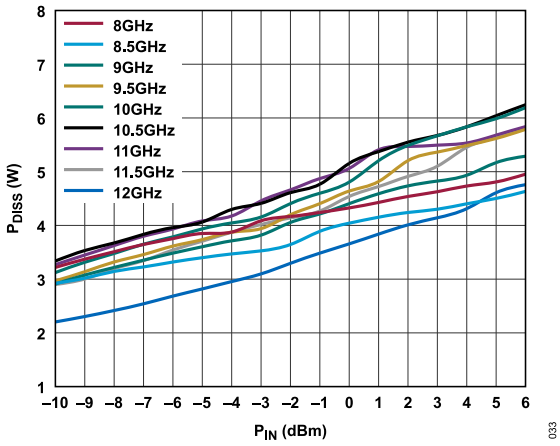

Figure 33. P_{DISS} vs. P_{IN} at Various Frequencies at 85°C

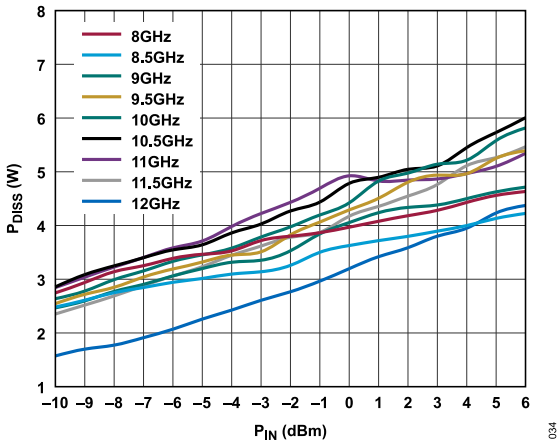

Figure 34. P_{DISS} vs. P_{IN} at Various Frequencies, Pulse Width = 500µs at 10% Duty Cycle

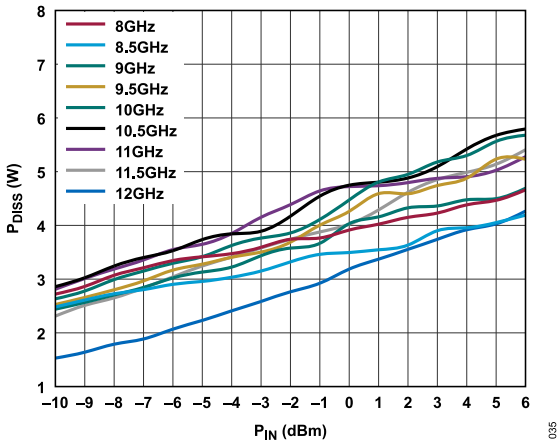

Figure 35. P_{DISS} vs. P_{IN} at Various Frequencies, Pulse Width = 1250µs at 10% Duty Cycle

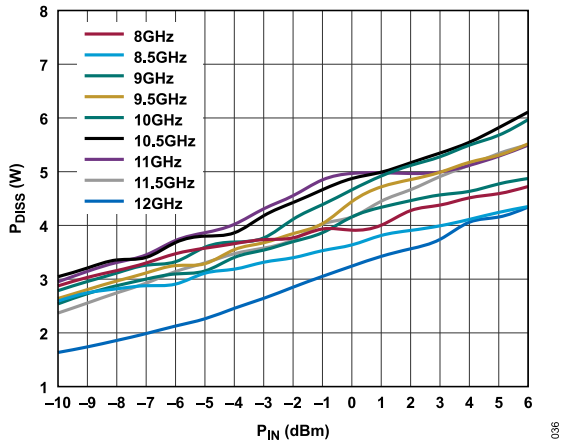

Figure 36. P_{DISS} vs. P_{IN} at Various Frequencies, Pulse Width = 100µs at 2% Duty Cycle

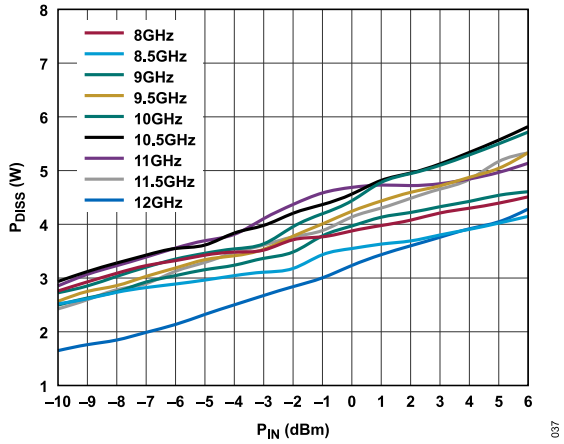

Figure 37. P_{DISS} vs. P_{IN} at Various Frequencies, Pulse Width = 100µs at 50% Duty Cycle

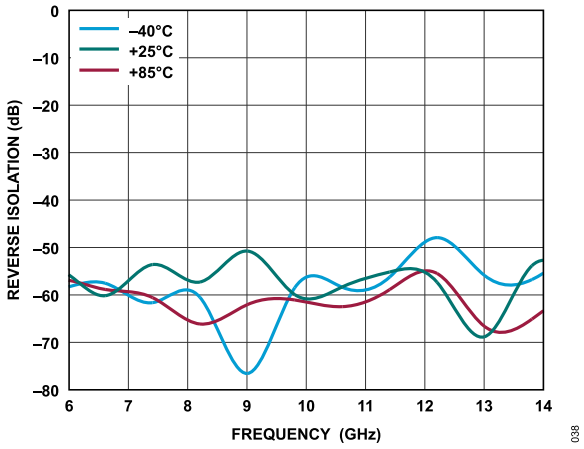

Figure 38. Reverse Isolation vs. Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

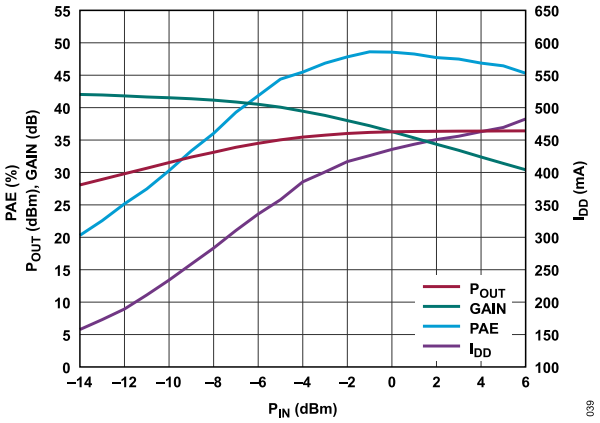

Figure 39. PAE, P_{OUT}, Gain, and Supply Current (I_{DD}) vs. P_{IN} at 8GHz

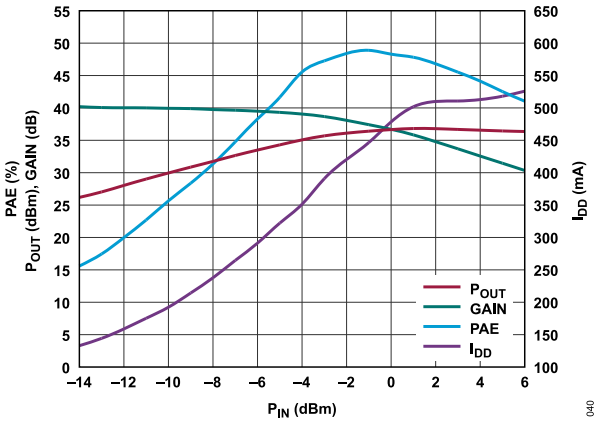

Figure 40. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 10GHz

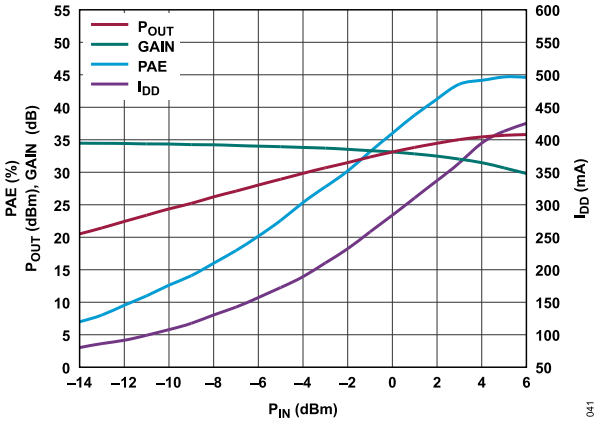

Figure 41. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 12GHz

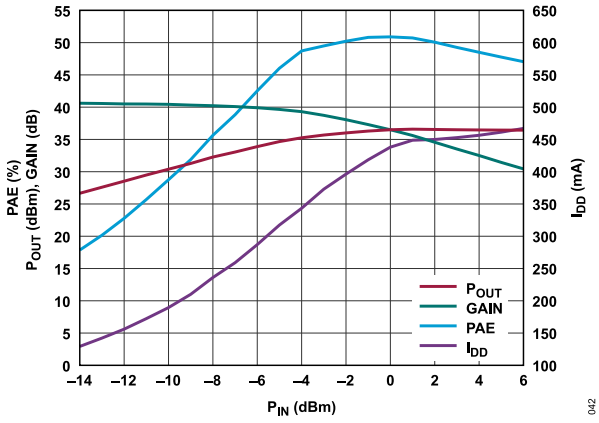

Figure 42. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 9GHz

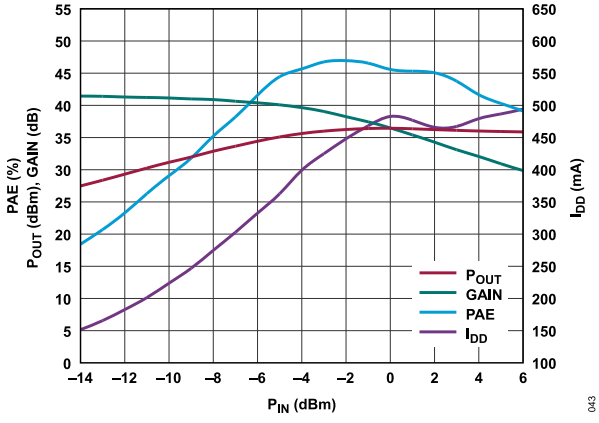

Figure 43. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 11GHz

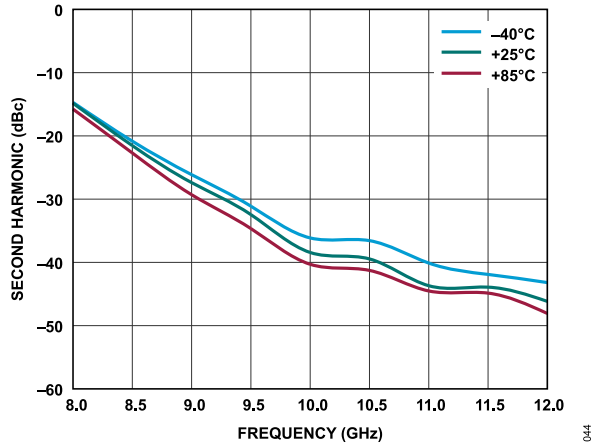

Figure 44. Second Harmonic at P_{IN} = 1dBm vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

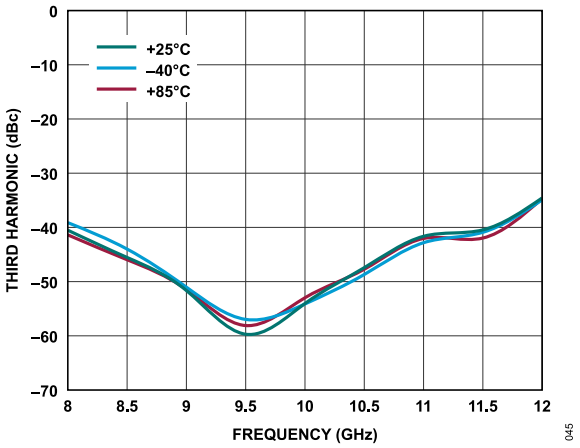

Figure 45. Third Harmonic at P_{IN} = 1dBm vs. Frequency for Various Temperatures

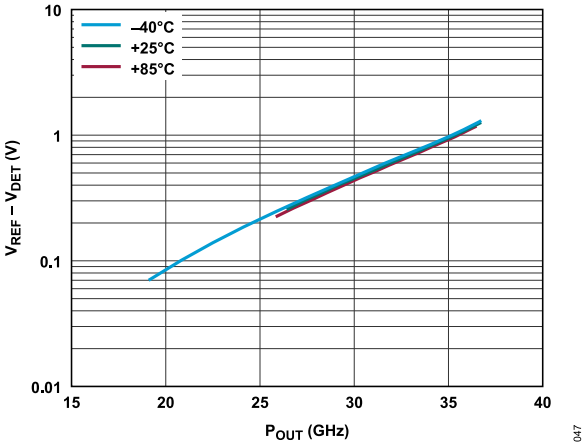

Figure 47. V_{REF} – V_{DET} vs. P_{OUT} for Various Temperatures

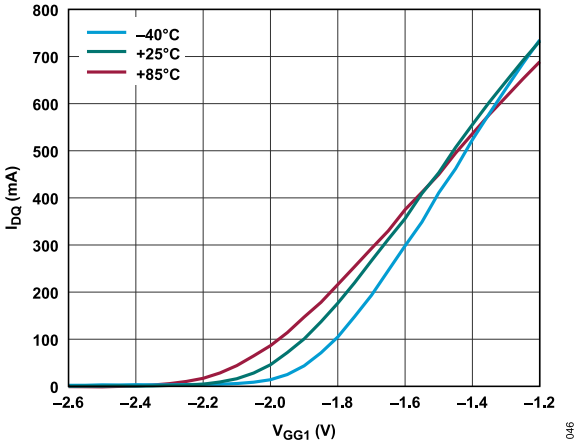

Figure 46. I_{DQ} vs. V_{GG1} for Various Temperatures

THEORY OF OPERATION

The ADPA1120 is a GaN power amplifier that delivers 36.5dBm (4.5W) of pulsed power. The device consists of four cascaded gain stages. A simplified block diagram is shown in Figure 48.

The positive bias voltage that applied to the VDD1-2, VDD3, and VDD4 pins provides bias to the drains of the first, second, third and fourth gain stages, respectively (a single common supply voltage must be used). The negative DC voltages are applied to the VGG1-2, VGG3, and VGG4 gates bias pins of the first, second, third and fourth gain stages, respectively, to allow control of the drain currents for each stage.

The recommended DC biasing results in a typical pulsed RF P_{OUT} and PAE of 36.5dBm and 47%, respectively, across the band of 9.5GHz to 11.5GHz when the input power is 1dBm.

The ADPA1120 has single-ended RFIN and RFOUT ports that are AC-coupled. The impedance of these ports are nominally 50Ω over the 8GHz to 12GHz operating frequency range. Consequently, the ADPA1120 can be directly inserted into a 50Ω system without the need for external impedance matching components or AC coupling capacitors.

A portion of the RF output signal (RFOUT) is directionally coupled to a diode to detect the RF P_{OUT}. When the diode is DC biased externally through a resistor, it rectifies the RF power and makes it available as a DC voltage at VDET. To allow temperature compensation of VDET, the reference DC voltage detected through an identical diode that is not coupled to the RF power is available on the VREF pin. The difference of $V_{REF} - V_{DET}$ provides a temperature-compensated detector voltage that is proportional to the RF P_{OUT}.

The small signal gain drops significantly at −40°C because the device is biased close to the transistor pinch-off voltage. At cold temperatures, the pinch-off voltage shifts more positive as can be seen in Figure 46. As a result, a more positive gate voltage is required to turn on the transistor and have current flow. The gain at small signal levels and cold temperatures are much lower than room temperature; however, the performance at large signal levels is as expected and shown in Figure 21.

The data in this data sheet was captured by setting the drain current to a nominal I_{DQ}, that is, 50mA. After this initial I_{DQ} was determined, the gate voltage was kept constant in subsequent testing and operation. It is possible that the I_{DQ} will increase by some amount with continued operation at that fixed VGG gate voltage. Keeping the gate voltage constant during long-term operation provides more consistent RF performance than keeping a nominal I_{DQ} constant.

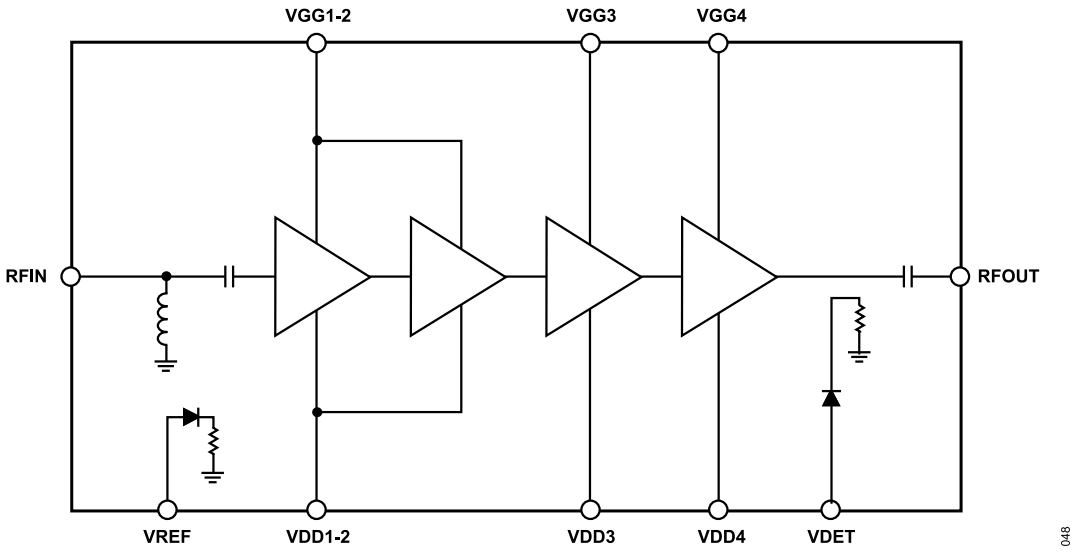

Figure 48. Basic Block Diagram

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for operating the ADPA1120 are shown in Figure 49. Apply a power supply voltage between 14V and 20V to the VDD1-2, VDD3, and VDD4 pins. Decouple the VGG1-2, VGG3, VGG4, VDD1-2, VDD3, and VDD4 pins with the capacitor and resistor values shown in Figure 49. The gate bias pins, VGG1-2, VGG3, and VGG4, are used to bias the ADPA1120. Pin 1 to Pin 3, Pin 7 to Pin 9, Pin 12, Pin 13, Pin 16 to Pin 19, Pin 21, Pin 22, Pin 24 to Pin 28, and Pin 32 are designated as the not internally connected (NIC) pins. Although these NIC pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

Apply a voltage between −3V and −1V to the VGGx pins to set the bias level and drain current. The ADPA1120 can support both continuous and pulsed operation; however, pulsed operation provides better thermal management by pulsing either the gate voltage or the drain voltage.

In gate pulsed mode, V_{DD} is held at a fixed level (nominally 20V) while the gate voltage is pulsed between −4V (off) and approximately −3V to −1V (on). The exact on level can be adjusted to achieve the desired I_{DQ}.

In drain pulsed mode, the V_{DD} voltage is pulsed on and off while the gate voltage is held at a fixed negative level between −3V and −1V. Because high currents and voltages are being switched on and off, a metal-oxide semiconductor field effect transistor (MOSFET) and a MOSFET switch driver are required in the circuit. Large capacitors are also required, which act as local reservoirs of charge, and these capacitors help provide the drain current required by the ADPA1120 while maintaining a steady drain voltage during the on time of the pulse.

The ADPA1120-EVALZ evaluation board package includes a plugin pulser board that contains the required circuitry to implement drain pulsed mode. See the ADPA1120-EVALZ user guide for more information.

To safely turn power on, the VGGx pins must be set to −4V before V_{DD} is applied. After the VGGx pins are increased to achieve the desired drain bias current, the RF input can be applied. Trigger the RF source so that the RF is applied only during the time the drain pulse is high. To safely turn power off, remove the RF input signal and decrease the VGGx pins to −4V. V_{DD} can then be decreased to 0V before increasing VGG1-2 to 0V.

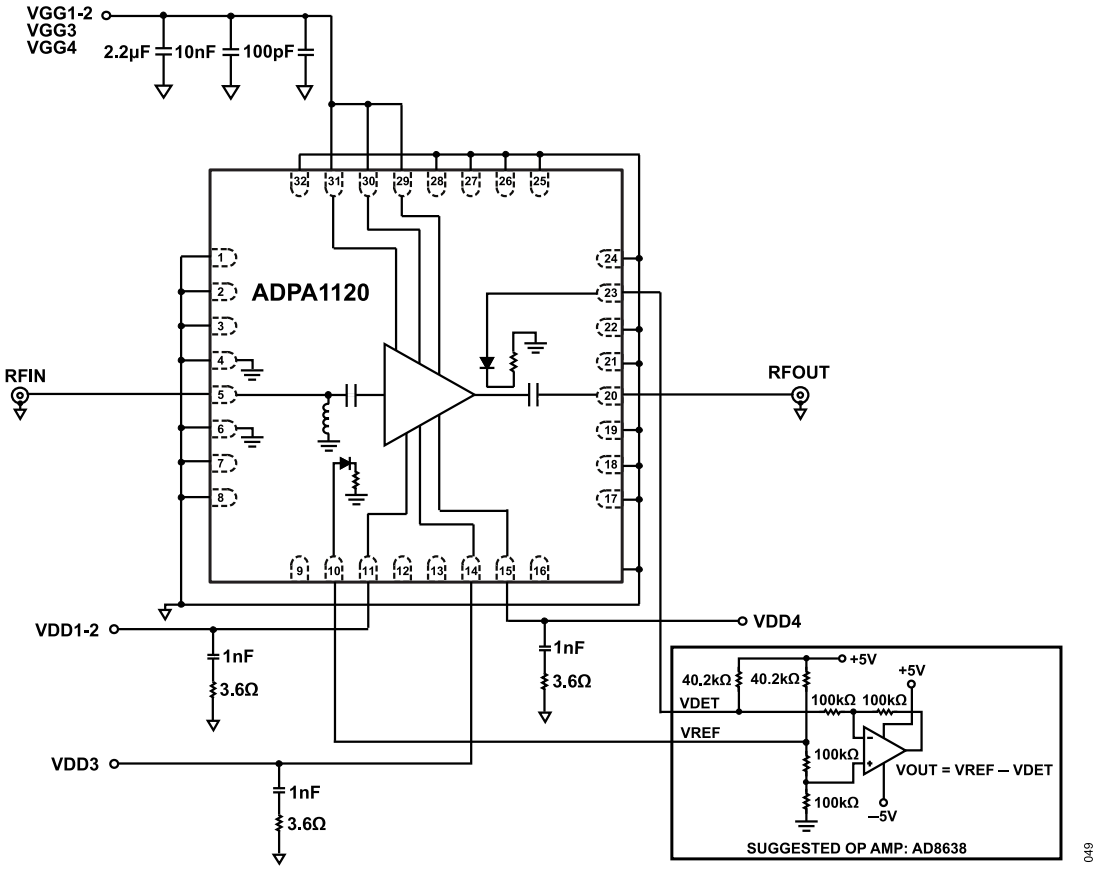

Figure 49. Basic Connections

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCE

The recommended bias sequence for power-up is as follows:

1. Connect all GND pins to ground.
2. Set the voltages on the VGG1-2, VGG3, and VGG4 pins to −4V.
3. Set the voltages on the VDD1-2, VDD3, and VDD4 pins to 20V.
4. Increase the voltages of the VGG1-2, VGG3, and VGG4 pins from −3V to −1V to achieve the desired I_{DQ}, nominally 50mA.
5. Apply the RF signal to the RFIN pin.

The recommended sequence for the transmit state during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the voltages of the VGG1-2, VGG3, and VGG4 pins to −4V.
3. Set the voltages on the VDD1-2, VDD3, and VDD4 pins to 0V.
4. Set the voltages on the VGG1-2, VGG3, and VGG4 pins to 0V.

All measurements and data shown in this data sheet were taken using the basic connections circuit (see Figure 49) and biased per the conditions in this section, unless otherwise noted. The bias conditions described in this section are the operating points recommended to optimize the overall device performance. Operation using other bias conditions can result in performance that differs from what is shown in the Typical Performance Characteristics section. To obtain optimal performance while not damaging the device, follow the recommended biasing sequences described in this section and adhere to the values shown in the Absolute Maximum Ratings section.

DRAIN PULSING

To implement drain pulsed operation on the ADPA1120, apply a negative voltage to the gate pins of the power amplifier while the voltage on the drain pins are pulsed between 0V and 20V.

The power supplies used to provide the drain voltages to the ADPA1120 must have a fast transient response to minimize voltage droop.

Drain Pulsing Setup

Take the following steps to set up drain pulsing:

1. Connect all power supply, ground, and control signals to the ADPA1120, see Figure 49.
2. To pulse the power amplifier, set the voltages on the VGG1-2, VGG3 and VGG4 pins to −4V and set the voltages on the VDD1-2, VDD3, and VDD4 pins to 20V.
3. Turn on the drain voltage pulse pins, VDD1-2, VDD3 and VDD4, pulsing between 0V and 20V, 100µs, and 10% duty cycle typical.
4. Adjust the voltages on the VGG1-2, VGG3 and VGG4 pins between −3V and −1V until the target pulsed I_{DQ} is reached (nominally 50mA).
5. Apply the RF input signal.

GATE PULSING

To implement gate pulsed operation on the ADPA1120, apply a pulsed negative voltage to the gate pins of the power amplifier while the voltage on the drain pins are held constant.

The power supplies used to provide the drain voltages to the ADPA1120 must have a fast transient response to minimize voltage droop.

Gate Pulsing Setup

Take the following steps to set up gate pulsing:

1. Connect all power supply, ground, and control signals to the ADPA1120, see Figure 49.
2. To pulse the power amplifier, set the voltages on the VGG1-2, VGG3 and VGG4 pins to −4V and set the voltages on the VDD1-2, VDD3 and VDD4 pins to 20V.
3. Turn on the gate voltage pulse pins, VGG1-2, VGG3 and VGG4, pulsing between −4V and approximately −3V, 100µs, and 10% duty cycle typical.
4. Adjust the gate voltage pulse high-voltage between −3V and −1V to achieve the target pulsed I_{DQ} (nominally 50mA) while maintaining the pulse off voltage level at −4V.
5. Apply the RF input signal

APPLICATIONS INFORMATION

THERMAL MANAGEMENT

Proper thermal management is critical to achieve the specified performance and rated operating life. The ADPA1120 can support both continuous and pulsed operation; however, pulsed biasing provides better thermal management to maintain a safe channel temperature (T_{CHAN}). T_{CHAN} (or the die temperature) correlates closely with the mean time to failure.

Consider a continuous bias case (see Figure 50). When bias is applied, the T_{CHAN} of the ADPA1120 rises through a turn-on transient interval and eventually settles to a steady state value. Calculate the thermal resistance (θ_{JC}) of the device as the rise in T_{CHAN} above the starting base temperature (T_{BASE}) divided by the total device P_{DISS} with the following equation:

$$\theta_{JC} = t_{RISE}/P_{DISS}$$

where:
t_{RISE} is the rise in T_{CHAN} of the ADPA1120 above the T_{BASE} (°C).
P_{DISS} is the power dissipation (W) of the ADPA1120.

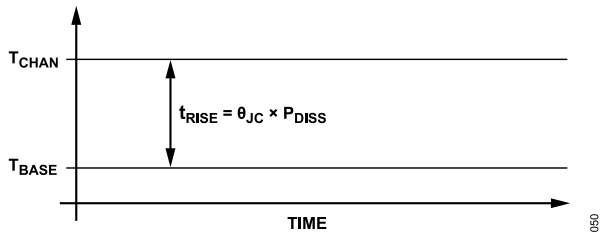

Figure 50. Channel Temperature Rise for Continuous Bias Condition

Next, consider a pulsed bias case at low duty cycle (see Figure 51). When bias is applied, the T_{CHAN} of the ADPA1120 can be described as a series of exponentially rising and decaying pulses. The peak T_{CHAN} reached during consecutive pulses increases during the turn-on transient interval, and eventually, this temperature settles to a steady state condition where the peak T_{CHAN} from pulse to pulse stabilizes.

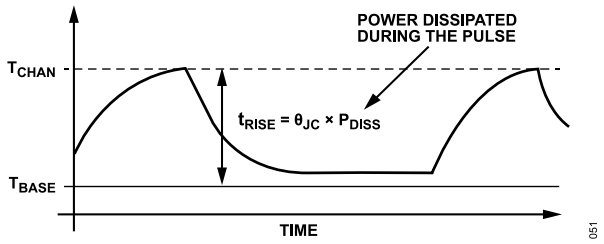

Figure 51. Pulsed Bias at Low Duty Cycle

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CP-32-13	LFCSP	32-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA1120ACPZN	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	Tape, 1	CP-32-13
ADPA1120ACPZN-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 1500	CP-32-13

[1] Z = RoHS Compliant Part.