2GHz to 22GHz, 15W, GaN Power Amplifier

FEATURES

- Frequency range: 2GHz to 22GHz
- 50Ω matched input and output
- Power gain: 12dB typical from 8GHz to 16GHz
- P_{OUT}: 42dBm typical from 8GHz to 16GHz
- PAE: 24% typical from 8GHz to 16GHz
- S21: 20dB typical from 8GHz to 16GHz
- OIP3: 43.5dBm typical from 8GHz to 16GHz
- Integrated RF power detector
- V_{DD}: 28V
- I_{DQ}: 600mA

APPLICATIONS

- Electronic warfare
- Test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

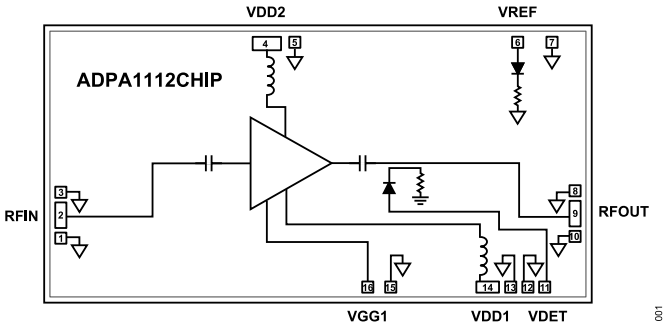

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADPA1112CHIP is a 2GHz to 22GHz wideband power amplifier with a saturated output power (P_{OUT}) of 42dBm, power added efficiency (PAE) of 24%, and a power gain of 12dB typical from 8GHz to 16GHz at input power (P_{IN}) of 30dBm. The RF input and RF output are internally matched and AC-coupled. A drain bias voltage (V_{DD}) of 28V is applied to the VDD1 and VDD2 pads, which have integrated bias inductors. The drain current is set by applying a negative voltage to the VGG1 pad. A temperature-compensated RF detector is integrated allowing monitoring of the RF output power.

The ADPA1112CHIP is fabricated on a gallium nitride (GaN) process and is specified for operation from −55°C to +85°C.

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REVISION HISTORY

8/2025—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

2GHz TO 8GHz FREQUENCY RANGE

T_{CASE} = 25°C, VDD1 drain bias voltage (V_{DD1}) and VDD2 drain bias voltage (V_{DD2}) = 28V, target quiescent current (I_{DQ}) = 600mA, and frequency range = 2GHz to 8GHz, unless otherwise stated.

Table 1. 2GHz to 8GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2		8	GHz	
GAIN					
Small Signal Gain (S21)	16.5	20.5		dB	
Gain Flatness		±0.5		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
Input (S11)		16		dB	
Output (S22)		10		dB	
POWER					P_{IN} = 30.0dBm
Output (P_{OUT})	39.5	41.5		dBm	
Gain	9.5	11.5		dB	
Power Added Efficiency (PAE)		24		%	
OIP3		44.5		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		51		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust the gate control voltage (V_{GG1}) between −3V and −1V to achieve an I_{DQ} = 600mA typical

8GHz TO 16GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 8GHz to 16GHz, unless otherwise stated.

Table 2. 8GHz to 16GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8		16	GHz	
GAIN					
S21	16	20		dB	
Gain Flatness		±0.3		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		16		dB	
S22		13		dB	
POWER					P_{IN} = 30.0dBm
P_{OUT}	40	42		dBm	
Gain	10	12		dB	
PAE		24		%	
OIP3		43.5		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		54		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

ELECTRICAL SPECIFICATIONS

16GHz TO 20GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 16GHz to 20GHz, unless otherwise stated.

Table 3. 16GHz to 20GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	16		20	GHz	
GAIN					
S21	16.5	20.5		dB	
Gain Flatness		±0.5		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		16		dB	
S22		14		dB	
POWER					P_{IN} = 30.0dBm
P_{OUT}	39.5	41.5		dBm	
Gain	9.5	11.5		dB	
PAE		21		%	
OIP3		44		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		55		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

20GHz TO 22GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} and V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 20GHz to 22GHz, unless otherwise stated

Table 4. 20GHz to 22GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	20		22	GHz	
GAIN					
S21		19.5		dB	
Gain Flatness		±1.2		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		12		dB	
S22		13		dB	
POWER					P_{IN} = 30.0dBm
P_{OUT}		40.5		dBm	
Gain		10.5		dB	
PAE		16		%	
OIP3		44		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		55		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
Bias Voltage	
Drain (V_{DD1} and V_{DD2})	35V
Gate (V_{GG1})	−8.0V DC to 0V DC
Bias Current	
Gate Current (I_{GG1}) at 85°C	7.2mA (see Figure 51)
RF Input Power (RFIN)	33 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C, Derate 452mW/°C Above 85°C	63.3W
Temperature	
Nominal Peak Channel, T_{CASE} = 85°C, P_{IN} = 30dBm, P_{DISS} = 52.5W at 20GHz	201°C
Storage Range	−55°C to +150°C
Operating Range	−55°C to +85°C
Maximum Channel	225°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to the carrier or substrate on which the die is mounted. Careful attention is required with each material used in the thermal path under the IC. With an epoxy layer of nominal thickness assumed under the die, θ_{JC} is the thermal resistance from the die channel to the bottom of the epoxy layer.

Table 6. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
C-16-6	2.21	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel to the bottom of the epoxy layer with the ground pad beneath the die held constant at an 85°C operating temperature.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1112CHIP

Table 7. ADPA1112CHIP, 16-Pad Bare Die

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

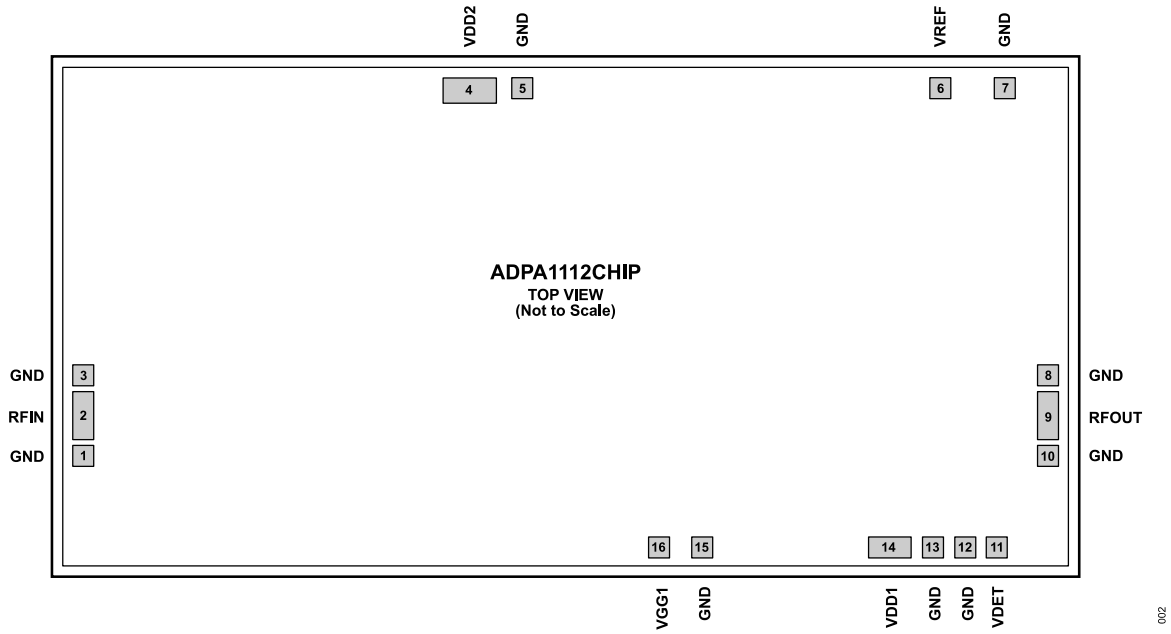

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 7, 8, 10, 12, 13, 15	GND	Ground. Do not bond the GND pins. See Figure 3 for the interface schematic.
2	RFIN	RF Input. The RFIN pin is AC-coupled and matched to 50Ω. See Figure 4 for the interface schematic.
4	VDD2	Drain Bias for the Second Gain Stage. Capacitively bypass as shown in the typical application circuit (see Figure 56). See Figure 5 for the interface schematic.
6	VREF	Reference Diode for Temperature Compensation of the VDET RF P_{OUT} Measurements. Connect a 40.2kΩ resistor between the VREF pin and 5V to provide the DC bias. See Figure 6 for the interface schematic.
9	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50Ω. See Figure 5 for the interface schematic.
11	VDET	Detector Diode to Measure the RF P_{OUT}. Used in combination with the VREF pin. The difference in voltage (VREF voltage (V_{REF}) − VDET voltage (V_{DET})) is a temperature compensated DC voltage that is proportional to the RF P_{OUT}. Connect a 40.2kΩ resistor between the VDET pin and 5V to provide the DC bias. See Figure 5 for the interface schematic.
14	VDD1	Drain Bias for the First Gain Stage. Capacitively bypass as shown in the typical application circuit (see Figure 56). See Figure 7 for the interface schematic.
16	VGG1	Gate Bias for the First and Second Gain Stages. Adjust the negative voltage on the VGG1 pin to set the I_{DQ} to the desired level. See Figure 8 for the interface schematic.
Die Bottom	GND	Ground. Connect the die bottom to the RF and DC ground. See Figure 3 for the interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

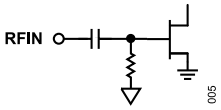

Figure 4. RFIN Interface Schematic

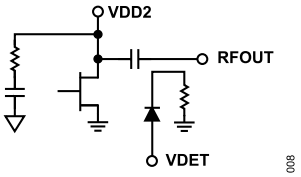

Figure 5. VDD2, VDET, and RFOUT Interface Schematic

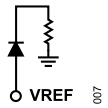

Figure 6. VREF Interface Schematic

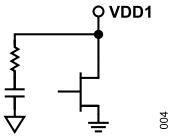

Figure 7. VDD1 Interface Schematic

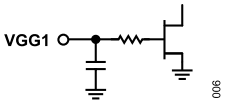

Figure 8. VGG1 interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

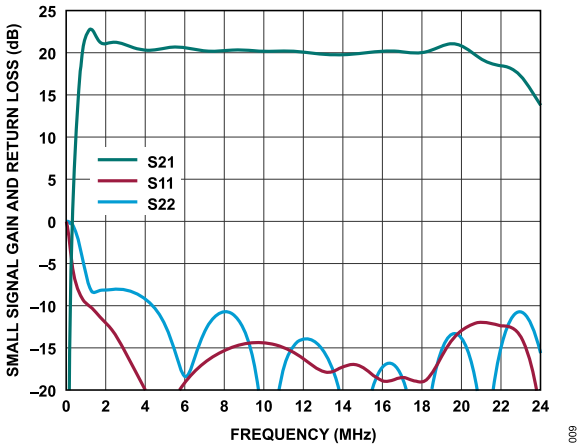

Figure 9. Small Signal Gain and Return Loss vs. Frequency, V_{DD} = 28V, I_{DQ} = 600mA

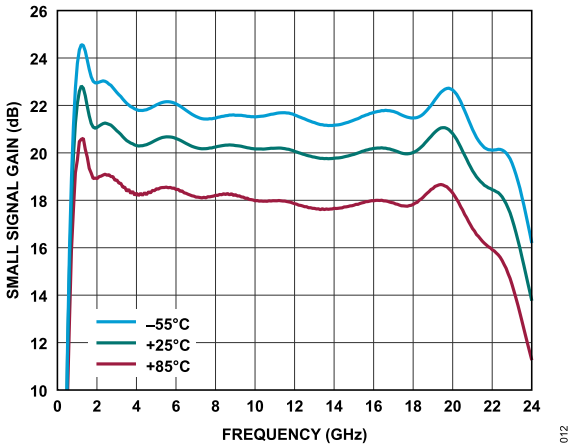

Figure 12. Small Signal Gain vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

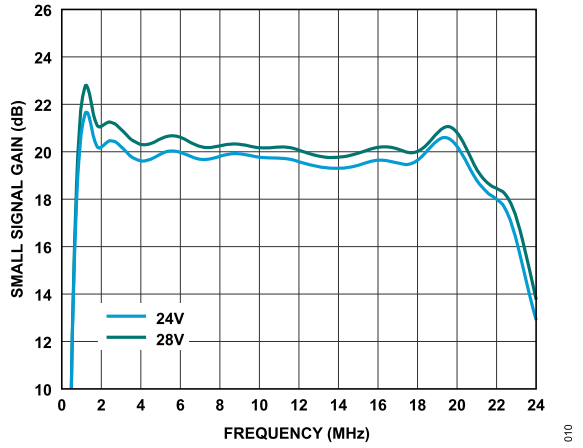

Figure 10. Small Signal Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

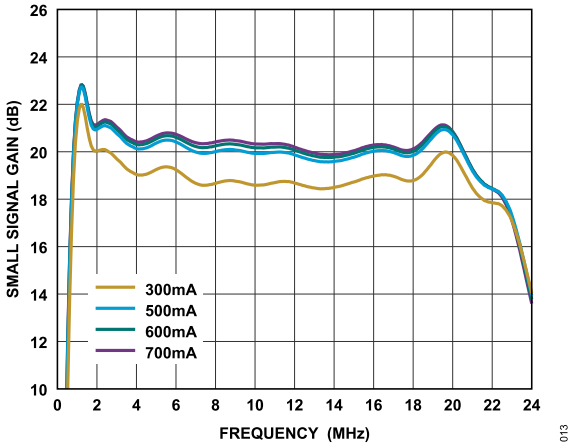

Figure 13. Small Signal Gain vs. Frequency for Various Supply Currents, V_{DD} = 28V

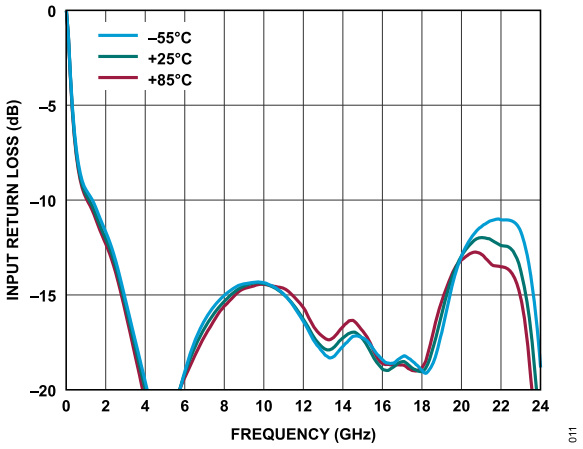

Figure 11. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

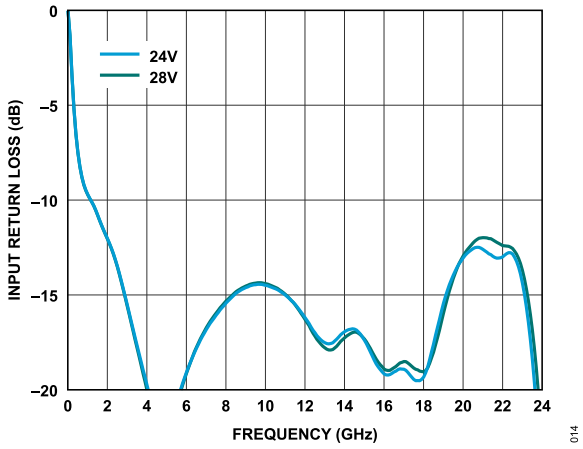

Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

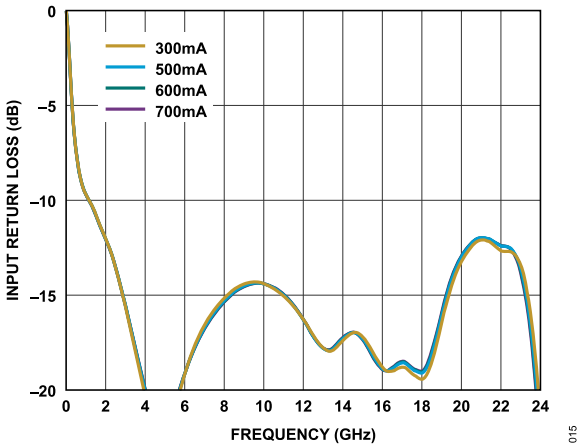

Figure 15. Input Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 28V

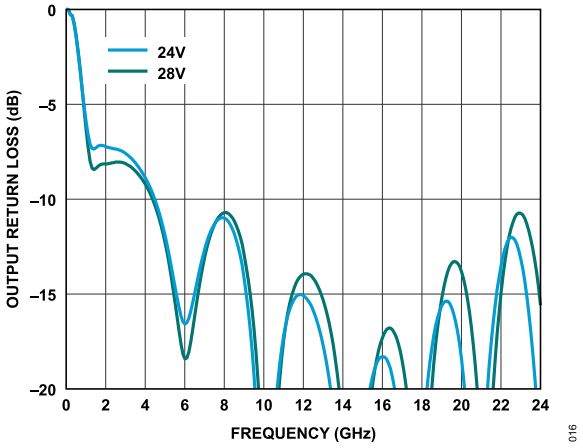

Figure 16. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

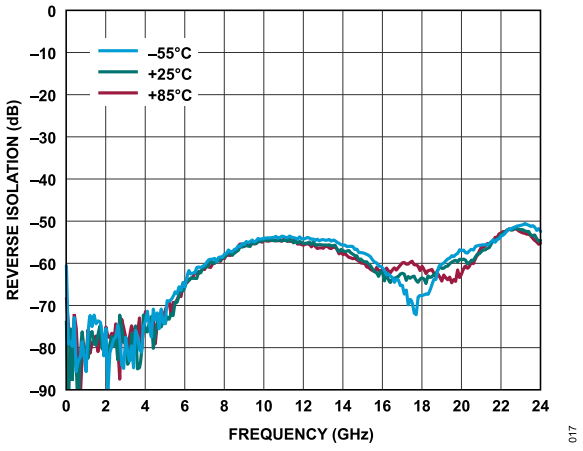

Figure 17. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

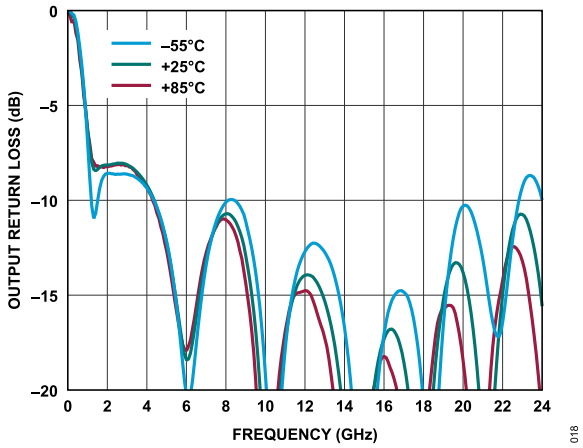

Figure 18. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

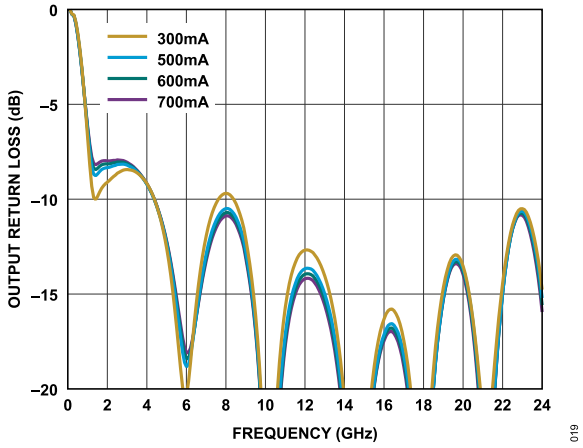

Figure 19. Output Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 28V

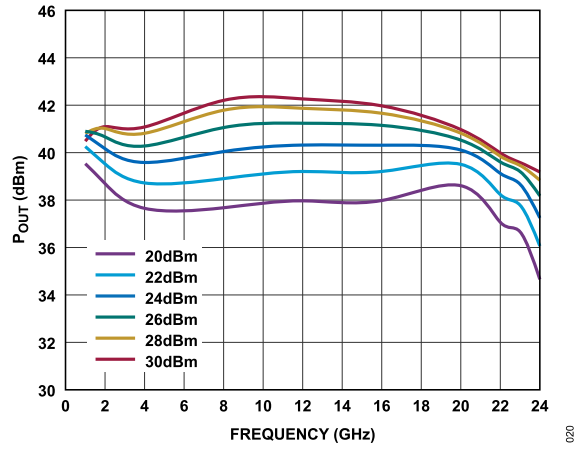

Figure 20. P_{OUT} vs. Frequency for Various P_{IN} Levels, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

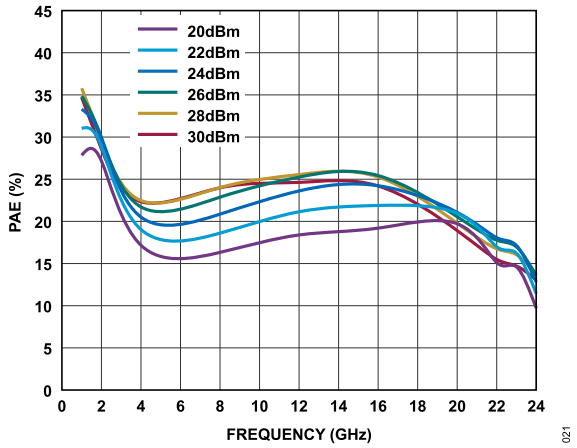

Figure 21. PAE vs. Frequency for Various P_{IN} Levels, V_{DD} = 28V, I_{DQ} = 600mA

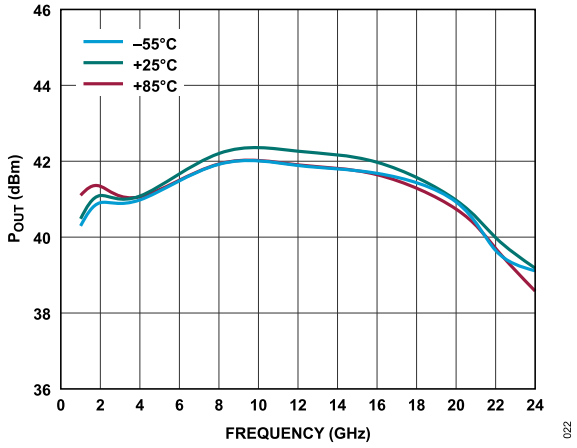

Figure 22. P_{OUT} vs. Frequency at Various Temperatures for P_{IN} = 30dBm, V_{DD} = 28V, I_{DQ} = 600mA

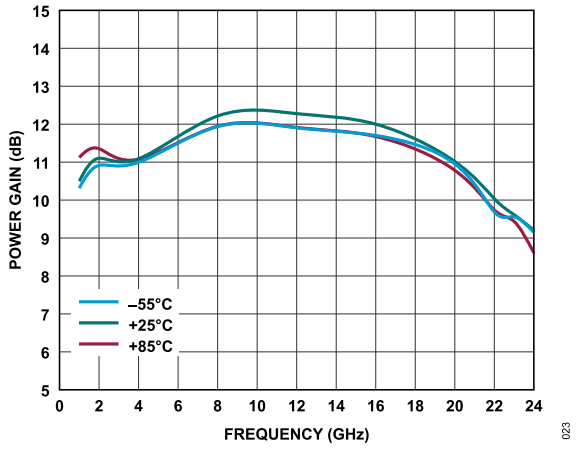

Figure 23. Power Gain vs. Frequency at Various Temperatures for P_{IN} = 30dBm, V_{DD} = 28V, I_{DQ} = 600mA

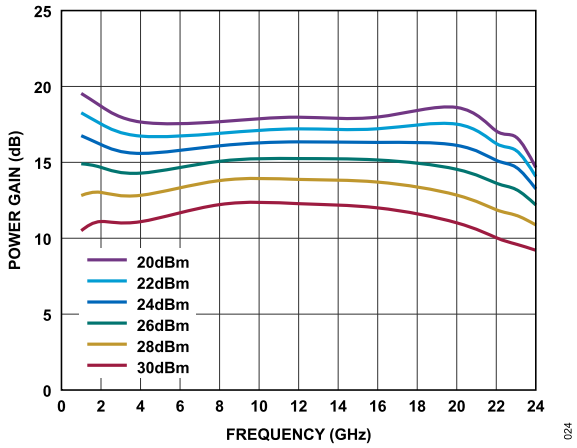

Figure 24. Power Gain vs. Frequency for Various P_{IN} Levels, V_{DD} = 28V, I_{DQ} = 600mA

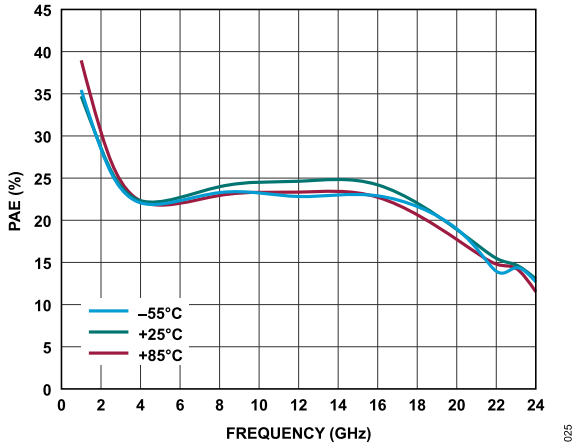

Figure 25. PAE vs. Frequency at Various Temperatures for P_{IN} = 30dBm, V_{DD} = 28V, I_{DQ} = 600mA

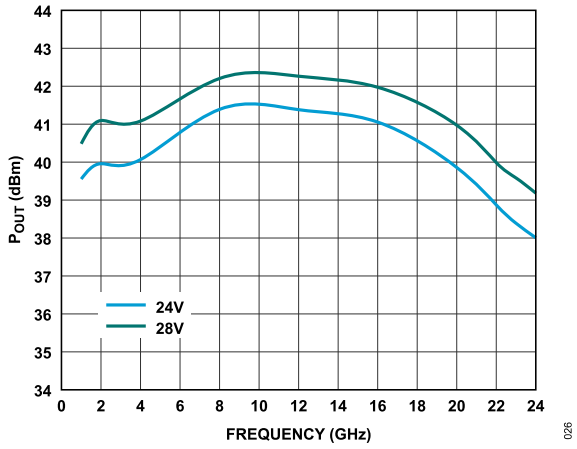

Figure 26. P_{OUT} vs. Frequency for Various Supply Voltages at P_{IN} = 30dBm, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

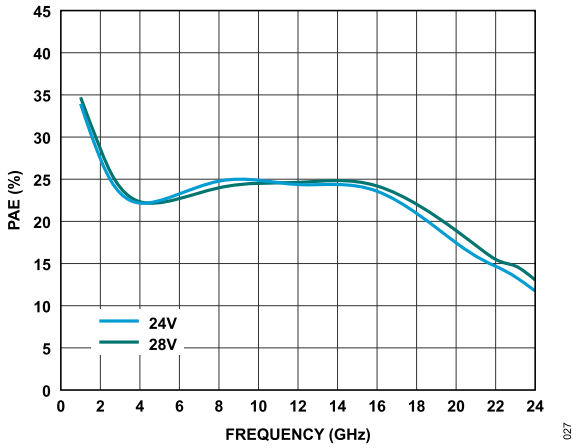

Figure 27. PAE vs. Frequency for Various Supply Voltages at P_{IN} = 30dBm, I_{DQ} = 600mA

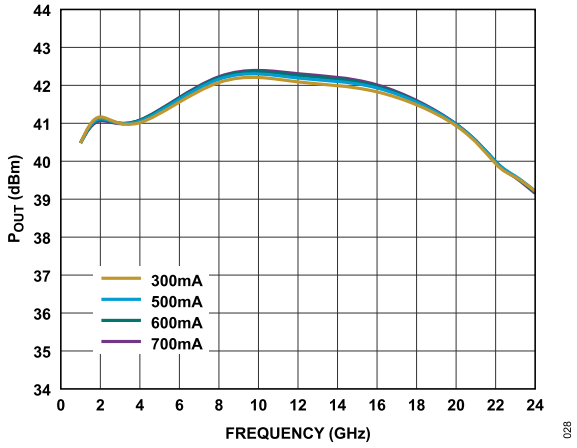

Figure 28. P_{OUT} vs. Frequency for Various Supply Currents at P_{IN} = 30dBm, V_{DD} = 28V

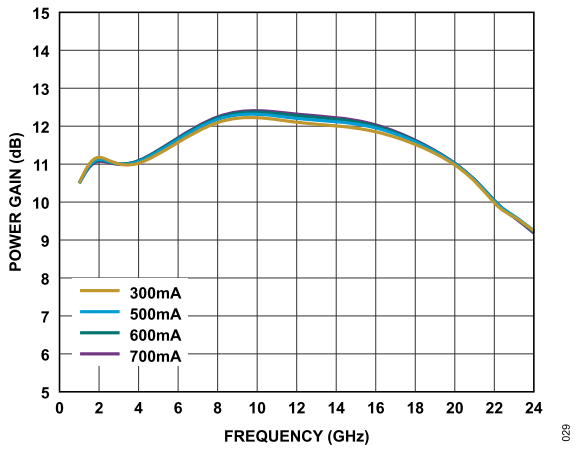

Figure 29. Power Gain vs. Frequency for Various Supply Currents at P_{IN} = 30dBm, V_{DD} = 28V

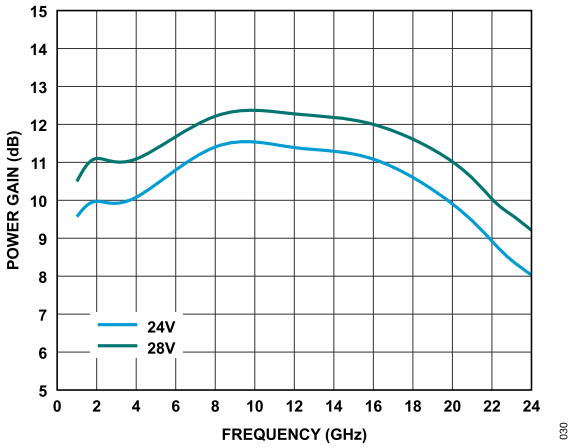

Figure 30. Power Gain vs. Frequency for Various Supply Voltages at P_{IN} = 30dBm I_{DQ} = 600mA

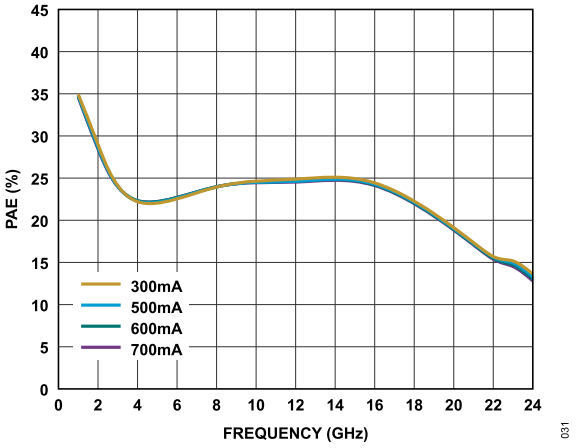

Figure 31. PAE vs. Frequency for Various Supply Currents at P_{IN} = 30dBm, V_{DD} = 28V

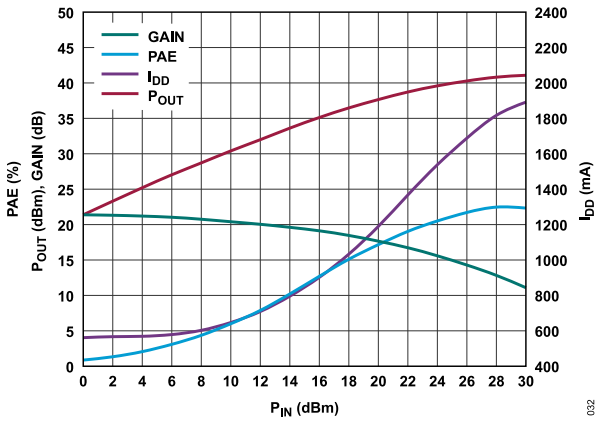

Figure 32. PAE, P_{OUT}, Gain, and Supply Current (I_{DD}) vs. P_{IN} at 4GHz, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

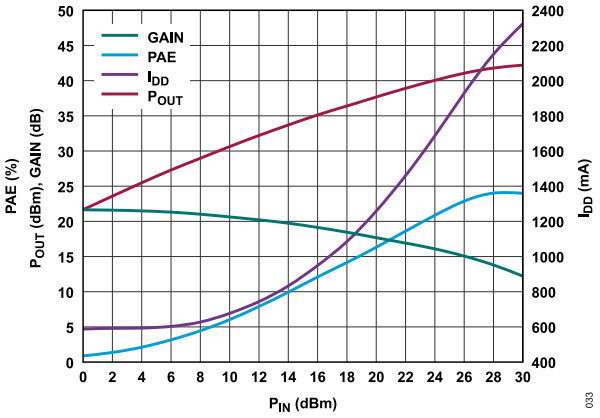

Figure 33. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 8GHz, V_{DD} = 28V, I_{DQ} = 600mA

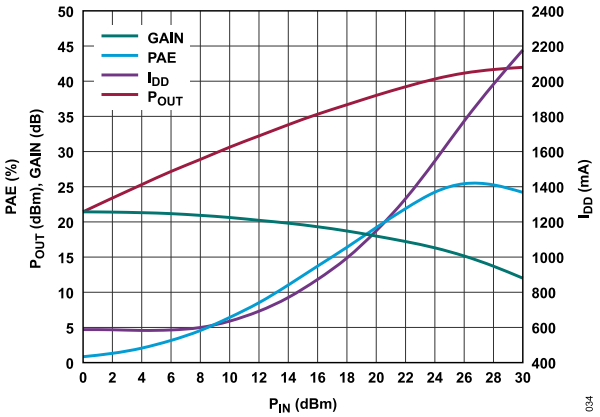

Figure 34. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 16GHz, V_{DD} = 28V, I_{DQ} = 600mA

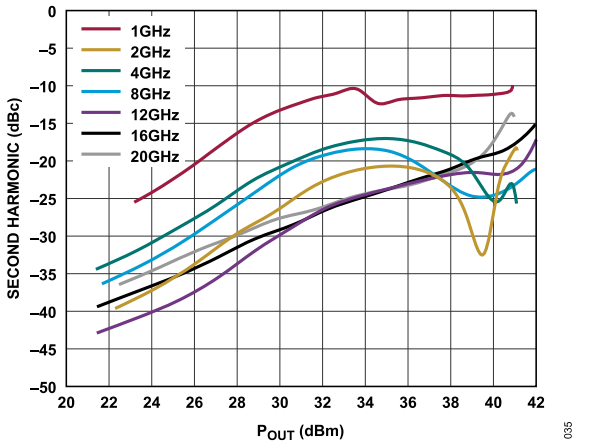

Figure 35. Second Harmonic vs. P_{OUT} for Various Frequencies, V_{DD} = 28V, I_{DQ} = 600mA

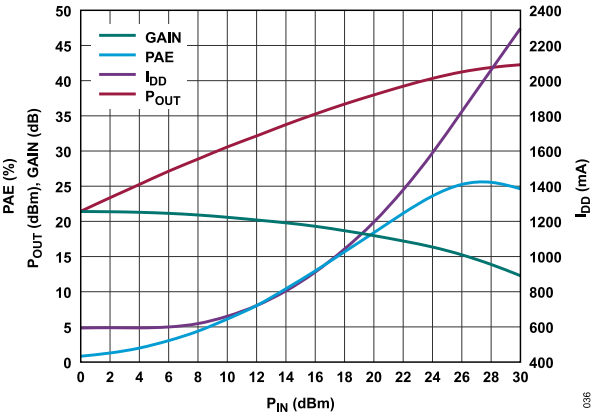

Figure 36. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 12GHz, V_{DD} = 28V, I_{DQ} = 600mA

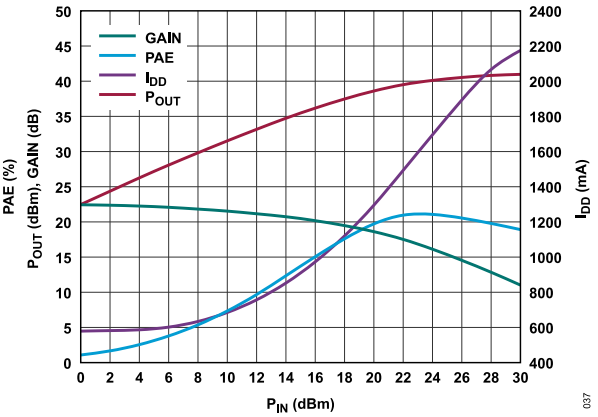

Figure 37. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 20GHz, V_{DD} = 28V, I_{DQ} = 600mA

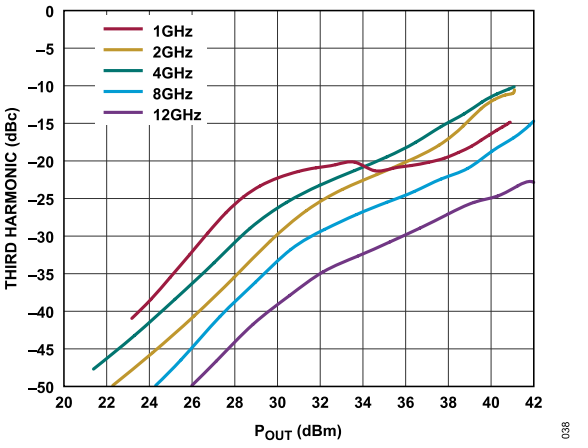

Figure 38. Third Harmonic vs. P_{OUT} for Various Frequencies, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

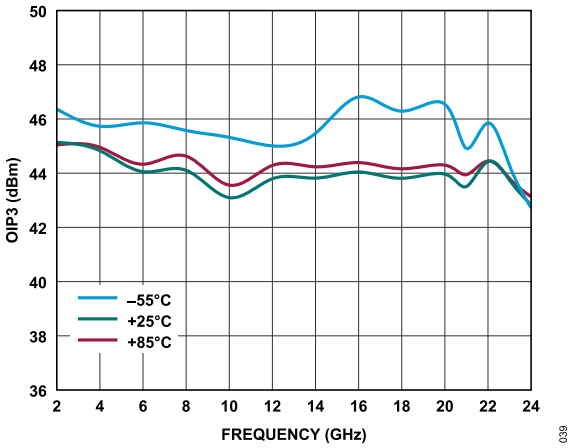

Figure 39. OIP3 vs. Frequency for Various Temperatures at P_{OUT} per Tone = 32dBm, V_{DD} = 28V, I_{DQ} = 600mA

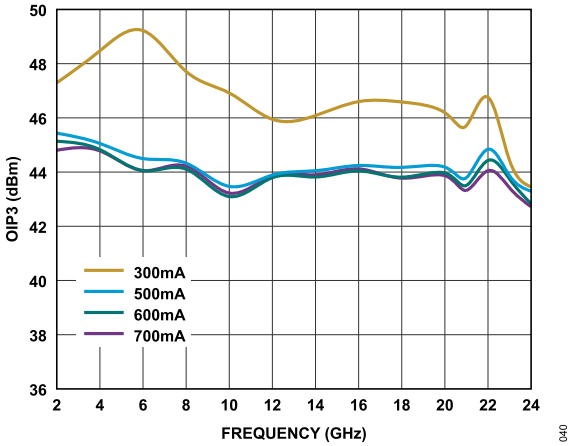

Figure 40. OIP3 vs. Frequency for Various Supply Currents at P_{OUT} per Tone = 32dBm, V_{DD} = 28V, I_{DQ} = 600mA

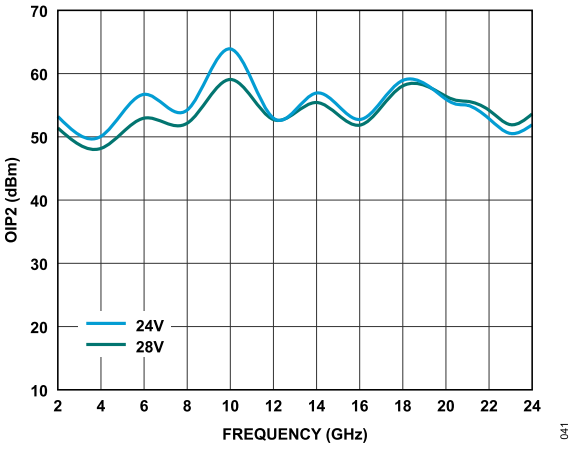

Figure 41. OIP2 vs. Frequency for Various Supply Voltages at P_{OUT} per Tone = 32dBm I_{DQ} = 600mA

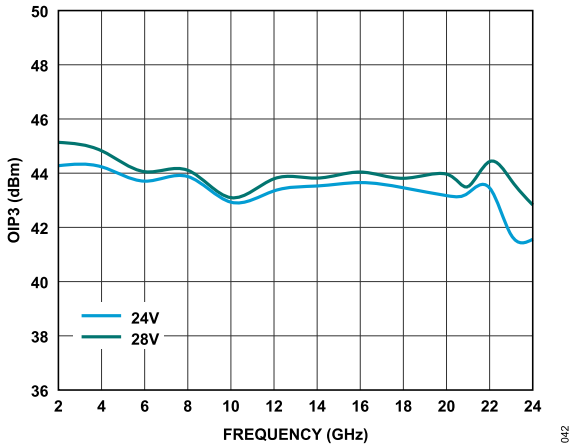

Figure 42. OIP3 vs. Frequency for Various Supply Voltages at P_{OUT} per Tone = 32dBm, I_{DQ} = 600mA

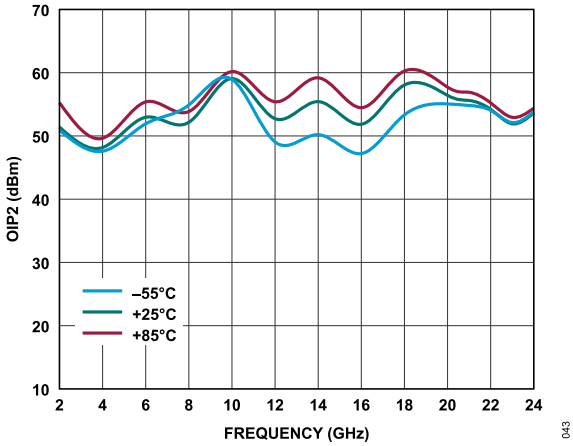

Figure 43. OIP2 vs. Frequency for Various Temperatures at P_{OUT} per Tone = 32dBm V_{DD} = 28V, I_{DQ} = 600mA

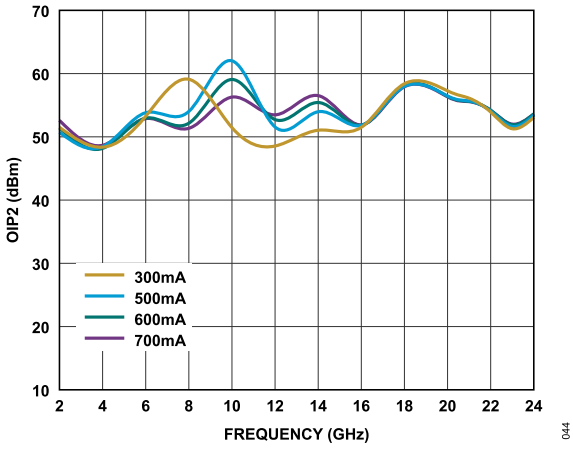

Figure 44. OIP2 vs. Frequency for Various Supply Currents at P_{OUT} per Tone = 32dBm V_{DD} = 28V

TYPICAL PERFORMANCE CHARACTERISTICS

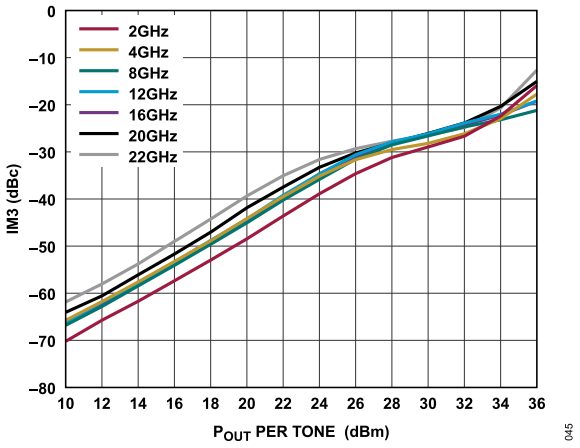

Figure 45. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 28V, I_{DQ} = 600mA

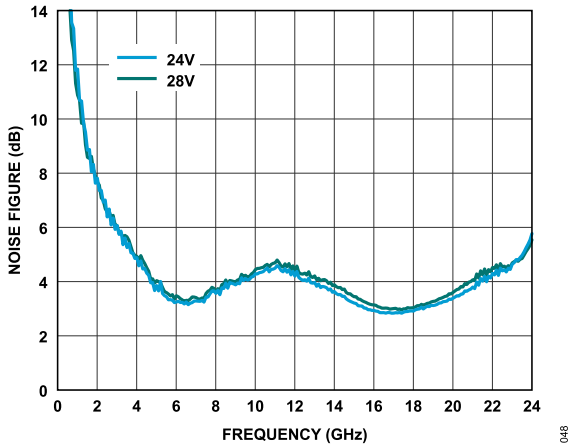

Figure 48. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

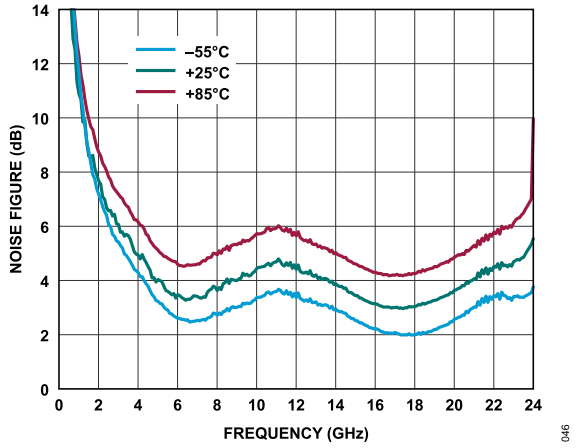

Figure 46. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

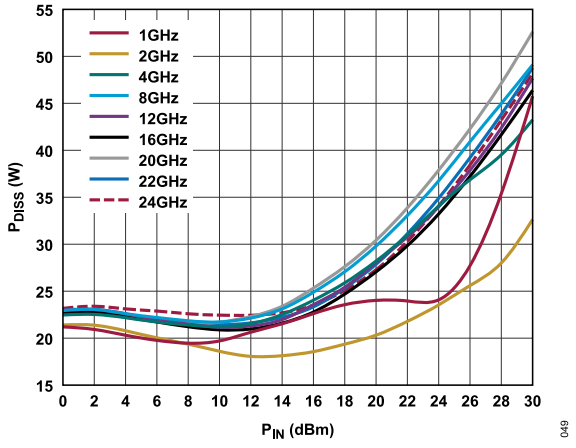

Figure 49. P_{DISS} vs. P_{IN} for Various Frequencies at T_{CASE} = 85°C, V_{DD} = 28V, I_{DQ} = 600mA

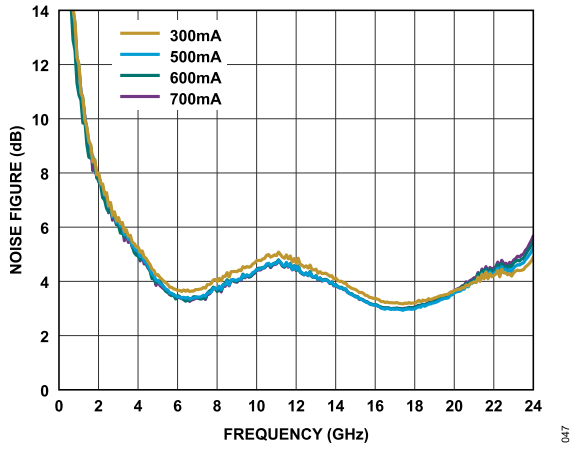

Figure 47. Noise Figure vs. Frequency for Various Supply Currents, V_{DD} = 28V

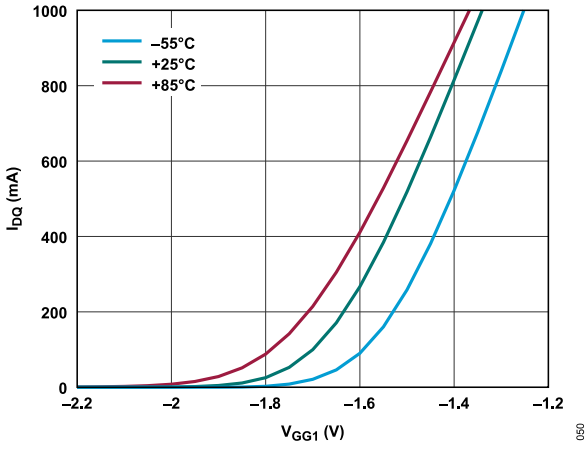

Figure 50. I_{DQ} vs. V_{GG1} for Various Temperatures, V_{DD} = 28V

TYPICAL PERFORMANCE CHARACTERISTICS

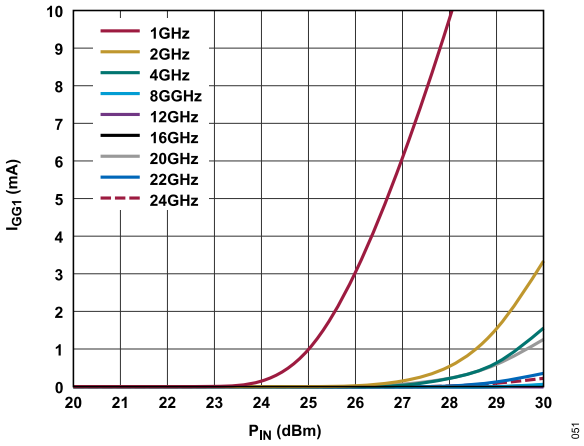

Figure 51. I_{GG1} vs. P_{IN} for Various Frequencies at V_{DD} = 28V, I_{DQ} = 600mA at 85°C

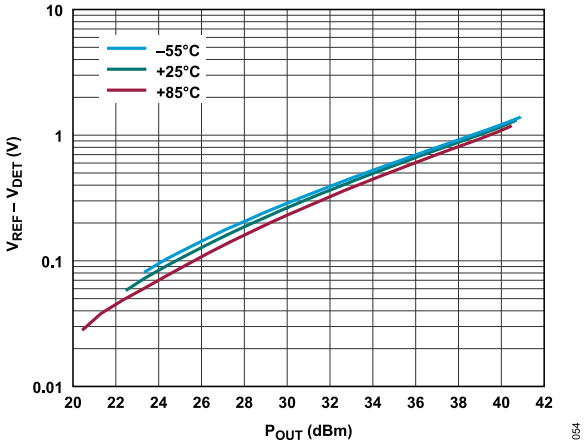

Figure 54. $V_{REF} – V_{DET}$ vs. P_{OUT} for Various Temperature at 20GHz, V_{DD} = 28V, I_{DQ} = 600mA

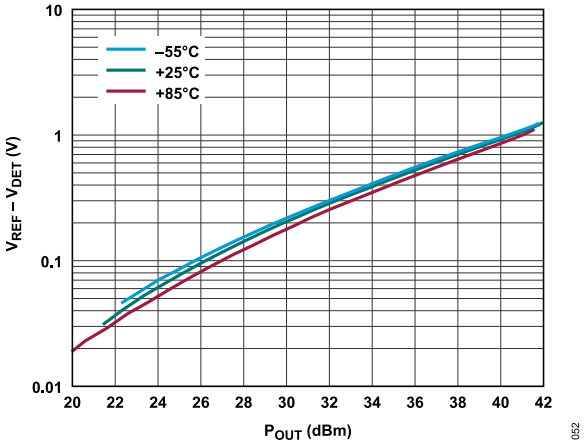

Figure 52. $V_{REF} – V_{DET}$ vs. P_{OUT} for Various Temperature at 12GHz, V_{DD} = 28V, I_{DQ} = 600mA

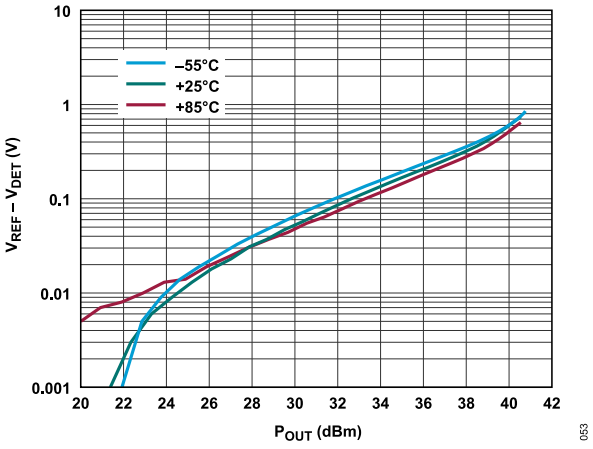

Figure 53. $V_{REF} – V_{DET}$ vs. P_{OUT} for Various Temperature at 4GHz, V_{DD} = 28V, I_{DQ} = 600mA

THEORY OF OPERATION

The ADPA1112CHIP is a GaN power amplifier with cascaded gain stages that are biased by a positive drain supply (V_{DD1} and V_{DD2}) and an externally applied negative gate voltage (V_{GG1}). A nominal 28V is applied to the first and second stage drains (VDD1 and VDD2) and a negative voltage is applied to VGG1 to set the total I_{DQ} to 600mA nominal.

When biased as described, the ADPA1112CHIP operates in Class AB, resulting in the maximum PAE at saturation. The ADPA1112CHIP features integrated RF chokes for each drain plus on-chip DC blocking of the RFIN and RFOUT ports.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF $P_{OUT.}$ When the diode is DC biased, the diode rectifies the coupled RF power and makes it available for measurement as a DC voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit without the coupled RF power is available through VREF. Taking the difference of V_{REF} − V_{DET} provides a temperature-compensated signal that is proportional to the RF output.

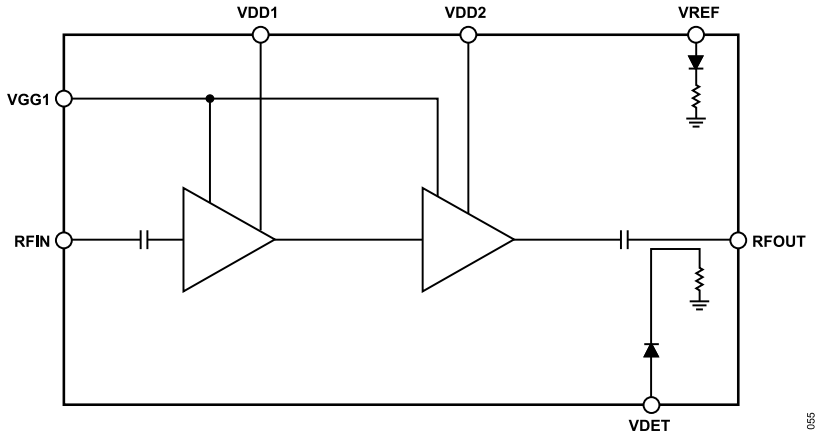

Figure 55. Basic Block Diagram

APPLICATIONS INFORMATION

POWER-UP SEQUENCE

To turn on the ADPA1112CHIP, take the following steps:

1. Connect the power supply grounds to GND.
2. Set V_{GG1} to −4V.
3. Set V_{DD1} and V_{DD2} to 28V.
4. Adjust V_{GG1} more positive to achieve an I_{DQ} of 600mA, approximately −2V.
5. Apply the RF signal.

POWER-DOWN SEQUENCE

To turn off the ADPA1112CHIP, take the following steps:

1. Turn off the RF signal.
2. Set V_{GG1} to −4V to achieve an I_{DQ} of 0mA.
3. Set the voltage on V_{DD1} and V_{DD2} to 0V.
4. Increase V_{GG1} to 0V.

OPERATION LESS THAN 2GHz

Though the ADPA1112CHIP is specified for operation from 2GHz to 22GHz, there may be uses for the device as low as 1GHz. Approaching saturation at less than 2GHz, the gate current may increase more than its 7.2mA absolute maximum rating. For typical I_{GG1} vs. P_{IN} performance, see Figure 51. To limit that current, a series resistor can be inserted in the gate line. Note that the series resistor may affect performance.

TYPICAL APPLICATION CIRCUIT

Figure 56 shows the typical application circuit.

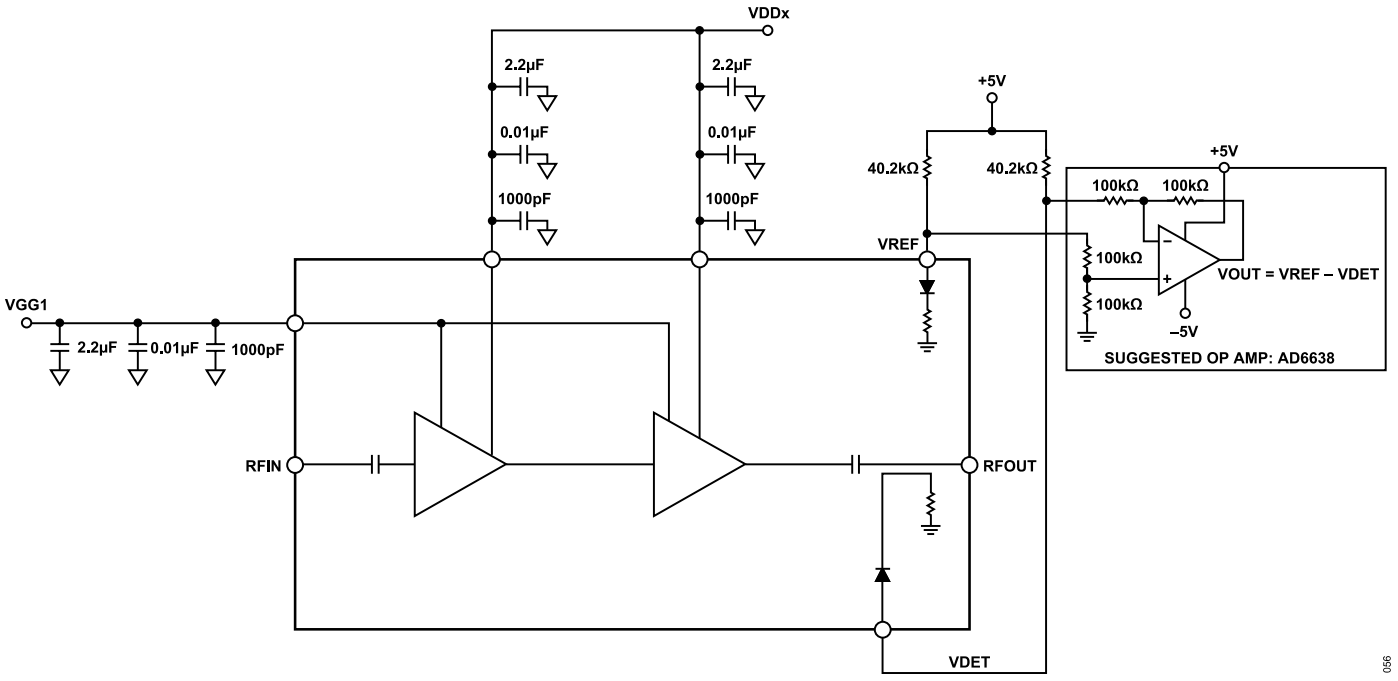

Figure 56. Typical Application Circuit

ASSEMBLY DIAGRAM

Figure 57 shows the assembly diagram for the ADPA1112CHIP.

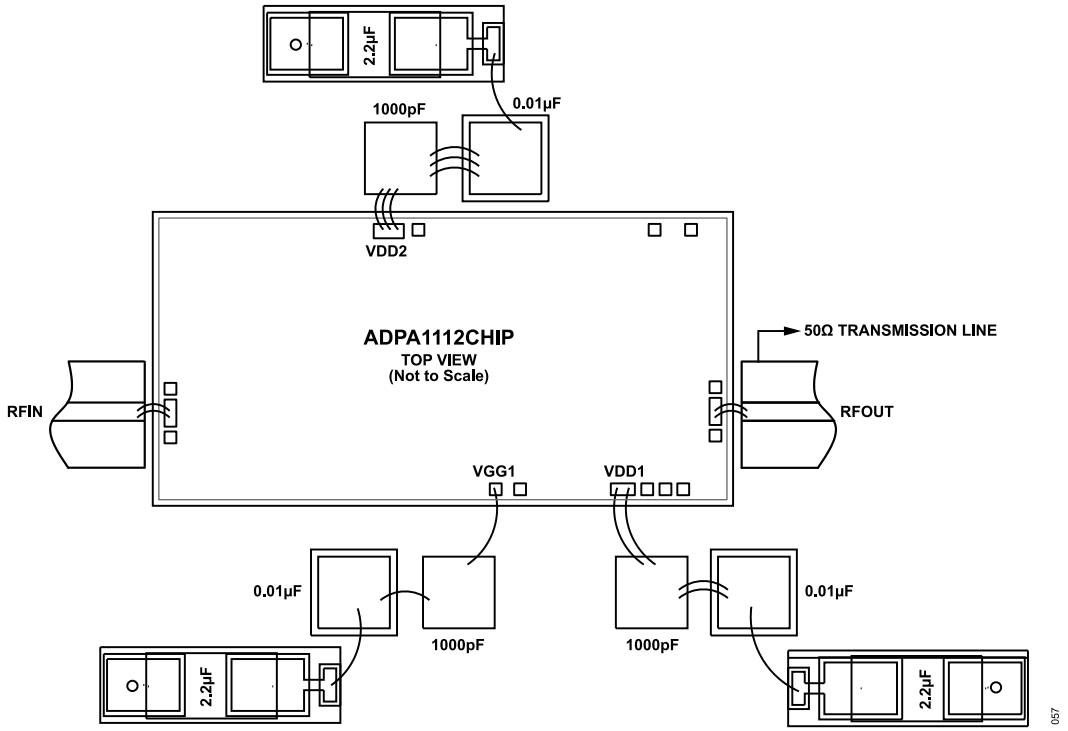

Figure 57. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE, GAN, MONOLITHIC MICROWAVE ICS (MMICS)

Attach the die directly to the ground plane with high thermal conductive epoxy (see the Handling Precaution section, the Mounting section, and the Wire Bonding section).

Place the microstrip substrates as close to the die as possible to wire bond length. Typical die to substrate spacing is 0.076mm to 0.152mm (3mil to 6mil).

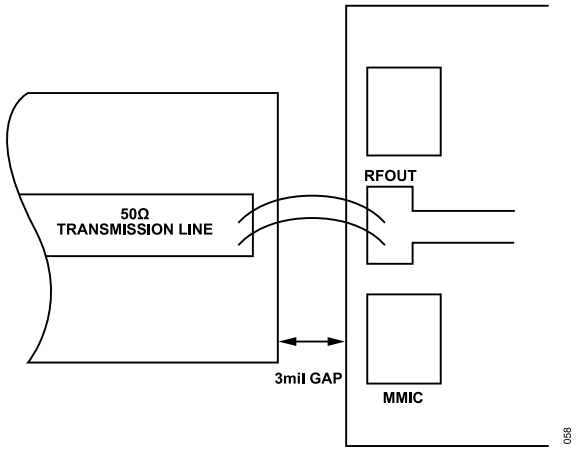

Figure 58. Input Wire Bonding and Substrate Spacing

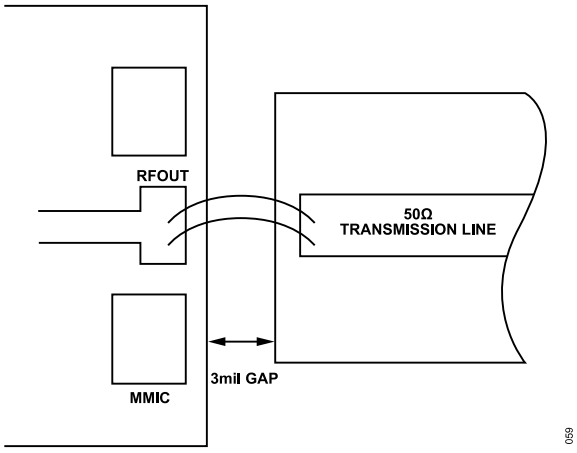

Figure 59. Output Wire Bonding and Substrate Spacing

HANDLING PRECAUTION

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle-based or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all dies in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers.

MOUNTING

Before the die is attached, apply enough high thermal conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

WIRE BONDING

RF bonds made with 1mil gold wire are recommended for the RF pads. These bonds must be thermosonically bonded with a force of 40g to 60g. Thermosonically bonded DC bonds of 0.025mm diameter (0.001in) are recommended. Create ball bonds with a force of 40g to 50g, and wedge bonds with a force of 18g to 22g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31mm (12mil).

OUTLINE DIMENSIONS

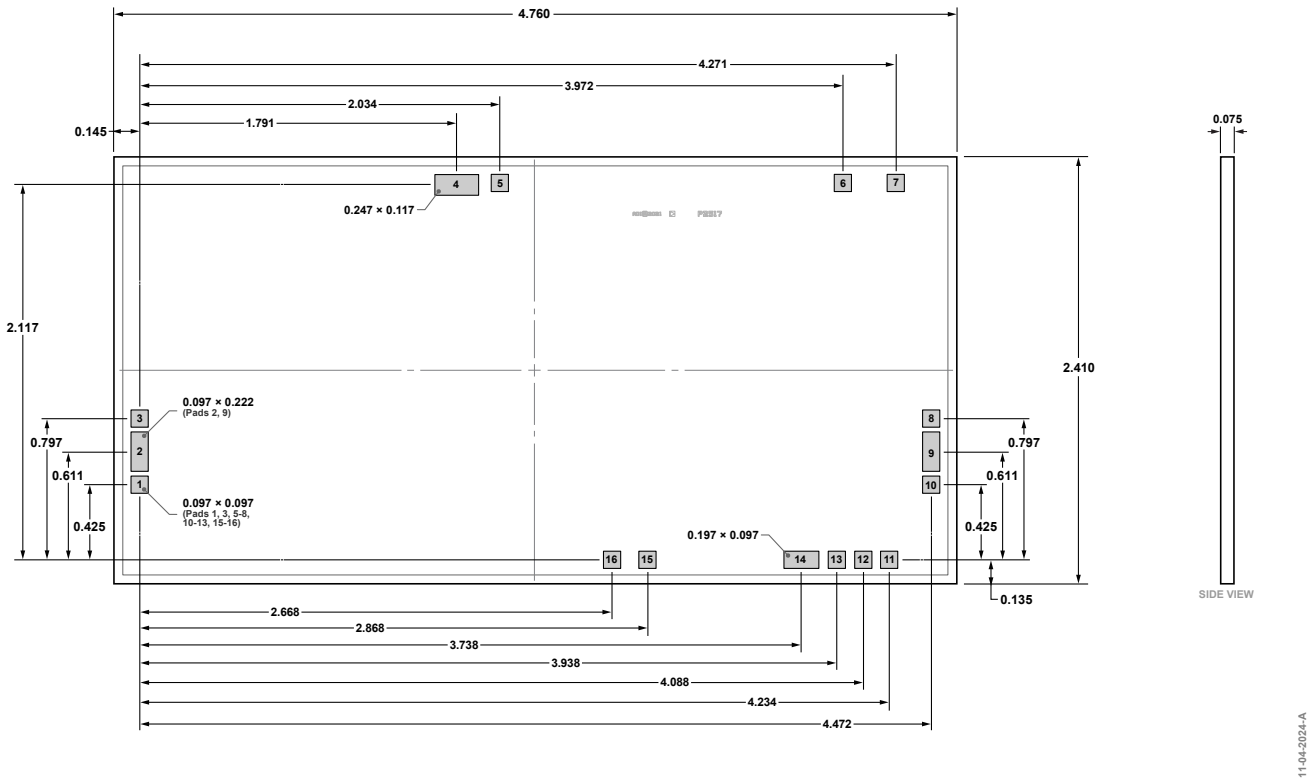

Figure 60. 16-Pad Bare Die [CHIP]
(C-16-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADPA1112CHIP	−55°C to +85°C	16-Pad Bare Die [CHIP]	C-16-6
ADPA1112CHIP-SX	−55°C to +85°C	Die Sample Pack	C-16-6

[1] Z = RoHS Compliant Part.