0.5GHz to 9GHz, Digitally Tunable, High-Pass Filters and Low-Pass Filters

FEATURES

- Digitally tunable, high-pass and low-pass tuning
- Suboctave bandwidths with additional user adjustability
- Rejection: 40dB
- Single-chip replacement for discrete filter banks
- Compact, 8mm × 8mm × 1.07mm LGA package

APPLICATIONS

- Land mobile radios
- Test and measurement equipment
- Military radars, electronic warfare, and electronic countermeasures
- Satellite communications
- Industrial and medical equipment

GENERAL DESCRIPTION

The ADMV8809 is a fully monolithic microwave IC (MMIC) that features digitally selectable operating frequencies. The device features four independently controlled high-pass filters (HPFs) and low-pass filters (LPFs) that span the 0.5GHz to 9GHz frequency range (f_{CENTER}).

The flexible architecture of the ADMV8809 allows the 3dB cutoff frequency (f_{3dB}) of the high-pass and low-pass filters to be controlled independently. The digital logic control on each filter is 3-bits wide (eight states) and controls the on-chip reactive elements to adjust the f_{3dB}. The typical insertion loss is <6.2dB. When using the HPF = LPF state, the filter has 40dB rejection for the low side at 0.5 × f_{U3dB} and for the high side at 2 × f_{L3dB}, which is ideally suited for minimizing system second-order intercept (IP2) and harmonics.

This tunable filter can be used as a smaller alternative to large switched filter banks and discrete component-based tunable filters, and the ADMV8809 provides a dynamically adjustable solution in advanced communications applications.

FUNCTIONAL BLOCK DIAGRAM

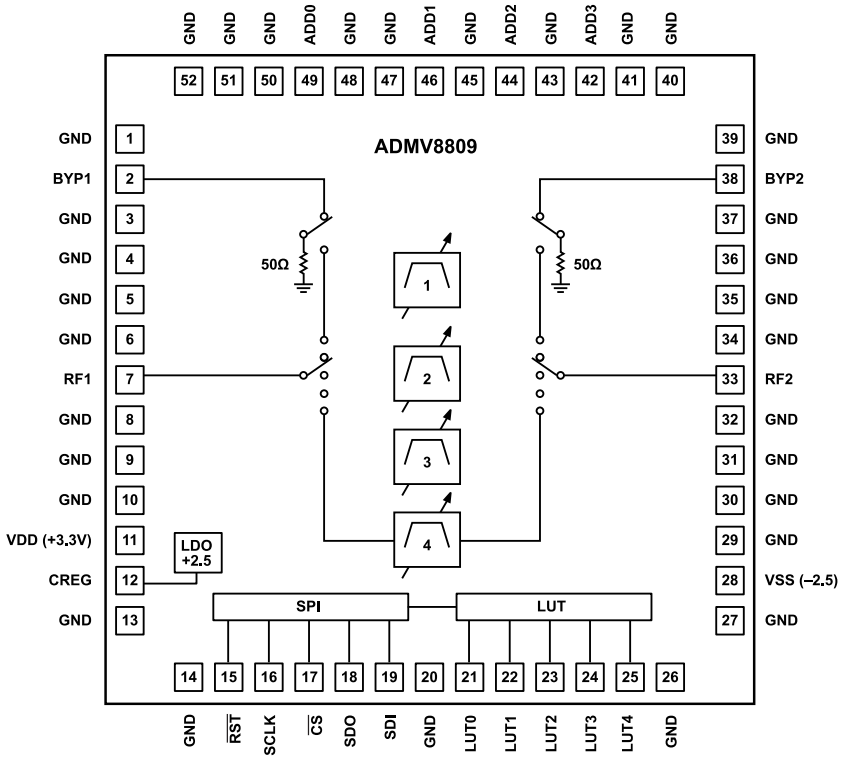

Figure 1. Functional Block Diagram

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REVISION HISTORY

10/2025—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, HPF and LPF at same states, unless otherwise noted.

Table 1. Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE (f_{CENTER})					
Bypass Configuration	<0.01		13	GHz	
Filter Band 1		0.55		GHz	HPF and LPF, State 0
		1.05		GHz	HPF and LPF, State 7
Filter Band 2		1.23		GHz	HPF and LPF, State 0
		2.25		GHz	HPF and LPF, State 7
Filter Band 3		2.4		GHz	HPF and LPF, State 0
		4.6		GHz	HPF and LPF, State 7
Filter Band 4		5		GHz	HPF and LPF, State 0
		8.2		GHz	HPF and LPF, State 7
USABLE PASS-BAND FREQUENCY					
Filter Band 1					
Lower Pass-Band Frequency (f_{L3dB})		0.43		GHz	HPF, State 0
Upper Pass-Band Frequency (f_{U3dB})		1.27		GHz	LPF, State 7
Filter Band 2					
f_{L3dB}		0.97		GHz	HPF, State 0
f_{U3dB}		2.71		GHz	LPF, State 7
Filter Band 3					
f_{L3dB}		1.84		GHz	HPF, State 0
f_{U3dB}		5.6		GHz	LPF, State 7
Filter Band 4					
f_{L3dB}		3.74		GHz	HPF, State 0
f_{U3dB}		10.08		GHz	LPF, State 7
BANDWIDTH (3dB)		40		%	HPF and LPF same state (average value for all bands); bandwidth can be varied from 9% to 100% by using different combinations of HPF and LPF states
RESOLUTION					
Filter Band 1					
HPF		0.06		GHz	
LPF		0.09		GHz	
Filter Band 2					
HPF		0.12		GHz	
LPF		0.17		GHz	
Filter Band 3					
HPF		0.25		GHz	
LPF		0.37		GHz	
Filter Band 4					
HPF		0.38		GHz	
LPF		0.57		GHz	
REJECTION (40dB)					
Low-Side		0.5 × f_{U3dB}		GHz	
High-Side		2× f_{L3dB}		GHz	
RE-ENTRY FREQUENCY		>40		GHz	>40dB for Band 1 to Band 3 and >30dB for Band 4

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INSERTION LOSS					
Bypass Configuration		<1.5		dB	
Filter Band 1		6.2		dB	
Filter Band 2		4.7		dB	
Filter Band 3		4.5		dB	
Filter Band 4		5		dB	
RETURN LOSS		>10		dB	
DYNAMIC PERFORMANCE					
Input Compression (P0.1dB)					
Bypass Configuration		27		dBm	
Filter Band 1		26.10		dBm	
Filter Band 2		26.83		dBm	
Filter Band 3		27		dBm	
Filter Band 4		24.66		dBm	
Input Third-Order Intercept (IP3)					Input power (P_{IN}) = 10dBm per tone
Bypass Configuration		52		dBm	
Filter Band 1		47		dBm	
Filter Band 2		51		dBm	
Filter Band 3		50		dBm	
Filter Band 4		46		dBm	
Group Delay		<5.4		ns	
Amplitude Settling Time		<0.5		µs	
Drift Rate					
Amplitude					
Filter Band 1		0.01		dB/°C	HPF = LPF, State 4
Filter Band 2		0.01		dB/°C	HPF = LPF, State 4
Filter Band 3		0.01		dB/°C	HPF = LPF, State 4
Filter Band 4		0.01		dB/°C	HPF = LPF, State 4
Frequency					
Filter Band 1		−68		ppm/°C	HPF = LPF, State 4
Filter Band 2		−65		ppm/°C	HPF = LPF, State 4
Filter Band 3		−99		ppm/°C	HPF = LPF, State 4
Filter Band 4		−105		ppm/°C	HPF = LPF, State 4
SUPPLY VOLTAGE					
VSS	−2.6	−2.5	−2.4	V	
VDD	3.2	3.3	3.4	V	
SUPPLY CURRENT (STATIC)					
Static					
VSS Current (I_{SS})		2		µA	
VDD Current (I_{DD})		700		µA	
Dynamic					
I_{DD}		f_{SCLK}/4		mA	Where f_{SCLK} is the SCLK toggle frequency in MHz, for example, continuous serial peripheral interface (SPI) writing at 10MHz yields 2.5mA of dynamic I_{DD}
LOGIC INPUT AND OUTPUT ($\overline{RST}$, $\overline{CS}$, SCLK, SDI, AND SDO)					
Logic Low	−0.3	0	+0.8	V	
Logic High	1.2	3.3	3.6	V	

SPECIFICATIONS

TIMING SPECIFICATIONS

Table 2. Timing Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
t_1	10			ns	$\overline{RST}$ low time to perform reset
	10			ns	SCLK cycle time (write)
t_2	20			ns	SCLK cycle time (read)
t_3	2.5			ns	SCLK high time
t_4	2.5			ns	SCLK low time
t_5	5			ns	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_6	2			ns	SCLK rising edge to hold time
t_7	5			ns	Minimum $\overline{CS}$ high time for latching in data (for multiple SPI transactions)
t_8	5			ns	$\overline{CS}$ rising edge to next SCLK rising edge ignore
t_9	5			ns	SDI data setup time
t_{10}	2			ns	SDI data hold time
t_{11}		6		ns	SCLK falling edge to SDO valid (load capacitance (C_L) = 10 pF)
t_{12}		5		ns	SDO rise and fall time (C_L = 10 pF)
t_{13}		4		ns	$\overline{CS}$ rising edge to SDO tristate (C_L = 10 pF)
t_{14}	10			ns	$\overline{CS}$ rising edge (end of SPI transaction) to lookup table (LUT) rising edge time (entering LUT control mode)
t_{15}	10			ns	LUT setup time LUT rising edge to $\overline{CS}$ rising edge (LUT control mode)
t_{16}	2			ns	LUT hold time $\overline{CS}$ rising edge to $\overline{CS}$ high (LUT control mode)
t_{17}	2.5			ns	$\overline{CS}$ high time (LUT control mode)
t_{18}	2.5			bs	$\overline{CS}$ low time (LUT control mode)

Timing Diagram

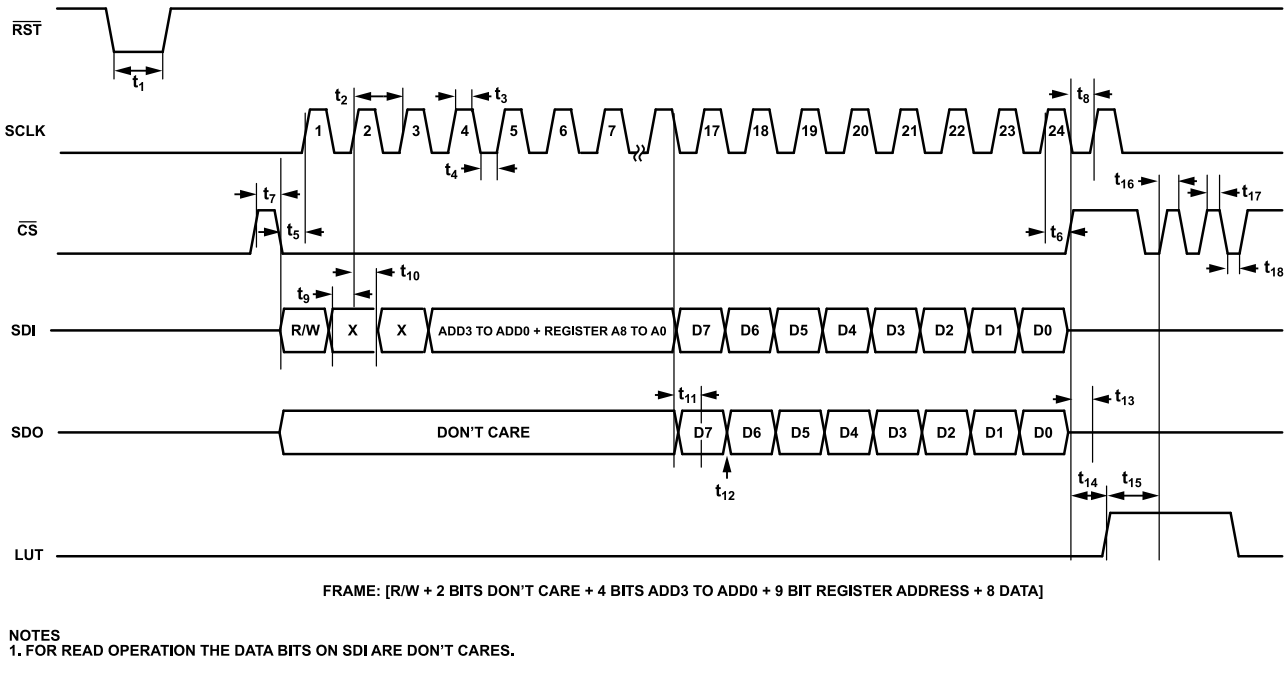

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
SUPPLY	
VDD	–0.3V to +3.6V
VSS	–2.75V to +0.3V
Digital Control Inputs	
Voltage	–0.3V to VDD + 0.3V
Current	2mA
Continuous RF Input Power	P0.1dB
Temperature	
Operating Range	–40°C to +85°C
Storage Range	–55°C to +150°C
Junction to Maintain 1 Million Hours Mean Time to Failure (MTTF)	135°C
Nominal Junction (Paddle Temperature (T_{PADDLE}) = 85°C)	90°C
Moisture Sensitivity Level (MSL) Rating	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2010.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADMV8809

Table 4. ADMV8809, 52-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx Pins	750	1B
Supply and Digital Pins	1500	1C
FICDM	250	C1

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

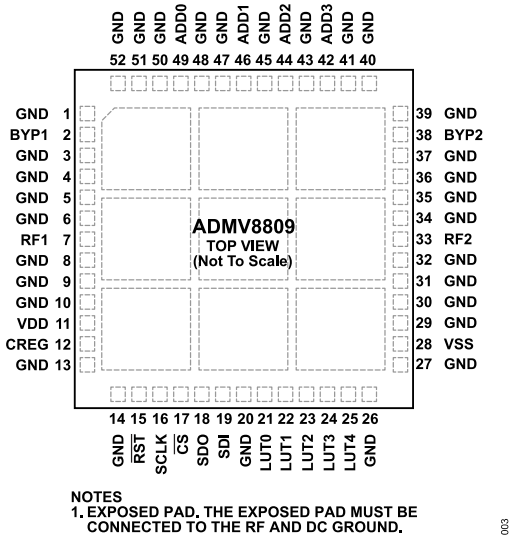

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3 to 6, 8 to 10, 13, 14, 20, 26, 27, 29 to 32, 34 to 37, 39 to 41, 43, 45, 47, 48, 50 to 52	GND	Ground. Connect the GND pins to the RF and DC ground.
2	BYP1	Bypass Pin 1. BYP1 is DC-coupled and matched to 50Ω. Do not apply an external voltage to BYP1.
7	RF1	RF Pin 1. RF1 is DC-coupled and matched to 50Ω. Do not apply an external voltage to RF1.
11	VDD	The 3.3V Power Supply Pin. Place 0.1µF and 100pF decoupling capacitors close to VDD.
12	CREG	The 2.5V Power Supply Pin. Place 47µF, 0.1µF, and 100pF decoupling capacitors close to CREG.
15	$\overline{RST}$	Chip Reset, 3.3V Logic. Active low. The $\overline{RST}$ pin is internally pulled low with a 268kΩ resistor
16	SCLK	SPI Clock, 3.3V Logic. The SCLK pin is internally pulled low with a 268kΩ resistor.
17	$\overline{CS}$	SPI Chip Select, 3.3V Logic. Active low. The $\overline{CS}$ pin is internally pulled low with a 260kΩ resistor.
18	SDO	SPI Data Output, 3.3V Logic. The SDO pin is a tristate buffer.
19	SDI	SPI Data Input, 3.3V Logic. The SDI pin is internally pulled low with a 268kΩ resistor.
21	LUT0	Filter Address Bit 0, 3.3V logic. The LUT0 pin is internally pulled high with a 268kΩ resistor.
22	LUT1	Filter Address Bit 1, 3.3V logic. The LUT1 pin is internally pulled high with a 268kΩ resistor.
23	LUT2	Filter Address Bit 2, 3.3V logic. The LUT2 pin is internally pulled high with a 268kΩ resistor.
24	LUT3	Filter Address Bit 3, 3.3V logic. The LUT3 pin is internally pulled high with a 268kΩ resistor.
25	LUT4	Filter Address Bit 4, 3.3V logic. The LUT4 pin is internally pulled high with a 268kΩ resistor.
28	VSS	The –2.5V Power Supply Pin. Place 0.1µF and 100pF decoupling capacitors close to VSS.
33	RF2	RF Pin 2. RF2 is DC-coupled and matched to 50Ω. Do not apply an external voltage to RF2.
38	BYP2	Bypass Pin 2. BYP2 is DC-coupled and matched to 50Ω. Do not apply an external voltage to BYP2.
42	ADD3	Chip Address Bit 3, 3.3V logic. The ADD3 pin is internally pulled high with a 268kΩ resistor.
44	ADD2	Chip Address Bit 2, 3.3V logic. The ADD2 pin is internally pulled high with a 268kΩ resistor.
46	ADD1	Chip Address Bit 1, 3.3V logic. The ADD1 pin is internally pulled high with a 268kΩ resistor.
49	ADD0	Chip Address Bit 0, 3.3V logic. The ADD0 pin is internally pulled high with a 268kΩ resistor.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground.

TYPICAL PERFORMANCE CHARACTERISTICS

BAND-PASS CONFIGURATION, FILTER BAND 1

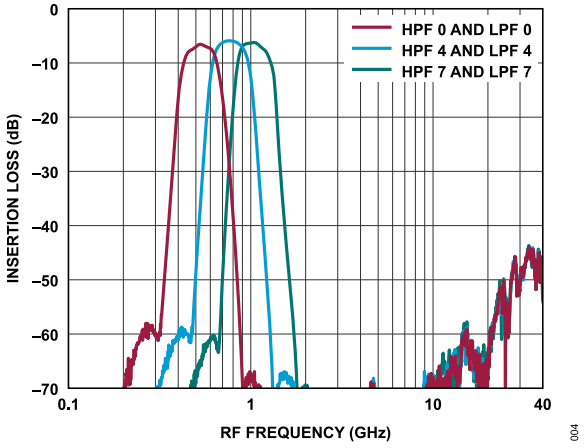

Figure 4. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

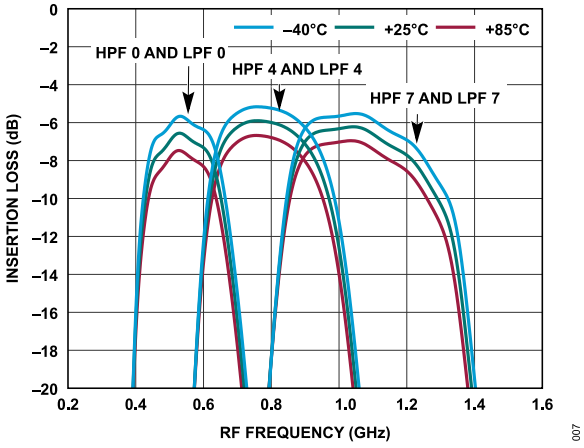

Figure 7. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

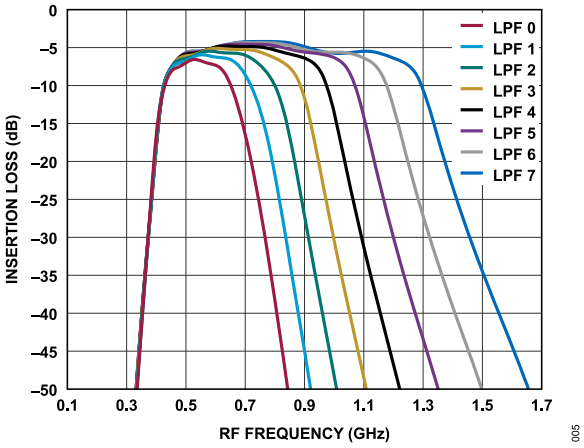

Figure 5. Insertion Loss vs. RF Frequency at HPF, State 0 and Swept LPF State

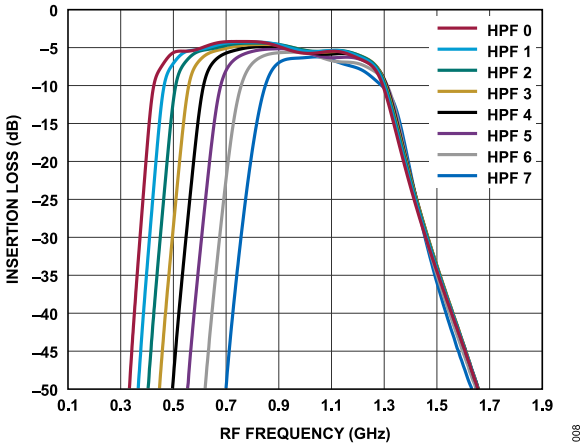

Figure 8. Insertion Loss vs. RF Frequency at LPF, State 7 and Swept HPF State

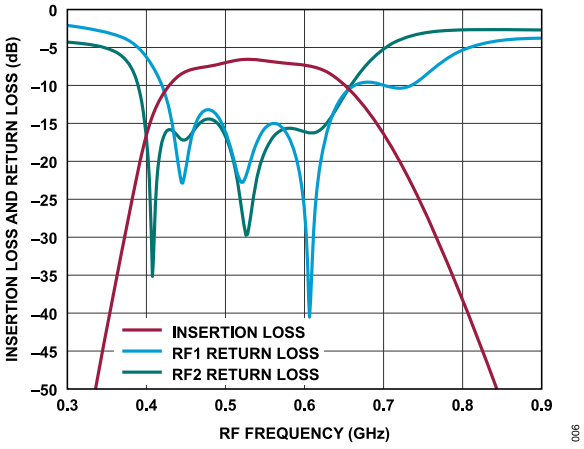

Figure 6. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 0

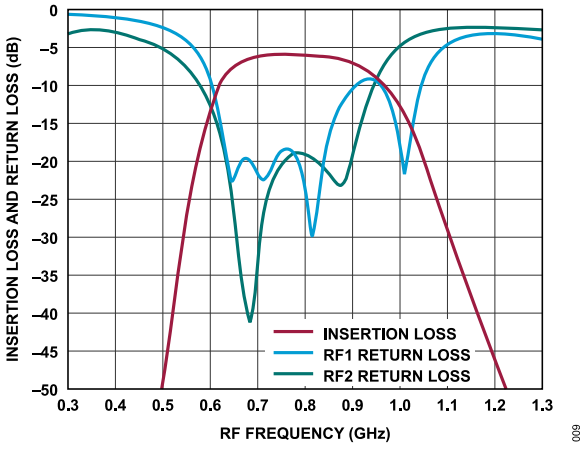

Figure 9. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 4

TYPICAL PERFORMANCE CHARACTERISTICS

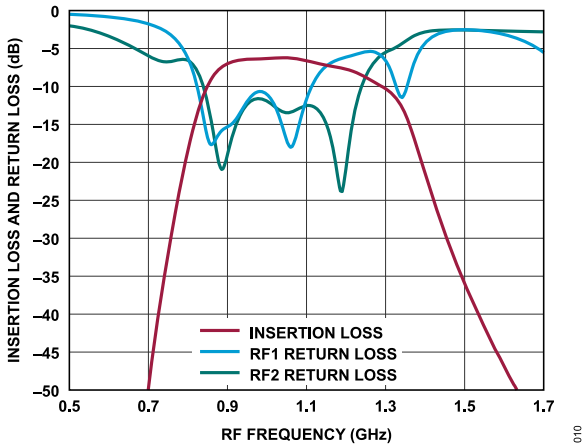

Figure 10. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 7

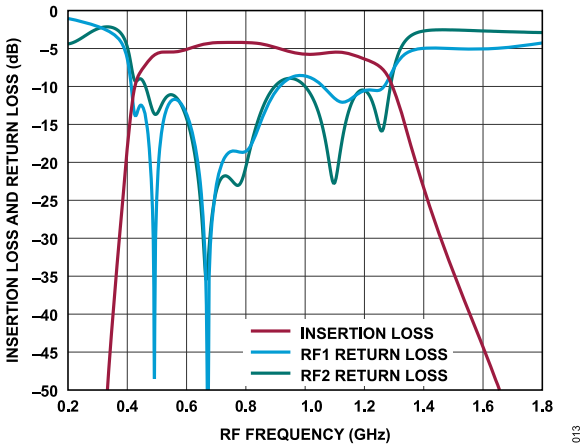

Figure 13. Insertion Loss and Return Loss vs. RF Frequency at HPF, State 0 and LPF, State 7

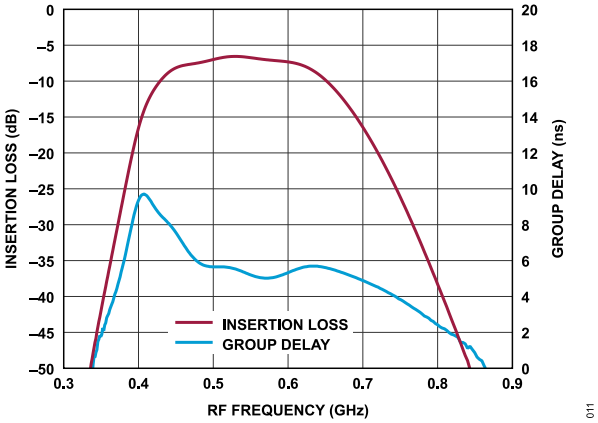

Figure 11. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 0

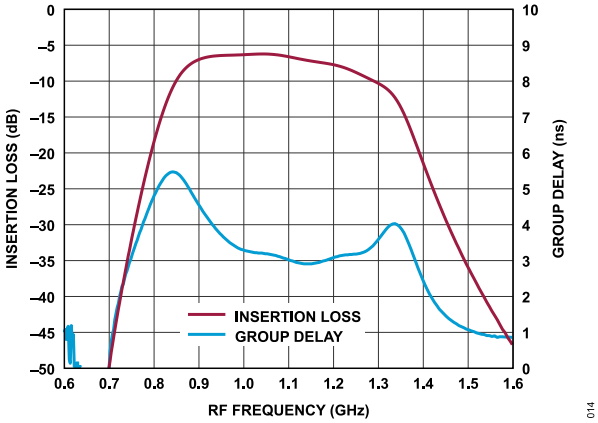

Figure 14. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 7

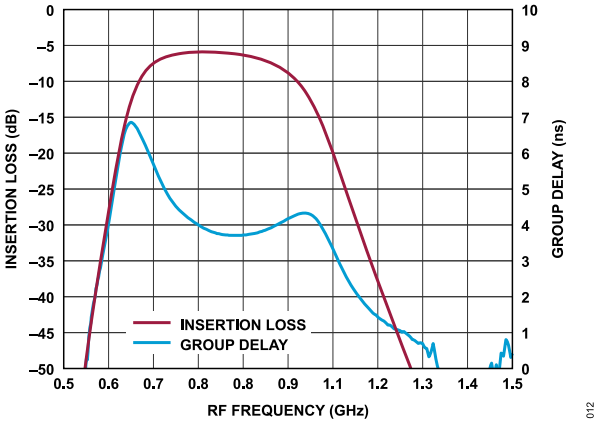

Figure 12. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 4

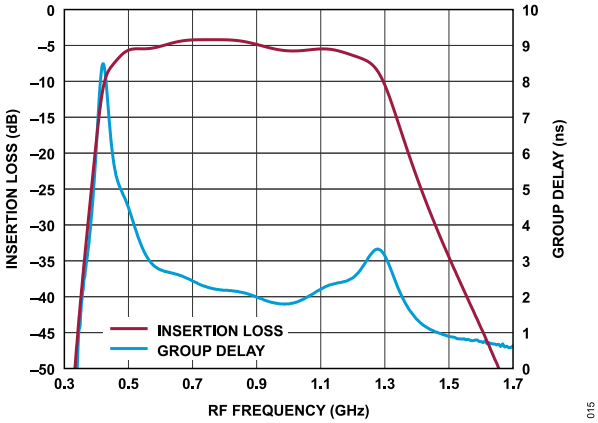

Figure 15. Insertion Loss and Group Delay vs. RF Frequency at HPF, State 0 and LPF, State 7

TYPICAL PERFORMANCE CHARACTERISTICS

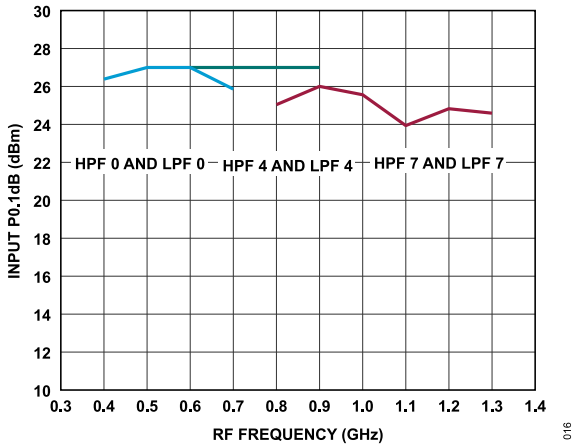

Figure 16. Input P0.1dB vs. RF Frequency at HPF and LFP, State 0, State 4, and State 7

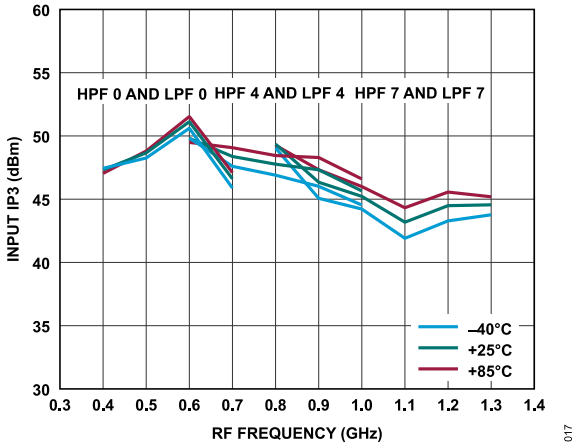

Figure 17. Input IP3 vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

BAND-PASS CONFIGURATION, FILTER BAND 2

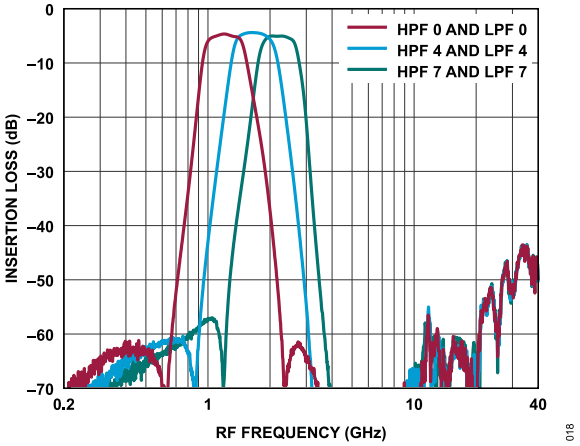

Figure 18. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

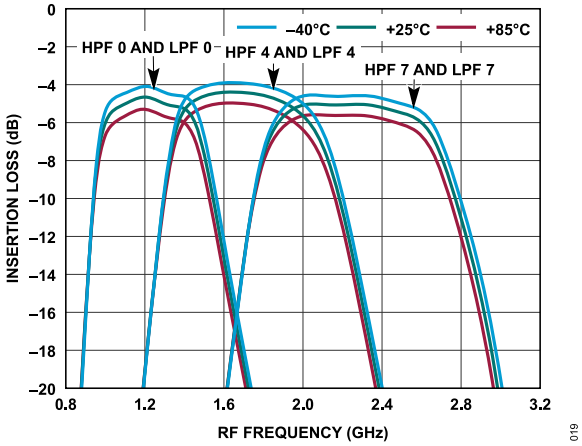

Figure 21. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

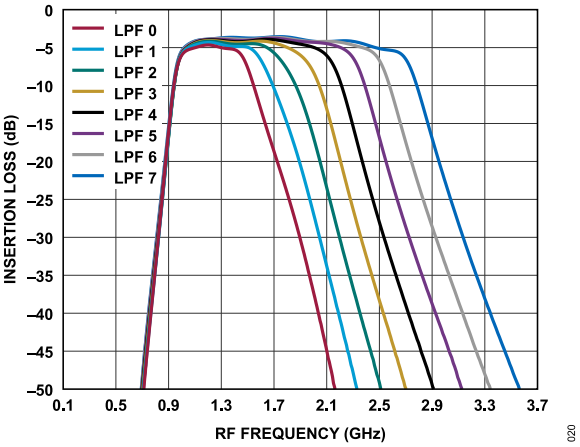

Figure 19. Insertion Loss vs. RF Frequency at HPF, State 0 and Swept LPF State

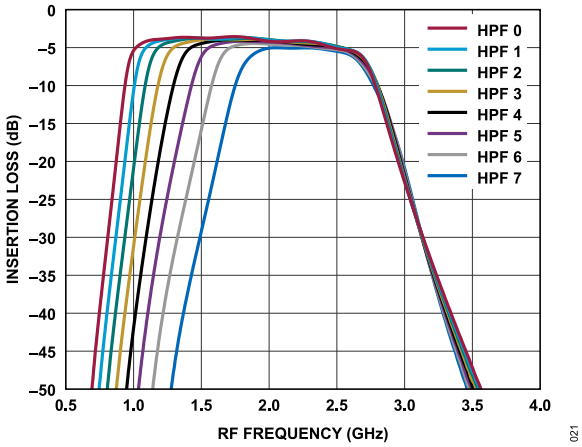

Figure 22. Insertion Loss vs. RF Frequency at LPF, State 7 and Swept HPF State

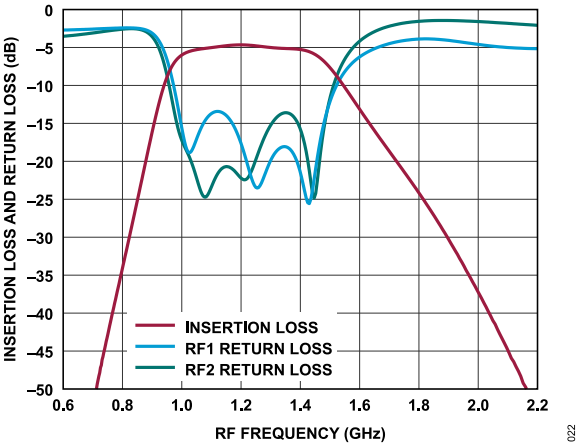

Figure 20. Insertion Loss and Return Loss vs. RF Frequency at State 0

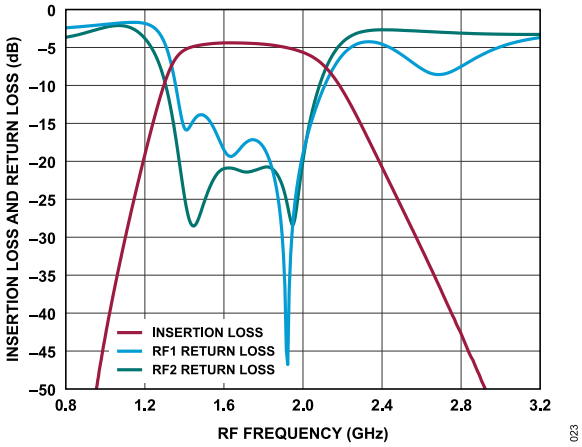

Figure 23. Insertion Loss and Return Loss vs. RF Frequency at State 4

TYPICAL PERFORMANCE CHARACTERISTICS

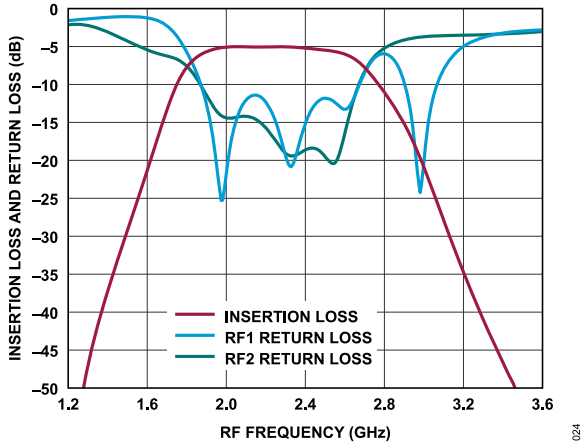

Figure 24. Insertion Loss and Return Loss vs. RF Frequency at State 7

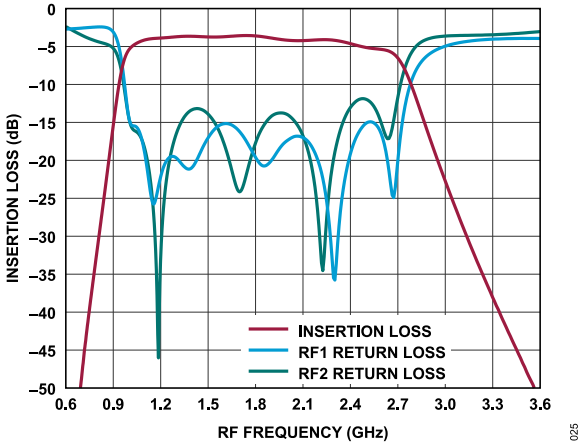

Figure 27. Insertion Loss and Return Loss vs. RF Frequency at HPF, State 0 and LPF, State 7

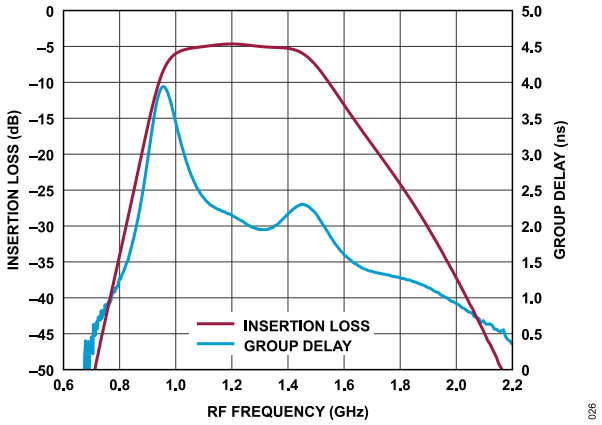

Figure 25. Insertion Loss and Group Delay vs. RF Frequency at State 0

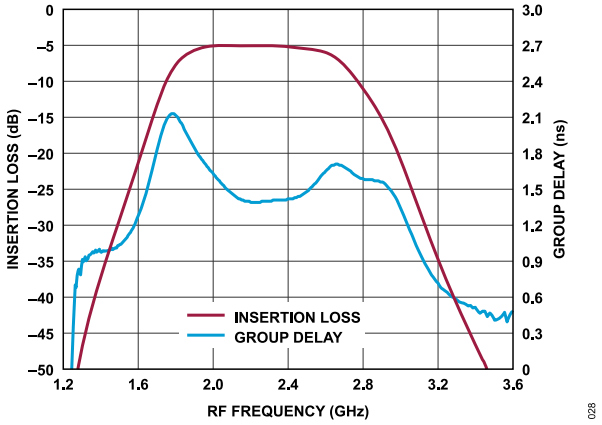

Figure 28. Insertion Loss and Group Delay vs. RF Frequency at State 7

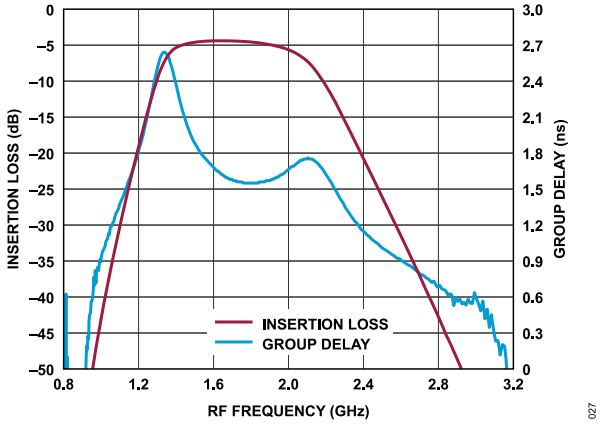

Figure 26. Insertion Loss and Group Delay vs. RF Frequency at State 4

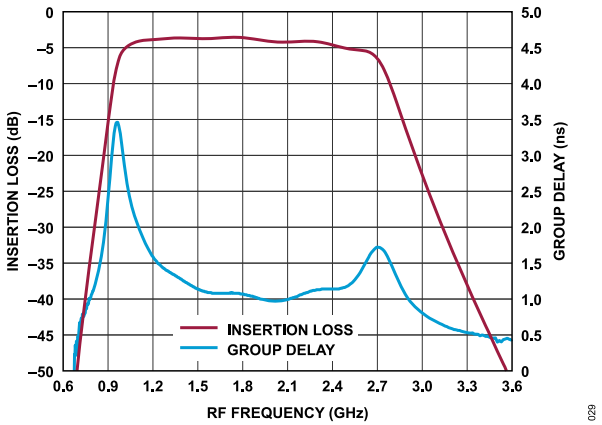

Figure 29. Insertion Loss and Group Delay vs. RF Frequency at HPF, State 0 and LPF, State 7

TYPICAL PERFORMANCE CHARACTERISTICS

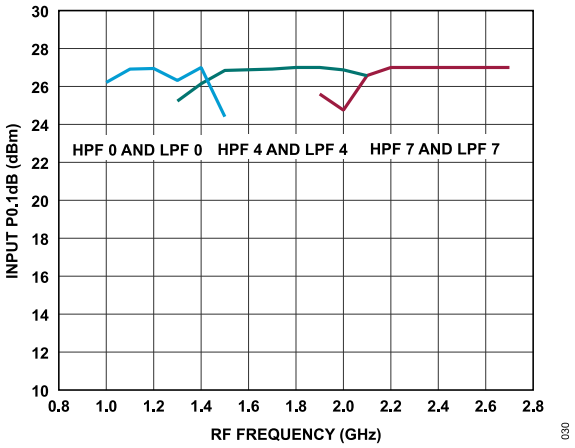

Figure 30. Input P0.1dB vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

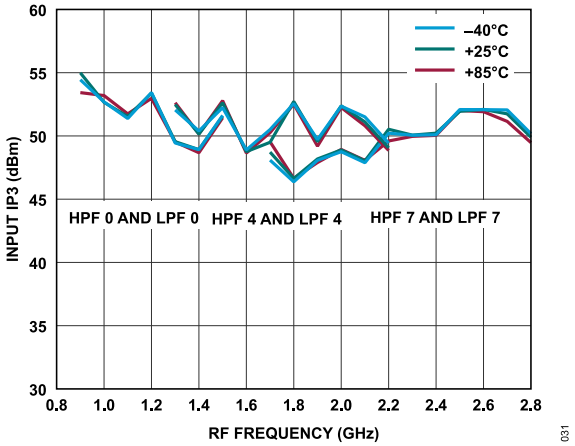

Figure 31. Input IP3 vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

BAND-PASS CONFIGURATION, FILTER BAND 3

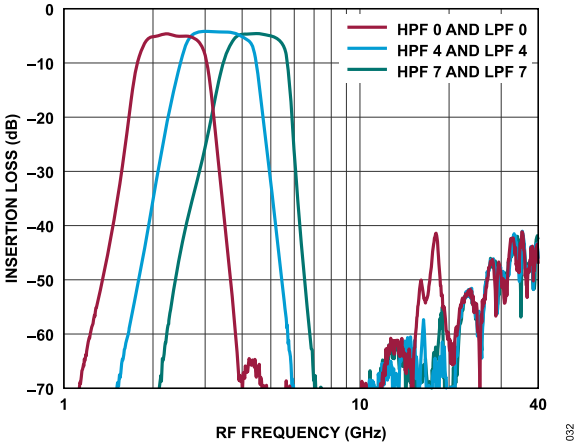

Figure 32. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

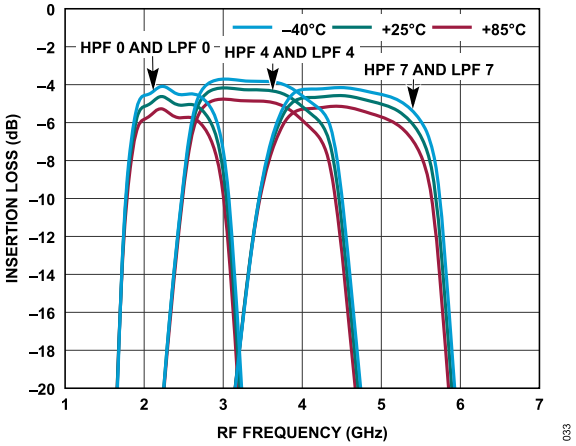

Figure 35. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

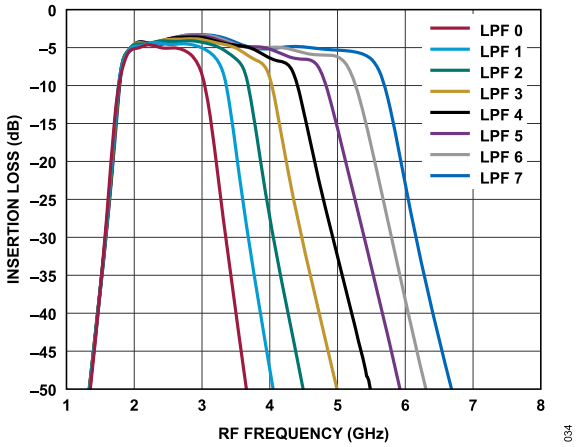

Figure 33. Insertion Loss vs. RF Frequency at HPF, State 0 and Swept LPF State

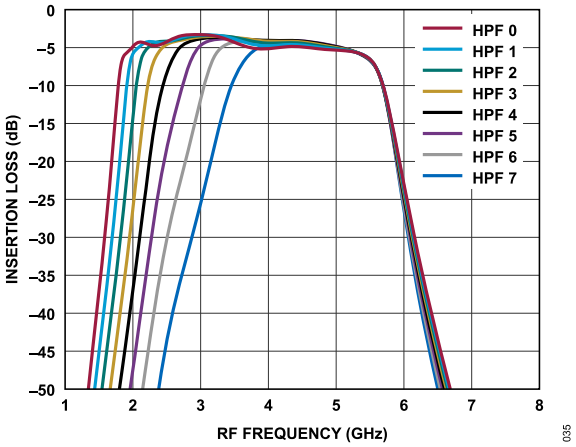

Figure 36. Insertion Loss vs. RF Frequency at LPF, State 7 and Swept HPF State

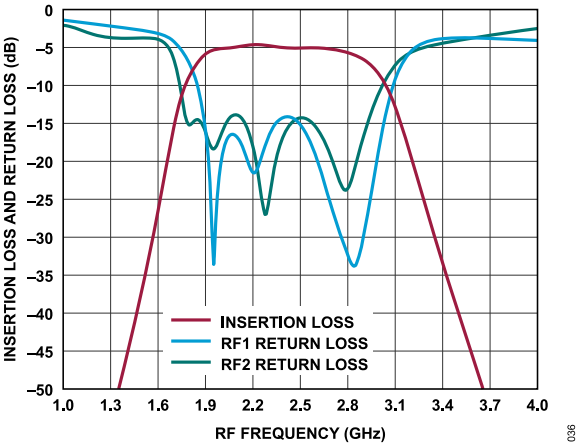

Figure 34. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 0

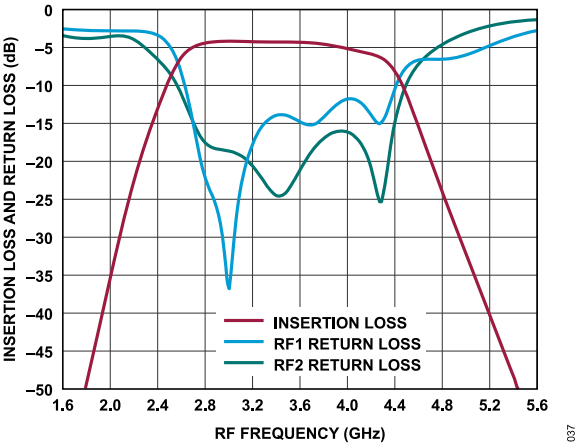

Figure 37. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 4

TYPICAL PERFORMANCE CHARACTERISTICS

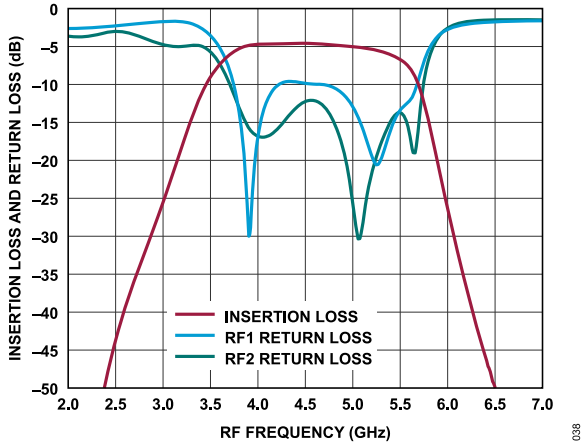

Figure 38. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 7

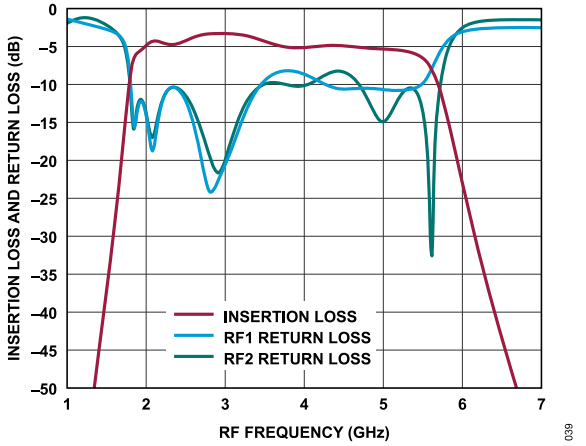

Figure 41. Insertion Loss and Return Loss vs. RF Frequency at HPF, State 0 and LPF, State 7

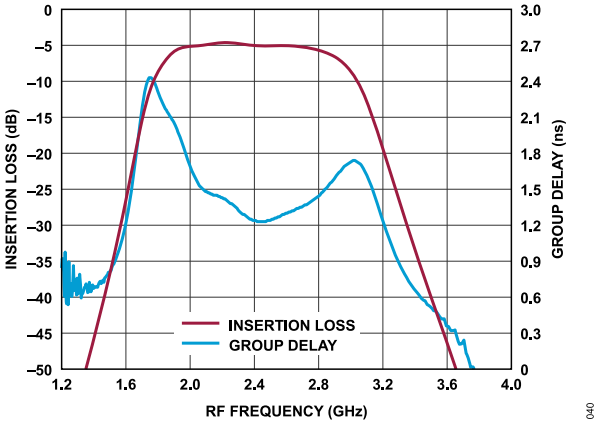

Figure 39. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 0

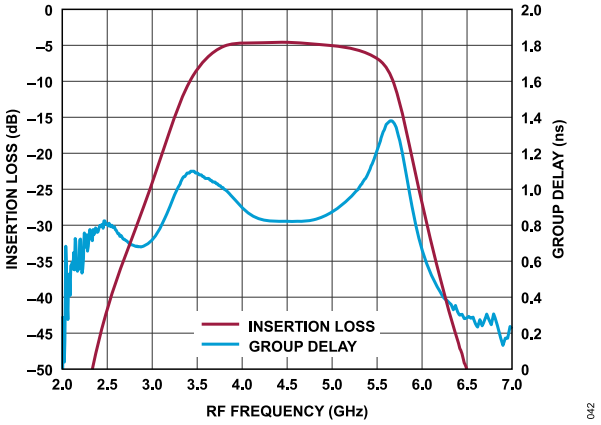

Figure 42. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 7

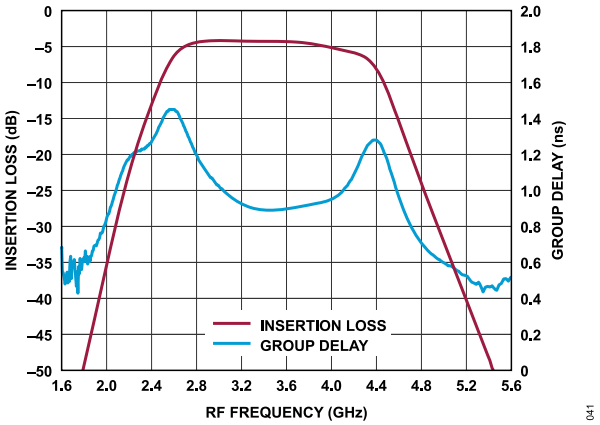

Figure 40. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 4

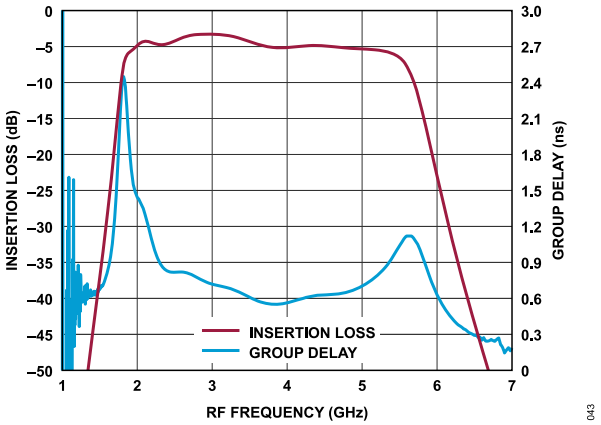

Figure 43. Insertion Loss and Group Delay vs. RF Frequency at HPF, State 0 and LPF, State 7

TYPICAL PERFORMANCE CHARACTERISTICS

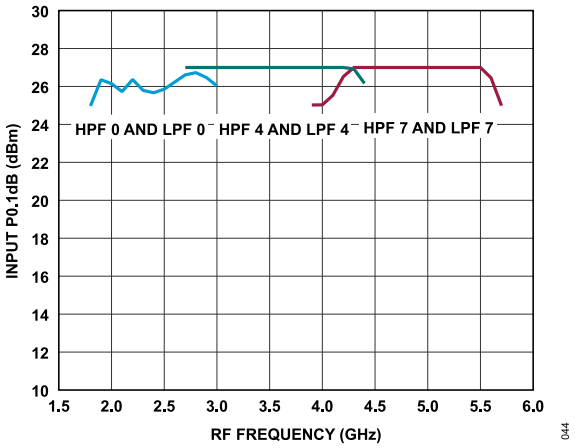

Figure 44. Input P0.1dB vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

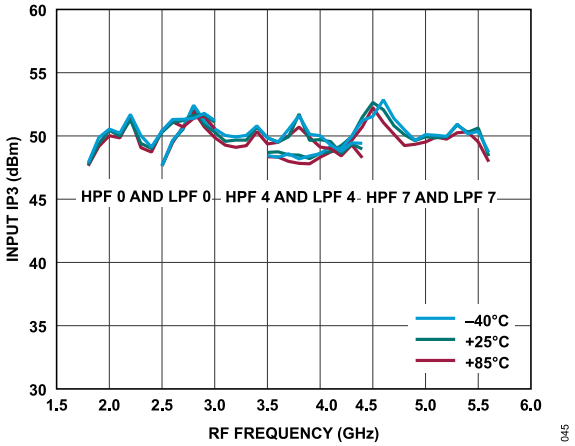

Figure 45. Input IP3 vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

BAND-PASS CONFIGURATION, FILTER BAND 4

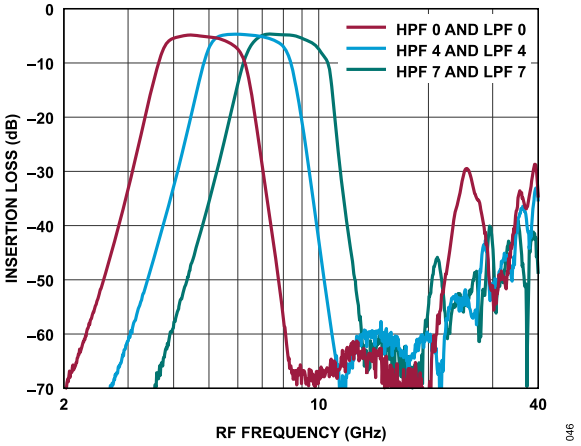

Figure 46. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

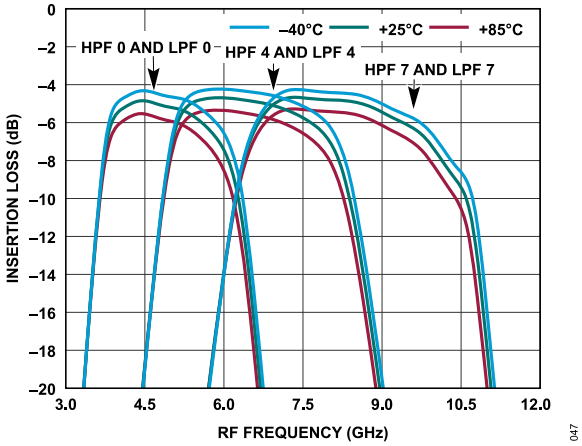

Figure 49. Insertion Loss vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

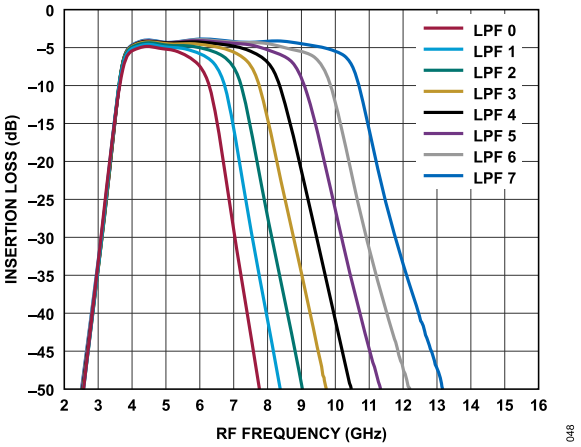

Figure 47. Insertion Loss vs. RF Frequency at HPF, State 0 and Swept LPF State

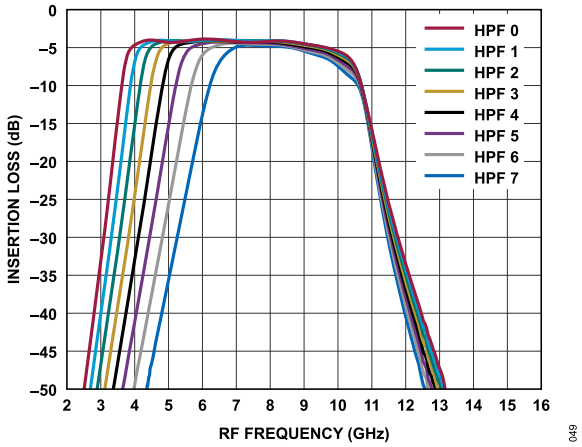

Figure 50. Insertion Loss vs. RF Frequency at LPF, State 7 and Swept HPF State

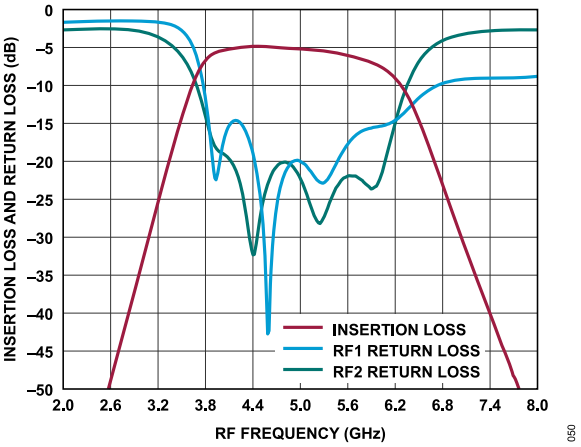

Figure 48. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 0

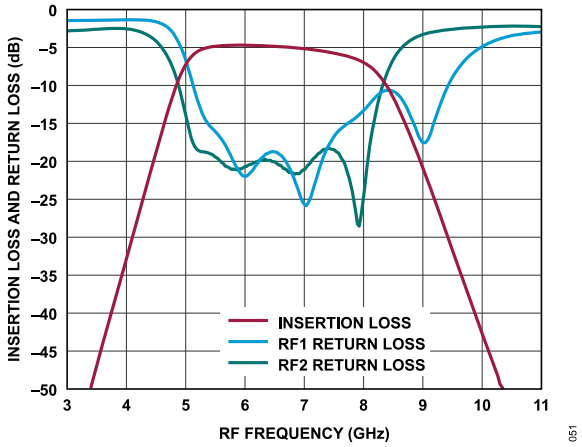

Figure 51. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 4

TYPICAL PERFORMANCE CHARACTERISTICS

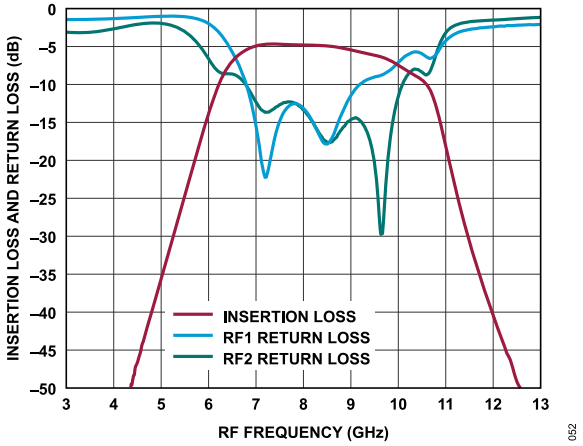

Figure 52. Insertion Loss and Return Loss vs. RF Frequency at HPF and LPF, State 7

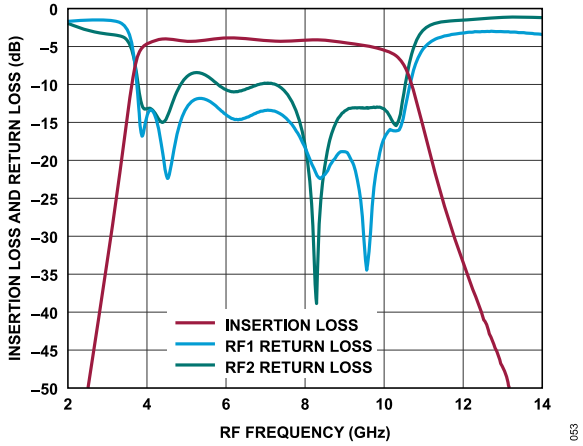

Figure 55. Insertion Loss and Return Loss vs. RF Frequency at HPF, State 0 and LPF, State 7

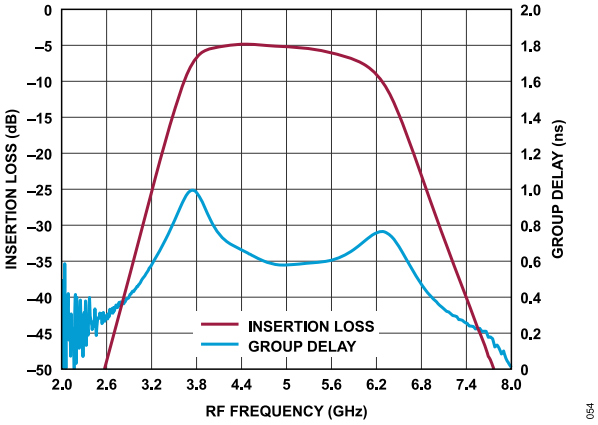

Figure 53. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 0

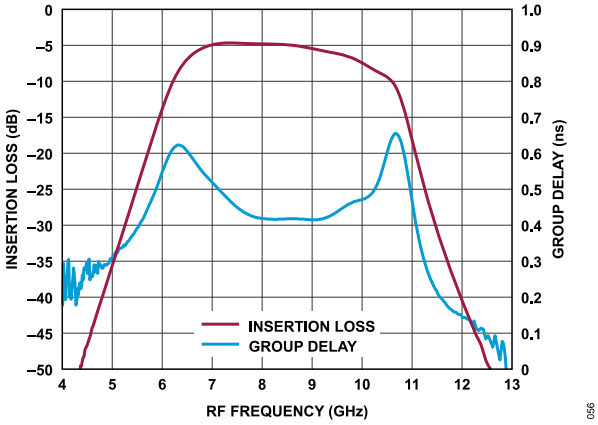

Figure 56. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 7

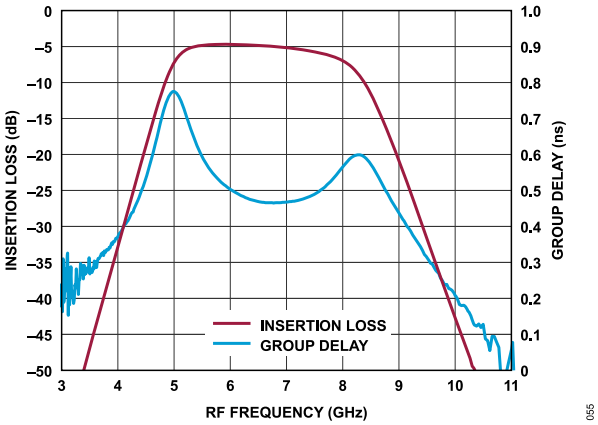

Figure 54. Insertion Loss and Group Delay vs. RF Frequency at HPF and LPF, State 4

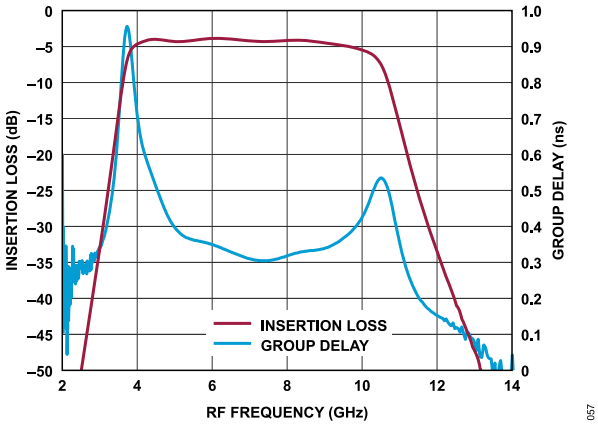

Figure 57. Insertion Loss and Group Delay vs. RF Frequency at HPF, State 0 and LPF, State 7

TYPICAL PERFORMANCE CHARACTERISTICS

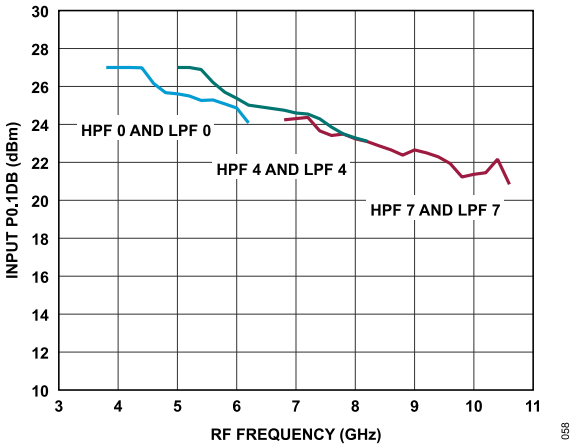

Figure 58. Input P0.1dB vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7

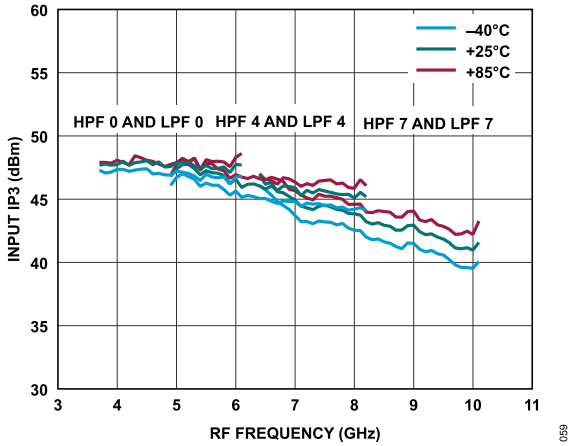

Figure 59. Input IP3 vs. RF Frequency at HPF and LPF, State 0, State 4, and State 7 in Various Temperatures

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BYPASS CONFIGURATION DATA

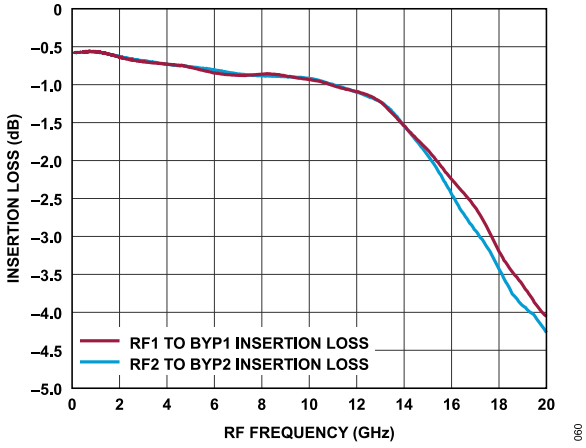

Figure 60. Insertion Loss vs. RF Frequency

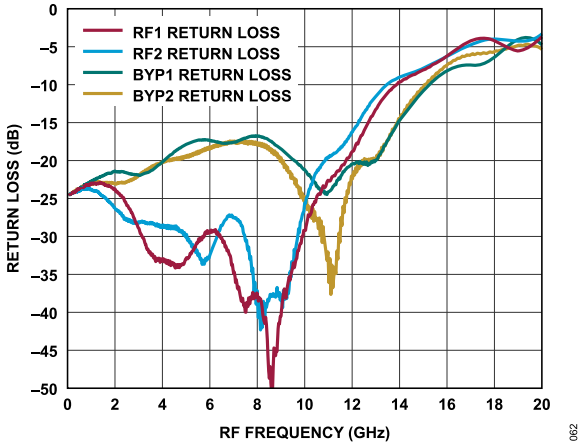

Figure 62. Input and Bypass Return Loss vs. RF Frequency

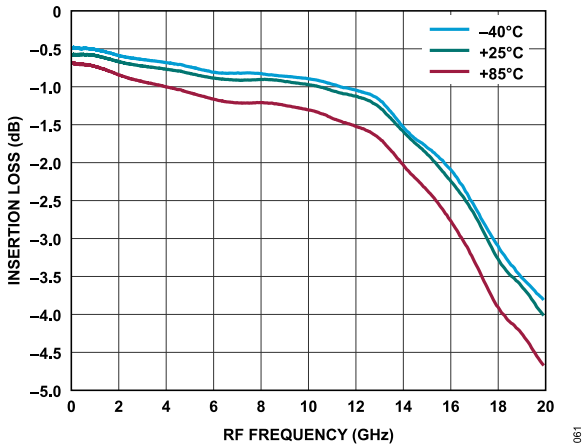

Figure 61. Insertion Loss vs. RF Frequency in Various Temperatures

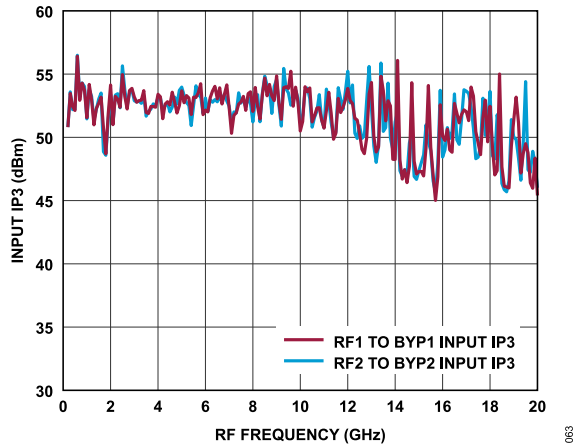

Figure 63. Input IP3 vs. RF Frequency

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SPI CONFIGURATION

The SPI of the ADMV8809 allows configuration of the device for specific functions or operations via the 5-pin SPI. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDI, SDO, and $\overline{CS}$.

The SPI protocol consists of an R/W bit followed by 15 register address bits and 8 data bits. The address field and data field are organized MSB first and end with the LSB.

Set the MSB to 0 for a write operation and set the MSB to 1 for a read operation. The write cycle must be sampled on the rising edge of SCLK. The 24 bits of the serial write address and data are shifted in on the SDI control line, MSB to LSB. The ADMV8809 input logic level for the write cycle supports a 3.3V interface.

For a read cycle, the R/W bit and the 15 register address bits shift in on the rising edge of SCLK on the SDI control line. Then, 8 bits of serial read data shift out on the SDO control line, MSB first, on the falling edge of SCLK. The output logic level for a read cycle is 3.3V. The output drivers of the SDO are enabled after the last rising edge of SCLK of the instruction cycle and remain active until the end of the read cycle. In a read operation, when $\overline{CS}$ is deasserted, SDO returns to high impedance until the next read transaction. $\overline{CS}$ is active low and must be deasserted at the end of the write or read sequence.

An active low input on $\overline{CS}$ starts and gates a communication cycle. The $\overline{CS}$ pin allows more than one device to be used on the same serial communications lines. The SDO pin goes to a high impedance state when the $\overline{CS}$ input is high. During the communication cycle, $\overline{CS}$ must stay low. The SPI communications protocol follows the Analog Devices Inc, SPI standard. For more information, see the ADI-SPI Serial Control Interface Standard (Rev 1.0).

CHIP ADDRESS

The four chip address pins enable the independent control of multiple chips using the same SPI bus. In the 24-bit SPI frame, Bit 20 to Bit 17 are defined by the ADD3 to ADD0 pins.

A write instruction to Register 0x00 broadcasts to all chips in a system regardless of the chip address pins.

Do not perform a read instruction of Register 0x00 in a multichip system.

All references to register addresses in this section have the ADD3 to ADD0 pins set to zero, unless otherwise noted.

RF CONNECTIONS

The RF1 and RF2 pins of the ADMV8809 are DC-coupled to on-chip ESD protection diodes. If a DC voltage is present on the RF1 and RF2 pins from other components within the system, it is recommended to place DC blocking capacitors in series with these pins. The DC blocking capacitors must be selected based on the operating frequency of the filter. Generally, a value greater than 10nF is sufficient to minimize insertion loss at the lower operating frequencies. At higher operating frequencies, it may be necessary to consider the parasitic elements of the selected capacitor. Figure 64 shows a general model of a capacitor with the parasitic elements. The parasitic series inductance (L_{ESL}) is typically of most concern given that its impedance can become dominant. The other parasitic elements, including the leakage resistance (R_L), the dielectric absorption resistance (R_{DA}), the dielectric absorption capacitance (C_{DA}), and electrical series resistance (R_{ESR}) are less critical elements for consideration but are shown in Figure 64 for completeness.

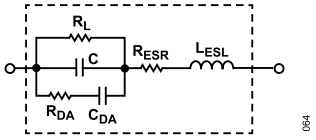

Figure 64. Model of a Capacitor

MODE SELECTION

The ADMV8809 has two modes of operation: SPI write and LUT control. SPI write mode is the normal operating mode, whereas the LUT control mode uses the 5-pin LUT control port to load the configuration from the on-chip LUT.

To select SPI write mode, set the LUT_BYPASS bit (Bit 3) of Register 0x11 to 1.

For operation in LUT control mode, set the LUT_BYPASS bit to 0.

SPI WRITE MODE

SPI write mode uses Register 0x13 (WR_SW) and Register 0x14 (WR_FILTER).

The WR_SW register includes the SW_SELECT bits can be used to control which filter band the switches are toggled to.

The WR_FILTER register includes the FILTER_SELECT, HPF, and LPF bits. Use the HPF and LPF bits (Bits[5:3] and Bits[2:0], respectively) to configure the high-pass filter state and low-pass filter state for each filter band. Use the FILTER_SELECT bits (Bits[7:6]) to select the filter band that requires adjustment. The HPF and LPF bit values dictate the new state for the HPF and LPF of the selected filter band.

LUT CONTROL MODE

The ADMV8809 has a LUT feature that can be used to store multiple filter conditions on LUT registers. See the Register Details section for further information on the LUT registers.

There are two registers that control the functionality of the LUT control mode for the ADMV8809. Register 0x11 (LUT_CTL1) includes the LUT_BYPASS, LUT_LATCH, LUT_MODE, and LUT_ACTIVE_SELECT bits (Bit 3, Bit 2, Bit 1, and Bit 0, respectively). Use these bits to bypass the LUT, configure the output (latched or combinational) and mode (using LUT_INDEX_POINTER

THEORY OF OPERATION

or parallel pins), and select between LUTA or LUTB. Register 0x12 (LUT_CTL2) includes the LUT_INDEX_POINTER bits (Bits[4:0]), which indicate the LUT entry used in SPI mode.

Users can select between two LUTs to use, LUTA and LUTB. Register 0x20 through Register 0x5F are for LUTA, and Register 0x60 through Register 0x9F are for LUTB. Each LUT has 32 pairs of the LUT_SW and LUT_FILTER registers.

Once users have configured the LUT register values, users can use these LUT registers to configure the filter bands. Users can control the LUT pointer by using either SPI mode or the parallel pins. If using SPI mode, use Register 0x12 to control the LUT pointer.

If using the parallel pins, set the LUT_MODE bit to 1. Then, select the LUT entry using the parallel pins. If the filter update timing is required, set the LUT_LATCH bit to 1 to set it to latched mode, where the LUT entry selected only updates on the next rising edge of $\overline{CS}$. Having this bit set to latched mode, the unused filter bands will be set to HPF State 0 and LPF State 0, and these bands will keep their current values, unless the values are overwritten by the user.

If the LUT_LATCH bit is set to 0, it sets to combinational mode, where the default values of the unused filter bands will be written over. The filter bands default values are detailed in Register 0x00 through Register 0x03.

SWITCH SET

Register 0x13 (WR_SW) dictates the filter band direction the input and output will be directed. Both switches (shown in Figure 1) are paired to this register.

FILTER SETTINGS

Register 0x14 (WR_FILTER) allows users to encode both the HPF and LPF states assigned on a filter band. Use the FILTER_SELECT bits (Bits[7:6]) to select the filter band. The HPF bits (Bits[5:3]) and LPF bits (Bits[2:0]) hold the state value, which includes eight configurable states. A value of 0 corresponds to setting the f_{3dB} of the filter to its lowest possible frequency. Conversely, a value of 7 corresponds to setting the f_{3dB} of the filter to its highest possible frequency.

READBACK REGISTERS

The ADMV8809 has dedicated readback registers. Register 0x15 (READBACK_SWITCH) and Register 0x16 through Register 0x19 (READBACK_FILTER1, READBACK_FILTER2, READBACK_FILTER3, and READBACK_FILTER4). These registers represents the actual settings of the switch, LPF, and HPF. See Register Summary for further information.

FREQUENCY TERMINOLOGY

The 3dB bandwidth is a straightforward concept; however, because the ADMV8809 is designed to operate over a wide frequency range, there is frequency dependent insertion loss that results in a negative slope vs. frequency. Additionally, depending upon the selected filter and state, there may also be ripple within the pass band. Given these characteristics, a variation is necessary to establish a reference frequency (f_{REF}) from which the f_{3dB} for each filter can be computed. Analog Devices uses a consistent methodology for determining the f_{REF} and f_{3dB} is to rely on the group delay performance of a filter. The following is the methodology used for determining the ADMV8809 specifications:

1. Find the peak group delay (GD_{PEAK}) and peak group delay frequency (f_{PEAK}) as the filter insertion loss (S21) begins to roll off.
2. For a LPF, divide f_{PEAK} by 2 to find the average frequency (f_{AVG}). For a HPF, multiply f_{PEAK} by 2. When f_{AVG} is calculated, determine the group delay at this frequency. Generally, the group delay is flat and approximately equal to the average at this particular frequency (f_{AVG}).
3. Take the mathematical mean of the group delay from Step 1 and Step 2 to find the reference group delay (GD_{REF}), and then find the corresponding f_{REF} and reference insertion loss (IL_{REF}) for this group delay.
4. Subtract 3dB from the IL_{REF} to find the 3dB insertion loss (IL_{3dB}), and then find the corresponding f_{3dB}.

CHIP RESET

Two methods are available to reset the ADMV8809 registers to their default power-on state, a hard reset and a soft reset. The hard reset uses the $\overline{RST}$ pin, and the soft reset utilizes Register 0x00.

To perform a hard reset, momentarily bring the $\overline{RST}$ pin low and then high. See Figure 2 for the minimum required duration time for the $\overline{RST}$ pin to be low.

To perform a soft reset, set Register 0x00 to 0x81. This action sets the SOFTRESET and SOFTRESET_ bits high to initiate the reset. The SOFTRESET and SOFTRESET_ bits are self resetting once the reset operation completes.

Regardless of the reset method used, it is recommended to perform the following after the chip resets:

- Set Register 0x00 to 0x3C to enable the SDO pin and allow SPI streaming with Endian ascending order.
- Read back all registers on the chip.

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) DESIGN GUIDELINES

The PCB used to implement the ADMV8809 can use standard quality dielectric materials between the top metallization layer and internal ground layer, such as the Isola 370HR. Rogers 4003 or Rogers 4350 do not have to be used. The characteristic impedance of the transmission lines to the RF1 and RF2 pins of the ADMV8809 must be controlled to 50Ω to ensure optimal RF performance. Connect the GND pins and exposed pads of the ADMV8809 directly to the ground plane of the PCB. Use a sufficient number of via holes to connect the top and bottom ground planes of the PCB.

FLOW CHART

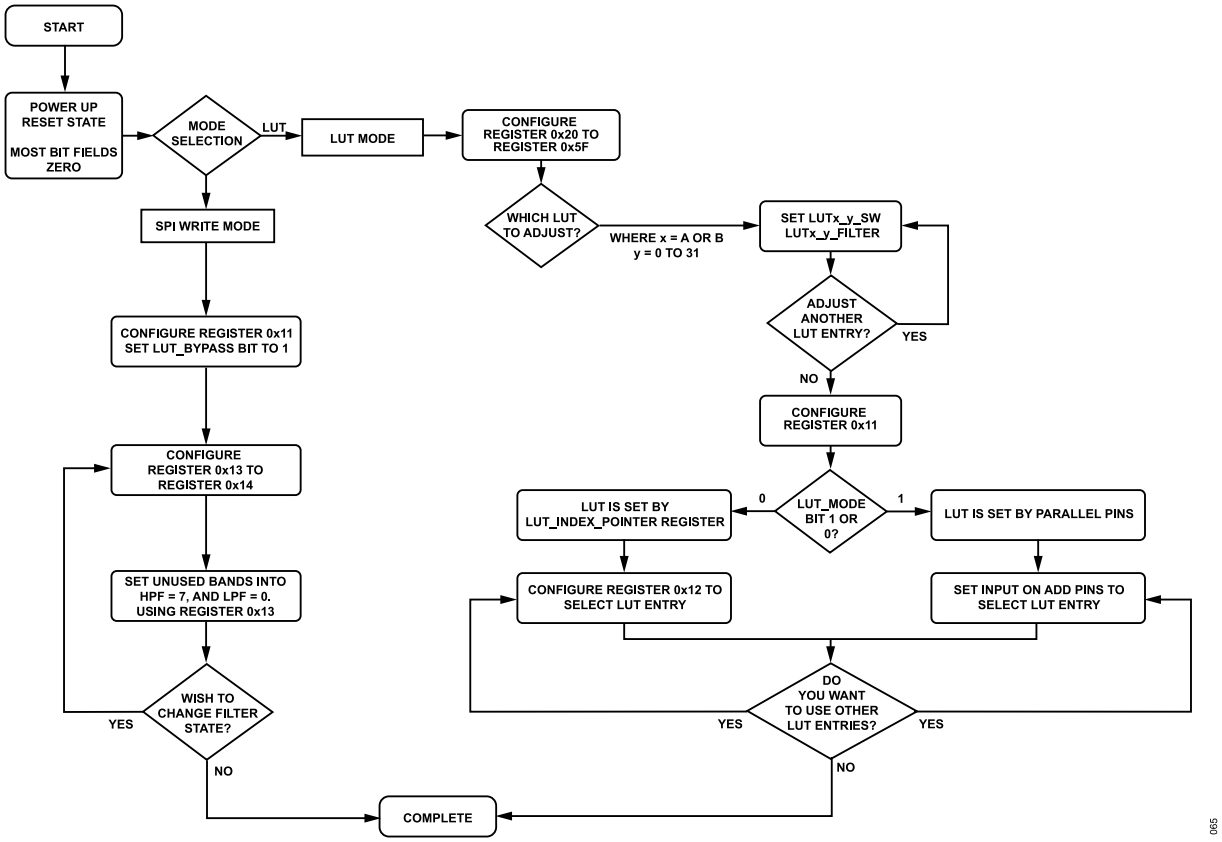

Figure 65. Programming Flow Chart

REGISTER SUMMARY

Table 6. ADMV8809 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	ADI_SPI_CONFIG_A	[7:0]	SOFT-RESET_	LSB_FIRST_	ENDIAN_	SDO-ACTIVE_	SDO-ACTIVE	ENDIAN	LSB_FIRST	SOFT-RESET	0x00	R/W
0x01	ADI_SPI_CONFIG_B	[7:0]	SINGLE_INSTRUC-TION	CSB_STALL	CON-TROLLER_TARGET_RB	RESERVED				CON-TROLLER_TARGET_TRANSFER	0x00	R/W
0x03	CHIPTYPE	[7:0]	CHIPTYPE								0x01	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID_L								0x34	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID_H								0x00	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_PAD								0x00	R/W
0x0C	VARIANT	[7:0]	RESERVED				VARIANT				0x00	R
0x10	SPI_LEVEL_CTL	[7:0]	RESERVED							SPI_LEVEL_CTL	0x00	R/W
0x11	LUT_CTL1	[7:0]	RESERVED				LUT_BYPASS	LUT_LATCH	LUT_MODE	LUT_ACTIVE_SELECT	0x0C	R/W
0x12	LUT_CTL2	[7:0]	RESERVED			LUT_INDEX_POINTER					0x00	R/W
0x13	WR_SW	[7:0]	RESERVED					SW_SELECT			0x00	R/W
0x14	WR_FILTER	[7:0]	FILTER_SELECT		HPF			LPF			0x00	R/W
0x15	READBACK_SWITCH	[7:0]	READBACK_SWITCH								0x00	R
0x16	READBACK_FILTER1	[7:0]	RESERVED	HPF1			RESERVED	LPF1			0x00	R
0x17	READBACK_FILTER2	[7:0]	RESERVED	HPF2			RESERVED	LPF2			0x00	R
0x18	READBACK_FILTER3	[7:0]	RESERVED	HPF3			RESERVED	LPF3			0x00	R
0x19	READBACK_FILTER4	[7:0]	RESERVED	HPF4			RESERVED	LPF4			0x00	R
0x1A	SPARE_WRITE_REG1	[7:0]	SPARE_WRITEBITS1								0x00	R/W
0x1B	SPARE_WRITE_REG2	[7:0]	SPARE_WRITEBITS2								0x00	R/W
0x1C	SPARE_WRITE_REG3	[7:0]	SPARE_WRITEBITS3								0x00	R/W
0x1D	SPARE_READ_REG1	[7:0]	SPARE_READBITS1								0x00	R
0x1E	SPARE_READ_REG2	[7:0]	SPARE_READBITS2								0x00	R
0x1F	SPARE_READ_REG3	[7:0]	SPARE_READBITS3								0x00	R
0x20	LUTA_0_SW	[7:0]	RESERVED					LUTA_0_SW_SELECT			0x00	R/W
0x21	LUTA_0_FILTER	[7:0]	LUTA_0_FILTER_POINTER		LUTA_0_HPF			LUTA_0_LPF			0x00	R/W
0x22	LUTA_1_SW	[7:0]	RESERVED					LUTA_1_SW_SELECT			0x00	R/W
0x23	LUTA_1_FILTER	[7:0]	LUTA_1_FILTER_POINTER		LUTA_1_HPF			LUTA_1_LPF			0x00	R/W
0x24	LUTA_2_SW	[7:0]	RESERVED					LUTA_2_SW_SELECT			0x00	R/W
0x25	LUTA_2_FILTER	[7:0]	LUTA_2_FILTER_POINTER		LUTA_2_HPF			LUTA_2_LPF			0x00	R/W

REGISTER SUMMARY

Table 6. ADMV8809 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x26	LUTA_3_SW	[7:0]	RESERVED					LUTA_3_SW_SELECT			0x00	R/W
0x27	LUTA_3_FILTER	[7:0]	LUTA_3_FILTER_POINTER			LUTA_3_HPF			LUTA_3_LPF		0x00	R/W
0x28	LUTA_4_SW	[7:0]	RESERVED					LUTA_4_SW_SELECT			0x00	R/W
0x29	LUTA_4_FILTER	[7:0]	LUTA_4_FILTER_POINTER			LUTA_4_HPF			LUTA_4_LPF		0x00	R/W
0x2A	LUTA_5_SW	[7:0]	RESERVED					LUTA_5_SW_SELECT			0x00	R/W
0x2B	LUTA_5_FILTER	[7:0]	LUTA_5_FILTER_POINTER			LUTA_5_HPF			LUTA_5_LPF		0x00	R/W
0x2C	LUTA_6_SW	[7:0]	RESERVED					LUTA_6_SW_SELECT			0x00	R/W
0x2D	LUTA_6_FILTER	[7:0]	LUTA_6_FILTER_POINTER			LUTA_6_HPF			LUTA_6_LPF		0x00	R/W
0x2E	LUTA_7_SW	[7:0]	RESERVED					LUTA_7_SW_SELECT			0x00	R/W
0x2F	LUTA_7_FILTER	[7:0]	LUTA_7_FILTER_POINTER			LUTA_7_HPF			LUTA_7_LPF		0x00	R/W
0x30	LUTA_8_SW	[7:0]	RESERVED					LUTA_8_SW_SELECT			0x00	R/W
0x31	LUTA_8_FILTER	[7:0]	LUTA_8_FILTER_POINTER			LUTA_8_HPF			LUTA_8_LPF		0x00	R/W
0x32	LUTA_9_SW	[7:0]	RESERVED					LUTA_9_SW_SELECT			0x00	R/W
0x33	LUTA_9_FILTER	[7:0]	LUTA_9_FILTER_POINTER			LUTA_9_HPF			LUTA_9_LPF		0x00	R/W
0x34	LUTA_10_SW	[7:0]	RESERVED					LUTA_10_SW_SELECT			0x00	R/W
0x35	LUTA_10_FILTER	[7:0]	LUTA_10_FILTER_POINTER			LUTA_10_HPF			LUTA_10_LPF		0x00	R/W
0x36	LUTA_11_SW	[7:0]	RESERVED					LUTA_11_SW_SELECT			0x00	R/W
0x37	LUTA_11_FILTER	[7:0]	LUTA_11_FILTER_POINTER			LUTA_11_HPF			LUTA_11_LPF		0x00	R/W
0x38	LUTA_12_SW	[7:0]	RESERVED					LUTA_12_SW_SELECT			0x00	R/W
0x39	LUTA_12_FILTER	[7:0]	LUTA_12_FILTER_POINTER			LUTA_12_HPF			LUTA_12_LPF		0x00	R/W
0x3A	LUTA_13_SW	[7:0]	RESERVED					LUTA_13_SW_SELECT			0x00	R/W
0x3B	LUTA_13_FILTER	[7:0]	LUTA_13_FILTER_POINTER			LUTA_13_HPF			LUTA_13_LPF		0x00	R/W
0x3C	LUTA_14_SW	[7:0]	RESERVED					LUTA_14_SW_SELECT			0x00	R/W
0x3D	LUTA_14_FILTER	[7:0]	LUTA_14_FILTER_POINTER			LUTA_14_HPF			LUTA_14_LPF		0x00	R/W
0x3E	LUTA_15_SW	[7:0]	RESERVED					LUTA_15_SW_SELECT			0x00	R/W
0x3F	LUTA_15_FILTER	[7:0]	LUTA_15_FILTER_POINTER			LUTA_15_HPF			LUTA_15_LPF		0x00	R/W
0x40	LUTA_16_SW	[7:0]	RESERVED					LUTA_16_SW_SELECT			0x00	R/W
0x41	LUTA_16_FILTER	[7:0]	LUTA_16_FILTER_POINTER			LUTA_16_HPF			LUTA_16_LPF		0x00	R/W
0x42	LUTA_17_SW	[7:0]	RESERVED					LUTA_17_SW_SELECT			0x00	R/W
0x43	LUTA_17_FILTER	[7:0]	LUTA_17_FILTER_POINTER			LUTA_17_HPF			LUTA_17_LPF		0x00	R/W
0x44	LUTA_18_SW	[7:0]	RESERVED					LUTA_18_SW_SELECT			0x00	R/W
0x45	LUTA_18_FILTER	[7:0]	LUTA_18_FILTER_POINTER			LUTA_18_HPF			LUTA_18_LPF		0x00	R/W
0x46	LUTA_19_SW	[7:0]	RESERVED					LUTA_19_SW_SELECT			0x00	R/W

REGISTER SUMMARY

Table 6. ADMV8809 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x47	LUTA_19_FILTER	[7:0]	LUTA_19_FILTER_POINTER			LUTA_19_HPF			LUTA_19_LPF		0x00	R/W
0x48	LUTA_20_SW	[7:0]			RESERVED				LUTA_20_SW_SELECT		0x00	R/W
0x49	LUTA_20_FILTER	[7:0]	LUTA_20_FILTER_POINTER			LUTA_20_HPF			LUTA_20_LPF		0x00	R/W
0x4A	LUTA_21_SW	[7:0]			RESERVED				LUTA_21_SW_SELECT		0x00	R/W
0x4B	LUTA_21_FILTER	[7:0]	LUTA_21_FILTER_POINTER			LUTA_21_HPF			LUTA_21_LPF		0x00	R/W
0x4C	LUTA_22_SW	[7:0]			RESERVED				LUTA_22_SW_SELECT		0x00	R/W
0x4D	LUTA_22_FILTER	[7:0]	LUTA_22_FILTER_POINTER			LUTA_22_HPF			LUTA_22_LPF		0x00	R/W
0x4E	LUTA_23_SW	[7:0]			RESERVED				LUTA_23_SW_SELECT		0x00	R/W
0x4F	LUTA_23_FILTER	[7:0]	LUTA_23_FILTER_POINTER			LUTA_23_HPF			LUTA_23_LPF		0x00	R/W
0x50	LUTA_24_SW	[7:0]			RESERVED				LUTA_24_SW_SELECT		0x00	R/W
0x51	LUTA_24_FILTER	[7:0]	LUTA_24_FILTER_POINTER			LUTA_24_HPF			LUTA_24_LPF		0x00	R/W
0x52	LUTA_25_SW	[7:0]			RESERVED				LUTA_25_SW_SELECT		0x00	R/W
0x53	LUTA_25_FILTER	[7:0]	LUTA_25_FILTER_POINTER			LUTA_25_HPF			LUTA_25_LPF		0x00	R/W
0x54	LUTA_26_SW	[7:0]			RESERVED				LUTA_26_SW_SELECT		0x00	R/W
0x55	LUTA_26_FILTER	[7:0]	LUTA_26_FILTER_POINTER			LUTA_26_HPF			LUTA_26_LPF		0x00	R/W
0x56	LUTA_27_SW	[7:0]			RESERVED				LUTA_27_SW_SELECT		0x00	R/W
0x57	LUTA_27_FILTER	[7:0]	LUTA_27_FILTER_POINTER			LUTA_27_HPF			LUTA_27_LPF		0x00	R/W
0x58	LUTA_28_SW	[7:0]			RESERVED				LUTA_28_SW_SELECT		0x00	R/W
0x59	LUTA_28_FILTER	[7:0]	LUTA_28_FILTER_POINTER			LUTA_28_HPF			LUTA_28_LPF		0x00	R/W
0x5A	LUTA_29_SW	[7:0]			RESERVED				LUTA_29_SW_SELECT		0x00	R/W
0x5B	LUTA_29_FILTER	[7:0]	LUTA_29_FILTER_POINTER			LUTA_29_HPF			LUTA_29_LPF		0x00	R/W
0x5C	LUTA_30_SW	[7:0]			RESERVED				LUTA_30_SW_SELECT		0x00	R/W
0x5D	LUTA_30_FILTER	[7:0]	LUTA_30_FILTER_POINTER			LUTA_30_HPF			LUTA_30_LPF		0x00	R/W
0x5E	LUTA_31_SW	[7:0]			RESERVED				LUTA_31_SW_SELECT		0x00	R/W
0x5F	LUTA_31_FILTER	[7:0]	LUTA_31_FILTER_POINTER			LUTA_31_HPF			LUTA_31_LPF		0x00	R/W
0x60	LUTB_0_SW	[7:0]			RESERVED				LUTB_0_SW_SELECT		0x00	R/W
0x61	LUTB_0_FILTER	[7:0]	LUTB_0_FILTER_POINTER			LUTB_0_HPF			LUTB_0_LPF		0x00	R/W
0x62	LUTB_1_SW	[7:0]			RESERVED				LUTB_1_SW_SELECT		0x00	R/W
0x63	LUTB_1_FILTER	[7:0]	LUTB_1_FILTER_POINTER			LUTB_1_HPF			LUTB_1_LPF		0x00	R/W
0x64	LUTB_2_SW	[7:0]			RESERVED				LUTB_2_SW_SELECT		0x00	R/W
0x65	LUTB_2_FILTER	[7:0]	LUTB_2_FILTER_POINTER			LUTB_2_HPF			LUTB_2_LPF		0x00	R/W
0x66	LUTB_3_SW	[7:0]			RESERVED				LUTB_3_SW_SELECT		0x00	R/W

REGISTER SUMMARY

Table 6. ADMV8809 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x67	LUTB_3_FILTER	[7:0]	LUTB_3_FILTER_POINTER		LUTB_3_HPF			LUTB_3_LPF			0x00	R/W
0x68	LUTB_4_SW	[7:0]	RESERVED					LUTB_4_SW_SELECT			0x00	R/W
0x69	LUTB_4_FILTER	[7:0]	LUTB_4_FILTER_POINTER		LUTB_4_HPF			LUTB_4_LPF			0x00	R/W
0x6A	LUTB_5_SW	[7:0]	RESERVED					LUTB_5_SW_SELECT			0x00	R/W
0x6B	LUTB_5_FILTER	[7:0]	LUTB_5_FILTER_POINTER		LUTB_5_HPF			LUTB_5_LPF			0x00	R/W
0x6C	LUTB_6_SW	[7:0]	RESERVED					LUTB_6_SW_SELECT			0x00	R/W
0x6D	LUTB_6_FILTER	[7:0]	LUTB_6_FILTER_POINTER		LUTB_6_HPF			LUTB_6_LPF			0x00	R/W
0x6E	LUTB_7_SW	[7:0]	RESERVED					LUTB_7_SW_SELECT			0x00	R/W
0x6F	LUTB_7_FILTER	[7:0]	LUTB_7_FILTER_POINTER		LUTB_7_HPF			LUTB_7_LPF			0x00	R/W
0x70	LUTB_8_SW	[7:0]	RESERVED					LUTB_8_SW_SELECT			0x00	R/W
0x71	LUTB_8_FILTER	[7:0]	LUTB_8_FILTER_POINTER		LUTB_8_HPF			LUTB_8_LPF			0x00	R/W
0x72	LUTB_9_SW	[7:0]	RESERVED					LUTB_9_SW_SELECT			0x00	R/W
0x73	LUTB_9_FILTER	[7:0]	LUTB_9_FILTER_POINTER		LUTB_9_HPF			LUTB_9_LPF			0x00	R/W
0x74	LUTB_10_SW	[7:0]	RESERVED					LUTB_10_SW_SELECT			0x00	R/W
0x75	LUTB_10_FILTER	[7:0]	LUTB_10_FILTER_POINTER		LUTB_10_HPF			LUTB_10_LPF			0x00	R/W
0x76	LUTB_11_SW	[7:0]	RESERVED					LUTB_11_SW_SELECT			0x00	R/W
0x77	LUTB_11_FILTER	[7:0]	LUTB_11_FILTER_POINTER		LUTB_11_HPF			LUTB_11_LPF			0x00	R/W
0x78	LUTB_12_SW	[7:0]	RESERVED					LUTB_12_SW_SELECT			0x00	R/W
0x79	LUTB_12_FILTER	[7:0]	LUTB_12_FILTER_POINTER		LUTB_12_HPF			LUTB_12_LPF			0x00	R/W
0x7A	LUTB_13_SW	[7:0]	RESERVED					LUTB_13_SW_SELECT			0x00	R/W
0x7B	LUTB_13_FILTER	[7:0]	LUTB_13_FILTER_POINTER		LUTB_13_HPF			LUTB_13_LPF			0x00	R/W
0x7C	LUTB_14_SW	[7:0]	RESERVED					LUTB_14_SW_SELECT			0x00	R/W
0x7D	LUTB_14_FILTER	[7:0]	LUTB_14_FILTER_POINTER		LUTB_14_HPF			LUTB_14_LPF			0x00	R/W
0x7E	LUTB_15_SW	[7:0]	RESERVED					LUTB_15_SW_SELECT			0x00	R/W
0x7F	LUTB_15_FILTER	[7:0]	LUTB_15_FILTER_POINTER		LUTB_15_HPF			LUTB_15_LPF			0x00	R/W
0x80	LUTB_16_SW	[7:0]	RESERVED					LUTB_16_SW_SELECT			0x00	R/W
0x81	LUTB_16_FILTER	[7:0]	LUTB_16_FILTER_POINTER		LUTB_16_HPF			LUTB_16_LPF			0x00	R/W
0x82	LUTB_17_SW	[7:0]	RESERVED					LUTB_17_SW_SELECT			0x00	R/W
0x83	LUTB_17_FILTER	[7:0]	LUTB_17_FILTER_POINTER		LUTB_17_HPF			LUTB_17_LPF			0x00	R/W
0x84	LUTB_18_SW	[7:0]	RESERVED					LUTB_18_SW_SELECT			0x00	R/W
0x85	LUTB_18_FILTER	[7:0]	LUTB_18_FILTER_POINTER		LUTB_18_HPF			LUTB_18_LPF			0x00	R/W
0x86	LUTB_19_SW	[7:0]	RESERVED					LUTB_19_SW_SELECT			0x00	R/W

REGISTER SUMMARY

Table 6. ADMV8809 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x87	LUTB_19_FILTER	[7:0]	LUTB_19_FILTER_POINTER		LUTB_19_HPF			LUTB_19_LPF			0x00	R/W
0x88	LUTB_20_SW	[7:0]	RESERVED					LUTB_20_SW_SELECT			0x00	R/W
0x89	LUTB_20_FILTER	[7:0]	LUTB_20_FILTER_POINTER		LUTB_20_HPF			LUTB_20_LPF			0x00	R/W
0x8A	LUTB_21_SW	[7:0]	RESERVED					LUTB_21_SW_SELECT			0x00	R/W
0x8B	LUTB_21_FILTER	[7:0]	LUTB_21_FILTER_POINTER		LUTB_21_HPF			LUTB_21_LPF			0x00	R/W
0x8C	LUTB_22_SW	[7:0]	RESERVED					LUTB_22_SW_SELECT			0x00	R/W
0x8D	LUTB_22_FILTER	[7:0]	LUTB_22_FILTER_POINTER		LUTB_22_HPF			LUTB_22_LPF			0x00	R/W
0x8E	LUTB_23_SW	[7:0]	RESERVED					LUTB_23_SW_SELECT			0x00	R/W
0x8F	LUTB_23_FILTER	[7:0]	LUTB_23_FILTER_POINTER		LUTB_23_HPF			LUTB_23_LPF			0x00	R/W
0x90	LUTB_24_SW	[7:0]	RESERVED					LUTB_24_SW_SELECT			0x00	R/W
0x91	LUTB_24_FILTER	[7:0]	LUTB_24_FILTER_POINTER		LUTB_24_HPF			LUTB_24_LPF			0x00	R/W
0x92	LUTB_25_SW	[7:0]	RESERVED					LUTB_25_SW_SELECT			0x00	R/W
0x93	LUTB_25_FILTER	[7:0]	LUTB_25_FILTER_POINTER		LUTB_25_HPF			LUTB_25_LPF			0x00	R/W
0x94	LUTB_26_SW	[7:0]	RESERVED					LUTB_26_SW_SELECT			0x00	R/W
0x95	LUTB_26_FILTER	[7:0]	LUTB_26_FILTER_POINTER		LUTB_26_HPF			LUTB_26_LPF			0x00	R/W
0x96	LUTB_27_SW	[7:0]	RESERVED					LUTB_27_SW_SELECT			0x00	R/W
0x97	LUTB_27_FILTER	[7:0]	LUTB_27_FILTER_POINTER		LUTB_27_HPF			LUTB_27_LPF			0x00	R/W
0x98	LUTB_28_SW	[7:0]	RESERVED					LUTB_28_SW_SELECT			0x00	R/W
0x99	LUTB_28_FILTER	[7:0]	LUTB_28_FILTER_POINTER		LUTB_28_HPF			LUTB_28_LPF			0x00	R/W
0x9A	LUTB_29_SW	[7:0]	RESERVED					LUTB_29_SW_SELECT			0x00	R/W
0x9B	LUTB_29_FILTER	[7:0]	LUTB_29_FILTER_POINTER		LUTB_29_HPF			LUTB_29_LPF			0x00	R/W
0x9C	LUTB_30_SW	[7:0]	RESERVED					LUTB_30_SW_SELECT			0x00	R/W
0x9D	LUTB_30_FILTER	[7:0]	LUTB_30_FILTER_POINTER		LUTB_30_HPF			LUTB_30_LPF			0x00	R/W
0x9E	LUTB_31_SW	[7:0]	RESERVED					LUTB_31_SW_SELECT			0x00	R/W
0x9F	LUTB_31_FILTER	[7:0]	LUTB_31_FILTER_POINTER		LUTB_31_HPF			LUTB_31_LPF			0x00	R/W
0xA0	BAND1_DEFAULT	[7:0]	RESERVED		HPF1_DEFAULT			LPF1_DEFAULT			0x00	R/W
0xA1	BAND2_DEFAULT	[7:0]	RESERVED		HPF2_DEFAULT			LPF2_DEFAULT			0x00	R/W
0xA2	BAND3_DEFAULT	[7:0]	RESERVED		HPF3_DEFAULT			LPF3_DEFAULT			0x00	R/W
0xA3	BAND4_DEFAULT	[7:0]	RESERVED		HPF4_DEFAULT			LPF4_DEFAULT			0x00	R/W

REGISTER DETAILS

Address: 0x00, Reset: 0x00, Name: ADI_SPI_CONFIG_A

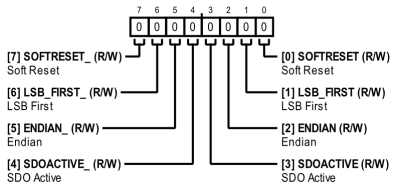

Figure 66.

Table 7. Bit Descriptions for ADI_SPI_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SOFTRESET_	Soft Reset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W
6	LSB_FIRST_	LSB First. 0: MSB First. 1: LSB First.	0x0	R/W
5	ENDIAN_	Endian. 0: Little Endian. 1: Big Endian.	0x0	R/W
4	SDOACTIVE_	SDO Active. 0: SDO Inactive. 1: SDO Active.	0x0	R/W
3	SDOACTIVE	SDO Active. 0: SDO Inactive. 1: SDO Active.	0x0	R/W
2	ENDIAN	Endian. 0: Little Endian. 1: Big Endian.	0x0	R/W
1	LSB_FIRST	LSB First. 0: MSB First. 1: LSB First.	0x0	R/W
0	SOFTRESET	Soft Reset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W

Address: 0x01, Reset: 0x00, Name: ADI_SPI_CONFIG_B

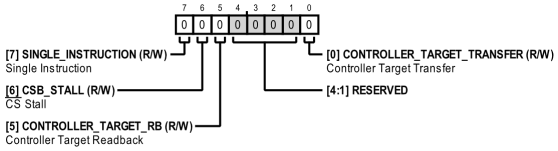

Figure 67.

Table 8. Bit Descriptions for ADI_SPI_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. 0: Enable Streaming. 1: Disable Streaming Regardless of $\overline{CS}$.	0x0	R/W
6	CSB_STALL	$\overline{CS}$ Stall.	0x0	R/W

REGISTER DETAILS

Table 8. Bit Descriptions for ADI_SPI_CONFIG_B (Continued)

Bits	Bit Name	Description	Reset	Access
5	CONTROLLER_TARGET_RB	Controller Target Readback.	0x0	R/W
[4:1]	RESERVED	Reserved.	0x0	R
0	CONTROLLER_TARGET_TRANSFER	Controller Target Transfer.	0x0	R/W

Address: 0x03, Reset: 0x01, Name: CHIPTYPE

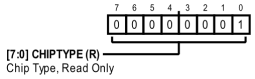

Figure 68.

Table 9. Bit Descriptions for CHIPTYPE

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIPTYPE	Chip Type, Read Only.	0x1	R

Address: 0x04, Reset: 0x34, Name: PRODUCT_ID_L

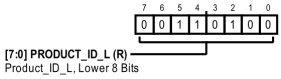

Figure 69.

Table 10. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_L	Product_ID_L, Lower 8 Bits.	0x34	R

Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

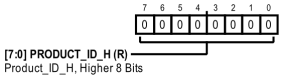

Figure 70.

Table 11. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_H	Product_ID_H, Higher 8 Bits.	0x0	R

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

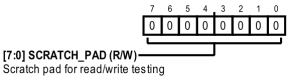

Figure 71.

Table 12. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_PAD	Scratch pad for read/write testing.	0x0	R/W

REGISTER DETAILS

Address: 0x0C, Reset: 0x00, Name: VARIANT

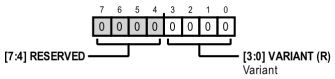

Figure 72.

Table 13. Bit Descriptions for VARIANT

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	VARIANT	Variant.	0x0	R

Address: 0x10, Reset: 0x00, Name: SPI_LEVEL_CTL

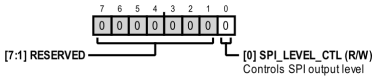

Figure 73.

Table 14. Bit Descriptions for SPI_LEVEL_CTL

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	SPI_LEVEL_CTL	Controls the SPI output level. 0: 1.8V. 1: 3.3V.	0x0	R/W

Address: 0x11, Reset: 0x0C, Name: LUT_CTL1

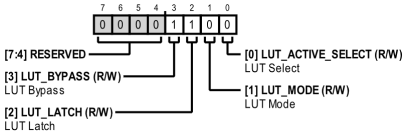

Figure 74.

Table 15. Bit Descriptions for LUT_CTL1

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	LUT_BYPASS	LUT Bypass. 0: Filters set by LUT. 1: Filters set by Register WR_SW and Register WR_FILTER.	0x1	R/W
2	LUT_LATCH	LUT Latch. Indicates if control output is latched (1) or combinational (0). 0: Control output is combinational. 1: Control output is latched.	0x1	R/W
1	LUT_MODE	LUT Mode. 0: LUT set by Register LUT_INDEX_POINTER. 1: LUT set by the parallel pins.	0x0	R/W
0	LUT_ACTIVE_SELECT	LUT Select. 0: LUT A. 1: LUT B.	0x0	R/W

REGISTER DETAILS

Address: 0x12, Reset: 0x00, Name: LUT_CTL2

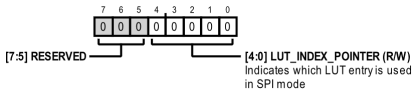

Figure 75.

Table 16. Bit Descriptions for LUT_CTL2

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LUT_INDEX_POINTER	Indicates which LUT entry is used in SPI mode.	0x0	R/W

Address: 0x13, Reset: 0x00, Name: WR_SW

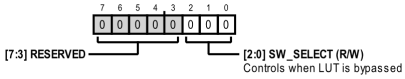

Figure 76.

Table 17. Bit Descriptions for WR_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	SW_SELECT	Controls when LUT is bypassed. 100: Filter Band 0—Bypass. 000: Filter Band 1—0.5GHz to 1.2GHz. 001: Filter Band 2—1,1GHz to 2.4GHz. 010: Filter Band 3—2.2GHz to 5GHz. 011: Filter Band 4—4.5GHz to 9GHz.	0x0	R/W

Address: 0x14, Reset: 0x00, Name: WR_FILTER

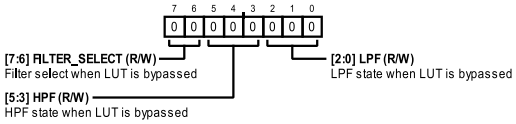

Figure 77.

Table 18. Bit Descriptions for WR_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	FILTER_SELECT	Filter select when LUT is bypassed. 00: LPF 1, HPF 1. 01: LPF 2, HPF 2. 10: LPF 3, HPF 3. 11: LPF 4, HPF 4.	0x0	R/W
[5:3]	HPF	HPF state when LUT is bypassed.	0x0	R/W
[2:0]	LPF	LPF state when LUT is bypassed.	0x0	R/W

REGISTER DETAILS

Address: 0x15, Reset: 0x00, Name: READBACK_SWITCH

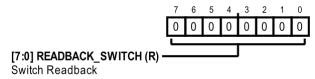

Figure 78.

Table 19. Bit Descriptions for READBACK_SWITCH

Bits	Bit Name	Description	Reset	Access
[7:0]	READBACK_SWITCH	Switch Readback.	0x0	R

Address: 0x16, Reset: 0x00, Name: READBACK_FILTER1

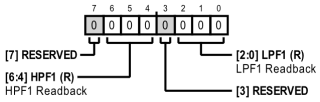

Figure 79.

Table 20. Bit Descriptions for READBACK_FILTER1

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	HPF1	HPF1 Readback.	0x0	R
3	RESERVED	Reserved.	0x0	R
[2:0]	LPF1	LPF1 Readback.	0x0	R

Address: 0x17, Reset: 0x00, Name: READBACK_FILTER2

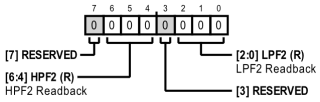

Figure 80.

Table 21. Bit Descriptions for READBACK_FILTER2

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	HPF2	HPF2 Readback.	0x0	R
3	RESERVED	Reserved.	0x0	R
[2:0]	LPF2	LPF2 Readback.	0x0	R

Address: 0x18, Reset: 0x00, Name: READBACK_FILTER3

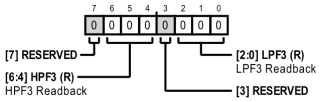

Figure 81.

Table 22. Bit Descriptions for READBACK_FILTER3

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	HPF3	HPF3 Readback.	0x0	R
3	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 22. Bit Descriptions for READBACK_FILTER3 (Continued)

Bits	Bit Name	Description	Reset	Access
[2:0]	LPF3	LPF3 Readback.	0x0	R

Address: 0x19, Reset: 0x00, Name: READBACK_FILTER4

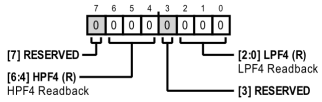

Figure 82.

Table 23. Bit Descriptions for READBACK_FILTER4

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	HPF4	HPF4 Readback.	0x0	R
3	RESERVED	Reserved.	0x0	R
[2:0]	LPF4	LPF4 Readback.	0x0	R

Address: 0x1A, Reset: 0x00, Name: SPARE_WRITE_REG1

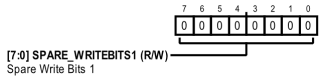

Figure 83.

Table 24. Bit Descriptions for SPARE_WRITE_REG1

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_WRITEBITS1	Spare Write Bits 1.	0x0	R/W

Address: 0x1B, Reset: 0x00, Name: SPARE_WRITE_REG2

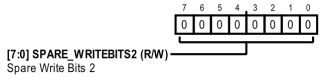

Figure 84.

Table 25. Bit Descriptions for SPARE_WRITE_REG2

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_WRITEBITS2	Spare Write Bits 2.	0x0	R/W

Address: 0x1C, Reset: 0x00, Name: SPARE_WRITE_REG3

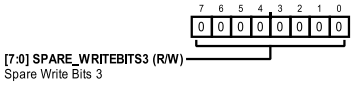

Figure 85.

Table 26. Bit Descriptions for SPARE_WRITE_REG3

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_WRITEBITS3	Spare Write Bits 3.	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: SPARE_READ_REG1

REGISTER DETAILS

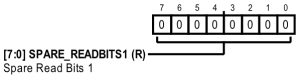

Figure 86.

Table 27. Bit Descriptions for SPARE_READ_REG1

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_READBITS1	Spare Read Bits 1.	0x0	R

Address: 0x1E, Reset: 0x00, Name: SPARE_READ_REG2

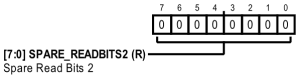

Figure 87.

Table 28. Bit Descriptions for SPARE_READ_REG2

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_READBITS2	Spare Read Bits 2.	0x0	R

Address: 0x1F, Reset: 0x00, Name: SPARE_READ_REG3

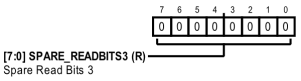

Figure 88.

Table 29. Bit Descriptions for SPARE_READ_REG3

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_READBITS3	Spare Read Bits 3.	0x0	R

Address: 0x20, Reset: 0x00, Name: LUTA_0_SW

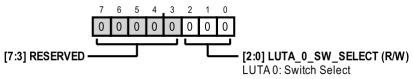

Figure 89.

Table 30. Bit Descriptions for LUTA_0_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_0_SW_SELECT	LUTA 0: Switch Select.	0x0	R/W

Address: 0x21, Reset: 0x00, Name: LUTA_0_FILTER

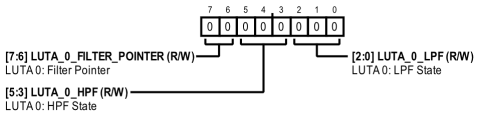

Figure 90.

REGISTER DETAILS

Table 31. Bit Descriptions for LUTA_0_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_0_FILTER_POINTER	LUTA 0: Filter Pointer.	0x0	R/W
[5:3]	LUTA_0_HPF	LUTA 0: HPF State.	0x0	R/W
[2:0]	LUTA_0_LPF	LUTA 0: LPF State.	0x0	R/W

Address: 0x22, Reset: 0x00, Name: LUTA_1_SW

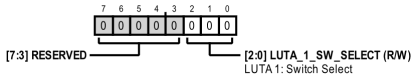

Figure 91.

Table 32. Bit Descriptions for LUTA_1_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_1_SW_SELECT	LUTA 1: Switch Select.	0x0	R/W

Address: 0x23, Reset: 0x00, Name: LUTA_1_FILTER

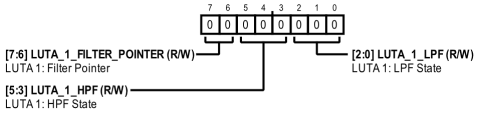

Figure 92.

Table 33. Bit Descriptions for LUTA_1_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_1_FILTER_POINTER	LUTA 1: Filter Pointer.	0x0	R/W
[5:3]	LUTA_1_HPF	LUTA 1: HPF State.	0x0	R/W
[2:0]	LUTA_1_LPF	LUTA 1: LPF State.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: LUTA_2_SW

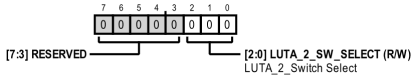

Figure 93.

Table 34. Bit Descriptions for LUTA_2_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_2_SW_SELECT	LUTA_2_Switch Select.	0x0	R/W

Address: 0x25, Reset: 0x00, Name: LUTA_2_FILTER

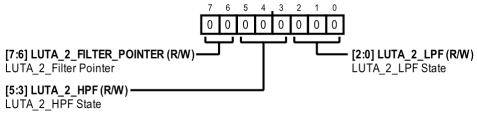

Figure 94.

REGISTER DETAILS

Table 35. Bit Descriptions for LUTA_2_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_2_FILTER_POINTER	LUTA_2_Filter Pointer.	0x0	R/W
[5:3]	LUTA_2_HPF	LUTA_2_HPF State.	0x0	R/W
[2:0]	LUTA_2_LPF	LUTA_2_LPF State.	0x0	R/W

Address: 0x26, Reset: 0x00, Name: LUTA_3_SW

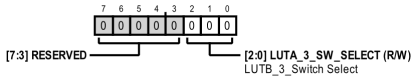

Figure 95.

Table 36. Bit Descriptions for LUTA_3_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_3_SW_SELECT	LUTB_3_Switch Select.	0x0	R/W

Address: 0x27, Reset: 0x00, Name: LUTA_3_FILTER

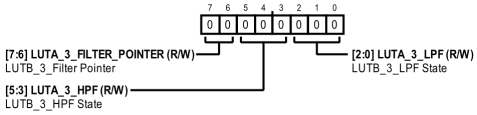

Figure 96.

Table 37. Bit Descriptions for LUTA_3_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_3_FILTER_POINTER	LUTB_3_Filter Pointer.	0x0	R/W
[5:3]	LUTA_3_HPF	LUTB_3_HPF State.	0x0	R/W
[2:0]	LUTA_3_LPF	LUTB_3_LPF State.	0x0	R/W

Address: 0x28, Reset: 0x00, Name: LUTA_4_SW

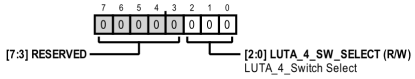

Figure 97.

Table 38. Bit Descriptions for LUTA_4_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_4_SW_SELECT	LUTA_4_Switch Select.	0x0	R/W

Address: 0x29, Reset: 0x00, Name: LUTA_4_FILTER

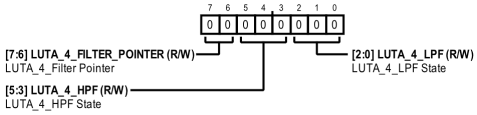

Figure 98.

REGISTER DETAILS

Table 39. Bit Descriptions for LUTA_4_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_4_FILTER_POINTER	LUTA_4_Filter Pointer.	0x0	R/W
[5:3]	LUTA_4_HPF	LUTA_4_HPF State.	0x0	R/W
[2:0]	LUTA_4_LPF	LUTA_4_LPF State.	0x0	R/W

Address: 0x2A, Reset: 0x00, Name: LUTA_5_SW

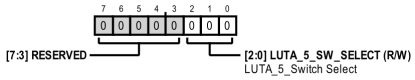

Figure 99.

Table 40. Bit Descriptions for LUTA_5_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_5_SW_SELECT	LUTA_5_Switch Select.	0x0	R/W

Address: 0x2B, Reset: 0x00, Name: LUTA_5_FILTER

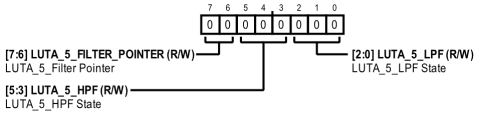

Figure 100.

Table 41. Bit Descriptions for LUTA_5_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_5_FILTER_POINTER	LUTA_5_Filter Pointer.	0x0	R/W
[5:3]	LUTA_5_HPF	LUTA_5_HPF State.	0x0	R/W
[2:0]	LUTA_5_LPF	LUTA_5_LPF State.	0x0	R/W

Address: 0x2C, Reset: 0x00, Name: LUTA_6_SW

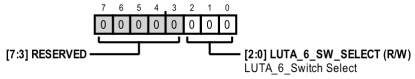

Figure 101.

Table 42. Bit Descriptions for LUTA_6_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_6_SW_SELECT	LUTA_6_Switch Select.	0x0	R/W

Address: 0x2D, Reset: 0x00, Name: LUTA_6_FILTER

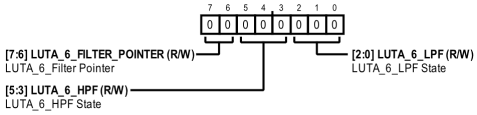

Figure 102.

REGISTER DETAILS

Table 43. Bit Descriptions for LUTA_6_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_6_FILTER_POINTER	LUTA_6_Filter Pointer.	0x0	R/W
[5:3]	LUTA_6_HPF	LUTA_6_HPF State.	0x0	R/W
[2:0]	LUTA_6_LPF	LUTA_6_LPF State.	0x0	R/W

Address: 0x2E, Reset: 0x00, Name: LUTA_7_SW

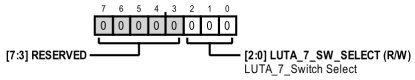

Figure 103.

Table 44. Bit Descriptions for LUTA_7_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_7_SW_SELECT	LUTA_7_Switch Select.	0x0	R/W

Address: 0x2F, Reset: 0x00, Name: LUTA_7_FILTER

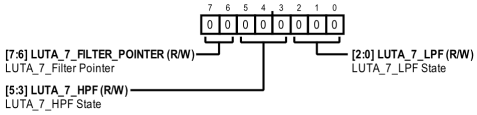

Figure 104.

Table 45. Bit Descriptions for LUTA_7_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_7_FILTER_POINTER	LUTA_7_Filter Pointer.	0x0	R/W
[5:3]	LUTA_7_HPF	LUTA_7_HPF State.	0x0	R/W
[2:0]	LUTA_7_LPF	LUTA_7_LPF State.	0x0	R/W

Address: 0x30, Reset: 0x00, Name: LUTA_8_SW

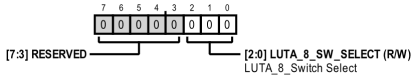

Figure 105.

Table 46. Bit Descriptions for LUTA_8_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_8_SW_SELECT	LUTA_8_Switch Select.	0x0	R/W

Address: 0x31, Reset: 0x00, Name: LUTA_8_FILTER

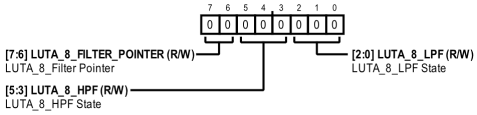

Figure 106.

REGISTER DETAILS

Table 47. Bit Descriptions for LUTA_8_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_8_FILTER_POINTER	LUTA_8_Filter Pointer.	0x0	R/W
[5:3]	LUTA_8_HPF	LUTA_8_HPF State.	0x0	R/W
[2:0]	LUTA_8_LPF	LUTA_8_LPF State.	0x0	R/W

Address: 0x32, Reset: 0x00, Name: LUTA_9_SW

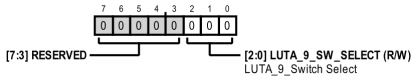

Figure 107.

Table 48. Bit Descriptions for LUTA_9_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_9_SW_SELECT	LUTA_9_Switch Select.	0x0	R/W

Address: 0x33, Reset: 0x00, Name: LUTA_9_FILTER

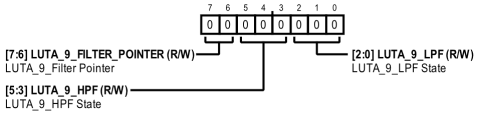

Figure 108.

Table 49. Bit Descriptions for LUTA_9_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_9_FILTER_POINTER	LUTA_9_Filter Pointer.	0x0	R/W
[5:3]	LUTA_9_HPF	LUTA_9_HPF State.	0x0	R/W
[2:0]	LUTA_9_LPF	LUTA_9_LPF State.	0x0	R/W

Address: 0x34, Reset: 0x00, Name: LUTA_10_SW

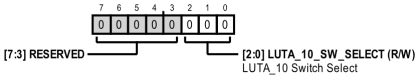

Figure 109.

Table 50. Bit Descriptions for LUTA_10_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_10_SW_SELECT	LUTA_10 Switch Select.	0x0	R/W

Address: 0x35, Reset: 0x00, Name: LUTA_10_FILTER

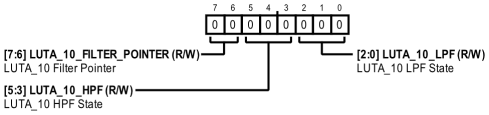

Figure 110.

REGISTER DETAILS

Table 51. Bit Descriptions for LUTA_10_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_10_FILTER_POINTER	LUTA_10 Filter Pointer.	0x0	R/W
[5:3]	LUTA_10_HPF	LUTA_10 HPF State.	0x0	R/W
[2:0]	LUTA_10_LPF	LUTA_10 LPF State.	0x0	R/W

Address: 0x36, Reset: 0x00, Name: LUTA_11_SW

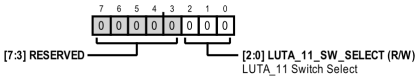

Figure 111.

Table 52. Bit Descriptions for LUTA_11_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_11_SW_SELECT	LUTA_11 Switch Select.	0x0	R/W

Address: 0x37, Reset: 0x00, Name: LUTA_11_FILTER

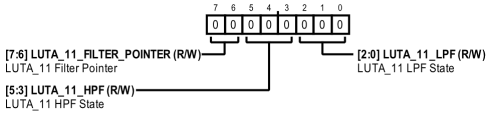

Figure 112.

Table 53. Bit Descriptions for LUTA_11_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_11_FILTER_POINTER	LUTA_11 Filter Pointer.	0x0	R/W
[5:3]	LUTA_11_HPF	LUTA_11 HPF State.	0x0	R/W
[2:0]	LUTA_11_LPF	LUTA_11 LPF State.	0x0	R/W

Address: 0x38, Reset: 0x00, Name: LUTA_12_SW

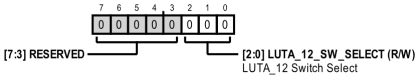

Figure 113.

Table 54. Bit Descriptions for LUTA_12_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_12_SW_SELECT	LUTA_12 Switch Select.	0x0	R/W

Address: 0x39, Reset: 0x00, Name: LUTA_12_FILTER

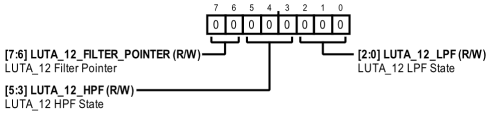

Figure 114.

REGISTER DETAILS

Table 55. Bit Descriptions for LUTA_12_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_12_FILTER_POINTER	LUTA_12 Filter Pointer.	0x0	R/W
[5:3]	LUTA_12_HPF	LUTA_12 HPF State.	0x0	R/W
[2:0]	LUTA_12_LPF	LUTA_12 LPF State.	0x0	R/W

Address: 0x3A, Reset: 0x00, Name: LUTA_13_SW

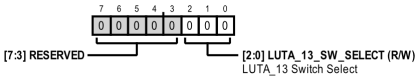

Figure 115.

Table 56. Bit Descriptions for LUTA_13_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_13_SW_SELECT	LUTA_13 Switch Select.	0x0	R/W

Address: 0x3B, Reset: 0x00, Name: LUTA_13_FILTER

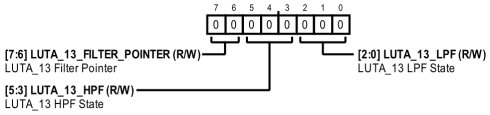

Figure 116.

Table 57. Bit Descriptions for LUTA_13_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_13_FILTER_POINTER	LUTA_13 Filter Pointer.	0x0	R/W
[5:3]	LUTA_13_HPF	LUTA_13 HPF State.	0x0	R/W
[2:0]	LUTA_13_LPF	LUTA_13 LPF State.	0x0	R/W

Address: 0x3C, Reset: 0x00, Name: LUTA_14_SW

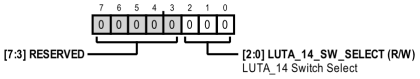

Figure 117.

Table 58. Bit Descriptions for LUTA_14_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_14_SW_SELECT	LUTA_14 Switch Select.	0x0	R/W

Address: 0x3D, Reset: 0x00, Name: LUTA_14_FILTER

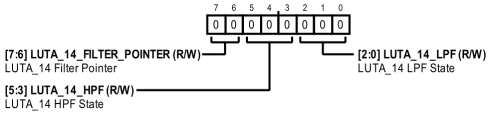

Figure 118.

REGISTER DETAILS

Table 59. Bit Descriptions for LUTA_14_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_14_FILTER_POINTER	LUTA_14 Filter Pointer.	0x0	R/W
[5:3]	LUTA_14_HPF	LUTA_14 HPF State.	0x0	R/W
[2:0]	LUTA_14_LPF	LUTA_14 LPF State.	0x0	R/W

Address: 0x3E, Reset: 0x00, Name: LUTA_15_SW

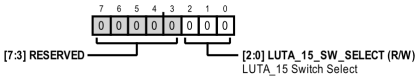

Figure 119.

Table 60. Bit Descriptions for LUTA_15_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_15_SW_SELECT	LUTA_15 Switch Select.	0x0	R/W

Address: 0x3F, Reset: 0x00, Name: LUTA_15_FILTER

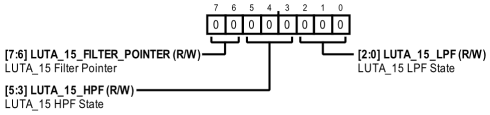

Figure 120.

Table 61. Bit Descriptions for LUTA_15_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_15_FILTER_POINTER	LUTA_15 Filter Pointer.	0x0	R/W
[5:3]	LUTA_15_HPF	LUTA_15 HPF State.	0x0	R/W
[2:0]	LUTA_15_LPF	LUTA_15 LPF State.	0x0	R/W

Address: 0x40, Reset: 0x00, Name: LUTA_16_SW

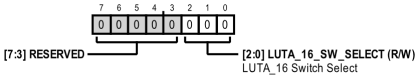

Figure 121.

Table 62. Bit Descriptions for LUTA_16_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_16_SW_SELECT	LUTA_16 Switch Select.	0x0	R/W

Address: 0x41, Reset: 0x00, Name: LUTA_16_FILTER

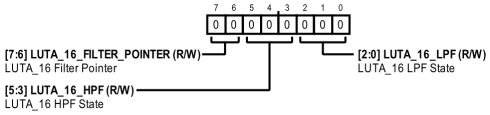

Figure 122.

REGISTER DETAILS

Table 63. Bit Descriptions for LUTA_16_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_16_FILTER_POINTER	LUTA_16 Filter Pointer.	0x0	R/W
[5:3]	LUTA_16_HPF	LUTA_16 HPF State.	0x0	R/W
[2:0]	LUTA_16_LPF	LUTA_16 LPF State.	0x0	R/W

Address: 0x42, Reset: 0x00, Name: LUTA_17_SW

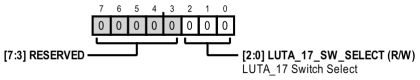

Figure 123.

Table 64. Bit Descriptions for LUTA_17_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_17_SW_SELECT	LUTA_17 Switch Select.	0x0	R/W

Address: 0x43, Reset: 0x00, Name: LUTA_17_FILTER

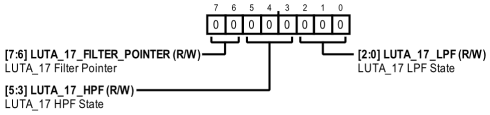

Figure 124.

Table 65. Bit Descriptions for LUTA_17_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_17_FILTER_POINTER	LUTA_17 Filter Pointer.	0x0	R/W
[5:3]	LUTA_17_HPF	LUTA_17 HPF State.	0x0	R/W
[2:0]	LUTA_17_LPF	LUTA_17 LPF State.	0x0	R/W

Address: 0x44, Reset: 0x00, Name: LUTA_18_SW

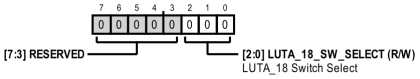

Figure 125.

Table 66. Bit Descriptions for LUTA_18_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_18_SW_SELECT	LUTA_18 Switch Select.	0x0	R/W

Address: 0x45, Reset: 0x00, Name: LUTA_18_FILTER

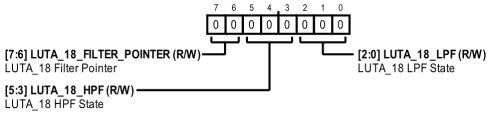

Figure 126.

REGISTER DETAILS

Table 67. Bit Descriptions for LUTA_18_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_18_FILTER_POINTER	LUTA_18 Filter Pointer.	0x0	R/W
[5:3]	LUTA_18_HPF	LUTA_18 HPF State.	0x0	R/W
[2:0]	LUTA_18_LPF	LUTA_18 LPF State.	0x0	R/W

Address: 0x46, Reset: 0x00, Name: LUTA_19_SW

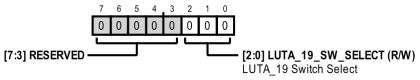

Figure 127.

Table 68. Bit Descriptions for LUTA_19_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_19_SW_SELECT	LUTA_19 Switch Select.	0x0	R/W

Address: 0x47, Reset: 0x00, Name: LUTA_19_FILTER

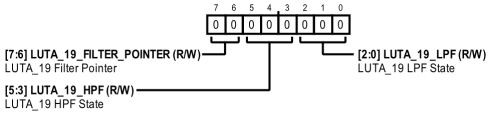

Figure 128.

Table 69. Bit Descriptions for LUTA_19_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_19_FILTER_POINTER	LUTA_19 Filter Pointer.	0x0	R/W
[5:3]	LUTA_19_HPF	LUTA_19 HPF State.	0x0	R/W
[2:0]	LUTA_19_LPF	LUTA_19 LPF State.	0x0	R/W

Address: 0x48, Reset: 0x00, Name: LUTA_20_SW

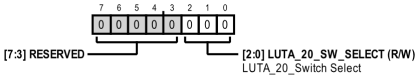

Figure 129.

Table 70. Bit Descriptions for LUTA_20_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_20_SW_SELECT	LUTA_20_Switch Select.	0x0	R/W

Address: 0x49, Reset: 0x00, Name: LUTA_20_FILTER

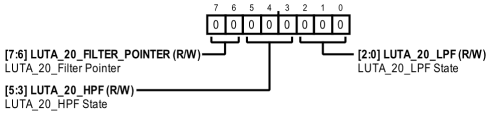

Figure 130.

REGISTER DETAILS

Table 71. Bit Descriptions for LUTA_20_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_20_FILTER_POINTER	LUTA_20_Filter Pointer.	0x0	R/W
[5:3]	LUTA_20_HPF	LUTA_20_HPF State.	0x0	R/W
[2:0]	LUTA_20_LPF	LUTA_20_LPF State.	0x0	R/W

Address: 0x4A, Reset: 0x00, Name: LUTA_21_SW

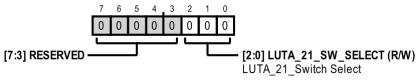

Figure 131.

Table 72. Bit Descriptions for LUTA_21_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_21_SW_SELECT	LUTA_21_Switch Select.	0x0	R/W

Address: 0x4B, Reset: 0x00, Name: LUTA_21_FILTER

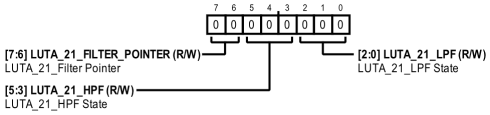

Figure 132.

Table 73. Bit Descriptions for LUTA_21_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_21_FILTER_POINTER	LUTA_21_Filter Pointer.	0x0	R/W
[5:3]	LUTA_21_HPF	LUTA_21_HPF State.	0x0	R/W
[2:0]	LUTA_21_LPF	LUTA_21_LPF State.	0x0	R/W

Address: 0x4C, Reset: 0x00, Name: LUTA_22_SW

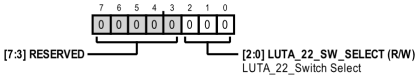

Figure 133.

Table 74. Bit Descriptions for LUTA_22_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_22_SW_SELECT	LUTA_22_Switch Select.	0x0	R/W

Address: 0x4D, Reset: 0x00, Name: LUTA_22_FILTER

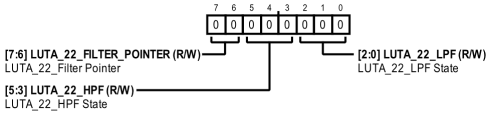

Figure 134.

REGISTER DETAILS

Table 75. Bit Descriptions for LUTA_22_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_22_FILTER_POINTER	LUTA_22_Filter Pointer.	0x0	R/W
[5:3]	LUTA_22_HPF	LUTA_22_HPF State.	0x0	R/W
[2:0]	LUTA_22_LPF	LUTA_22_LPF State.	0x0	R/W

Address: 0x4E, Reset: 0x00, Name: LUTA_23_SW

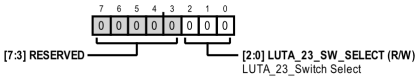

Figure 135.

Table 76. Bit Descriptions for LUTA_23_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_23_SW_SELECT	LUTA_23_Switch Select.	0x0	R/W

Address: 0x4F, Reset: 0x00, Name: LUTA_23_FILTER

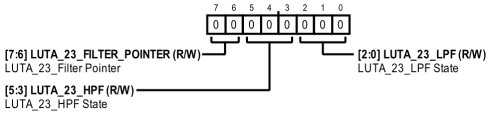

Figure 136.

Table 77. Bit Descriptions for LUTA_23_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_23_FILTER_POINTER	LUTA_23_Filter Pointer.	0x0	R/W
[5:3]	LUTA_23_HPF	LUTA_23_HPF State.	0x0	R/W
[2:0]	LUTA_23_LPF	LUTA_23_LPF State.	0x0	R/W

Address: 0x50, Reset: 0x00, Name: LUTA_24_SW

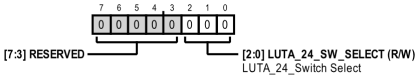

Figure 137.

Table 78. Bit Descriptions for LUTA_24_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_24_SW_SELECT	LUTA_24_Switch Select.	0x0	R/W

Address: 0x51, Reset: 0x00, Name: LUTA_24_FILTER

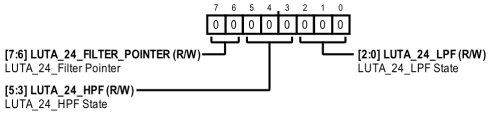

Figure 138.

REGISTER DETAILS

Table 79. Bit Descriptions for LUTA_24_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_24_FILTER_POINTER	LUTA_24_Filter Pointer.	0x0	R/W
[5:3]	LUTA_24_HPF	LUTA_24_HPF State.	0x0	R/W
[2:0]	LUTA_24_LPF	LUTA_24_LPF State.	0x0	R/W

Address: 0x52, Reset: 0x00, Name: LUTA_25_SW

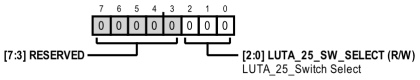

Figure 139.

Table 80. Bit Descriptions for LUTA_25_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_25_SW_SELECT	LUTA_25_Switch Select.	0x0	R/W

Address: 0x53, Reset: 0x00, Name: LUTA_25_FILTER

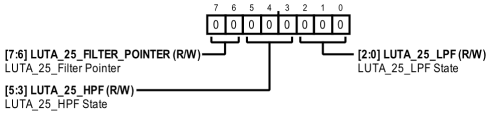

Figure 140.

Table 81. Bit Descriptions for LUTA_25_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_25_FILTER_POINTER	LUTA_25_Filter Pointer.	0x0	R/W
[5:3]	LUTA_25_HPF	LUTA_25_HPF State.	0x0	R/W
[2:0]	LUTA_25_LPF	LUTA_25_LPF State.	0x0	R/W

Address: 0x54, Reset: 0x00, Name: LUTA_26_SW

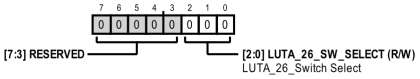

Figure 141.

Table 82. Bit Descriptions for LUTA_26_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_26_SW_SELECT	LUTA_26_Switch Select.	0x0	R/W

Address: 0x55, Reset: 0x00, Name: LUTA_26_FILTER

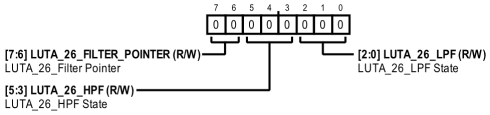

Figure 142.

REGISTER DETAILS

Table 83. Bit Descriptions for LUTA_26_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_26_FILTER_POINTER	LUTA_26_Filter Pointer.	0x0	R/W
[5:3]	LUTA_26_HPF	LUTA_26_HPF State.	0x0	R/W
[2:0]	LUTA_26_LPF	LUTA_26_LPF State.	0x0	R/W

Address: 0x56, Reset: 0x00, Name: LUTA_27_SW

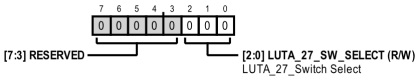

Figure 143.

Table 84. Bit Descriptions for LUTA_27_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_27_SW_SELECT	LUTA_27_Switch Select.	0x0	R/W

Address: 0x57, Reset: 0x00, Name: LUTA_27_FILTER

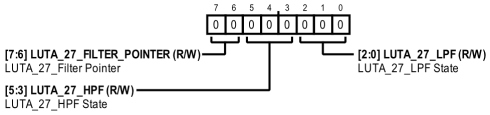

Figure 144.

Table 85. Bit Descriptions for LUTA_27_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_27_FILTER_POINTER	LUTA_27_Filter Pointer.	0x0	R/W
[5:3]	LUTA_27_HPF	LUTA_27_HPF State.	0x0	R/W
[2:0]	LUTA_27_LPF	LUTA_27_LPF State.	0x0	R/W

Address: 0x58, Reset: 0x00, Name: LUTA_28_SW

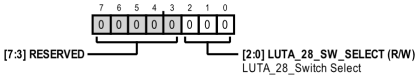

Figure 145.

Table 86. Bit Descriptions for LUTA_28_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_28_SW_SELECT	LUTA_28_Switch Select.	0x0	R/W

Address: 0x59, Reset: 0x00, Name: LUTA_28_FILTER

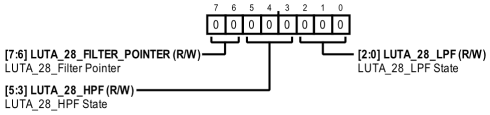

Figure 146.

REGISTER DETAILS

Table 87. Bit Descriptions for LUTA_28_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_28_FILTER_POINTER	LUTA_28_Filter Pointer.	0x0	R/W
[5:3]	LUTA_28_HPF	LUTA_28_HPF State.	0x0	R/W
[2:0]	LUTA_28_LPF	LUTA_28_LPF State.	0x0	R/W

Address: 0x5A, Reset: 0x00, Name: LUTA_29_SW

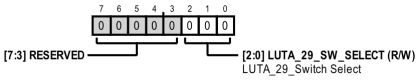

Figure 147.

Table 88. Bit Descriptions for LUTA_29_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_29_SW_SELECT	LUTA_29_Switch Select.	0x0	R/W

Address: 0x5B, Reset: 0x00, Name: LUTA_29_FILTER

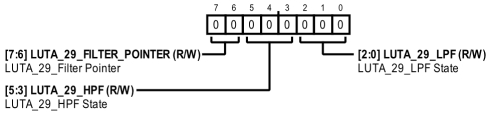

Figure 148.

Table 89. Bit Descriptions for LUTA_29_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_29_FILTER_POINTER	LUTA_29_Filter Pointer.	0x0	R/W
[5:3]	LUTA_29_HPF	LUTA_29_HPF State.	0x0	R/W
[2:0]	LUTA_29_LPF	LUTA_29_LPF State.	0x0	R/W

Address: 0x5C, Reset: 0x00, Name: LUTA_30_SW

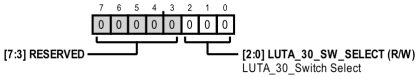

Figure 149.

Table 90. Bit Descriptions for LUTA_30_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_30_SW_SELECT	LUTA_30_Switch Select.	0x0	R/W

Address: 0x5D, Reset: 0x00, Name: LUTA_30_FILTER

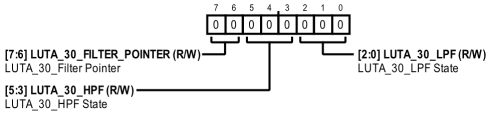

Figure 150.

REGISTER DETAILS

Table 91. Bit Descriptions for LUTA_30_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_30_FILTER_POINTER	LUTA_30_Filter Pointer.	0x0	R/W
[5:3]	LUTA_30_HPF	LUTA_30_HPF State.	0x0	R/W
[2:0]	LUTA_30_LPF	LUTA_30_LPF State.	0x0	R/W

Address: 0x5E, Reset: 0x00, Name: LUTA_31_SW

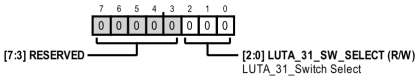

Figure 151.

Table 92. Bit Descriptions for LUTA_31_SW

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	LUTA_31_SW_SELECT	LUTA_31_Switch Select.	0x0	R/W

Address: 0x5F, Reset: 0x00, Name: LUTA_31_FILTER

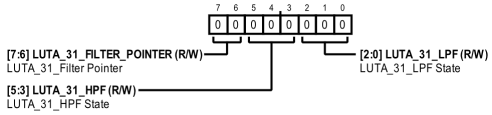

Figure 152.

Table 93. Bit Descriptions for LUTA_31_FILTER

Bits	Bit Name	Description	Reset	Access
[7:6]	LUTA_31_FILTER_POINTER	LUTA_31_Filter Pointer.	0x0	R/W
[5:3]	LUTA_31_HPF	LUTA_31_HPF State.	0x0	R/W
[2:0]	LUTA_31_LPF	LUTA_31_LPF State.	0x0	R/W

Note: LUTB_0 to LUTB_31 bit field functionality (Register 0x60 through Register 0x9F) is similar to LUTA_0 to LUTA_31 (Register 0x20 through Register 0x5F).

Address: 0xA0, Reset: 0x00, Name: BAND1_DEFAULT

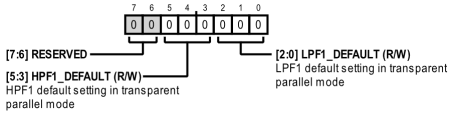

Figure 153.

Table 94. Bit Descriptions for BAND1_DEFAULT

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	HPF1_DEFAULT	HPF1 default setting in transparent parallel mode.	0x0	R/W
[2:0]	LPF1_DEFAULT	LPF1 default setting in transparent parallel mode.	0x0	R/W

Address: 0xA1, Reset: 0x00, Name: BAND2_DEFAULT

REGISTER DETAILS

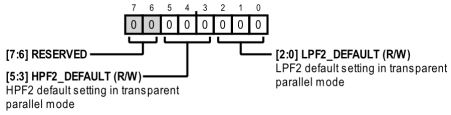

Figure 154.

Table 95. Bit Descriptions for BAND2_DEFAULT

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	HPF2_DEFAULT	HPF2 default setting in transparent parallel mode.	0x0	R/W
[2:0]	LPF2_DEFAULT	LPF2 default setting in transparent parallel mode.	0x0	R/W

Address: 0xA2, Reset: 0x00, Name: BAND3_DEFAULT

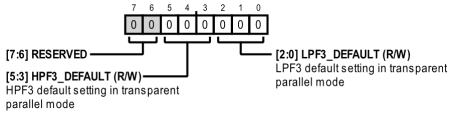

Figure 155.

Table 96. Bit Descriptions for BAND3_DEFAULT

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	HPF3_DEFAULT	HPF3 default setting in transparent parallel mode.	0x0	R/W
[2:0]	LPF3_DEFAULT	LPF3 default setting in transparent parallel mode.	0x0	R/W

Address: 0xA3, Reset: 0x00, Name: BAND4_DEFAULT

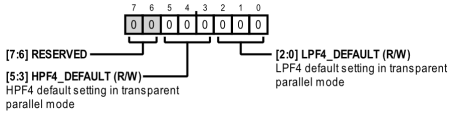

Figure 156.

Table 97. Bit Descriptions for BAND4_DEFAULT

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	HPF4_DEFAULT	HPF4 default setting in transparent parallel mode.	0x0	R/W
[2:0]	LPF4_DEFAULT	LPF4 default setting in transparent parallel mode.	0x0	R/W

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-52-5	LGA	52-Terminal Land Grid Array Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADMV8809ACCZ-PT	–40°C to +85°C	52-Terminal LGA	Tape, 750	CC-52-5
ADMV8809ACCZ-R7	–40°C to +85°C	52-Terminal LGA	Reel, 750	CC-52-5

[1] Z = RoHS Compliant Part.