

37.0 GHz to 43.5 GHz Transmit/Receive Dual Polarization Beamformer

FEATURES

- ▶ RF range: 37.0 GHz to 43.5 GHz
- ▶ 16 configurable (2 × 8) transmit and receive channels
- ▶ High linearity transmit performance with high back-off and peak efficiency that supports up to 1600 MHz 5G NR signal bandwidth
- ▶ High efficiency under multiple output power levels with several supply voltage levels
- ▶ Dual polarization, 8 horizontal and 8 vertical channels with single-ended RF inputs and outputs
- ▶ Fast TDD switching using TRX_x pins
- ▶ On-chip temperature sensor for receive and transmit
- ▶ Integrated power detector per transmit channel with digital filtering
- ▶ Automatic temperature compensation for gain for receive and transmit
- ▶ High resolution, 6-bit vector modulator for 360° phase control, 6-bit and 5-bit DVGAs for amplitude control
- ▶ Memory for 2048 shared transmit and receive beam positions
- ▶ NVM for phase and gain calibration
- ▶ Dual power supplies required: 3.3 V and 1.8 V with an on-chip LDO voltage regulator for 1.2 V and 1.0 V
- ▶ 3-wire or 4-wire SPI that supports up to 133 MHz SPI clock speed

APPLICATIONS

- ▶ mmW 5G application
- ▶ Broadband communications

GENERAL DESCRIPTION

The ADMV49281 is a silicon on insulator (SOI), 37.0 GHz to 43.5 GHz, mmW 5G beamformer. The RFIC is highly integrated and contains 16 independent transmit and receive channels. The ADMV49281 supports eight horizontal and eight vertical polarized antennas via independent RFC_V and RFC_H inputs and outputs.

In transmit mode, both the RFC_V input and RFC_H input signals feed into separate digital variable gain amplifiers (DVGAs). Each path after the DVGAs splits into eight independent channels via the 1:8 power splitters. In receive mode, input signals pass through either the vertical or horizontal receive channels and combine via two independent 8:1 combiners to separate DVGAs to the common RFC_V pin or RFC_H pin. In either mode, each transmit and receive channel includes a vector modulator to control the phase,

and one DVGA to control the amplitude. The vector modulator provides a full 360° phase adjustment range in either transmit or receive mode to provide 6 bits of resolution for 5.625° phase steps. A phase step policy for the transmit and receive vector modulator is provided to ensure optimum phase step performance. The total DVGA dynamic range in transmit mode is 34.5 dB, which provides 6 bits of resolution that results in 0.5 dB amplitude steps and 5 bits of resolution that results in 1 dB amplitude steps. In receive mode, the total dynamic range is 28 dB, which provides 5 bits of resolution that results in 0.5 dB amplitude steps and 5 bits of resolution that results in 1 dB amplitude steps. The DVGAs provide a flat phase response across the full gain range. Each transmit channel contains a power detector to detect either modulated or continuous wave signals to calibrate for each channel gain as well as channel to channel gain mismatch. The ADMV49281 RF ports can be connected directly to a patch antenna to create a dual or single polarization mmW 5G subarray.

The ADMV49281 can be programmed using a 3-wire or 4-wire serial port interface (SPI). An integrated, on-chip low dropout (LDO) voltage regulator generates the 1.2 V and 1.0 V supply for various circuits to reduce the number of supply domains required. Various SPI modes are available to enable fast startup and control during normal operation. The amplitude and phase for each channel can be set individually, or multiple channels can be programmed simultaneously using the on-chip memory for beamforming. The on-chip memory can store up to 2048 beam positions that can be allocated for either transmit mode or receive mode for the horizontal channels and vertical channels. On-chip nonvolatile memory (NVM) is used to store the calibrated gain and phase offset coefficients and the reference values for each individual channel from the factory. These values are used to perform channel to channel or chip to chip calibration. In addition, four address pins (CHIP_ADDx) allow independent SPI control of up to 14 devices on the same serial lines. A dedicated horizontal and vertical polarization load pin (LOAD) provides the synchronization of all devices in the same array. A horizontal and vertical polarization transmit mode and receive mode control pin (TRX_H or TRX_V) is provided for fast switching between transmit mode and receive mode.

The ADMV49281 comes in a compact, 245-ball, 11 mm × 7 mm chip scale package ball grid array (CSP_BGA). The ADMV49281 operates over the -40°C to +95°C T_C range. This CSP_BGA package allows the ADMV49281 to heatsink from the topside of the package for the most efficient thermal heatsink and to allow flexible antenna placement on the opposite side of the printed circuit board (PCB).

For more information on the ADMV49281, contact mmWave5G@analog.com.

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