Data Sheet

ADM33051E

±60V Fault Protected 3.3V ±20kV ESD High Speed CAN FD Transceiver

FEATURES

- Protected from Overvoltage Line Faults Up to ±60V
- 3.3V Supply Voltage
- High Speed CAN FD Operation Up to 2Mbps
- ±20kV ESD Protection on Interface Pins, ±8kV All Other Pins
- Variable Slew Rate Driver with Active Symmetry Control and SPLIT Pin for Low Electromagnetic Emission (EME)
- Extended Common-Mode Range (±25V)
- Ideal Passive Behavior to CAN Bus with Supply Off
- Current Limited Drivers and Thermal Shutdown
- Power-Up/Down Glitch-Free Driver Outputs
- 1µA (typ) Micropower Shutdown Mode
- Transmit Data (TXD) Dominant Timeout Function
- ISO 11898-2 and CAN FD Compliant
- Operating Temperature Range from –40°C to +125°C
- 8-Lead SO Package

APPLICATIONS

- Industrial Control and Instrumentation Networks
- Building Automation, Security Systems, HVAC
- Medical Equipment
- Transportation Electronics

GENERAL DESCRIPTION

The ADM33051E is a robust high speed, low-power CAN transceiver operating with a 3.3V supply. The ADM33051E features ±60V overvoltage fault protection on the data transmission lines during all modes of operation, including power-down. The 2Mbps maximum data rate supports high speed protocols based on the CAN physical layer with flexible data rate (CAN FD). Enhanced ESD protection allows the device to withstand up to ±20kV HBM on the transceiver interface pins without latch-up or damage.

Extended ±25V input common-mode range and high common-mode rejection on the CAN receiver provides extra tolerance for large ground loop voltages. The ADM33051E is a sophisticated CAN driver with active symmetry control maintains tight control of the common-mode voltage for excellent electromagnetic emission and includes a variable slew rate and split termination support for improved EME reduction.

SIMPLIFIED APPLICATION DIAGRAM

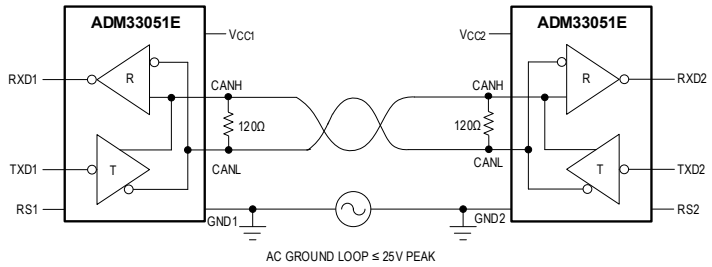

Figure 1. CAN Bus Link with Large Ground Loop Voltage

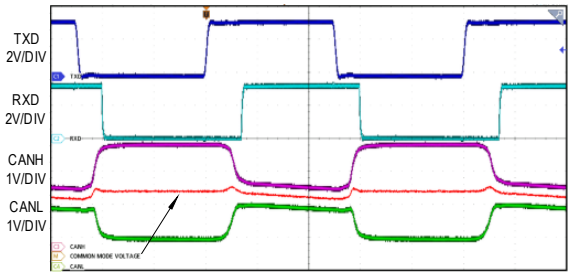

Figure 2. ADM33051E Transmitting at 2Mbps

19-102126; Rev. 0; 3/26

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/26	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(The • denotes the specifications which apply over the full-operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, *Figure 3* applies with R_L = 60Ω, V_{RS} = 0V, TYP values at V_{CC} = 3.3V, unless otherwise noted. ([1], [4]))

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Supplies							
Supply Voltage	V_{CC}		•	3	3.3	3.6	V
Supply Current (Recessive)	$I_{CC(R)}$		•	1	1.8	3	mA
Supply Current (Dominant)	$I_{CC(D)}$		•	25	37	60	mA
Supply Current in Shutdown Mode	I_{CCS}	V_{RS} = TXD = V_{CC}, RXD Open	•		1	15	µA
Driver							
CANH Bus Output Voltage (Dominant)	$V_{O(D)}$ (CANH)	t < t_{TOTXD}	•	2.15	2.9	3.3	V
CANL Bus Output Voltage (Dominant)	$V_{O(D)}$ (CANL)	t < t_{TOTXD}	•	0.5	0.9	1.65	V
Bus Output Voltage (Recessive)	$V_{O(R)}$	No Load (*Figure 3*)	•	1.45	1.95	2.45	V
Differential Output Voltage (Dominant)	$V_{OD(D)}$	R_L = 50Ω to 65Ω (*Figure 3*)	•	1.5	1.96	3.0	V
Differential Output Voltage (Recessive)	$V_{OD(R)}$	No Load (*Figure 3*)	•	−500	0	+50	mV
Common-Mode Output Voltage (Dominant)	$V_{OC(D)}$	(*Figure 3*)	•	1.45	1.95	2.45	V
CANH Bus Output Short-Circuit Current (Dominant)	$I_{OS(D)}$ (CANH)	CANH = 0V	•	−100	−75	−40	mA
		−60V ≤ CANH ≤ +60V	•	−100		+3	mA
CANL Bus Output Short-Circuit Current (Dominant)	$I_{OS(D)}$ (CANL)	CANL = 3.3V	•	40	75	100	mA
		−60V ≤ CANL ≤ +60V	•	−3		+100	mA

(The • denotes the specifications which apply over the full-operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, *Figure 3* applies with R_L = 60Ω, V_{RS} = 0V, TYP values at V_{CC} = 3.3V, unless otherwise noted. ([1], [4]))

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Receiver							
Bus Common-Mode Voltage = (CANH + CANL)/2 for Data Reception	V_{CM}		•			±25	V
Bus Input Differential Threshold Voltage (Positive-Going)	V_{TH+}	−25V ≤ V_{CM} ≤ +25V	•		775	900	mV
Bus Input Differential Threshold Voltage (Negative-Going)	V_{TH-}	−25V ≤ V_{CM} ≤ +25V	•	500	625		mV
Bus Input Differential Hysteresis Voltage	ΔV_{TH}	−25V ≤ V_{CM} ≤ +25V			120		mV
Input Resistance (CANH and CANL)	R_{IN}	TXD = V_{CC}, R_{IN} = ΔV/ΔI, ΔI = ±20µA	•	25	40	50	kΩ
Differential Input Resistance	R_{ID}	TXD = V_{CC}, R_{IN} = ΔV/ΔI, ΔI = ±20µA	•	50	80	100	kΩ
Input Resistance Matching	ΔR_{IN}	R_{IN} (CANH) to R_{IN} (CANL)	•			±1	%
Input Capacitance to GND (CANH)	C_{IH}	([3])			32		pF
Input Capacitance to GND (CANL)	C_{IL}	([3])			8		pF
Differential Input Capacitance	C_{ID}	([3])			8.4		pF
Bus Leakage Current (Power Off)	I_L	V_{CC} = 0V, CANH = CANL = 3.3V	•			±40	µA
Common-Mode Stabilization Output SPLIT							
SPLIT Output Voltage	V_{O_SPLIT}	−500µA ≤ I_{SPLIT} ≤ +500µA	•	0.9	1.9	2.9	V

(The • denotes the specifications which apply over the full-operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, *Figure 3* applies with R_L = 60Ω, V_{RS} = 0V, TYP values at V_{CC} = 3.3V, unless otherwise noted. ([1], [4]))

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
SPLIT Short-Circuit Current	I_{OS_SPLIT}	−60V ≤ SPLIT ≤ +60V	•	−3		+3	mA
Receiver Output RXD							
Receiver Output High Voltage	V_{OH_RXD}	I_{RXD} = −3mA (Sourcing)	•	V_{CC} − 0.4V			V
Receiver Output Low Voltage	V_{OL_RXD}	I_{RXD} = 3mA (Sinking)	•			0.4	V
Receiver Short-Circuit Current	I_{OS_RXD}	RXD = 0V or V_{CC}	•		±8	±18	mA
Logic Input TXD							
High Level Input Voltage	V_{IH_TXD}		•	0.67 × V_{CC}			V
Low Level Input Voltage	V_{IL_TXD}		•			0.33 × V_{CC}	V
Logic Input Current	I_{IN_TXD}	0 ≤ TXD ≤ V_{CC}	•	−20	0	+10	µA
Logic/Slew Control Input RS							
High Level Input Voltage	V_{IH_RS}		•	0.9 × V_{CC}			V
Low Level Input Voltage	V_{IL_RS}		•			0.5 × V_{CC}	V
Logic Input Current	I_{IN_RS}	0 ≤ V_{RS} ≤ V_{CC}	•	−170	0	+10	µA

1 All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to device ground, unless otherwise specified.

2 Not tested in production.

3 Pin capacitance given for reference only and is not tested in production.

4 All limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Table 2. Switching Characteristics

(The • denotes the specifications which apply over the full-operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, *Figure 4* applies with R_L = 60Ω, C_L = 100pF, R_{SL} = 0Ω, V_{RS} = 0V, TYP values at V_{CC} = 3.3V, unless otherwise noted. ([1], [4]))

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Transceiver Timing							
Maximum Data Rate	f_{MAX}		•	2			Mbps
TXD to Bus Dominant Propagation Delay	t_{PTXBD}	(*Figure 4*, *Figure 5*)	•	45	80	130	ns
TXD to Bus Recessive Propagation Delay	t_{PTXBR}	(*Figure 4*, *Figure 5*)	•	80	120	170	ns
TXD to Bus Dominant Propagation Delay, Slow Slew	t_{PTXBDS}	R_{SL} = 200kΩ (*Figure 4*, *Figure 5*)	•	200	466	1220	ns
TXD to Bus Recessive Propagation Delay, Slow Slew	t_{PTXBRS}	R_{SL} = 200kΩ (*Figure 4*, *Figure 5*)	•	400	722	2010	ns
Bus Dominant to RXD Propagation Delay	t_{PBDRX}	(*Figure 4*, *Figure 5*)	•	25	40	65	ns
Bus Recessive to RXD Propagation Delay	t_{PBRRX}	(*Figure 4*, *Figure 5*)	•	25	45	80	ns
TXD to RXD Dominant Propagation Delay	t_{PTXRXD}	(*Figure 4*, *Figure 5*)	•	80	120	180	ns
TXD to RXD Recessive Propagation Delay	t_{PTXRXR}	(*Figure 4*, *Figure 5*)	•	115	165	215	ns
TXD to RXD Dominant Propagation Delay, Slow Slew	$t_{PTXRXDS}$	R_{SL} = 200kΩ (*Figure 4*, *Figure 5*)	•	190	432	1110	ns
TXD to RXD Recessive Propagation Delay, Slow Slew	$t_{PTXRXRS}$	R_{SL} = 200kΩ (*Figure 4*, *Figure 5*)	•	420	794	1910	ns
TXD Timeout Time	t_{TOTXD}	(*Figure 4*, *Figure 6*)	•	0.5	1.1	4	ms

(The • denotes the specifications which apply over the full-operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V, *Figure 4* applies with R_L = 60Ω, C_L = 100pF, R_{SL} = 0Ω, V_{RS} = 0V, TYP values at V_{CC} = 3.3V, unless otherwise noted. ([1], [4]))

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Receiver Output Recessive Bit Time, 2Mbps, Loop Delay Symmetry	$t_{BIT(RXD),\ 2M}$	(*Figure 9*)	•	400	455	550	ns
RXD Enable from Shutdown	t_{ENRX}	(*Figure 7*)	•			40	µs
TXD Enable from Shutdown	t_{ENTX}	(*Figure 4*, *Figure 8*) ([3])	•			40	µs
Time to Shutdown, RXD	t_{SHDNRX}	(*Figure 7*)	•			250	ns
Time to Shutdown, TXD	t_{SHDNTX}	(*Figure 4*, *Figure 8*)	•			250	ns
Transmitter Drive Symmetry (Common-Mode Voltage Fluctuation)							
Driver Symmetry (CANH + CANL – $2V_{O(R)}$) (Dynamic Peak Measurement)	V_{SYM}	R_L = 60Ω/Tol. < 1%, C_{SPLIT} = 4.7nF/5%, f_{TXD} = 250kHz, Input Impedance of Oscilloscope ≤ 20pF/≥ 1MΩ (*Figure 4*)	•			±500	mV

1 All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to device ground, unless otherwise specified.

2 Not tested in production.

3 TXD must make a high-to-low transition after this time to assert a bus dominant state.

4 All limits are 100% tested at T_A = 25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Test Circuits

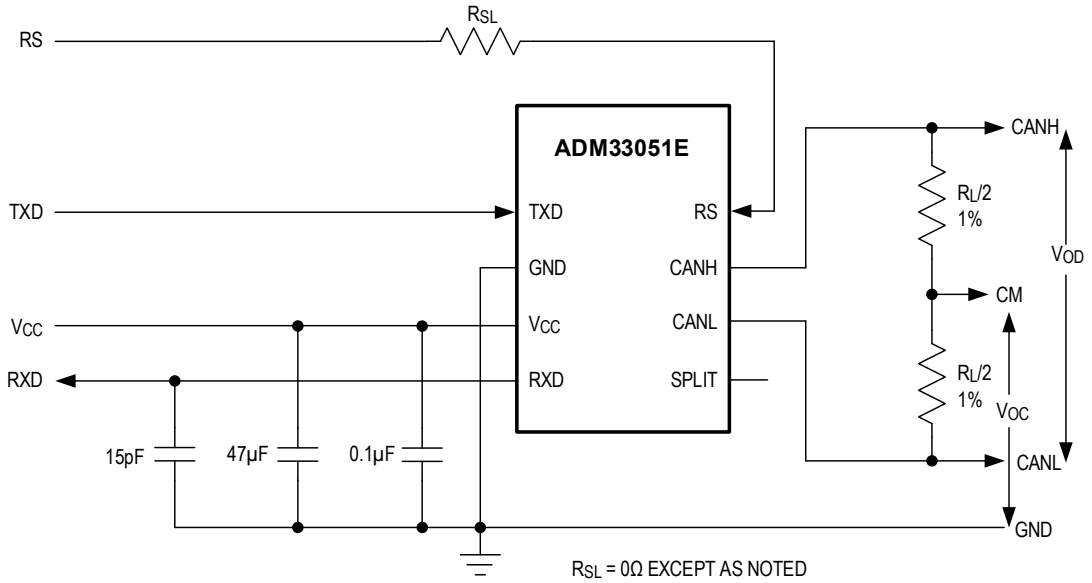


Figure 3. All Electrical Characteristic Measurements

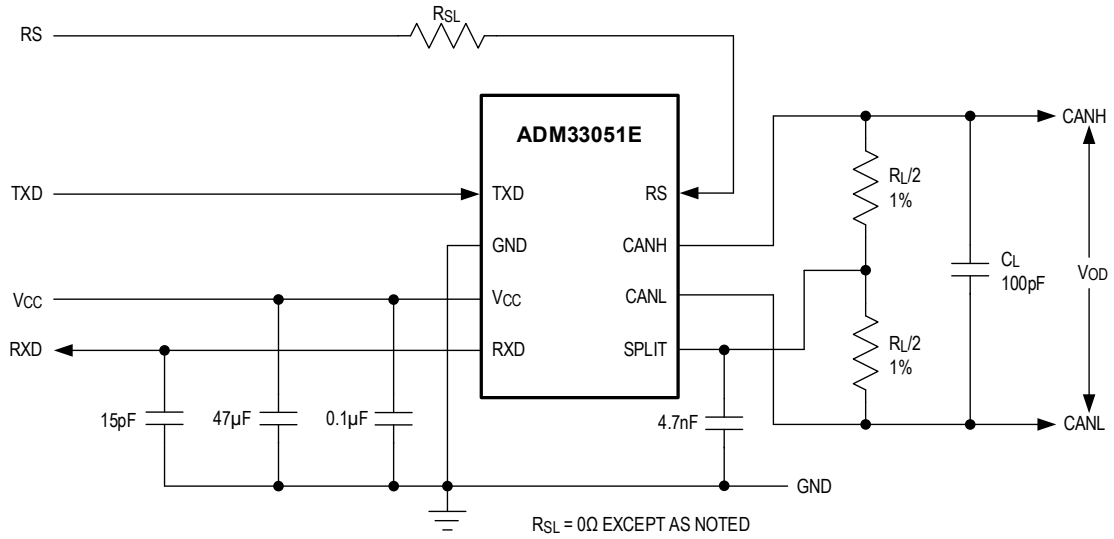


Figure 4. All Switching Characteristic Measurements Except Receiver Enable/Disable Times

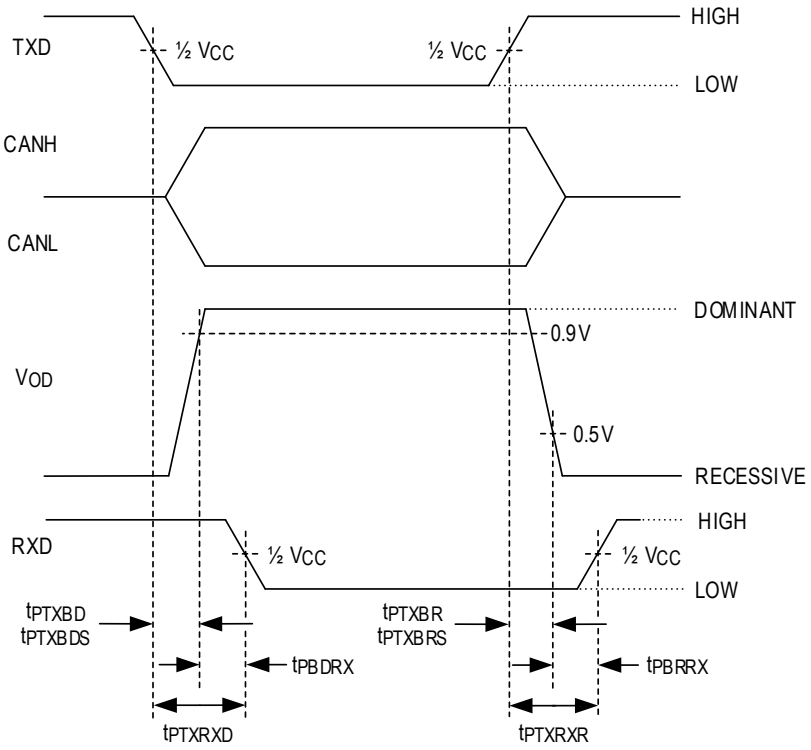


Figure 5. CAN Transceiver Data Propagation Timing Diagram

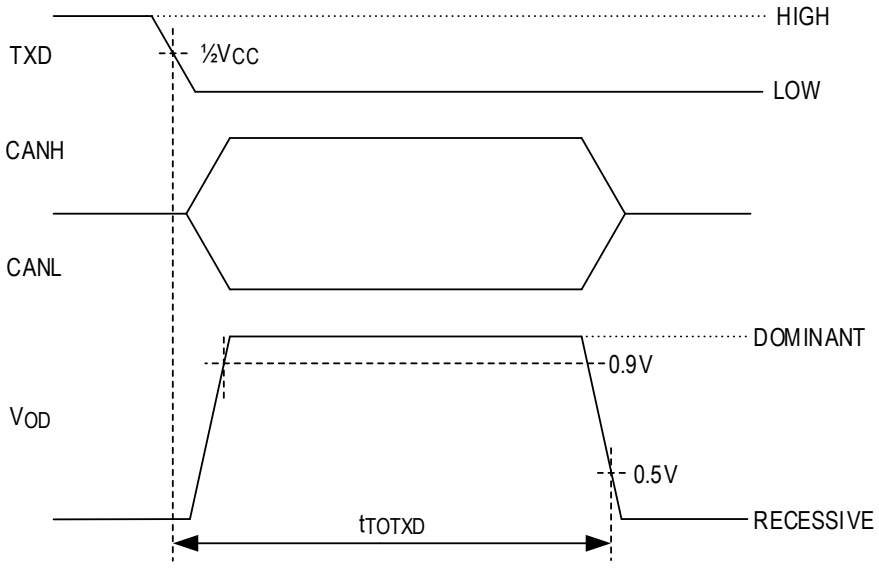


Figure 6. TXD Dominant Timeout Time

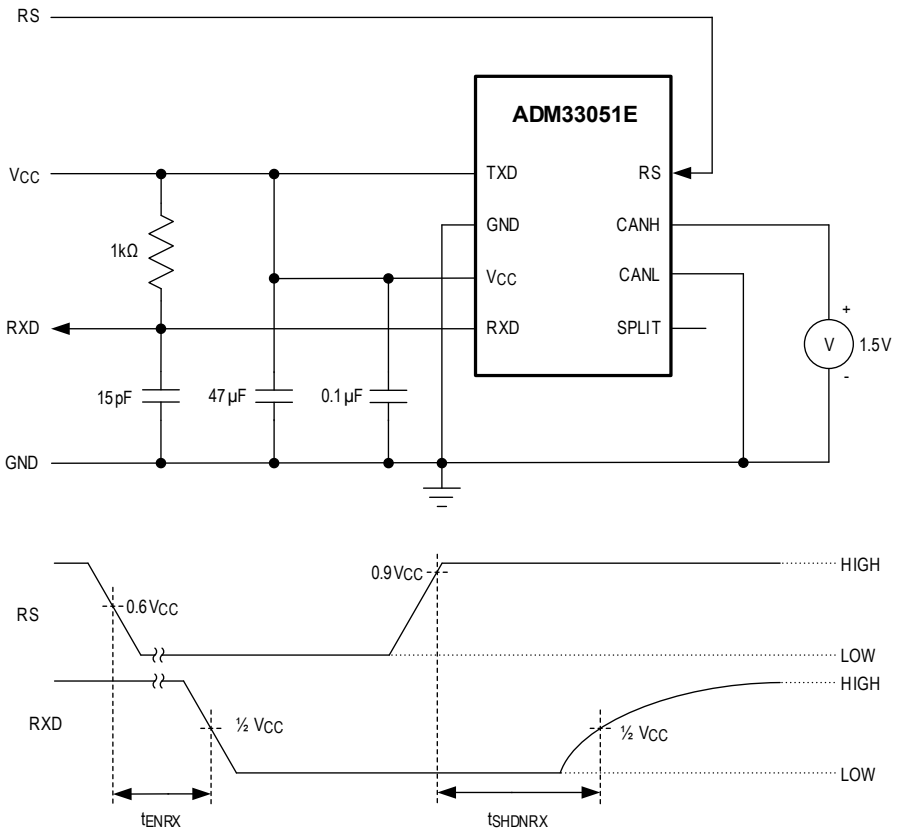


Figure 7. RXD Enable and Disable Timing

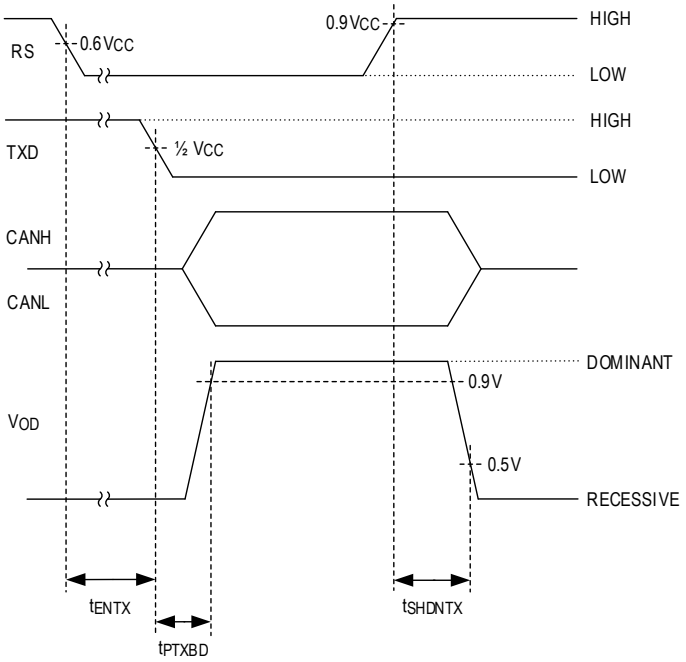


Figure 8. TXD Enable and Disable Timing

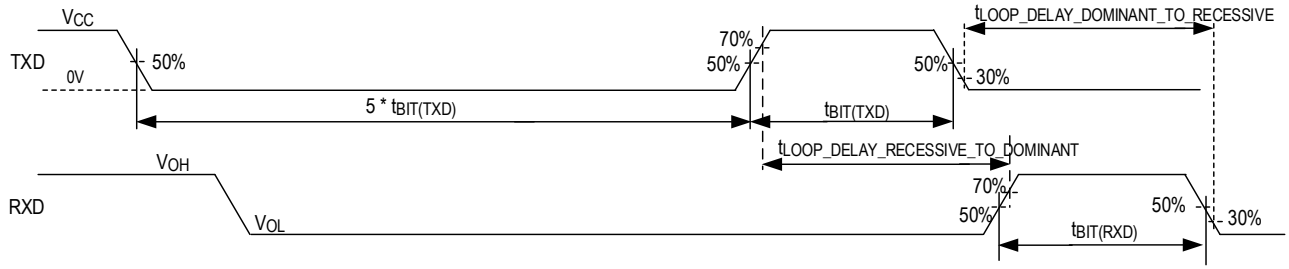


Figure 9. Loop Delay Symmetry

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified. All voltages referenced to GND.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC}	−0.3V to +6.0V
Logic Input Voltages (TXD, RS)	−0.3V to +6.0V
Interface I/O: CANH, CANL	−60V to +60V
Receiver Output (RXD)	−0.3V to (V_{CC} + 0.3)V
Bus Differential Voltage (CANH to CANL)	−120V to +120V
Continuous Power Dissipation (T_A = +70°C) (Derate 7.6mW/°C above +70°C)	606.1mW
Temperature	
Operating Ambient Range[1]	−40°C to +125°C
Storage Range	−65°C to +150°C
Maximum Junction (T_J)	+150°C
Lead (Soldering, 10sec)	+300°C

1 This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 170°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may result in device degradation or failure.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

PACKAGE TYPE	θ_{JA}	θ_{JC}	Ψ_{JB}	Ψ_{JT}	UNIT
S8+4C	132	38	84	6	°C/W

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

Table 5. ESD Ratings for ADM33051E

ESD MODEL	WITHSTAND THRESHOLD (kV)	CLASS
On Bus Pins (CANH, CANL)	±20	3B
All Other Pins	±8	3B

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

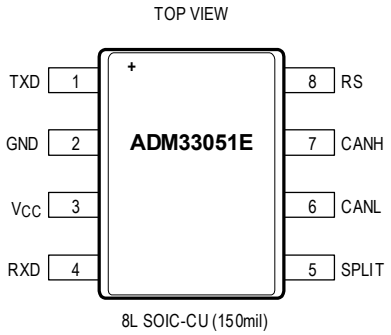


Figure 10. Pin Configuration

Pin Descriptions

Table 6. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION	REF SUPPLY	TYPE
1	TXD	Transmit Data Input. TXD is low in the dominant state. TXD features an integrated 500kΩ pull-up to V_{CC}.	V_{CC}	Digital
2	GND	Ground.	GND	
3	V_{CC}	Positive Supply. Bypass with 0.1µF ceramic capacitor as close to the device as possible.	V_{CC}	Power
4	RXD	Receiver Data Output. RXD is low in the dominant state. RXD features an integrated 500kΩ pull-up to V_{CC}.	V_{CC}	Digital
5	SPLIT	Common-Mode Stabilization Output, 1.9V (typ). If unused, leave open.	V_{CC}	Analog
6	CANL	Low Level CAN Bus Line.	V_{CC}	Analog
7	CANH	High Level CAN Bus Line.	V_{CC}	Analog
8	RS	Shutdown Mode/Slew Control Input. Drive RS high (> V_{IH_RS}) to put the chip into low-power shutdown state. Drive RS low (< V_{IL_RS}) to enable the device. Connect a resistor between RS to ground to control the slew rate. For more details, see the *RS Pin and Variable Slew Rate Control* section.	V_{CC}	Analog

Functional Tables

LOGIC INPUTS		MODE	CANH, CANL	RXD
RS	TXD			
0	0	Active	Dominant ($t < t_{TOTXD}$)	0
0	1	Active	Recessive	Receive Bus Data
~0.9V ≤ V_{RS} ≤ ~1.1V	–	Slew Control	–	–
1	X	Shutdown	High-Z	High-Z

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V, R_L = 60Ω, C_L = 100pF, V_{RS} = 0V, unless otherwise noted.

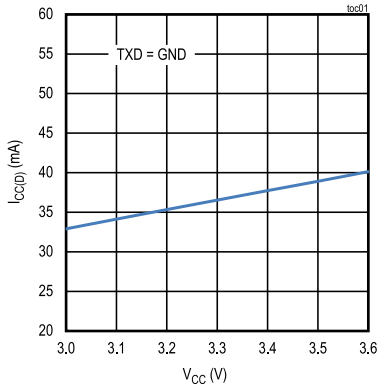


Figure 11. Supply Current (Dominant) vs. V_{CC}

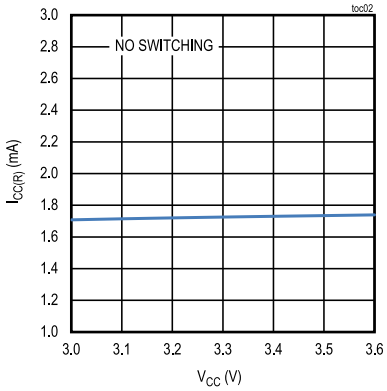


Figure 12. Supply Current (Recessive) vs. V_{CC}

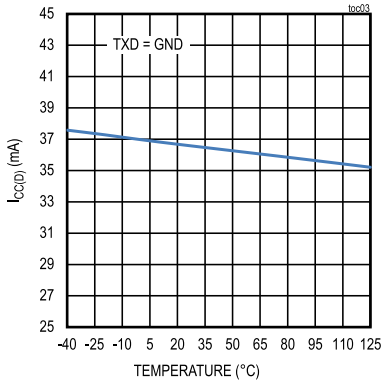


Figure 13. Supply Current (Dominant) vs. Temperature

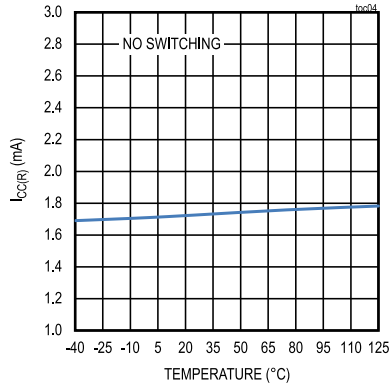


Figure 14. Supply Current (Recessive) vs. Temperature

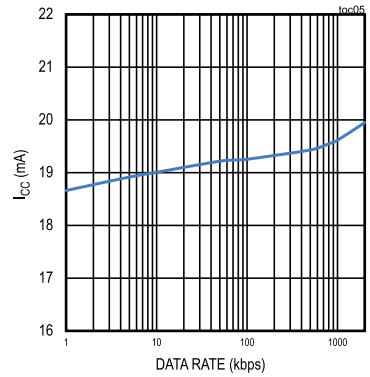


Figure 15. Supply Current vs. Data Rate

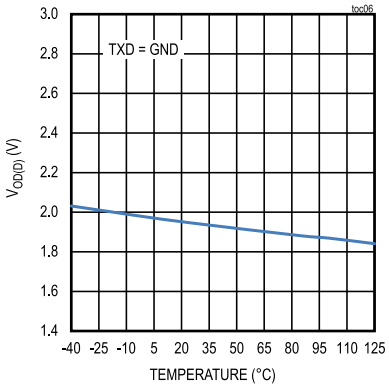


Figure 16. Driver Differential Output Voltage (Dominant) vs. Temperature

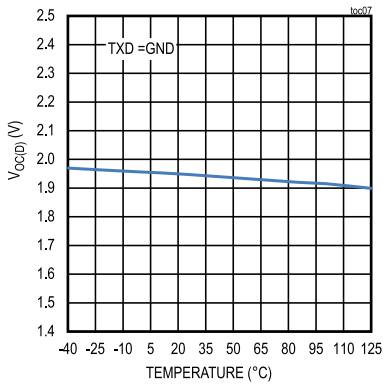


Figure 17. Common-Mode Output Voltage (Dominant) vs. Temperature

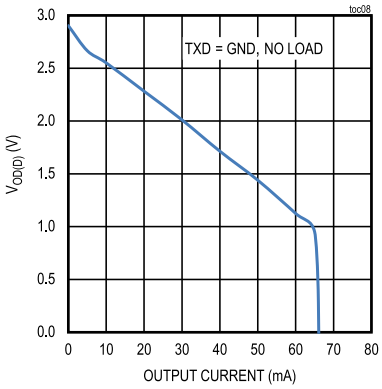


Figure 18. Driver Differential Output Voltage (Dominant) vs. Output Current

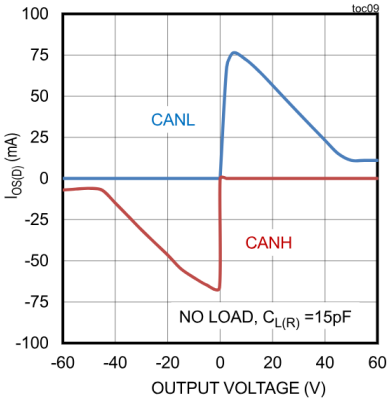


Figure 19. Driver Output Short-Circuit Current (Dominant) vs. Voltage

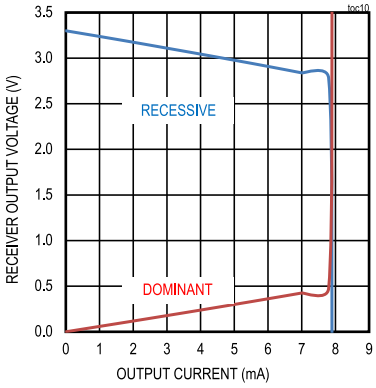


Figure 20. Receiver Output Voltage vs. Output Current

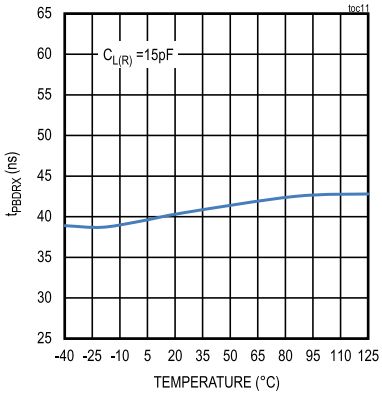


Figure 21. Bus Dominant to RXD Propagation Delay vs. Temperature

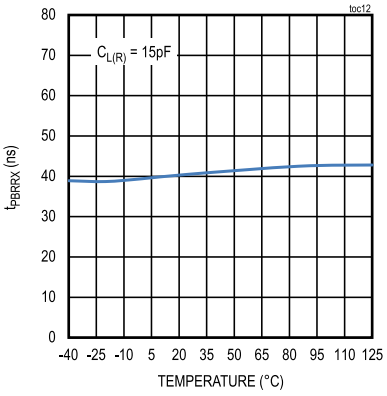


Figure 22. Bus Recessive to RXD Propagation Delay vs. Temperature

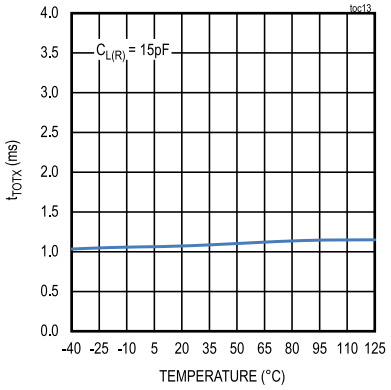


Figure 23. TXD Timeout Time vs. Temperature

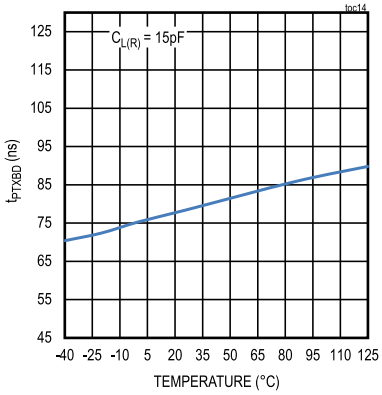


Figure 24. TXD to Bus Dominant Propagation Delay vs. Temperature

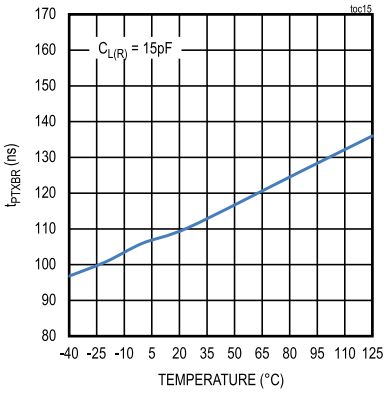


Figure 25. TXD to Bus Recessive Propagation Delay vs. Temperature

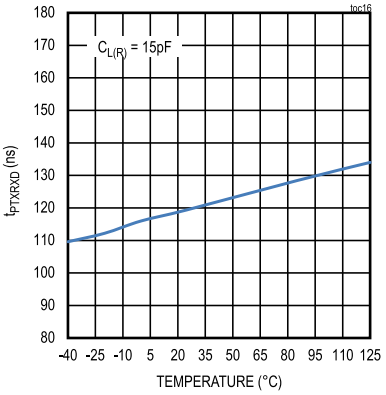


Figure 26. TXD to RXD Dominant Propagation Delay vs. Temperature

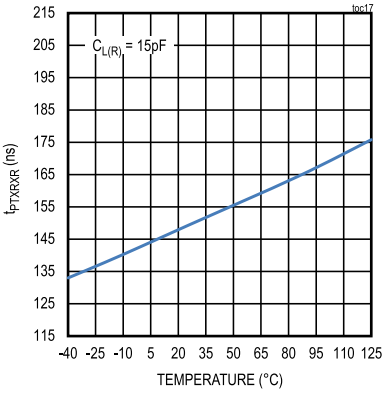


Figure 27. TXD to RXD Recessive Propagation Delay vs. Temperature

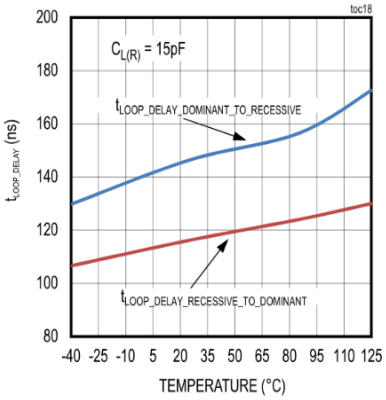


Figure 28. t_{LOOP_DELAY} vs. Temperature

BLOCK DIAGRAM

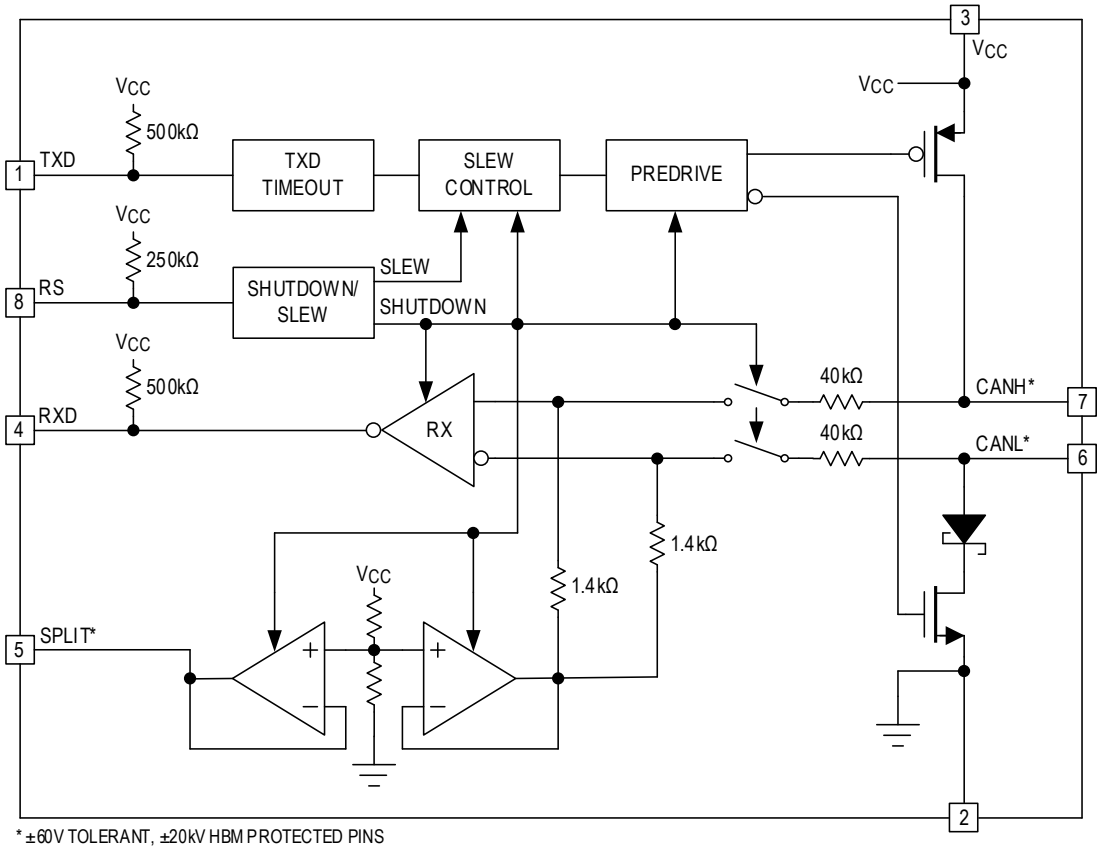


Figure 29. ADM33051E Simplified Block Diagram

THEORY OF OPERATION

±60V Fault Protection

The ADM33051E is an overvoltage tolerant CAN transceiver that operates with a 3.3V supply and provides extended common-mode operation, high noise immunity, and low electromagnetic emissions (EME). Industrial installations may encounter common-mode voltages between nodes far greater than the –2V to +7V range specified by the ISO 11898-2 standard. Competing CAN transceivers can be damaged by voltages beyond their typical absolute maximum ratings of –3V to +18V. The limited overvoltage tolerance makes implementation of effective external protection networks difficult without interfering with proper data network performance. Replacing standard CAN transceivers with ADM33051E devices can eliminate field failures due to overvoltage faults without using costly external protection devices.

The ±60V fault protection of the ADM33051E is achieved using a high voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered off and high-impedance conditions. The driver outputs use a progressive foldback current limit to protect against overvoltage faults while still allowing high current output drive.

The ADM33051E is protected from ±60V bus faults even with the loss of GND or V_{CC} (GND open faults are not tested in production). In the case of V_{CC} open, or shorted to GND, the ADM33051E is off, and the bus pins remain in a high-impedance state. Additional precautions must be taken in the case of V_{CC} present and GND open. The ADM33051E chip protects itself from damage but may turn on despite the open GND pin. When the RS or TXD input is pulled low with the GND pin floating, a sneak path to GND is established: through the ESD diode on the RS or TXD pin, out through the RS or TXD pin, and into the external driver that is pulling the pin low (*Figure 30*). The current in this path can have a maximum current of –100mA with a maximum voltage of approximately V_{CC} – 2.5V during an overvoltage fault condition on the CANL pin because the entire current that should flow out the GND pin may flow out the input pin instead. If a GND open fault with V_{CC} present is anticipated, the system designer should choose drivers for the RS and TXD inputs that are protected against shorts to V_{CC} – 2.5V.

The high voltage rating of the ADM33051E makes it simple to extend the overvoltage protection to higher levels using external protection components. Compared to lower voltage CAN transceivers, external protection devices with higher breakdown voltages can be used so as not to interfere with data transmission in the presence of large common-mode voltages. *Figure 35* shows a typical protection circuit against IEC Level 3 surge, while still providing up to ±25V common-mode range on the signal lines.

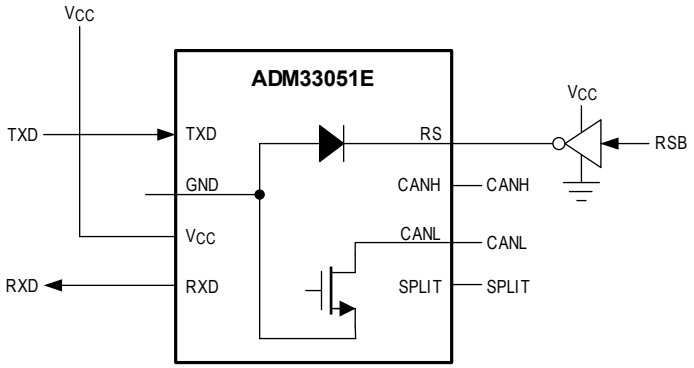


Figure 30. Sneak Path to GND with GND Pin Floating

±25V Extended Common-Mode Range

The ADM33051E receiver features an extended common-mode range of –25V to +25V. The wide common-mode increases the reliability of operation in environments with high common-mode voltages created by electrical noise or local ground potential differences due to ground loops. This extended common-mode range allows the ADM33051E to transmit and receive under conditions that cause data errors and possible device damage in competing products.

Driver

The driver provides full CAN compatibility. When TXD is low with the chip enabled (RS low), the dominant state is asserted on the CAN bus lines (subject to the TXD timeout t_{TOTXD}), the CANH driver pulls high and the CANL driver pulls low. When TXD is high and RS is low, the driver is in the recessive state, both the CANH and CANL drivers are in the Hi-Z state, and the bus termination resistor equalizes the voltage on CANH and CANL. In the recessive state, the impedance on CANH and CANL is determined by the receiver input resistance, R_{IN}. When RS is high, the ADM33051E is in shutdown, the CANH and CANL drivers are in the Hi-Z state, and the receiver input resistance R_{IN} is disconnected from the bus by a FET switch.

Transmit Dominant Timeout Function

The ADM33051E includes a 1.1ms (typ) timer to limit the time that the transmitter can hold the bus in the dominant state. If TXD is held low, a dominant state is asserted on CANH and CANL until the TXD timer times out at t_{TOTXD}, after which the transmitter reverts to the recessive state. The timer is reset when TXD is brought high. The transmitter asserts a dominant state upon the next TXD low.

The lowest data rate that can be communicated without interference from the transmit dominant timeout timer is 22kbps, corresponding to 11 consecutive dominant bits divided by a bit time equal to the minimum t_{TOTXD} value of 0.5ms. An 11 dominant bits is the maximum allowed by the CAN protocol, consisting of 5 dominant bits followed by an error frame of 6 dominant bits.

Driver Overvoltage, Overcurrent, and Overtemperature Protection

The driver outputs are protected from short-circuits to any voltage within the absolute maximum range of –60V to +60V. The maximum current in a fault condition is ±100mA. The driver includes a progressive foldback current limiting circuit that continuously reduces the driver current limit with increasing output fault voltage. The fault current is typically ±10mA for fault voltages of ±60V.

The ADM33051E also features thermal shutdown protection that disables the driver in case of excessive power dissipation (see Notes (1) and (2)). When the die temperature exceeds 170°C (typical), the transmitter is forced into the recessive state. The receiver remains operational.

Power-Up/Down Glitch-Free Outputs

The ADM33051E employs a supply undervoltage detection circuit to control the activation of the circuitry on-chip. During power-up, the CANH, CANL, and RXD outputs remain in a high-impedance state until the supply reaches a voltage sufficient to reliably operate the chip. At this point, the chip activates if RS is low. The receiver output goes active after a short delay t_{ENRX} and reflects the state at the CAN bus pins. The transmitter powers up in the transmit dominant timeout state regardless of the state of the TXD pin and remains in the recessive state until the first high-to-low transition on TXD after the TXD enable time t_{ENTX}. This ensures that the transmitter does not disturb the bus by glitching to the dominant state during power-up.

During power-down, the reverse occurs, the supply undervoltage detection circuit senses low supply voltage and immediately puts the chip into shutdown. CANH, CANL, and RXD outputs go to a high-impedance state. The voltage on RXD is pulled high by the 500kΩ pull-up resistor.

Common-Mode Voltage vs. Supply Voltage

When operating from a 3.3V supply the 2.5V nominal common-mode voltage specified in the ISO 11898-2 standard is too close to the 3.3V supply to provide symmetric drive levels while maintaining the necessary differential output voltage. To maintain driver symmetry, the common-mode reference voltage is lowered during 3.3V operation. The typical output common-mode voltage is 1.95V in the dominant state. The internal common-mode reference is set to $V_{CC}/2 + 0.3V = 1.95V$ to match the dominant state output common-mode voltage. This reference is independently buffered to supply the termination of the receiver input resistors and the SPLIT voltage output.

As the ADM33051E operates over a very wide common-mode range, this small shift of –0.55V in the common-mode when operating from 3.3V does not degrade data transmission or reception. An ADM33051E operating at 3.3V may share a bus with other CAN transceivers operating at 5V. However, the electromagnetic emissions may be larger if transceivers powered by different voltages share a bus, due to the fluctuation in the common-mode voltage from 1.95V (when an ADM33051E with a 3.3V supply is dominant on the bus) to 2.5V (when a CAN transceiver with a 5V supply is dominant on the bus).

RS Pin and Variable Slew Rate Control

The driver features adjustable slew rate for improved EME performance. The slew rate is set by the amount of current that is sourced by the RS pin when it is pulled below approximately 1.1V. This allows the slew rate to be set by a single slew control resistor R_{SL} in series with the RS pin (*Figure 3*).

Figure 31 shows the relationship between the series slew control resistor R_{SL} and the transmitter slew rate. $R_{SL} \leq 4k\Omega$ is recommended for high data rate communication. R_{SL} should be less than 200kΩ to ensure that the RS pin can be reliably pulled below V_{IL_RS} to enable the chip.

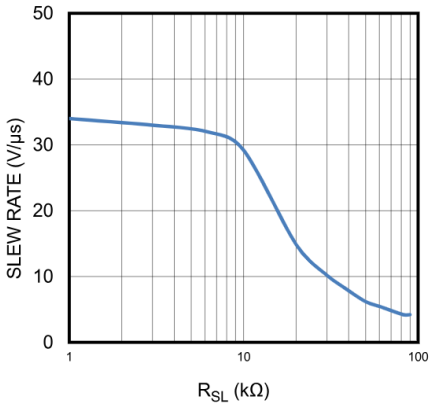


Figure 31. Slew Rate vs. Slew Control Resistor R_{SL}

When a voltage between 1.1V and V_{CC} is applied, the RS pin acts as a high-impedance receiver. A voltage above V_{IH_RS} puts the chip in shutdown, while a voltage below V_{IL_RS} but above 1.1V activates the chip and sets the transmitter to the minimum slew rate.

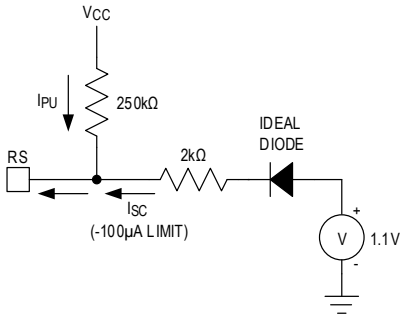


Figure 32. Equivalent Circuit of RS Pin

The slew control circuit on the RS pin is activated at applied voltages below 1.1V. The RS pin can be approximately modeled as a 1.1V voltage source with a series resistance of 2kΩ and a current compliance limit of –100µA, and a 250kΩ pull-up resistor to V_{CC} (*Figure 32*). Lowering the voltage on RS increases the slew control current I_{SC} being drawn from the slew control circuit until the voltage reaches ~0.9V, where the current drawn from the circuit is ~−100µA. Below an applied voltage of ~0.9V, the slew control circuit sources no additional current, and the current drawn from it remains at ~–100µA down to 0V.

The total current I_{RS} drawn from the RS pin for input voltage $0.9V \le V_{RS} \le 1.1V$ is the sum of the internal pull-up resistor current I_{RS} and the slew control current I_{SC}:

$$I_{RS(0.9V \le V_{RS} \le 1.1V)} = I_{PU} + I_{SC} = \frac{V_{CC} - V_{RS}}{250k\Omega} + \frac{1.1V - V_{RS}}{2k\Omega}$$

The transmitter slew rate is controlled by the slew control current I_{SC} with increasing current magnitude corresponding to higher slew rates. The slew rate can be controlled using a single slew control resistor R_{SL} in series with the RS pin. When the RS pin is pulled low towards ground by an external driver, the R_{SL} limits the amount of current drawn from the RS pin and sets the transmitter slew rate. Alternatively, the slew rate may be controlled by an external voltage or current source.

High Symmetry Driver with Variable Slew Rate

The electromagnetic emissions spectrum of a differential line transmitter is largely determined by the variation in the common-mode voltage during switching, as the differential component of the emissions from the two lines cancel, while the common-mode emissions of the two lines add. The ADM33051E transmitter has been designed to maintain highly symmetric transitions on the CANH and CANL lines to minimize the perturbation of the common-mode voltage during switching (*Figure 33*), resulting in low EME. The common-mode switching symmetry is guaranteed by the V_{SYM} specification.

In addition to full compliance with the ISO 11898-2 standard, the ADM33051E meets the more stringent requirements of ISO 11898-5 for bus driver symmetry. This requires that the common-mode voltage stay within the limits not only during the static dominant and recessive states, but during the bit transition states as well. Ultra-high speed peak detect circuits are used during manufacturing test to ensure that V_{SYM} limits are not exceeded at any point during the switching cycle.

The high frequency content may be reduced by choosing a lower data rate and a slower slew rate for the signal transitions. The ADM33051E provides an approximate 20 to 1 reduction in slew rate, with a corresponding decrease in the high frequency content. The lowest slew rate is suitable for data communication at 200kbps or below, while the highest slew rate supports 2Mbps. The slew rate limit circuit maintains consistent control of transmitter slew rates across voltage and temperature to ensure predictable performance under all operating conditions.

Figure 34 shows the reduction in high frequency content of the common-mode voltage achieved by the lowest slew rate compared to the highest slew rate at 200kbps.

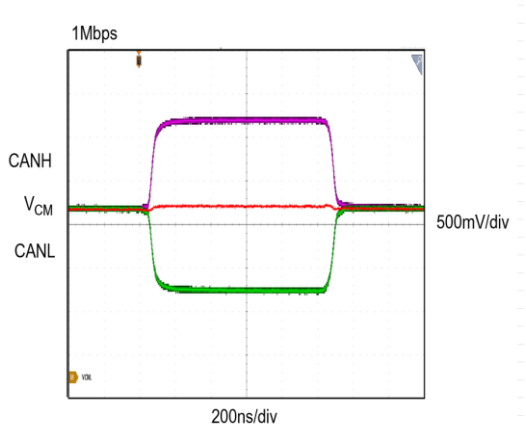


Figure 33. Low Perturbation of Common-Mode Voltage During Switching

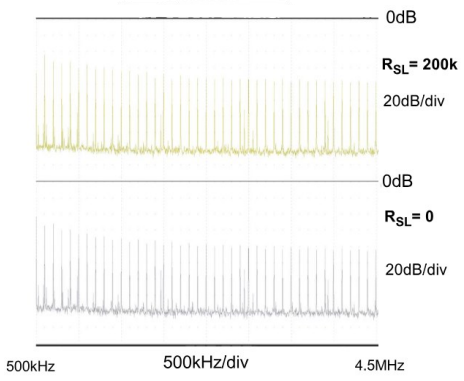


Figure 34. Power Spectrum of Common-Mode Voltage Showing High Frequency Reduction of Lowest Slew Rate (R_{SL} = 200kΩ) Compared to Highest Slew Rate (R_{SL}=0Ω)

SPLIT Pin Output for Split Termination Support

Split termination is an optional termination technique to reduce common-mode voltage perturbations that can produce EME. A split terminator divides the single line-end termination resistor (nominally 120Ω) into two series resistors of half the value of the single termination resistor (*Figure 4*). The center point of the two resistors is connected to a low-impedance voltage source that sets the recessive common-mode voltage.

Split termination suppresses common-mode voltage perturbations by providing a low-impedance load to common-mode noise sources such as transmitter noise or coupling to external noise sources. In the case of single resistor termination, the only load on a common-mode noise source is the parallel impedance of the input resistors of the CAN transceivers on the bus. This results in a common-mode impedance of several kilohms for a small network. The split termination, on the other hand, provides a common-mode load equal to the parallel resistance of the two split termination resistors, or ¼ the resistance of the single termination resistor (30Ω). This low common-mode impedance results in a reduction of the common-mode noise voltage compared to the much higher common-mode impedance of the single resistor termination.

The SPLIT pin on the ADM33051E provides a buffered voltage to bias the mid-point of the split termination resistors. The voltage on the SPLIT pin matches the common-mode voltage established by the transmitter in the dominant state and the receiver input resistor bias during the recessive state: $V_{CC}/2$ + 0.3V when V_{CC} = 3.3V. Decouple SPLIT with a 4.7nF capacitor to ground to lower the AC impedance to better suppress fast transients. SPLIT is a high voltage fault tolerant output that tolerates the same ±60V overvoltage faults and ±20kV ESD discharges (HBM) as CANH and CANL.

One disadvantage of the SPLIT termination is higher power supply current if the two terminating transceivers differ in their common-mode voltage due to differences in V_{CC} or GND potential or to chip-to-chip variations in the internal reference voltages. This results in the transceiver with the higher common-mode voltage sourcing current into the bus lines through its SPLIT pin, while the transceiver with the lower common-mode voltage sinks current through its SPLIT pin.

Ideal Passive Behavior to CAN Bus With Supply Off

When the power supply is removed or the chip is in shutdown, the CANH and CANL pins are in a high-impedance state. The receiver inputs are isolated from the CANH and CANL nodes by FET switches, which opens in the absence of power, thereby preventing the resistor dividers on the receiver input from loading the bus. The high-impedance state of the receiver is maintained over a range determined by the ESD protection of the receiver input, typically −0.3V to +10V. For bus voltages outside this range, the current flowing into the receiver is governed by the conduction voltages of the ESD device and the 40kΩ (typ) receiver input resistance.

Micropower Shutdown Mode

The low-power shutdown mode is entered by raising the voltage on the RS pin above its V_{IH_RS} threshold. This turns off all circuits that draw DC bias currents and disables all chip functionality. Any remaining supply current in shutdown is due to semiconductor device leakage currents. All the outputs −CANH, CANL, and RXD− are in a high-impedance state, with RXD pulled up to V_{CC} through a 500kΩ resistor to ensure it remains in the recessive state.

The chip is enabled by bringing the RS pin below its V_{IL_RS} threshold. The RXD output goes active after the time delay t_{ENRX} (40µs max). CANH and CANL switch to the dominant state at the first high-to-low transition of TXD after the t_{ENTX} delay.

Logic I/O Interface Voltages and Power Supply Sequencing

Logic inputs RS and TXD are protected by ground referenced ESD devices. These inputs do not draw a high current if driven by voltages exceeding V_{CC} as long as the absolute maximum ratings for these pins are not exceeded. The V_{CC} supply for the ADM33051E may be safely brought up before or after the supplies powering the logic driving the RXD and TXD inputs with no adverse consequences.

APPLICATIONS INFORMATION

±20kV ESD Protection

The ADM33051E features exceptionally robust ESD protection. The transceiver interface pins (CANH, CANL) feature protection with respect to GND to ±20kV HBM ESD without latchup or damage, during all modes of operation or while unpowered. All other pins are protected to ±8kV HBM ESD to make the ADM33051E reliable under severe environmental conditions.

Auxiliary Protection for IEC Surge, EFT, and ESD

A transceiver used in an industrial setting may be exposed to high levels of electrical overstress due to phenomena such as lightning surge, electrical fast transient (EFT) from switching high-current inductive loads, and ESD from the discharge of electrically charged personnel or equipment. Test methods to evaluate immunity of electronic equipment to these phenomena are defined in the IEC standards 61000-4-2, 61000-4-4, and 61000-4-5, which address ESD, EFT, and surge, respectively. The transients produced by the EFT and particularly the surge tests contain much more energy than ESD transients. The ADM33051E is designed for high robustness against ESD, but the on-chip protection is not able to absorb the energy associated with the 61000-4-5 surge transients. Therefore, external protections are necessary to achieve a high level of surge protection and can also extend the ESD and EFT performance of the ADM33051E.

To achieve the same protection levels with split-termination using SPLIT pin, an addition TVS is required, refer to the ADM33051E evaluation kit (EV kit) data sheet. The typical application circuit shown in *Figure 35* provides following protections for single resistor termination:

- IEC 61000-4-2 Edition 3.0 2025-03 ESD Level 4: ±15V air, ±10kV contact
  - Line to GND, direct discharge to bus pins with transceiver and protection circuit ground.
  - ESD test model shown in *Figure 36*, and ESD generator current waveform shown in *Figure 37*.
- IEC 61000-4-4 Edition 3.0 2012-04 EFT Level 4 (I/O Port): ±2kV
  - Line to GND, both 5kHz/100kHz repetition rate, 15ms/0.75ms burst duration, 60 second test duration.
  - EFT test model shown in *Figure 38*, and EFT waveform shown in *Figure 39*.
- IEC 61000-4-5 Edition 3.1 2017-08 Surge Level 3: ±2kV
  - Line to GND, 8/20µs waveform, each line coupled to generator through 80Ω resistor (per Edition 3.1 2017 Figure 11).
  - Surge test model shown in *Figure 40*, and surge voltage waveform shown in *Figure 41*.

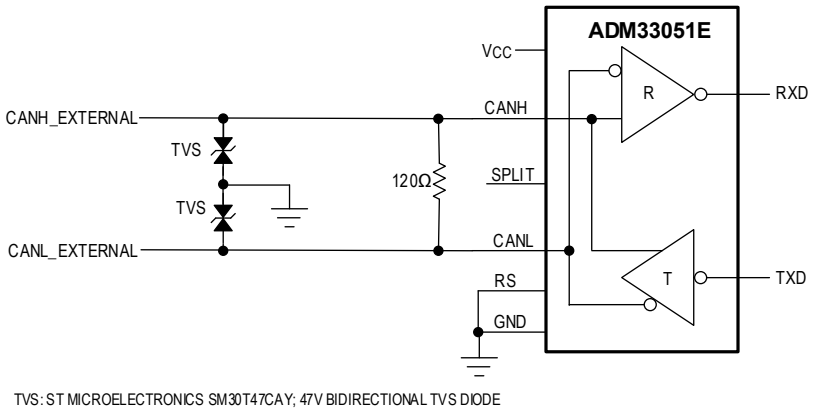


Figure 35. Typical Application with Protection Against IEC Surge, EFT, and ESD

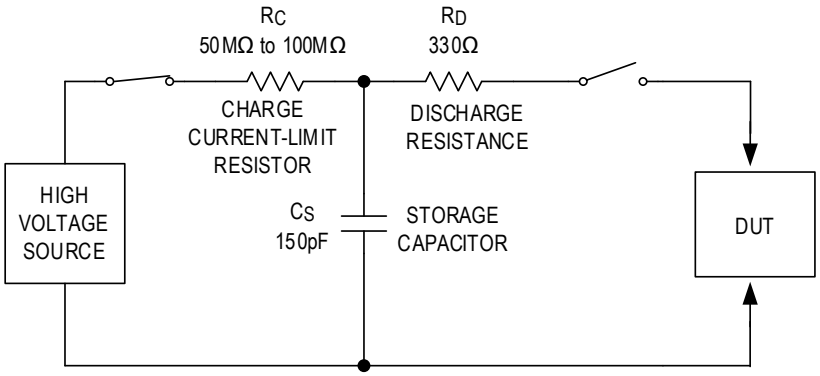


Figure 36. IEC 61000-4-2 ESD Test Model

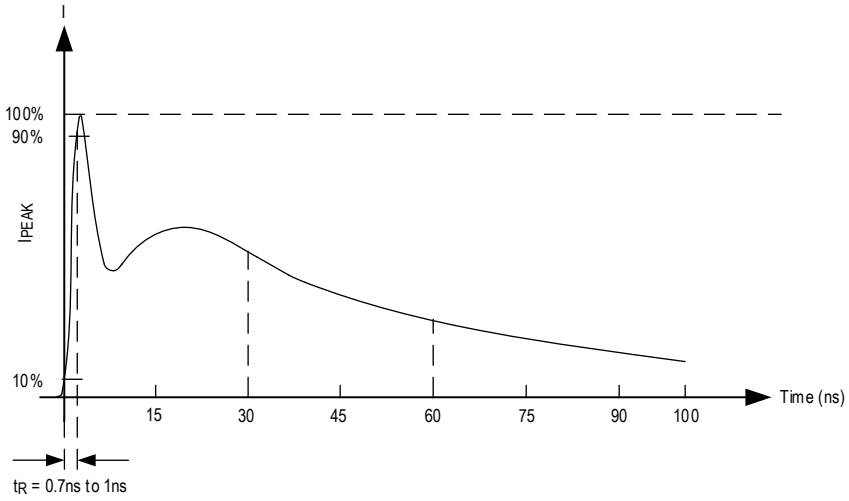


Figure 37. IEC 61000-4-2 ESD Generator Current Waveform

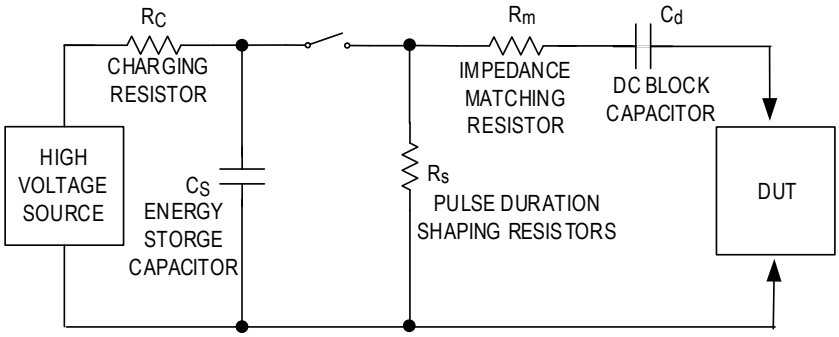


Figure 38. IEC 61000-4-4 Test Model

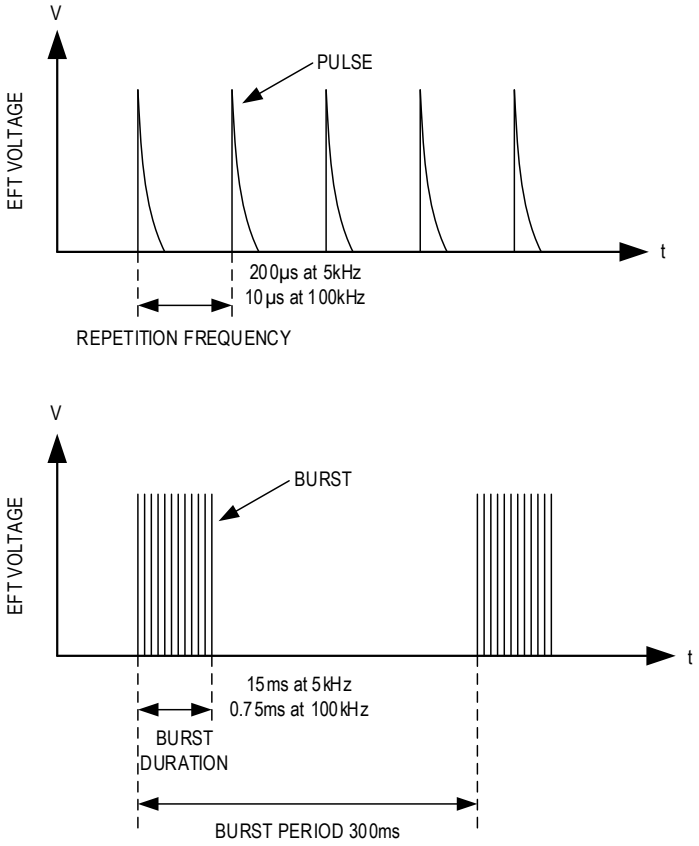


Figure 39. IEC 61000-4-4 Electrical Fast Transient/Burst Waveform

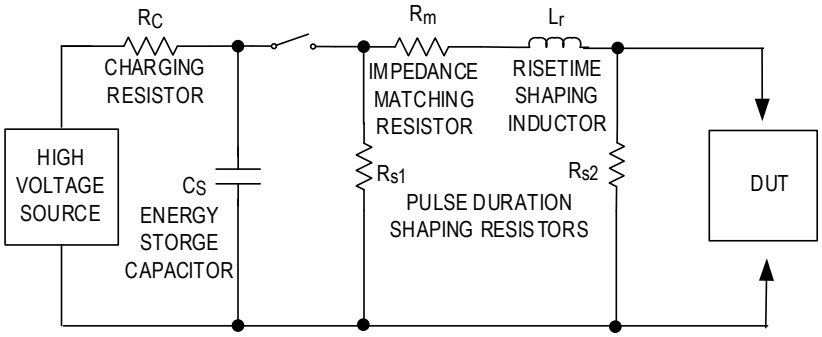


Figure 40. IEC 61000-4-5 Test Model

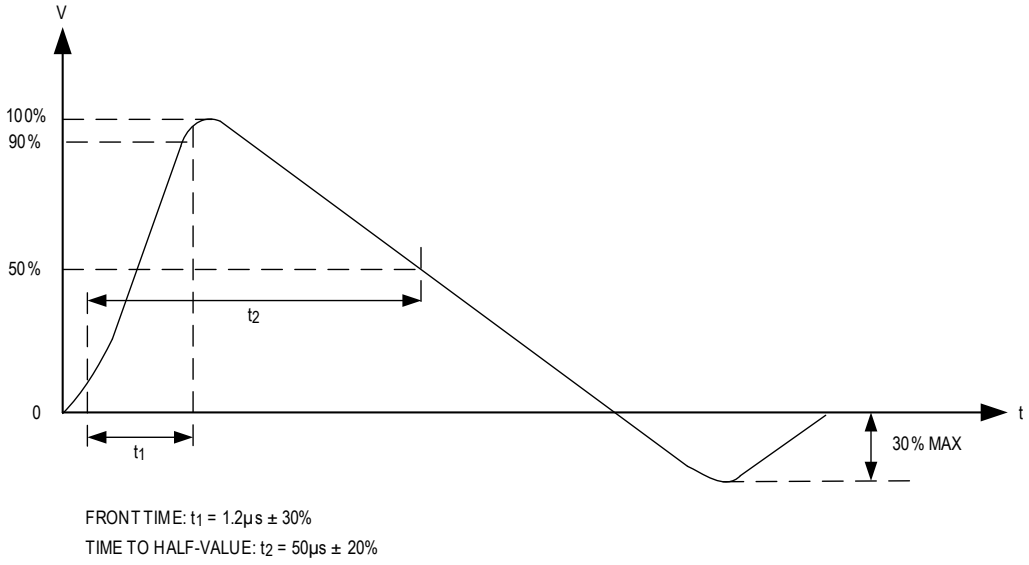
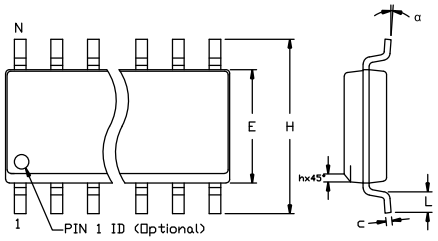
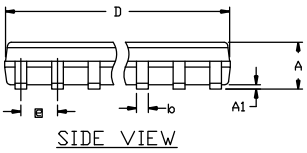


Figure 41. IEC 61000-4-5 1.2/50µs Surge Voltage Waveform

OUTLINE DIMENSIONS





COMMON DIMENSIONS						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
A	.053	.061	.069	1.35	1.55	1.75
A1	.004	.007	.010	0.10	0.18	0.25
b	.014	.017	.019	0.35	0.42	0.49
c	.007	.009	.010	0.19	0.22	0.25
E	.150	.154	.157	3.80	3.90	4.00
e	.050 BSC			1.27 BSC		
H	.228	.236	.244	5.80	6.00	6.20
L	.016	.033	.050	0.40	0.84	1.27
θx	0°	4°	8°	0°	4°	8°
h	0.01	0.015	0.019	0.25	0.38	0.5

* Typical value provided for reference only.
This is not a specification.

VARIATION A						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
D	.189	.193	.197	4.80	4.90	5.00
N	8					
MS012	AA					
PKG. CODE	S8+2, S8+2C, S8+4, S8+4C, S8+5, S8+6F, S8+7F, S8+8F, S8+10F, S8+11F, S8+16F, S8+19F, S8+20, S8+21, S8MK+1, S8M+5, S8MS+22, S8+22, S8+23, S8MS+23, S8MS+24, S8MS+24A					

VARIATION B						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
D	.337	.341	.344	8.55	8.65	8.75
N	14					
MS012	AB					
PKG. CODE	S14+1, S14+1C, S14+4, S14+5, S14+6, S14M+4, S14M+5, S14M+6, S14M+7					

VARIATION C						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
D	.386	.390	.394	9.80	9.90	10.00
N	16					
MS012	AC					
PKG. CODE	S16+1, S16+1C, S16+3, S16+5, S16+6, S16+8, S16+7F, S16+9F, S16+10F, S16M+3, S16M+6, S16M+11, S16MS+12					

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

ANALOG DEVICES

TITLE:
PACKAGE OUTLINE,
8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
ALIREZA REZVANI	21-0041	V	1/1

ORDERING GUIDE

Table 7. Ordering Guide

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
ADM33051EBRZ	–40°C to +125°C	8L SOIC-CU (150mil)	S8+4C
ADM33051EBRZ-RL	–40°C to +125°C	8L SOIC-CU (150mil)	S8+4C

Z = RoHS Compliant Part.