Data Sheet

ADM3055E/ADM3057E

5kV rms/3kV rms, Signal and Power Isolated, CAN Transceivers for CAN FD

FEATURES

- 5kV rms/3kV rms signal and power isolated CAN transceivers
- *iso*Power integrated isolated dc-to-dc converter
- V_{IO} pin for 1.7V to 5.5V logic levels
- ISO 11898-2:2016 compliant (CAN FD)
- Data rates up to 12Mbps for CAN FD
- Low maximum loop propagation delay: 150ns
- Extended common-mode range: ±25V
- Bus fault protection: ±40V on CANH and CANL pins
- Low power standby support remote wake request
- Extra isolated signal for control (such as termination switches)
- Passes EN 55022 Class B by 6 dB
- Slope control for reduced EMI
- Safety and regulatory approvals
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 595V peak
  - UL 1577
    - V_{ISO} = 5000V rms for 1 minute, ADM3055E
    - V_{ISO} = 3750V rms for 1 minute, ADM3057E
  - IEC/EN/CSA 62368-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB4943.1
- High common-mode transient immunity: >75kV/µs
- Industrial operating temperature range: −40°C to +105°C

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Industrial automation
- Process control and building control
- Transport and infrastructure

GENERAL DESCRIPTION

The ADM3055E/ADM3057E are 5kV rms and 3kV rms isolated controller area network (CAN) physical layer transceivers with integrated isolated dc-to-dc converters. The ADM3055E/ADM3057E meet flexible data rate (CAN FD) requirements for operation to 5Mbps and higher and comply with the ISO 11898-2: 2016 standard. The ADM3055E/ADM3057E are capable of supporting data rates as high as 12Mbps.

The devices employ Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a CAN transceiver, and an Analog Devices *iso*Power® dc-to-dc converter into a single, surface-mount, small outline integrated circuit (SOIC) package. The devices are powered by a single 5V supply, realizing a fully isolated solution for CAN and CAN FD. Radiated emissions from the high frequency switching of the dc-to-dc convertors are kept below EN 55022 Class B limits by continuous adjustments to the switching frequency.

The ADM3055E/ADM3057E provide complete isolation between the CAN controller and physical layer bus. Safety and regulatory approvals for 5kV rms isolation voltage, 10kV surge test, and 8.3mm creepage and clearance ensure the ADM3055E meets application reinforced isolation requirements. The ADM3057E has an isolation voltage of 3kV rms and 7.8mm creepage in a 20-lead, wide body SOIC.

Low propagation delays through the isolation support longer bus cables. Slope control mode is available for standard CAN at low data rates. Standby mode minimizes power consumption when the bus is idle or if the node goes offline. Silent mode allows the TXD input to be ignored for listen only mode.

Dominant timeout functionality protects against bus lock up in a fault condition. The current limiting and thermal shutdown features protect against output short circuits. The devices are fully specified over an industrial temperature range of −40°C to +105°C.

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FUNCTIONAL BLOCK DIAGRAM

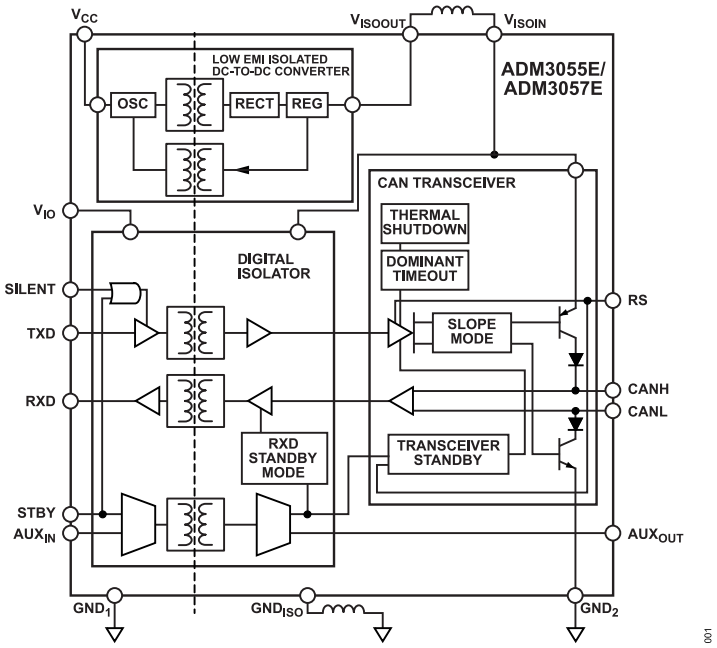

Figure 1. ADM3055E/ADM3057E Functional Block Diagram

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

All voltages are relative to their respective ground. 4.5V ≤ V_{CC} ≤ 5.5V, 1.7V ≤ V_{IO} ≤ 5.5V, T_{MIN} to T_{MAX}, and STBY low, unless otherwise noted. Typical specifications are at V_{CC} = V_{IO} = 5V and T_A = 25°C, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Logic Side *iso*Power Current	I_{CC}					
Standby			13.5	30	mA	STBY high, AUX_{IN} low, load resistance (R_L) = 60Ω
Recessive State (or Silent)			27	40	mA	TXD and/or SILENT high, R_L = 60Ω
Dominant State			180	260	mA	Fault condition, see the Theory of Operation section, R_L = 60Ω
70% Dominant/30% Recessive						Worst case, see the Theory of Operation section, R_L = 60Ω
1Mbps			138		mA	
5Mbps			151	200	mA	
12Mbps			177	220	mA	
Switching Frequency	f_{OSC}		180		MHz	Frequency hopping center
Logic Side *i*Coupler Current	I_{IO}					
Normal Mode			3.6	5	mA	TXD high, low or switching, AUX_{IN} low
Standby Mode			1.2	2	mA	STBY high
Isolated Supply Voltage	V_{ISO}		5.0		V	
DRIVER						
Differential Outputs						See Figure 28
Recessive State, Normal Mode						TXD high, R_L and common-mode filter capacitor (C_F) open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output Voltage	V_{OD}	−500		+50	mV	
Dominant State, Normal Mode						TXD and SILENT low, C_F open
CANH Voltage	V_{CANH}	2.75		4.5	V	50Ω ≤ R_L ≤ 65Ω
CANL Voltage	V_{CANL}	0.5		2.0	V	50Ω ≤ R_L ≤ 65Ω
Differential Output Voltage	V_{OD}	1.5		3.0	V	50Ω ≤ R_L ≤ 65Ω
		1.4		3.3	V	45Ω ≤ R_L ≤ 70Ω
		1.5		5.0	V	R_L = 2240Ω
Standby Mode						STBY high, R_L and C_F open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	−0.1		+0.1	V	
Differential Output Voltage	V_{OD}	−200		+200	mV	
Output Symmetry (V_{ISOIN} − V_{CANH} − V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60Ω, C_F = 4.7nF, RS low
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3V
CANL				115	mA	V_{CANL} = 18V
Steady State						
CANH				115	mA	V_{CANH} = −24V
CANL				115	mA	V_{CANL} = 24V
Logic Inputs (TXD, SILENT, STBY, AUX_{IN})						
Input Voltage						
High	V_{IH}	0.65 × V_{IO}			V	
Low	V_{IL}			0.35 × V_{IO}	V	

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Capacitance	C_{IN}		4		pF	
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	µA	Input high or low
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 29, C_{RXD} open, −25V < V_{CANL} < +25V, −25V < V_{CANH} < +25V
Recessive		−1.0		+0.5	V	
		−1.0		+0.4	V	STBY high
Dominant		0.9		5.0	V	
		1.15		5.0	V	STBY high
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\|I_{IN\ (OFF)}\|$			10	µA	V_{CANH}, V_{CANL} = 5V, V_{CC} = 0V
Input Resistance						
CANH, CANL	R_{INH}, R_{INL}	6		25	kΩ	
Differential	R_{DIFF}	20		100	kΩ	
Matching	m_R	−0.03		+0.03	Ω/Ω	$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
Input Capacitance						
CANH, CANL	C_{INH}, C_{INL}		35		pF	
Differential	C_{DIFF}		12		pF	
Logic Outputs (RXD, AUX_{OUT})						
Output Voltage						
Low	V_{OL}		0.2	0.4	V	Output current (I_{OUT}) = 2mA
High	V_{OH}					
RXD		V_{IO} − 0.2			V	I_{OUT} = −2mA
AUX_{OUT}		+2.4			V	I_{OUT} = −2mA
Short-Circuit Current	I_{OS}					
RXD		7		85	mA	Output voltage (V_{OUT}) = GND_1 or V_{IO}
COMMON-MODE TRANSIENT IMMUNITY[1]						Common-mode voltage (V_{CM}) ≥ 1kV, transient magnitude ≥ 800V
Input High, Recessive	$\|CM_H\|$	75	100		kV/µs	V_{IN} = V_{IO} (AUX_{IN}, TXD) or CANH/CANL recessive
Input Low, Dominant	$\|CM_L\|$	75	100		kV/µs	V_{IN} = 0V (AUX_{IN}, TXD) or CANH/CANL dominant
SLOPE CONTROL						
Input Voltage for Standby Mode	V_{STB}	4.0			V	
Current for Slope Control Mode	I_{SLOPE}			−240	µA	RS voltage (V_{RS}) = 0V
Slope Control Mode Voltage	V_{SLOPE}	2.1			V	RS current (I_{RS}) = 10µA
Input Voltage for High Speed Mode	V_{HS}			1	V	

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≥ 2.4V, CANH/CANL recessive, or RXD ≥ V_{IO} − 0.2V. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining AUX_{OUT} ≤ 0.4V, CANH/CANL dominant, or RXD ≤ 0.4V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

TIMING SPECIFICATIONS

All voltages are relative to their respective ground. 4.5V ≤ V_{CC} ≤ 5.5V, 1.7V ≤ V_{IO} ≤ 5.5V, T_{MIN} to T_{MAX}, and STBY low, unless otherwise noted. Typical specifications are at V_{CC} = V_{IO} = 5V and T_A = 25°C, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						SILENT low, bit time on the TXD pin as transmitted by the CAN controller (t_{BIT_TXD}) = 200ns, see Figure 2 and Figure 30, slope resistance (R_{SLOPE}) = 0Ω, R_L = 60Ω, load capacitance (C_L) = 100pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		46	70	ns	
Transmit Dominant Timeout	t_{DT}	1175		4000	µs	TXD low, see Figure 5
RECEIVER						SILENT low, see Figure 2 and Figure 31, R_L = 60Ω, C_L = 100pF, RXD capacitance (C_{RXD}) = 15pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}					
Full Speed Mode				150	ns	R_{SLOPE} = 0Ω, t_{BIT_TXD} = 200ns
Slope Control Mode				300	ns	R_{SLOPE} = 47kΩ, t_{BIT_TXD} = 1µs
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}					
Full Speed Mode				150	ns	R_{SLOPE} = 0Ω, t_{BIT_TXD} = 200ns
Slope Control Mode				300	ns	R_{SLOPE} = 47kΩ, t_{BIT_TXD} = 1µs
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2Mbps		450		550	ns	t_{BIT_TXD} = 500ns
5Mbps		160		220	ns	t_{BIT_TXD} = 200ns
8Mbps		85		140	ns	t_{BIT_TXD} = 125ns
12Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3ns
CANH, CANL SLEW RATE	|SR|		7		V/µs	SILENT low, see Figure 30, R_L = 60Ω, C_L = 100pF, R_{SLOPE} = 47kΩ
STANDBY MODE						
Minimum Pulse Width Detected (Receiver Filter Time)	t_{FILTER}	1		5	µs	STBY high, see Figure 4
Wake-Up Pattern Detection Reset Time	t_{WUPR}	1175		4000	µs	STBY high, see Figure 4
Normal Mode to Standby Mode Time	t_{STBY_ON}			25	µs	
Standby Mode to Normal Mode Time	t_{STBY_OFF}			25	µs	Time until RXD valid
AUXILIARY SIGNAL						
Maximum Switching Rate	f_{AUX}	20			kHz	
AUX_{IN} to AUX_{OUT} Propagation Delay	t_{AUX}			25	µs	
SILENT MODE						
Normal Mode to Silent Mode Time	t_{SILENT_ON}		40	100	ns	TXD low, R_{SLOPE} = 0Ω, see Figure 3
Silent Mode to Normal Mode Time	t_{SILENT_OFF}		50	100	ns	TXD low, R_{SLOPE} = 0Ω, see Figure 3

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Timing Diagrams

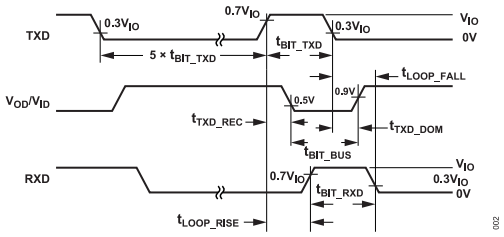

Figure 2. Transceiver Timing Diagram

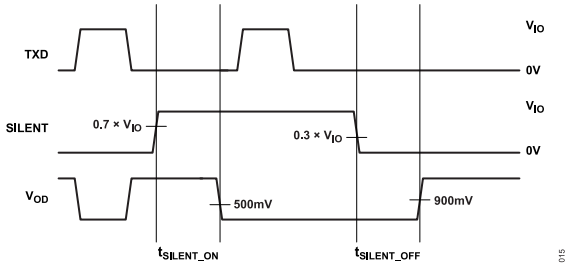

Figure 3. Silent Mode Timing Diagram

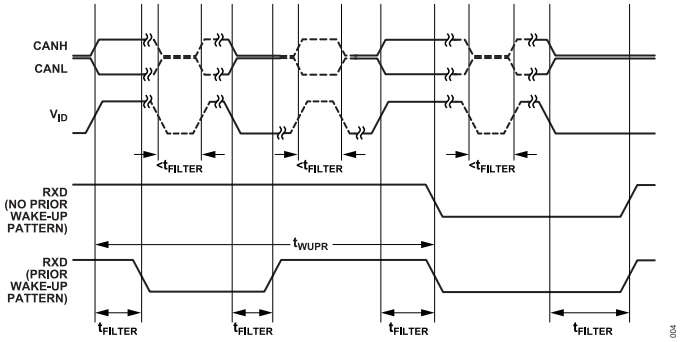

Figure 4. Wake-Up Pattern Detection and Filtered RXD in Standby Mode Timing Diagram

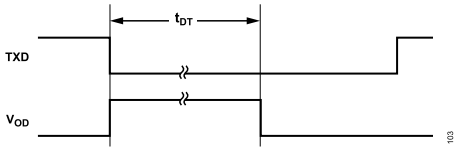

Figure 5. Dominant Timeout

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INSULATION SPECIFICATIONS

The ADM3055E/ADM3057E are suitable for "safe electrical insulation" only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADM3055E 20-Lead Increased Creepage SOIC [SOIC_IC] (RI-20-1) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	8.3	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	8.3	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	29.0	µm	Minimum internal
Comparative Tracking Index	CTI	>600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤ 300V rms
		I to III		Rated mains voltage ≤ 400V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Total Power Dissipation	P_{TOT}	2.55	W	$T_A \leq 25°C$, $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		20.4	mW/°C	$T_A > 25°C$, see Figure 6
Junction-to-Air Thermal Impedance	θ_{JA}	49	°C/W	See the Thermal Characteristics section
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	595	V peak	
Maximum Isolation Working Voltage	V_{IOWM}	420	V rms	AC voltage, end of life test, f = 60Hz
		595	V peak	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	8000	V peak	$V_{TEST} \geq 1.2 \times V_{IOTM}$, t = 1s (100% production)
Maximum Impulse Voltage	V_{IMP}	8000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	10400	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ minimum 10kV (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s
				Method b1 (100% production), $V_{ini} \geq 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s
Resistance (Input to Output)[1]	R_{IO}	$>10^{13}$	Ω	T_A = 25°C, V_{TEST} = 500V DC, t = 60s
	R_{IO_S}	$>10^{9}$	Ω	$T_A = T_S$, V_{TEST} = 500V DC, t = 60s
Capacitance (Input to Output)[1]	C_{IO}	3.7	pF	f_{TEST} = 1MHz
Climatic Category		40/105/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	5000	V rms	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)

[1] Device measured as a 2-terminal device with Pin 1 to Pin 10 connected and Pin 11 to Pin 20 connected.

SPECIFICATIONS

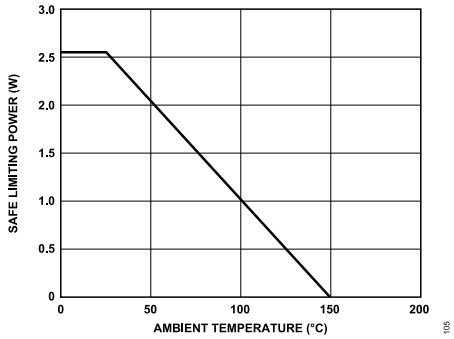

Figure 6. ADM3055E Thermal Derating Curve for 20-Lead Increased Creepage SOIC [SOIC_IC] (RI-20-1) Package, Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

Table 4. ADM3057E 20-Lead Wide SOIC [SOIC_W] (RW-20) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	7.8	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	7.8	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	29.0	µm	Minimum internal
Comparative Tracking Index	CTI	>600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤ 300V rms
		I to III		Rated mains voltage ≤ 400V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Total Power Dissipation	P_{TOT}	2.35	W	$T_A \leq 25°C$, $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		18.8	mW/°C	$T_A > 25°C$, see Figure 7
Junction-to-Air Thermal Impedance	θ_{JA}	53	°C/W	See the Thermal Characteristics section
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	595	V peak	
Maximum Isolation Working Voltage	V_{IOWM}	420	V rms	AC voltage, end of life test, f = 60Hz
		595	V peak	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	6000	V peak	$V_{TEST} \geq 1.2 \times V_{IOTM}$, t = 1s (100% production)
Maximum Impulse Voltage	V_{IMP}	6000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	10000	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ minimum 10kV (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s Method b1 (100% production), $V_{ini} \geq 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s
Resistance (Input to Output)[1]	R_{IO}	$>10^{13}$	Ω	T_A = 25°C, V_{TEST} = 500V DC, t = 60s
	R_{IO_S}	$>10^{9}$	Ω	$T_A = T_S$, V_{TEST} = 500V DC, t = 60s
Capacitance (Input to Output)[1]	C_{IO}	3.7	pF	f_{TEST} = 1MHz
Climatic Category		40/105/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	3750	V rms	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)

SPECIFICATIONS

[1] Device measured as a 2-terminal device with Pin 1 to Pin 10 connected and Pin 11 to Pin 20 connected.

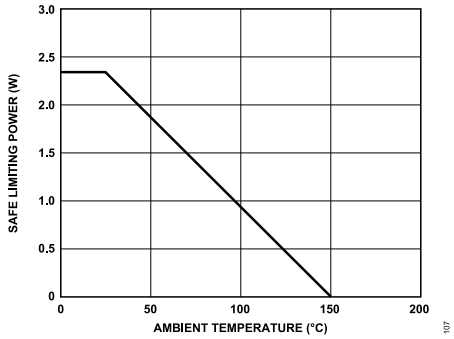

Figure 7. ADM3057E Thermal Derating Curve for 20-Lead Wide SOIC [SOIC_W] (RW-20) Package, Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

SPECIFICATIONS

REGULATORY INFORMATION

The ADM3055E has been approved by the organizations listed in Table 5. The ADM3057E has been approved by the organizations listed in Table 6. Copies of the relevant certificates are available at Safety and Regulatory Certifications for Digital Isolation.

Table 5. ADM3055E 20-Lead Increased Creepage SOIC [SOIC_IC] (RI-20-1) Package Certifications

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
UL	UL 1577 Single protection, 5000V rms isolation voltage	File E214100
CSA[1]	CSA/EN/IEC 62368-1 Basic insulation at 830V rms Reinforced insulation at 415V rms CSA/IEC 60601-1 2 MOPP at 261V rms CSA/IEC 61010-1 Basic insulation at 600V rms[2] Reinforced insulation at 300V rms	File 205078
TÜV SÜD[3]	EN/IEC 62368-1 Basic insulation at 830V rms Reinforced insulation at 415V rms	Certificate B 056232 0021
VDE	DIN EN IEC 60747-17 (VDE 0884-17) Reinforced insulation at 595V peak	Certificate 40011599
CQC	GB 4943.1 Basic insulation at 830V rms Reinforced insulation at 415V rms	Certificate CQC19001229561

1 Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM3055E/ADM3057E case material has been evaluated by CSA as Material Group I.

2 Overvoltage Category IV

3 Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM3055E/ADM3057E case material has been evaluated by TÜV SÜD as Material Group I.

Table 6. ADM3057E 20-Lead Wide SOIC [SOIC_W] (RW-20) Package Certifications

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
UL	UL 1577 Single protection, 3750V rms isolation voltage	File E214100
CSA[1]	CSA/EN/IEC 62368-1 Basic insulation at 780V rms Reinforced insulation at 390V rms CSA/IEC 60601-1 2 MOPP at 237.5V rms CSA/IEC 61010-1 Basic insulation at 600V rms Reinforced insulation at 300V rms	File 205078
TÜV SÜD[2]	EN/IEC 62368-1 Basic insulation at 780V rms Reinforced insulation at 390V rms	Certificate B 056232 0021
VDE	DIN EN IEC 60747-17 (VDE 0884-17) Reinforced insulation at 595V peak	Certificate 40011599
CQC	GB 4943.1 Basic insulation at 780V rms	Certificate CQC19001229560

SPECIFICATIONS

Table 6. ADM3057E 20-Lead Wide SOIC [SOIC_W] (RW-20) Package Certifications (Continued)

Regulatory Agency	Safety Standard/Rating	File or Certificate Number
	Reinforced insulation at 390V rms	

[1] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM3055E/ADM3057E case material has been evaluated by CSA as Material Group I.

[2] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM3055E/ADM3057E case material has been evaluated by TÜV SÜD as Material Group I.

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to GND_x are on the same side, unless otherwise noted.

Table 7.

Parameter	Rating
V_{CC}	−0.5V to +6V
V_{IO}	−0.5V to +6V
Logic Side Input/Output: TXD, RXD, AUX_{IN}, SILENT, STBY	−0.5V to V_{IO} + 0.5V
CANH, CANL	−40V to +40V
AUX_{OUT}, RS	−0.5V to V_{ISOIN} + 0.5V
Ambient Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Moisture Sensitivity Level (MSL)	3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Thermal resistance and characterization parameter values specified in Table 8 are defined and calculated based on the JEDEC JESD51 standards. For more details on their definition and usage, see JEDEC JESD51-12 and the Thermal Analysis section.

Table 8. Package Thermal Data

Package Type[1]	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
RI-20-1	49	30.9	24.0	9.8	°C/W
RW-20	53	47.9	30.8	10.0	°C/W

1 Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias and still air.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

Table 9. ADM3055E/ADM3057E ESD Ratings

ESD Model	Withstand Threshold (kV)	Class
HBM[1]	±4	3A
IEC[2]	±8 (contact discharge) to GND_2	Level 4
	±15 (air discharge) to GND_2	Level 4
	±8 (contact, across isolation barrier) to GND_1	Level 4

1 All pins, 1.5kΩ, 100pF.

2 The CANH and CANL pins only.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

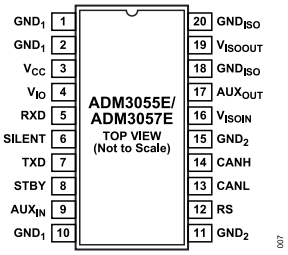

Figure 8. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 10	GND_1	Ground, Logic Side.
3	V_{CC}	*iso*Power Power Supply, 4.5V to 5.5V. This pin requires 0.1µF and 10µF decoupling capacitors.
4	V_{IO}	*i*Coupler Power Supply, 1.7V to 5.5V. This pin requires 0.01µF and 0.1µF decoupling capacitors.
5	RXD	Receiver Output Data.
6	SILENT	Silent Mode Select with Input High. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
7	TXD	Driver Input Data. This pin has a weak internal pull-up resistor to V_{IO}.
8	STBY	Standby Mode Select with Input High. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
9	AUX_{IN}	Auxiliary Channel Input. This pin sets the AUX_{OUT} output.
11, 15	GND_2	Ground, Bus Side.
12	RS	Slope Control Pin. Short this pin to ground for full speed operation or use a weak pull-down resistor (for example, 47kΩ) for slope control mode. An input high signal places the CAN transceiver in standby mode.
13	CANL	CAN Low Input/Output.
14	CANH	CAN High Input/Output.
16	V_{ISOIN}	Isolated Power Supply Input for the CAN Transceiver Bus Side Digital Isolator. This pin requires 0.01µF and 0.1µF decoupling capacitors.
17	AUX_{OUT}	Isolated Auxiliary Channel Output. The state of AUX_{OUT} is latched when STBY is high. By default, AUX_{OUT} is low at startup or when V_{IO} is unpowered.
18, 20	GND_{ISO}	Ground for the Isolated DC-to-DC Converter. Connect these pins together through one ferrite bead to PCB ground (bus side).
19	V_{ISOOUT}	Isolated Power Supply Output. This pin requires 0.22µF and 10µF capacitors to GND_{ISO}. Connect this pin through a ferrite bead and short the PCB trace to V_{ISOIN} for operation.

OPERATIONAL TRUTH TABLE

Table 11. Truth Table

Power		Inputs[1, 2]						Outputs[2]		Input/Output
V_{CC}	V_{IO}	TXD	SILENT	STBY	AUX_{IN}	RS	Mode	RXD[3]	AUX_{OUT}	CANH/CANL
On	On	Low	Low	Low	Low	Low/pull-down	Normal/slope mode	Low	Low	Dominant[4]
On	On	Low	Low	Low	High	Low/pull-down	Normal/slope mode	Low	High	Dominant[4]
On	On	High	Low	Low	Low	Low/pull-down	Normal/slope mode	High/per bus	Low	Recessive/set by bus
On	On	High	Low	Low	High	Low/pull-down	Normal/slope mode	High/per bus	High	Recessive/set by bus
On	On	X	High	Low	Low	X	Listen only	High/per bus	Low	Recessive/set by bus
On	On	X	High	Low	High	X	Listen only	High/per bus	High	Recessive/set by bus
On	On	X	X	High	X	X	Standby	High/WUP/filtered	Last state	Bias to GND_2/set by bus
On	On	X	X	X	Low	Pull-up	Standby[5]	High/WUP/filtered	Low	Bias to GND_2/set by bus
On	On	X	X	X	High	Pull-up	Standby[5]	High/WUP/filtered	High	Bias to GND_2/set by bus
On	Off	Z	Z	Z	Z	Low/pull-down	Normal/slope mode	Z	Low	Recessive/set by bus

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Truth Table (Continued)

Power		Inputs[1, 2]					Mode	Outputs[2]		Input/Output
V_{CC}	V_{IO}	TXD	SILENT	STBY	AUX_{IN}	RS		RXD[3]	AUX_{OUT}	CANH/CANL
Off	On	X	X	X	X	X	Transceiver off	High	Z	High impedance/set by bus
Off	Off	Z	Z	Z	Z	Z	Transceiver off	Z	Z	High impedance/set by bus

1 X means irrelevant.

2 Z means high impedance within one diode drop of ground.

3 WUP means remote wake-up pattern.

4 Limited by t_{DT}.

5 RS can only set the transceiver to standby mode. RS does not control the digital isolator.

TYPICAL PERFORMANCE CHARACTERISTICS

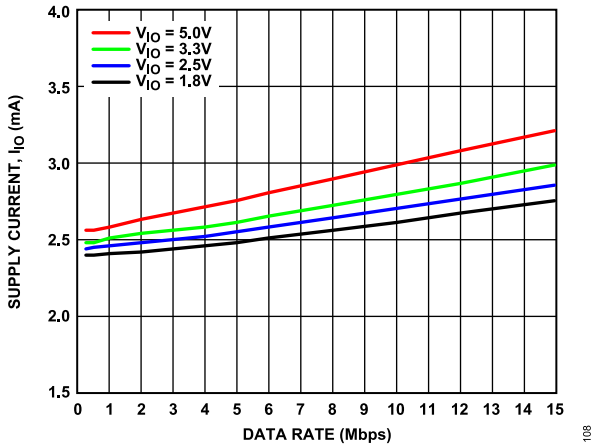

Figure 9. Supply Current, I_{IO} vs. Data Rate

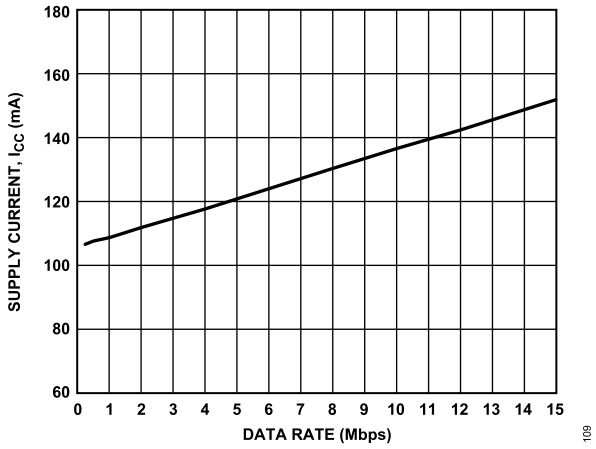

Figure 10. Supply Current, I_{CC} vs. Data Rate

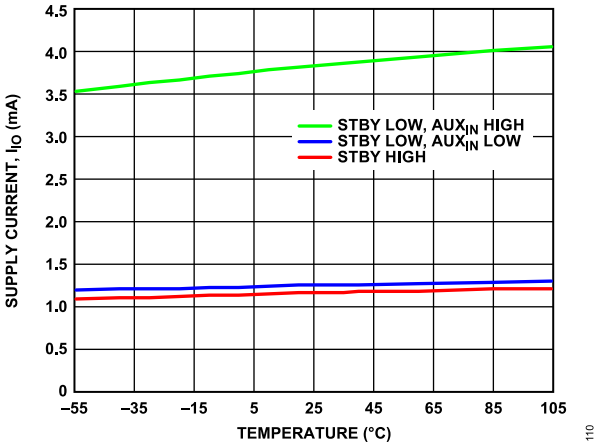

Figure 11. Supply Current, I_{IO} vs. Temperature (Inputs Idle)

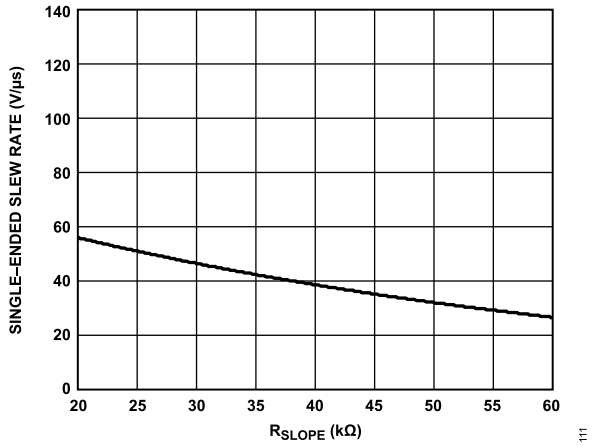

Figure 12. Single-Ended Slew Rate vs. R_{SLOPE}

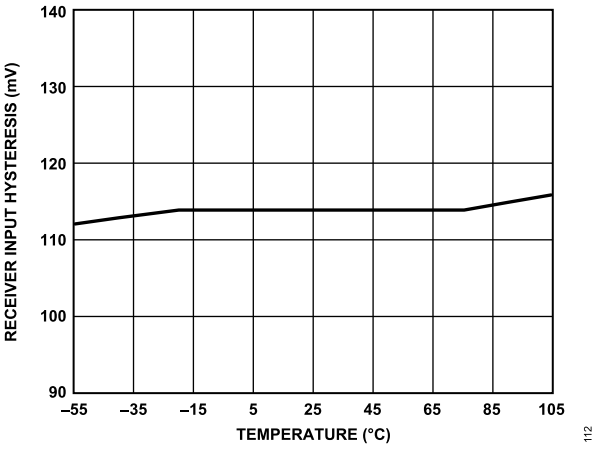

Figure 13. Receiver Input Hysteresis vs. Temperature

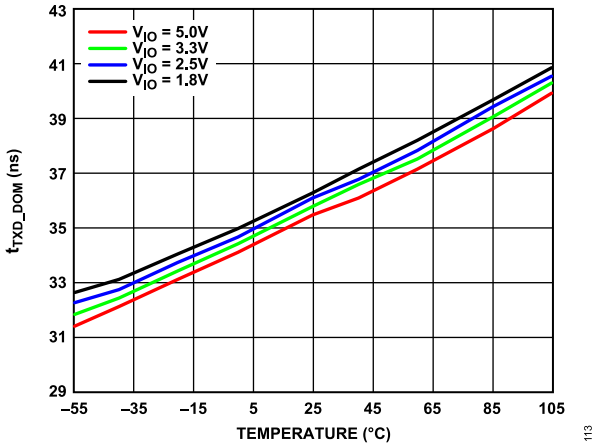

Figure 14. t_{TXD_DOM} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

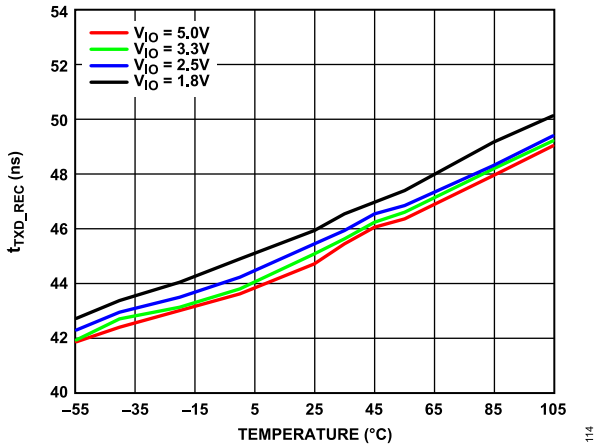

Figure 15. t_{TXD_REC} vs. Temperature

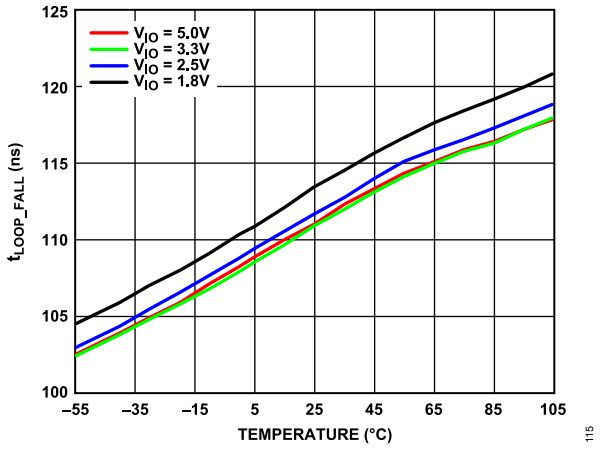

Figure 16. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 0Ω)

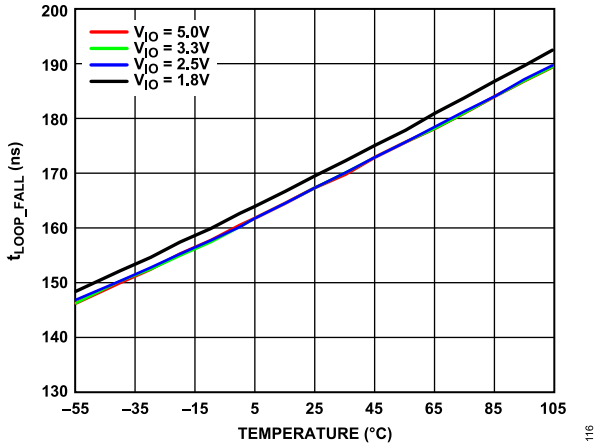

Figure 17. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 47kΩ)

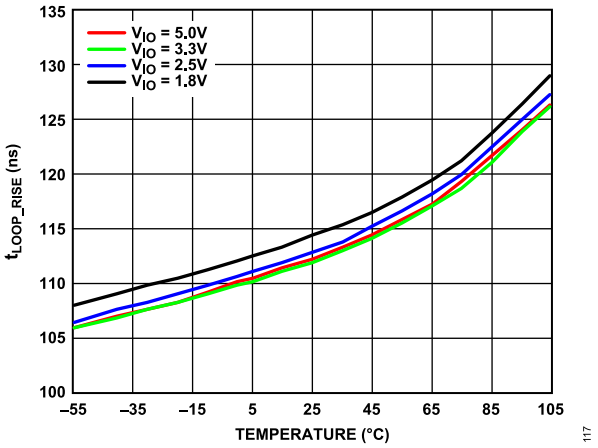

Figure 18. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 0Ω)

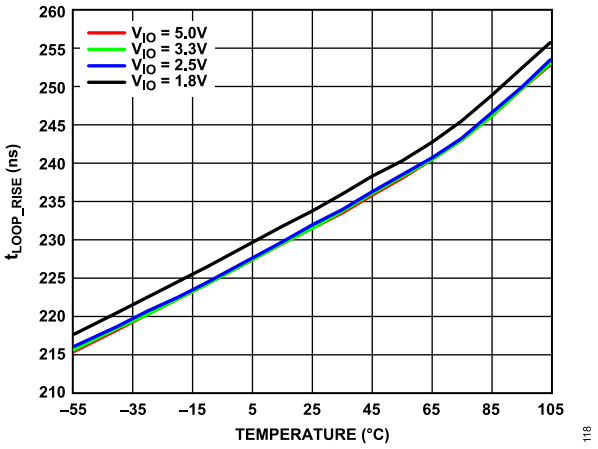

Figure 19. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 47kΩ)

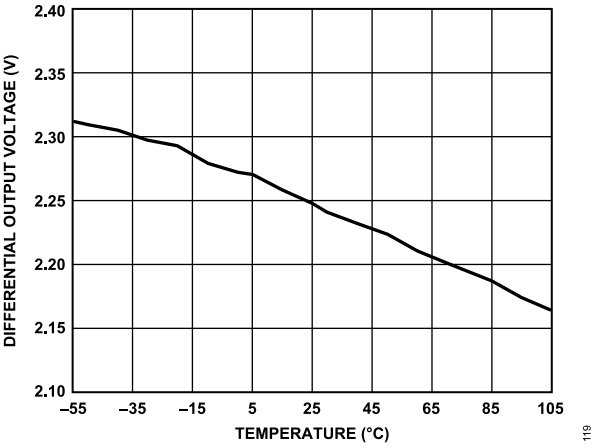

Figure 20. Differential Output Voltage (V_{OD}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

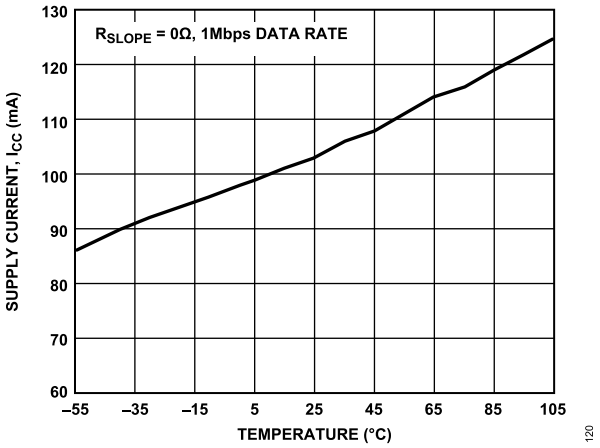

Figure 21. Supply Current, I_{CC} vs. Temperature

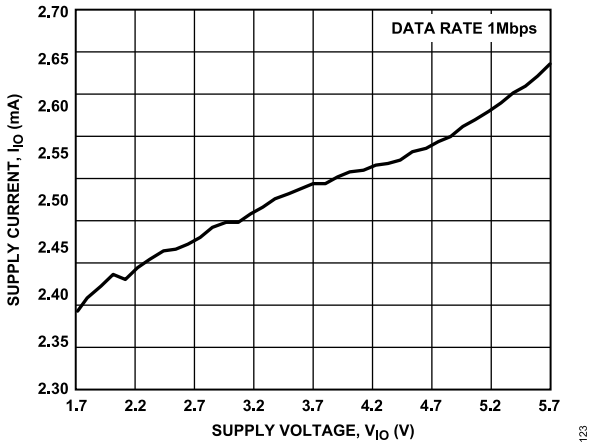

Figure 24. Supply Current, I_{IO} vs. Supply Voltage, V_{IO}, Data Rate = 1Mbps

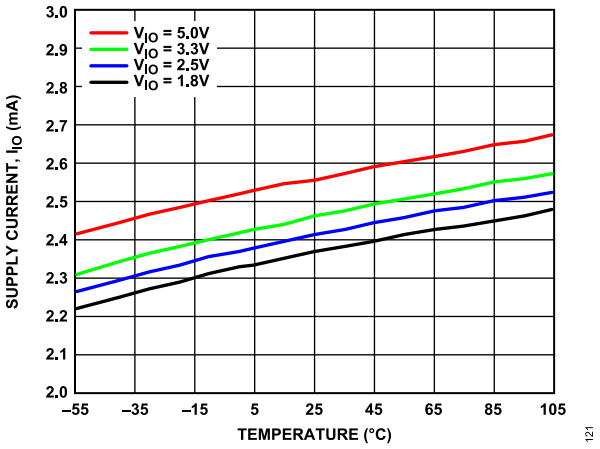

Figure 22. Supply Current, I_{IO} vs. Temperature, RS = 0Ω, 1Mbps

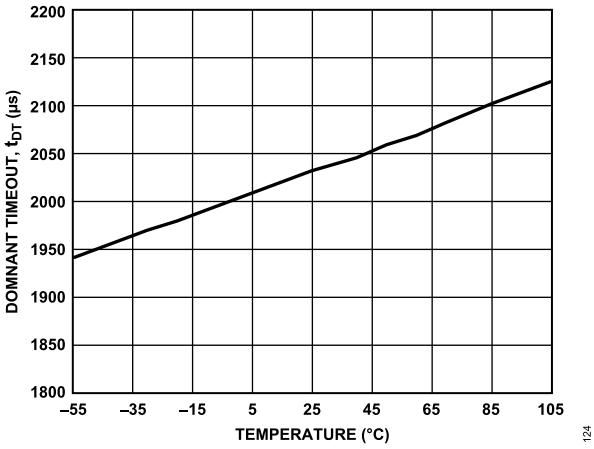

Figure 25. Dominant Timeout, t_{DT} vs. Temperature

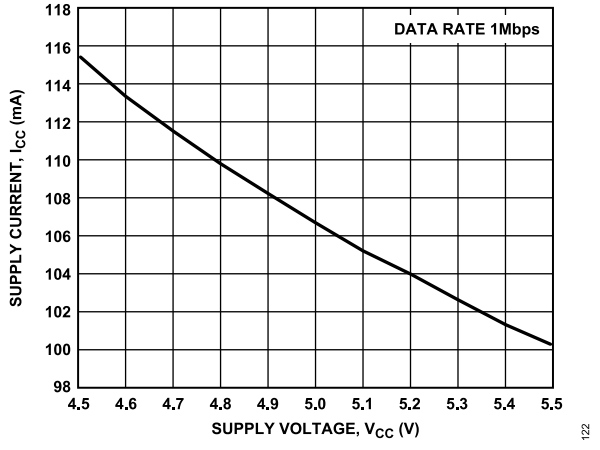

Figure 23. Supply Current, I_{CC} vs. Supply Voltage, V_{CC}, RS = 0Ω, 1Mbps

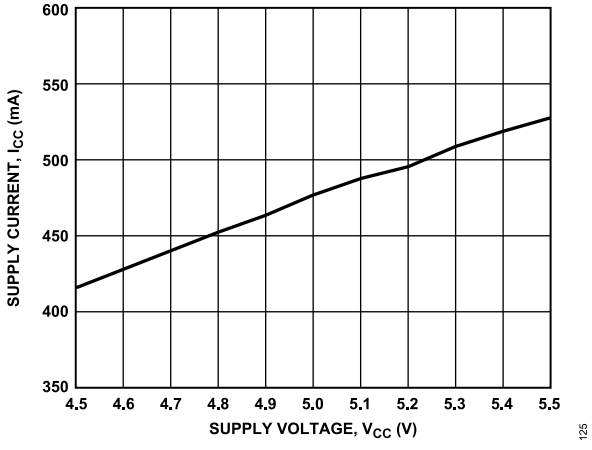

Figure 26. Supply Current, I_{CC} vs. Supply Voltage, V_{CC} (V_{ISOOUT} Shorted to GND_{ISO})

TYPICAL PERFORMANCE CHARACTERISTICS

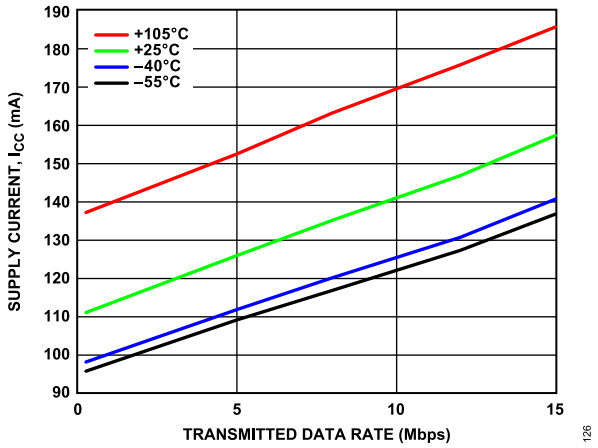

Figure 27. Supply Current, I_{CC} vs. Transmitted Data Rate

TEST CIRCUITS

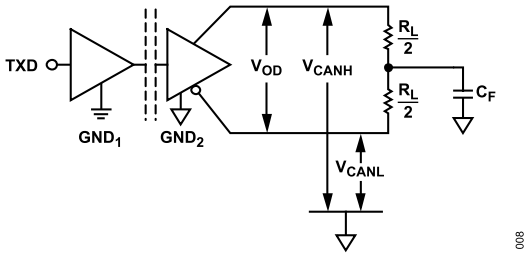

Figure 28. Driver Voltage Measurement

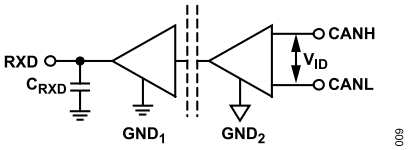

Figure 29. Receiver Voltage Measurement

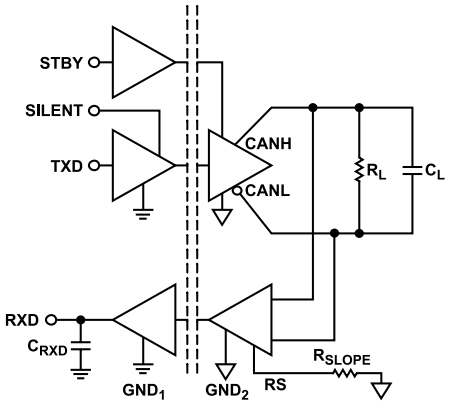

Figure 30. Switching Characteristics Measurements

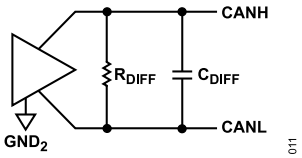

Figure 31. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

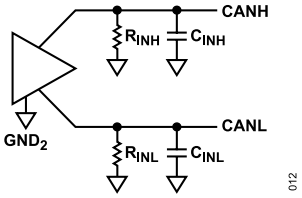

Figure 32. R_{IN} and C_{IN} Measured in Recessive State, Bus Disconnected

TERMINOLOGY

I_{CC}

I_{CC} is the current drawn by the V_{CC} pin. This pin powers the *iso*Power dc-to-dc converter.

I_{IO}

I_{IO} is the current drawn by the V_{IO} pin. This pin powers the *i*Coupler digital isolator.

I_{SC}

I_{SC} is the current drawn by the V_{ISOIN} pin under the specified fault condition.

V_{OD}

The V_{OD} is the difference of the CANH and CANL levels, which is V_{DIFF} in ISO 11898-2:2016.

f_{OSC}

f_{OSC} is the carrier frequency of the *iso*Power dc-to-dc converter that provides isolated power to the bus side.

t_{TXD_DOM}

t_{TXD_DOM} is the propagation delay from a low signal on TXD to transition the bus to a dominant state.

t_{TXD_REC}

t_{TXD_REC} is the propagation delay from a high signal on TXD to transition the bus to a recessive state.

t_{LOOP_FALL}

t_{LOOP_FALL} is the propagation delay of a low signal on the TXD pin to the bus dominant and transitions low on the RXD pin.

t_{LOOP_RISE}

t_{LOOP_RISE} is the propagation delay of a high signal on the TXD pin to the bus recessive and transitions high on the RXD pin.

t_{BIT_TXD}

t_{BIT_TXD} is the bit time on the TXD pin as transmitted by the CAN controller. See Figure 2 for level definitions.

t_{BIT_BUS}

t_{BIT_BUS} is the bit time transmitted by the transceiver to the bus. When compared with a given t_{BIT_TXD}, a measure of bit symmetry from the TXD digital isolation channel and CAN transceiver can be determined. See Figure 2 for level definitions.

t_{BIT_RXD}

t_{BIT_RXD} is the bit time on the RXD output pin that can be compared with t_{BIT_TXD} for a round trip measure of pulse width distortion through the TXD digital isolation channel, the CAN transceiver, and back through the RXD isolation channel.

Wake-Up Pattern (WUP)

WUP is a remote transmitted pattern required to trigger low speed data transmission by the CAN transceiver while in standby mode. The pattern does not force the transceiver out of standby mode.

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

The ADM3055E/ADM3057E facilitate communication between a CAN controller and the CAN bus. The CAN controller and the ADM3055E/ADM3057E communicate with standard 1.8V, 2.5V, 3.3V, or 5.0V CMOS levels. The internal transceiver translates the CMOS levels to and from the CAN bus.

The CAN bus has two states: dominant and recessive. The recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5V. In the recessive state, the CANH and CANL pins are set to high impedance and are loosely biased to a single-ended voltage of 2.5V. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 1.5V. The transceiver transmits a dominant state by driving the single-ended voltage of the CANH pin to 3.5V and the CANL pin to 1.5V. The recessive and dominant states correspond to CMOS high and CMOS low, respectively, on the RXD pin and TXD pin.

A dominant state from another node overwrites a recessive state on the bus. A CAN frame can be set for higher priority by using a longer string of dominant bits to gain control of the CAN bus during the arbitration phase. While transmitting, a CAN transceiver also reads back the state of the bus. When a CAN controller receives a dominant state while transmitting a recessive state during arbitration, the CAN controller surrenders the bus to the node still transmitting the dominant state. The node that gains control during the arbitration phase reads back only its own transmission. This interaction between recessive and dominant states allows competing nodes to negotiate for control of the bus while avoiding contention between nodes.

Industrial applications can have long cable runs. These long runs may have differences in local earth potential. Different sources may also power nodes. The ADM3055E transceiver has a ±25V common-mode range (CMR) that exceeds the ISO 11898-2:2016 requirement and further increases the tolerance to ground variation.

See the AN-1123 Application Note for additional information on CAN.

SIGNAL AND POWER ISOLATION

The ADM3055E and the ADM3057E provide galvanic signal isolation implemented on the logic side of the interface. The RXD and TXD isolation channels transmit and receive with an on/off keying (OOK) architecture on the *i*Coupler digital isolation technology.

The ADM3055E and the ADM3057E feature independent power supply pins for isolated power (the V_{CC} pin) and isolated signal (the V_{IO} pin). The V_{CC} pin requires a nominal 5V supply to produce the 5V isolated power. The V_{IO} pin may be supplied with a nominal 1.8V to a nominal 5V. The logic input and output levels scale to the voltage supplied to the V_{IO} pin. The isolated power from the V_{ISOOUT} pin must be supplied to the V_{ISOIN} pin to power the bus side digital isolator and transceiver.

STANDBY MODE

The STBY pin engages a reduced power standby mode that modifies the operation of both the CAN transceiver and digital isolation channels. Standby mode disables the TXD signal isolation channel and sets the transmitter output to a high impedance state loosely biased to GND_2. While in standby mode, the receiver filters bus data and responds only after the remote wake-up sequence is received.

When entering or exiting standby mode, the TXD input must be kept high and the RXD output must be ignored for the full t_{STBY_ON} and t_{STBY_OFF} times. STBY does not control or modify behavior of the *iso*Power integrated dc-to-dc converter. The dc-to-dc converter continues to operate and provide the power to the bus side.

REMOTE WAKE UP

The ADM3055E and the ADM3057E respond to the remote wake-up sequence as defined in ISO 11898-2:2016. When CAN channels are presented with the defined slow speed high low high sequence within the low wake-up pattern detection reset time (t_{WUPR}), low speed data transmission is allowed.

Successful receipt of the remote wake-up pattern does not bring the ADM3055E and the ADM3057E out of standby mode. The ADM3055E STBY pin must be brought low externally to exit standby mode. After the ADM3055E or ADM3057E device receives the remote wake-up pattern, the transceiver continues to receive low speed data until standby mode is exited.

SILENT MODE

Asserting the SILENT pin disables the TXD digital isolation channel. Any inputs to the TXD pin are ignored in this mode, and the transceiver presents a recessive bus state. The operation of the RXD channel is unaffected. The RXD channel continues to output data received from the internal CAN transceiver monitoring the bus.

Silent mode is useful when paired with a CAN controller using automatic baud rate detection. A CAN controller must be set to the same data rate as all attached nodes. The CAN controller produces an error frame and ties up the bus with a dominant state when the received data rate is different from expected. Other CAN nodes then echo this error frame. While in silent mode, the error frames produced by the CAN controller are kept from interrupting bus traffic, and the controller can continue listening to bus traffic to tune.

RS PIN

The RS pin sets the transceiver in one of three different modes of operation: high speed, slope control, or standby. This pin cannot be left floating.

For high speed mode, connect the RS pin directly to GND_2. Ensure that the transition time of the CAN bus signals are as short as possible to allow higher speed signaling. A shielded cable is recom-

THEORY OF OPERATION

mended to avoid electromagnetic interference (EMI) problems in high speed mode.

Slope control mode allows the use of unshielded twisted pair wires or parallel pair wires as bus lines. Slow the signal rise and fall transition times to reduce EMI and ringing in slope control mode. Adjust the rise and fall slopes by adding a resistor (R_{SLOPE}) connected from RS to GND_2. The slope is proportional to the current output at the RS pin.

The RS pin can also set the CAN transceiver to standby mode, which occurs when the pin is driven to a voltage above V_{STB}. In standby mode, high speed data is filtered, and the CANH and CANL lines are biased to GND_2.

The RS pin can only set the CAN transceiver to standby mode. The state of the RS pin does not modify the operation of digital isolation channels or the auxiliary channel.

AUXILIARY CHANNEL

The auxiliary channel is available for low speed data transmission at up to 20kHz (or 40kbps nonreturn-to-zero format) when STBY is not asserted. The data rate limit of the channel allows the data channel to be shared by the STBY signal.

In standby mode, or when STBY is driven high, the operation of the channel is modified to share the multiplexed signal path with the STBY signal (see Figure 1). The AUX_{OUT} pin remains latched in the state when STBY is asserted. Periodic pulses (<25µs wide) are sent to indicate that the logic side is powered and remains in standby mode.

In applications where AUX_{OUT} may be shorted to GND_2 or V_{DD2}, add a series resistance to the output channel.

An example of using this auxiliary channel to control a switchable termination from the logic side is demonstrated on the EVAL-ADM3055EEBZ evaluation board.

INTEGRATED AND CERTIFIED IEC EMC SOLUTION

Typically, designers must add protections against harsh operating environments while also making the product as small as possible. To reduce board space and the design effort needed to meet system level ESD standards, the ADM3055E and the ADM3057E include robust protection circuitry on chip for the CANH and CANL lines.

FAULT PROTECTION

Miswire events commonly occur when the system power supply is connected directly to the CANH and CANL bus lines during assembly. The ADM3055E and the ADM3057E CAN bus pins are protected against such high voltage miswire events. The ADM3055E and the ADM3057E CANH and CANL signal lines can withstand continuous ±40V with respect to GND_2 or +40V between the CAN bus lines without damage. This level of protection applies when the device is either powered or unpowered.

The ADM3055E provides IEC 61000-4-2 Level 4 ESD protection, but some applications may require further system level protection. The symmetrical nature of the ADM3055E ±40V bus fault protection and the ±25V CMR makes the selection of bidirectional transient voltage suppressor (TVS) diodes easier.

FAIL-SAFE FEATURES

In cases where the TXD input pin is allowed to float, to prevent bus traffic interruption, the TXD input channel has an internal pull-up to the V_{IO} pin. The pull-up holds the transceiver in the recessive state.

The ADM3055E and the ADM3057E feature a dominant timeout (t_{DT} in Table 2). A TXD line shorted to ground or malfunctioning CAN controller are examples of how a single node can indefinitely prevent further bus traffic. The dominant timeout limits how long the dominant state can transmit to the CAN bus by the transceiver. When the TXD pin is presented with a logic high, normal TXD functionality is restored.

The t_{DT} minimum also inherently creates a minimum data rate. Under normal operation, the CAN protocol allows five consecutive bits of the same polarity before stuffing a bit of the opposite polarity into the transmitting bit sequence. When an error is detected, the CAN controller purposely violates the bit stuffing rules by producing six consecutive dominant bits. At any given data rate, the CAN controller must transmit as many as 11 consecutive dominant bits to effectively limit the ADM3055E and the ADM3057E minimum data rate to 9600bps.

THERMAL SHUTDOWN

The ADM3055E and the ADM3057E contain thermal shutdown circuitry that protects the devices from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The circuitry disables the driver outputs when the die temperature reaches 175°C. When the die has cooled, the drivers are enabled again.

APPLICATIONS INFORMATION

PCB LAYOUT

Power supply bypassing is required at the logic input supply, V_{IO}, and at the shared CAN transceiver and digital isolator input supply pin, V_{ISOIN}. Low equivalent series resistance (ESR) bypass capacitors are required and must be placed as close to the chip pads as possible. The ADM3055E and the ADM3057E signal and power isolated CAN transceivers do not require external interface circuitry for the logic interfaces.

The integrated dc-to-dc converter supply input pin, V_{CC}, requires parallel 10µF and 0.1µF bypass capacitors placed close to the pin. Noise suppression requires a low inductance, high frequency capacitor. Ripple suppression and proper regulation require a large value capacitor. Effective bypass capacitance is also required on the isolated output supply pin, V_{ISOOUT}, for proper operation of the integrated dc-to-dc converter. Note that the total trace length between the ends of the low ESR capacitors and the input power supply pins, V_{CC}, V_{IO}, V_{ISOIN}, and V_{ISOOUT}, must not exceed 2mm.

RADIATED EMISSIONS AND PCB LAYOUT

The ADM3055E and the ADM3057E signal and power isolated CAN FD transceivers pass EN 55022 Class B by 6dB on a 2-layer PCB design with ferrite beads. Neither PCB stitching capacitance nor high voltage surface-mounted technology (SMT) safety capacitors are required to meet this emissions level.

The ADM3055E and the ADM3057E have an internal split pad lead frame on the bus side to isolate noise generated by the dc-to-dc converter from the transceiver. For best noise suppression, filter both the V_{ISOOUT} power supply pin and GND_{ISO} power supply return pin for high frequency currents before routing power to the transceiver. Use surface-mount ferrite beads in series with the signals, as shown in Figure 33.

The *iso*Power integrated dc-to-dc converters of the ADM3055E and the ADM3057E produce a 180MHz carrier frequency to transmit power through the chip scale transformer. The impedance of the ferrite bead must be approximately 2kΩ between the 100MHz and 1GHz frequency range to reduce the emissions of the 180MHz primary switching frequency and 360MHz secondary side rectifying frequency. See Table 12 for examples of appropriate surface-mount ferrite beads. Although the ferrite beads are beneficial for emissions performance, the ferrite beads are not required for functionality.

Table 12. Surface-Mount Ferrite Beads Example

Manufacturer	Part No.
Taiyo Yuden	BKH1005LM182-T
Murata Electronics	BLM15HD182SN1

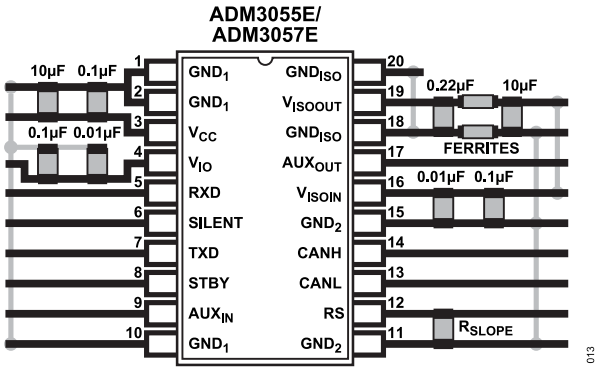

Figure 33. Recommended PCB Layout

THERMAL ANALYSIS

The ADM3055E and the ADM3057E consist of six internal die attached to a split lead frame with four die attach pads. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the thermal parameter values from Table 8. The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM3055E and the ADM3057E can operate at full load across the full temperature range without derating the output current.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the following equation:

$$T_J = \psi_{Jx} \times P_d + T_x \quad (1)$$

where

P_d is the dissipated power.

T_x is the measured temperature at location x and x is either B for the PCB or T for the package top.

The temperature measurement point for θ_{JB} and Ψ_{JB} is on the PCB between Pin 5 and Pin 6 on the outer edge of the pin footprint. The temperature measurement point for Ψ_{JT} is the center of the top side of the package.

APPLICATIONS INFORMATION

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3055E/ADM3057E according to IEC 60747-17.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, allowing the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and can therefore provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group.

The material group and creepage information for the ADM3055E are listed in Table 3 and for the ADM3057E they are listed in Table 4.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RI-20-1	SOIC_IC	20-Lead Standard Small Outline Package with Increased Creepage
RW-20	SOIC_W	20-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADM3055EBRIZ	−40°C to +105°C	20-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]	RI-20-1
ADM3055EBRIZ-RL	−40°C to +105°C	20-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC]	RI-20-1
ADM3057EBRWZ	−40°C to +105°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADM3057EBRWZ-RL	−40°C to +105°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20

[1] Z = RoHS Compliant Part.

[2] Use the EVAL-ADM3055EEBZ evaluation board to evaluate the ADM3057E.

EVALUATION BOARDS

Model[1]	Package Description
EVAL-ADM3055EEBZ	ADM3055E Evaluation Board

[1] Z = RoHS Compliant Part.