

FEATURES

- ▶ High gain: 25.5dB typical from 0.01GHz to 2GHz
- ▶ Low noise figure: <0.6dB typical from 0.5GHz to 2GHz
- ▶ Power-down voltage pin (VPD) for enabling and disabling the amplifier
- ▶ Single-supply bias
- ▶ Extended operating temperature range: -55°C to +125°C
- ▶ **RoHS-compliant, 2mm × 2mm, 8-lead LFCSP**

APPLICATIONS

- ▶ Telecommunications
- ▶ Military communications
- ▶ Radar
- ▶ Electronic warfare

GENERAL DESCRIPTION

The ADL8130 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), wideband low noise amplifier (LNA) that operates from 0.01GHz to 8GHz. The ADL8130 provides a typical gain of 25.5dB from 0.01GHz to 2GHz, a 0.6dB typical noise figure from 0.5GHz to 2GHz, and a typical output third-order intercept (OIP3) of 37dBm from 0.01GHz to 2GHz, requiring only a 90mA supply current (I_{DQ}) from a 5V supply voltage (V_{DD}). Power dissipation can be lowered at the expense of the OIP3 and output power (P_{OUT}). The internally matched, DC-coupled RF input (RFIN) and output (RFOUT) pins require external AC coupling capacitors along with a bias inductor on RFOUT. In addition, the RF input is biased through an external inductor connected between the VBIAS pin and RFIN pin.

The ADL8130 is housed in a RoHS-compliant, 2mm × 2mm, 8-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

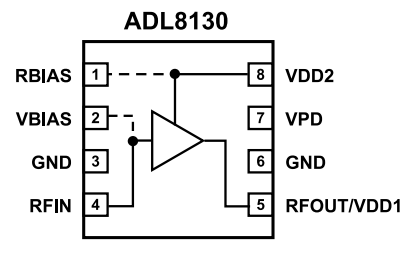


Figure 1. Functional Block Diagram

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TABLE OF CONTENTS

Features.....1

Applications.....1

Functional Block Diagram.....1

General Description.....1

Specifications.....3

 0.01GHz to 2GHz Frequency Range3

 2GHz to 5GHz Frequency Range3

 5GHz to 8GHz Frequency Range4

 DC Specifications.....4

Absolute Maximum Ratings.....5

 Thermal Resistance.....5

 Electrostatic Discharge (ESD) Ratings.....5

 ESD Caution.....5

Pin Configuration and Function Description.....6

 Interface Schematics.....7

Typical Performance Characteristics.....8

 Amplifier Off State ($V_{PD} = V_{DD}$).....27

Theory of Operation.....28

Applications Information.....29

 Recommended Bias Sequencing.....29

 Operation from 10kHz to 8GHz.....30

 Overdrive Recovery Optimization.....31

 Recommended Power Management Circuit.....32

Outline Dimensions.....33

 Ordering Guide.....33

REVISION HISTORY

9/2026—Revision 0: Initial Version

SPECIFICATIONS

0.01GHz to 2GHz Frequency Range

$V_{DD} = 5V$, $I_{DQ} = 90mA$, bias resistance (R_{BIAS}) = 835 Ω , and $T_{CASE} = 25^{\circ}C$, unless otherwise stated. V_{DD} refers to the VDD1 and VDD2 drain bias voltages.

Table 1. 0.01GHz to 2GHz Frequency Range

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
FREQUENCY RANGE			0.01		2	GHz
GAIN	S21		23.5	25.5		dB
Gain Variation Over Temperature				0.0258		dB/ $^{\circ}C$
NOISE FIGURE				0.7		dB
RETURN LOSS						
Input	S11			11		dB
Output	S22			10		dB
OUTPUT						
Output Power For 1dB Compression	OP1dB		19	21		dBm
Saturated Output Power	P_{SAT}			23		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 4dBm		37		dBm
Output Second-Order Intercept	OIP2	Measurement taken at P_{OUT} per tone = 4dBm		43		dBm
SUPPLY CURRENT	I_{DQ}			90		mA
SUPPLY VOLTAGE	V_{DD}			5		V
POWER ADDED EFFICIENCY	PAE	Measured at P_{SAT}		41		%

2GHz to 5GHz Frequency Range

$V_{DD} = 5V$, $I_{DQ} = 90mA$, $R_{BIAS} = 835\Omega$, and $T_{CASE} = 25^{\circ}C$, unless otherwise stated. V_{DD} refers to the VDD1 and VDD2 drain bias voltages.

Table 2. 2GHz to 5GHz Frequency Range

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
FREQUENCY RANGE			2		5	GHz
GAIN	S21		18	20.5		dB
Gain Variation Over Temperature				0.028		dB/ $^{\circ}C$
NOISE FIGURE				1		dB
RETURN LOSS						
Input	S11			10		dB
Output	S22			12		dB
OUTPUT						
Output Power For 1dB Compression	OP1dB		19	21		dBm
Saturated Output Power	P_{SAT}			22		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 4dBm		35		dBm

SPECIFICATIONS

Table 2. 2GHz to 5GHz Frequency Range (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Output Second-Order Intercept	OIP2	Measurement taken at P_{OUT} per tone = 4dBm		48		dBm
SUPPLY CURRENT	I_{DQ}			90		mA
SUPPLY VOLTAGE	V_{DD}			5		V
POWER ADDED EFFICIENCY	PAE	Measured at P_{SAT}		40		%

5GHz to 8GHz Frequency Range

$V_{DD} = 5V$, $I_{DQ} = 90mA$, $R_{BIAS} = 835\Omega$, and $T_{CASE} = 25^{\circ}C$, unless otherwise stated. V_{DD} refers to the VDD1 and VDD2 drain bias voltages.

Table 3. 5GHz to 8GHz Frequency Range

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
FREQUENCY RANGE			5		8	GHz
GAIN	S21		13.5	16		dB
Gain Variation Over Temperature				0.029		dB/ $^{\circ}C$
NOISE FIGURE				1.15		dB
RETURN LOSS						
Input	S11			15		dB
Output	S22			12		dB
OUTPUT						
Output Power For 1dB Compression	OP1dB		14.5	17		dBm
Saturated Output Power	P_{SAT}			20.5		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 4dBm		33		dBm
Output Second-Order Intercept	OIP2	Measurement taken at P_{OUT} per tone = 4dBm		46		dBm
SUPPLY CURRENT	I_{DQ}			90		mA
SUPPLY VOLTAGE	V_{DD}			5		V
POWER ADDED EFFICIENCY	PAE	Measured at P_{SAT}		27		%

DC Specifications

Table 4. DC Specifications

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
CURRENT						
Supply	I_{DQ}	Power-down voltage (V_{PD}) = 0V		90		mA
		$V_{PD} = V_{DD}$		10		mA
Amplifier	I_{DQ_AMP}			85.6		mA
RBIAS	I_{RBIAS}			4.4		mA
SUPPLY VOLTAGE	V_{DD}		3	5	6	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

PARAMETER	RATING
V_{DD}	7V
RF Input Power (RFIN)	30dBm
Continuous Power Dissipation (P_{DISS}), $T_{CASE} = 85^{\circ}\text{C}$ (Derate 19.2mW/ $^{\circ}\text{C}$ Above 85 $^{\circ}\text{C}$)	1.534W
Temperature	
Storage Range	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Operating Range	-55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
Quiescent Channel ($T_{CASE} = 85^{\circ}\text{C}$, $V_{DD} = 5\text{V}$, $I_{DQ} = 90\text{mA}$)	129.24 $^{\circ}\text{C}$
Maximum Channel	175 $^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance (channel to exposed metal ground pad on the underside of the device).

Table 6. Thermal Resistance

PACKAGE TYPE	θ_{JC}	UNIT
CP-8-30		
Quiescent, $T_{CASE} = 25^{\circ}\text{C}$	48.66	$^{\circ}\text{C}/\text{W}$
Worst Case ¹ , $T_{CASE} = 85^{\circ}\text{C}$	58.66	$^{\circ}\text{C}/\text{W}$

¹ Across all specified operating conditions.

Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8130

Table 7. ADL8130, 8-Lead LFCSP

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±250	1A

ESD Caution



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

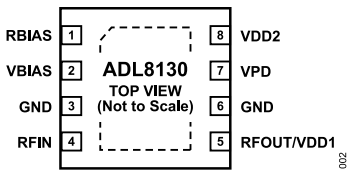


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

PIN NO.	MNEMONIC	DESCRIPTION
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD2 to set I_{DQ} . See the typical application circuit (see Figure 127) and the Applications Information section for more details. See Figure 3 for the interface schematic.
2	VBIAS	Bias Circuit Output Voltage. VBIAS sets the bias voltage for the RFIN pin. Connect VBIAS to RFIN using an inductor or ferrite bead as shown in Figure 127 . See Figure 4 for the interface schematic.
3, 6	GND	Grounds. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 5 for the interface schematic.
4	RFIN	RF Input. RFIN is DC-coupled and matched to 50Ω. See Figure 6 for the interface schematic.
5	RFOUT/VDD1	RF Output (RFOUT). The RFOUT pin is DC-coupled and matched to 50Ω. Drain Bias Voltage (VDD1). See Figure 7 for the interface schematic.
7	VPD	Power-Down Voltage. An active low digital signal enables the device, and an active high digital signal disables the device. See Figure 8 for the interface schematic.
8	VDD2	Drain Bias Voltage. Connect the VDD2 pin to the supply voltage. See Figure 9 for the interface schematic.
	EPAD	Ground Paddle. Connect the ground paddle to a ground plane which has a low electrical and thermal impedance.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Interface Schematics

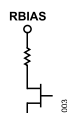


Figure 3. RBIAS Interface Schematic

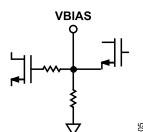


Figure 4. VBIAS Interface Schematic



Figure 5. GND Interface Schematic

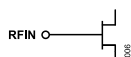


Figure 6. RFIN Interface Schematic

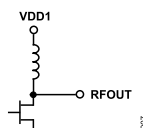


Figure 7. RFOUT/VDD1 Interface Schematic

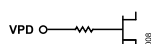


Figure 8. VPD Interface Schematic



Figure 9. VDD2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

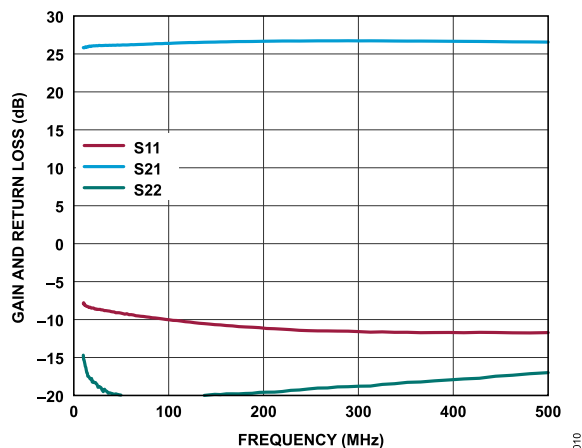


Figure 10. Gain and Return Loss vs. Frequency, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

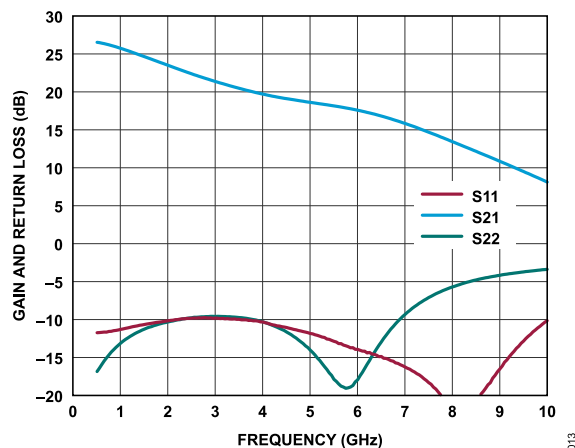


Figure 13. Gain and Return Loss vs. Frequency, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

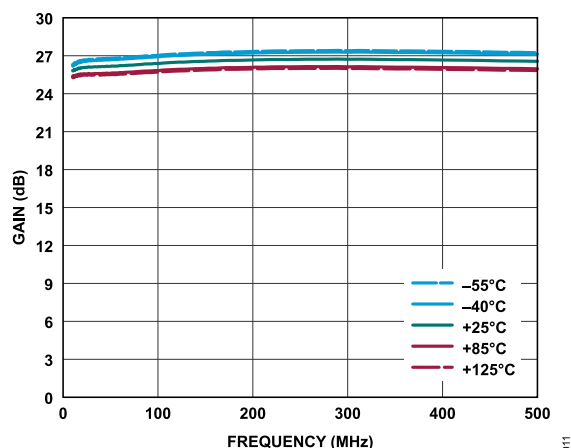


Figure 11. Gain vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

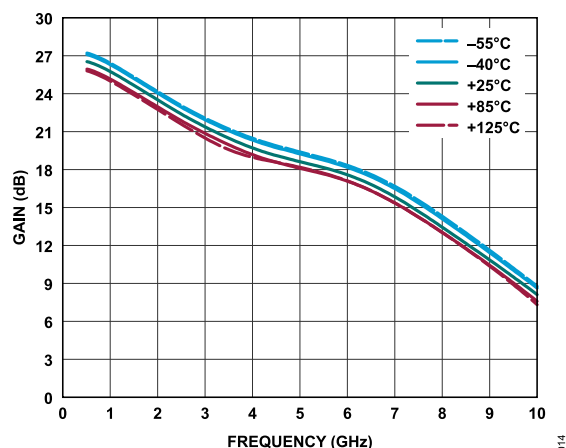


Figure 14. Gain vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

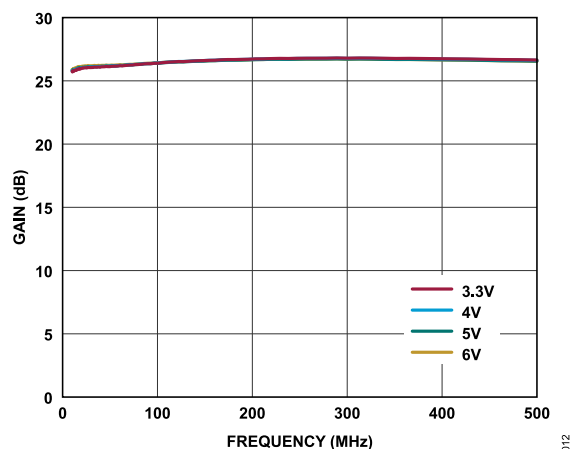


Figure 12. Gain vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90mA$

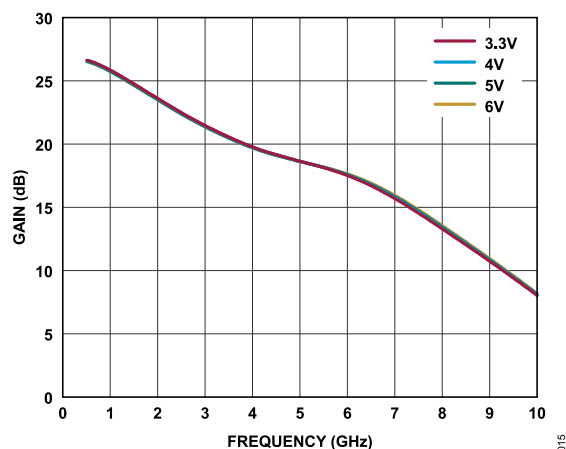


Figure 15. Gain vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90mA$

TYPICAL PERFORMANCE CHARACTERISTICS

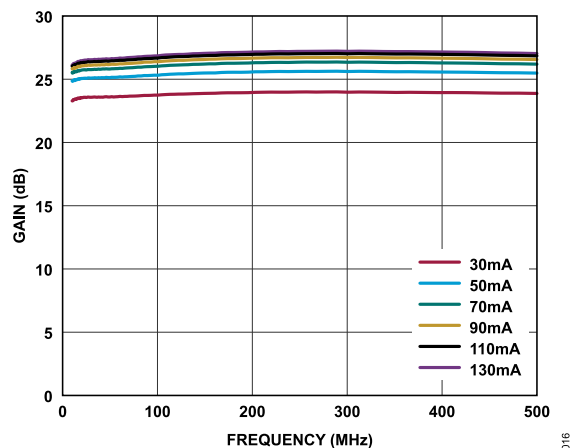


Figure 16. Gain vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5V$

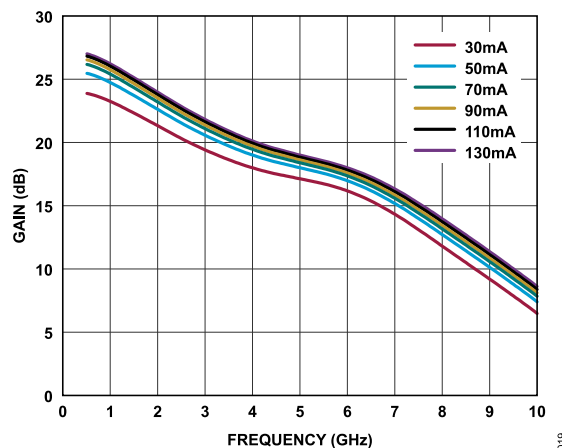


Figure 19. Gain vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5V$

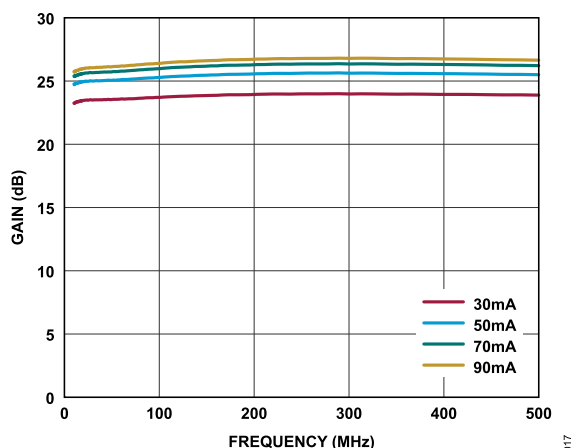


Figure 17. Gain vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3V$

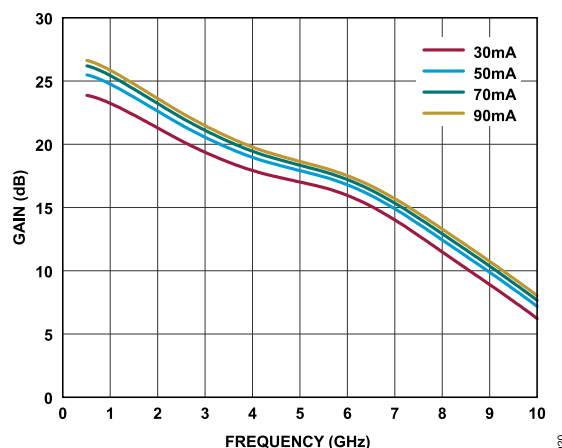


Figure 20. Gain vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3V$

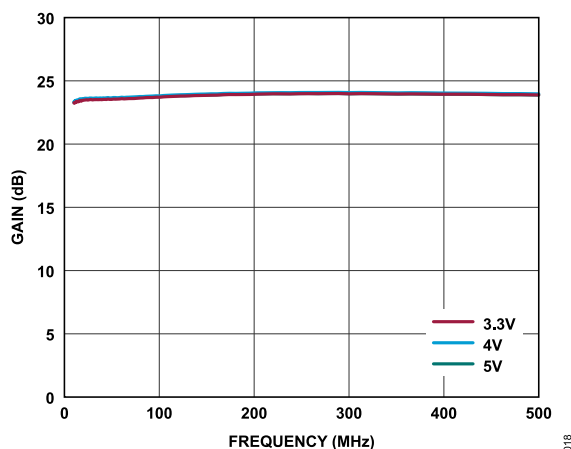


Figure 18. Gain vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30mA$

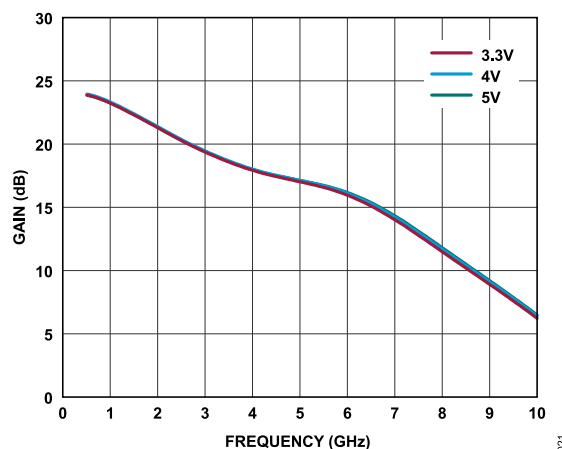


Figure 21. Gain vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30mA$

TYPICAL PERFORMANCE CHARACTERISTICS

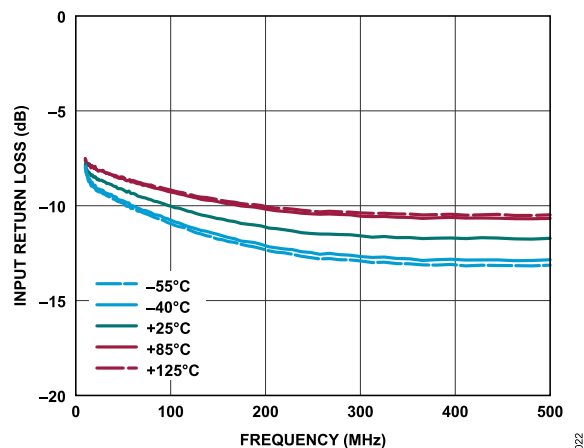


Figure 22. Input Return Loss vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

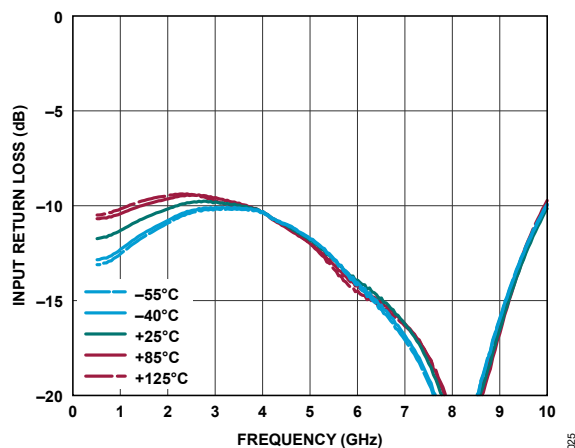


Figure 25. Input Return Loss vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

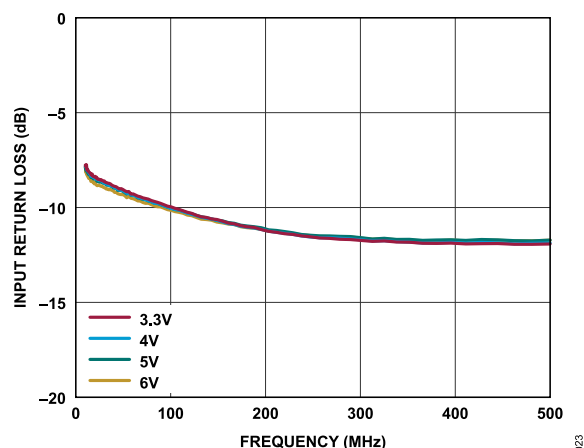


Figure 23. Input Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90mA$

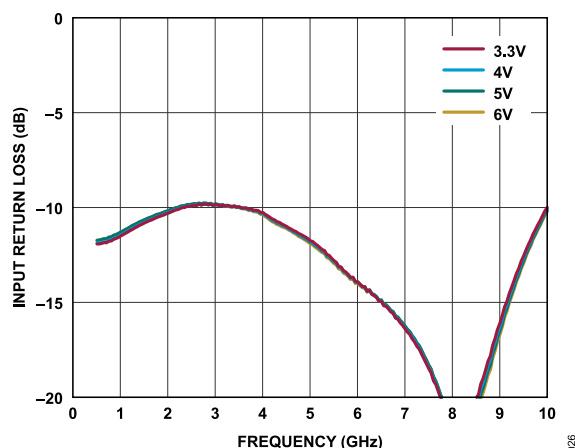


Figure 26. Input Return Loss vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90mA$

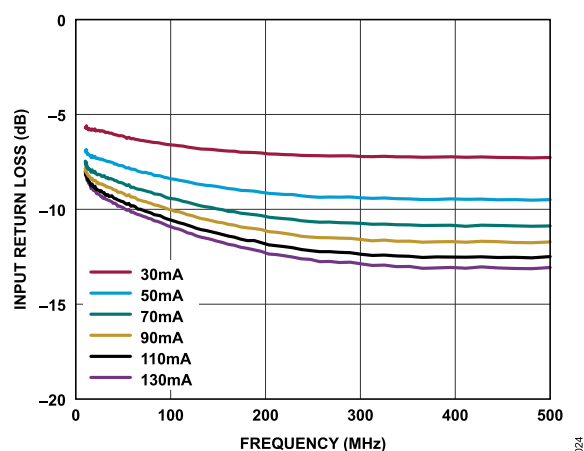


Figure 24. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5V$

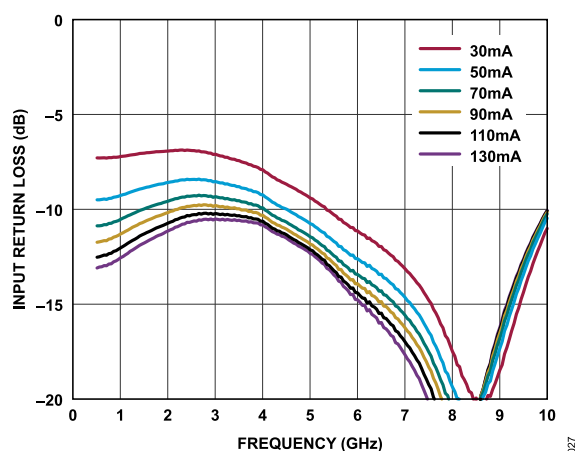


Figure 27. Input Return Loss vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5V$

TYPICAL PERFORMANCE CHARACTERISTICS

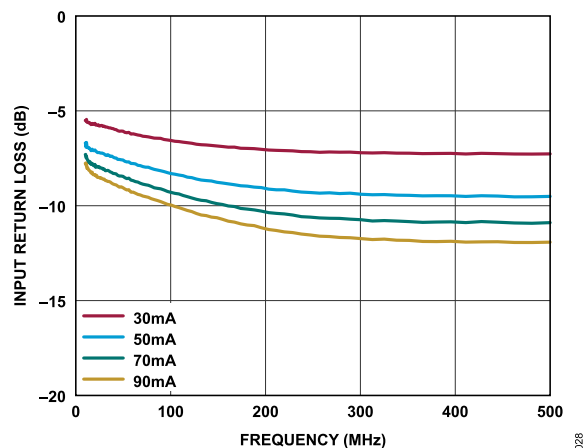


Figure 28. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3V$

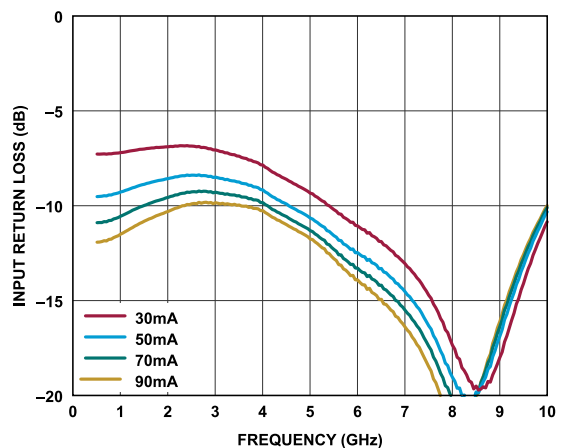


Figure 31. Input Return Loss vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3V$

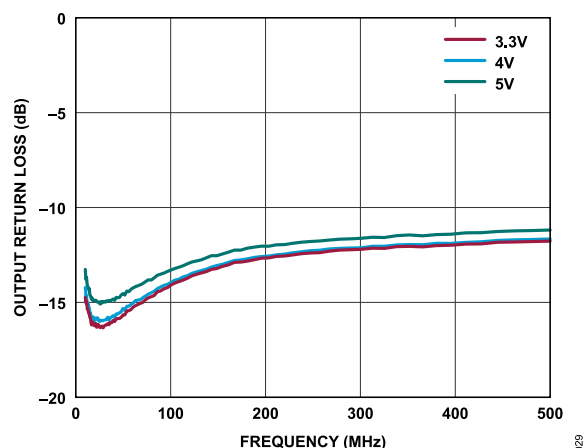


Figure 29. Output Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30mA$

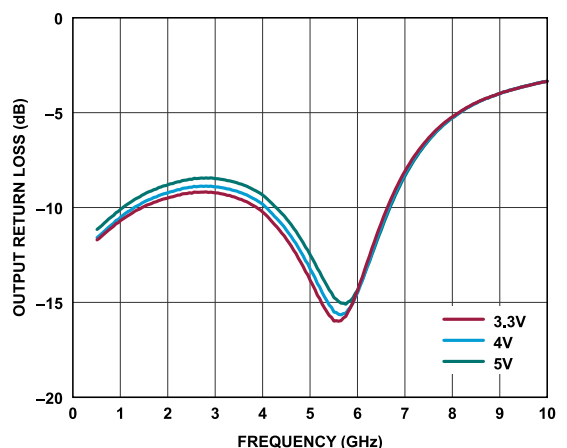


Figure 32. Output Return Loss vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30mA$

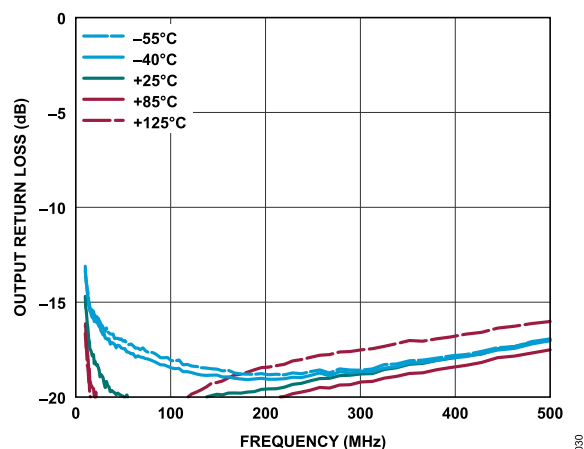


Figure 30. Output Return Loss vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

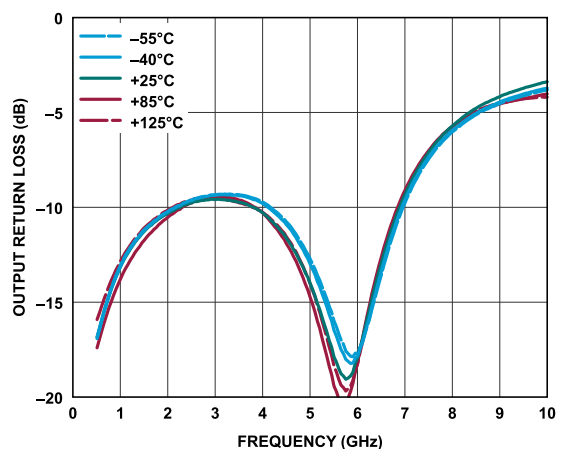


Figure 33. Output Return Loss vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

TYPICAL PERFORMANCE CHARACTERISTICS

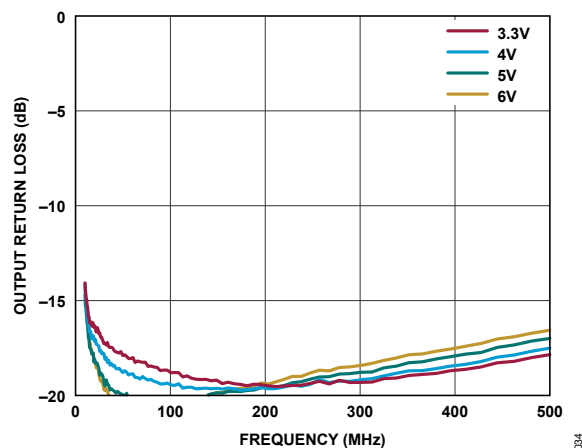


Figure 34. Output Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90\text{mA}$

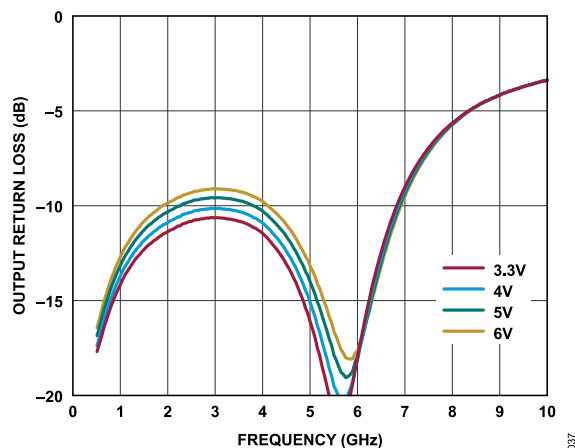


Figure 37. Output Return Loss vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90\text{mA}$

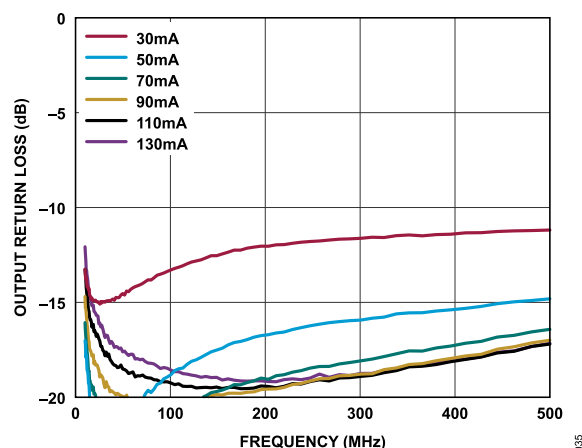


Figure 35. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5\text{V}$

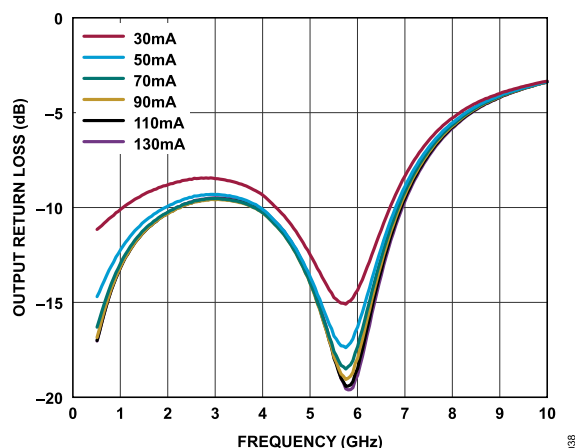


Figure 38. Output Return Loss vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5\text{V}$

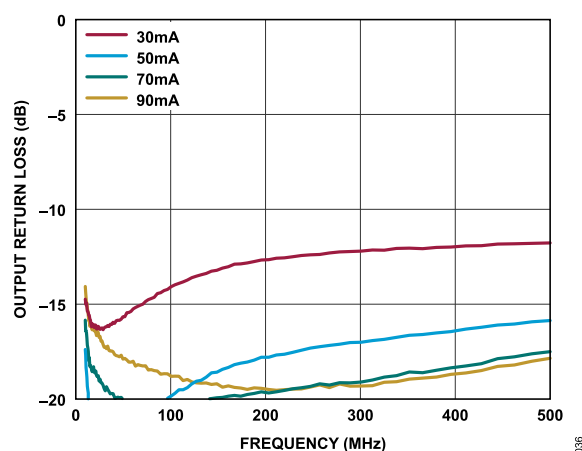


Figure 36. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3\text{V}$

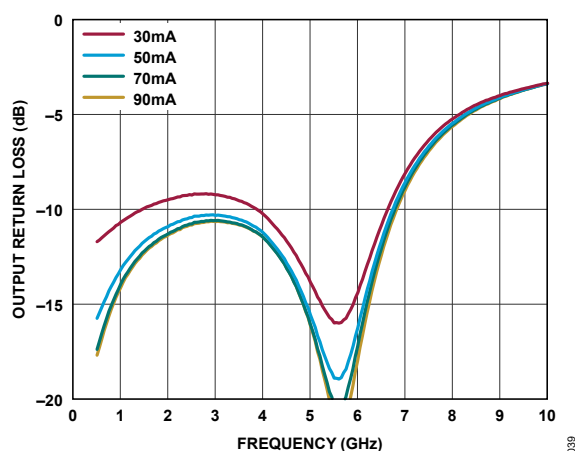


Figure 39. Output Return Loss vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3\text{V}$

TYPICAL PERFORMANCE CHARACTERISTICS

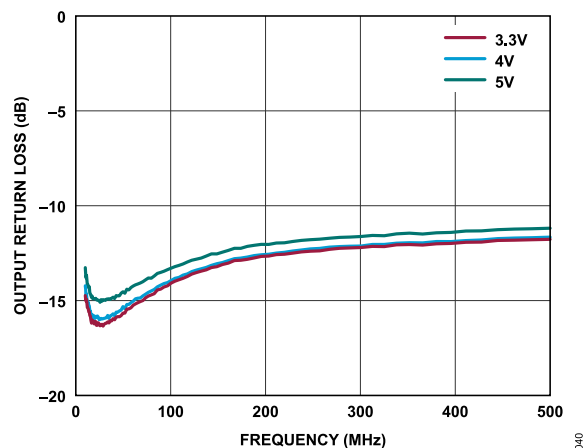


Figure 40. Output Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30\text{mA}$

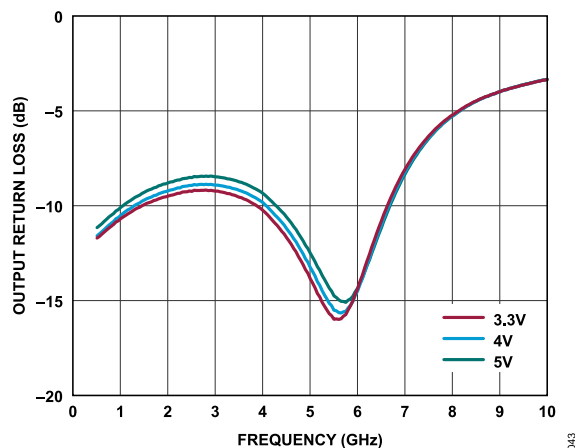


Figure 43. Output Return Loss vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30\text{mA}$

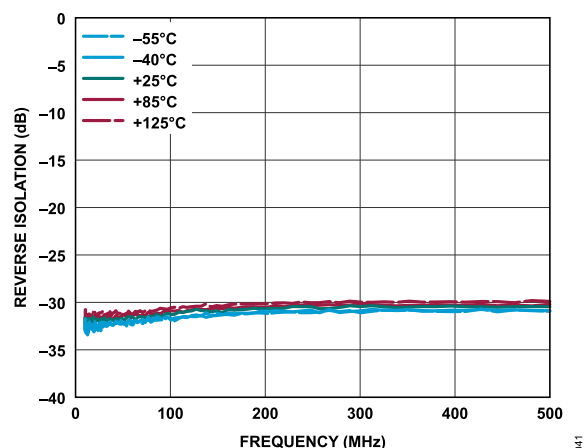


Figure 41. Reverse Isolation vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5\text{V}$, $I_{DQ} = 90\text{mA}$

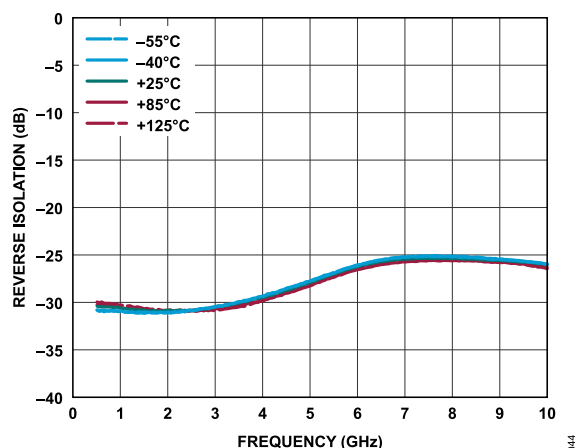


Figure 44. Reverse Isolation vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5\text{V}$, $I_{DQ} = 90\text{mA}$

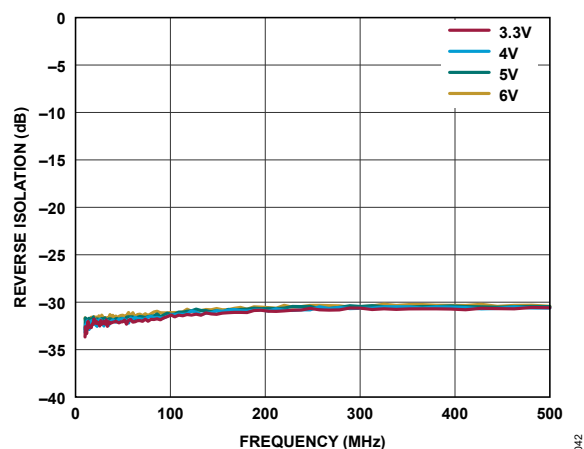


Figure 42. Reverse Isolation vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90\text{mA}$

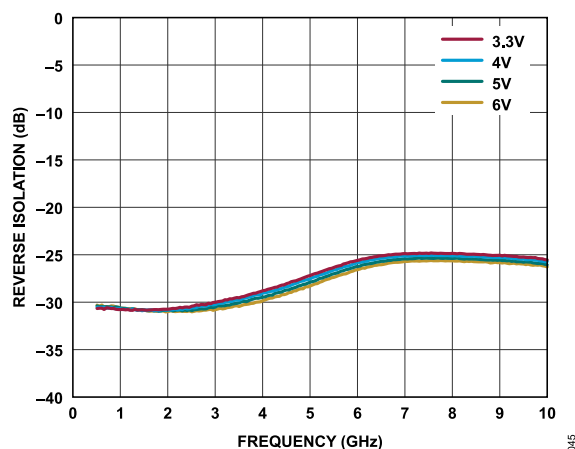


Figure 45. Reverse Isolation vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90\text{mA}$

TYPICAL PERFORMANCE CHARACTERISTICS

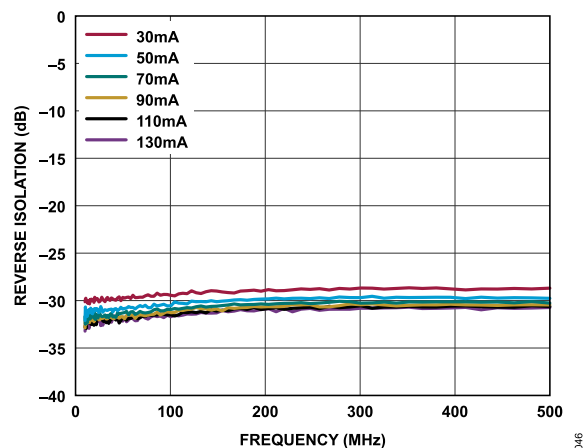


Figure 46. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5V$

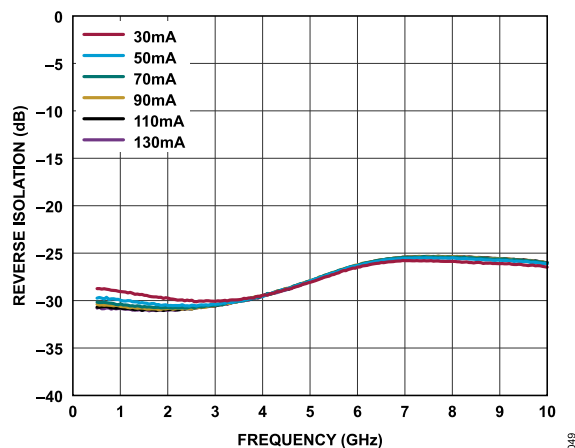


Figure 49. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5V$

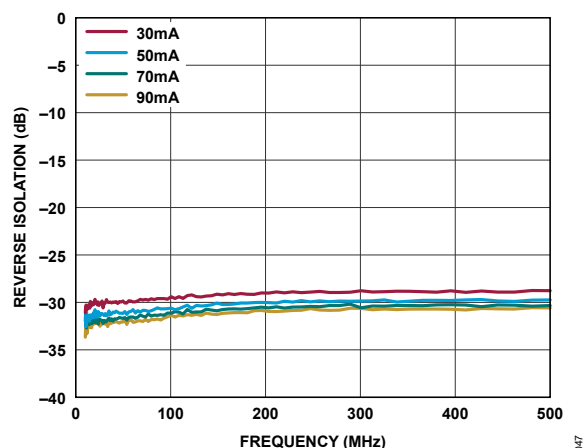


Figure 47. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3V$

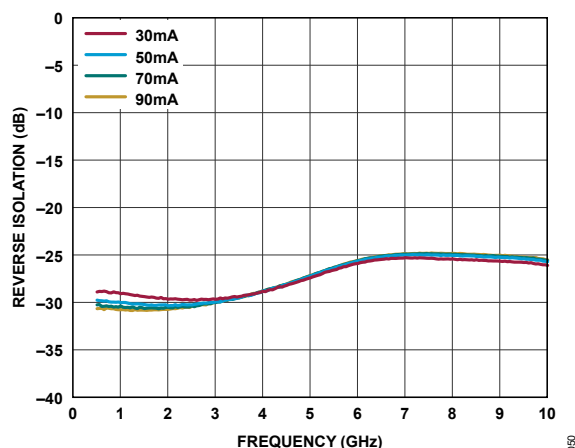


Figure 50. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3V$

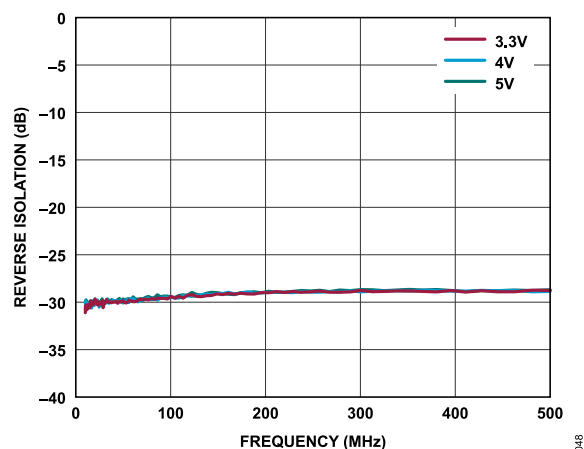


Figure 48. Reverse Isolation vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30mA$

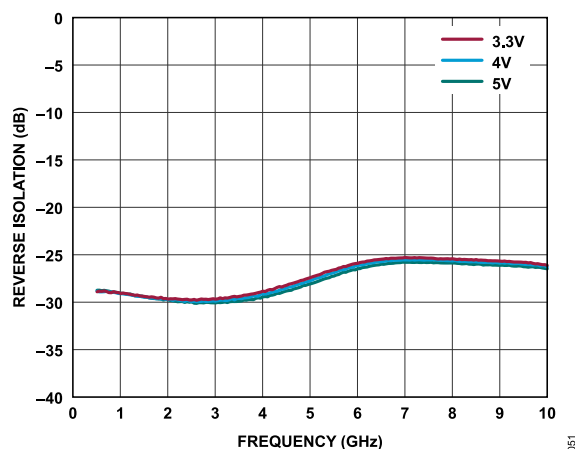


Figure 51. Reverse Isolation vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30mA$

TYPICAL PERFORMANCE CHARACTERISTICS

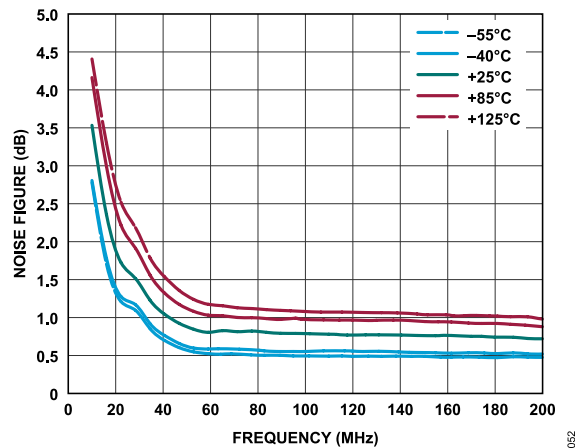


Figure 52. Noise Figure vs. Frequency for Various Temperatures, 10MHz to 200MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

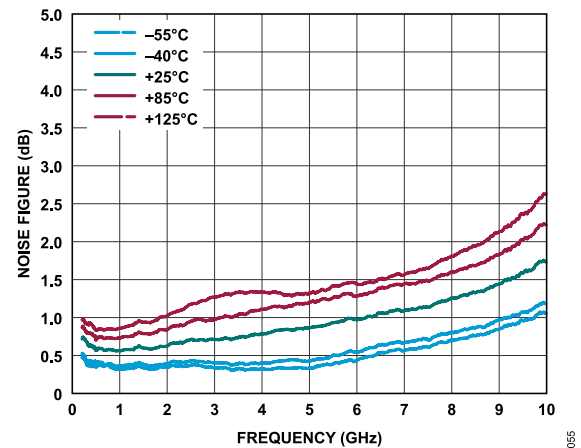


Figure 55. Noise Figure vs. Frequency for Various Temperatures, 200MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

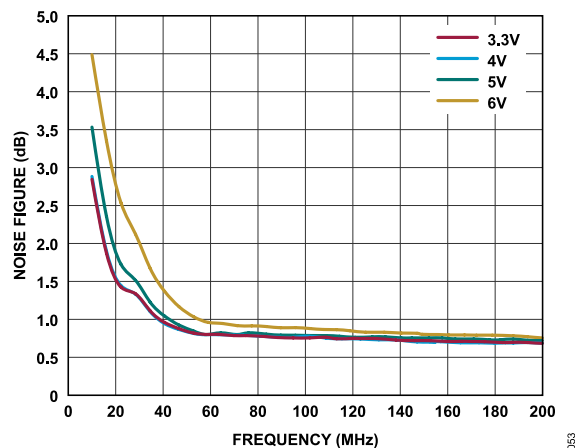


Figure 53. Noise Figure vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, $I_{DQ} = 90mA$

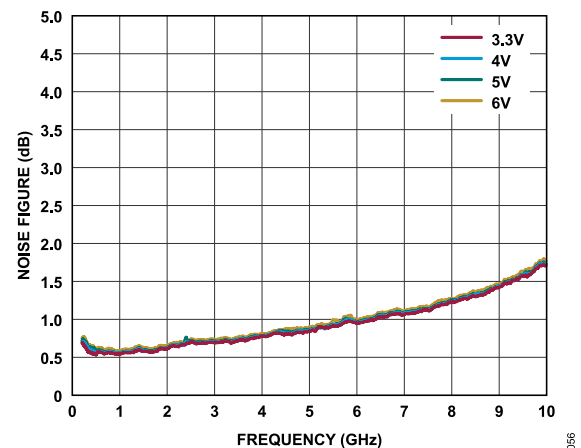


Figure 56. Noise Figure vs. Frequency for Various Supply Voltages, 200MHz to 10GHz, $I_{DQ} = 90mA$

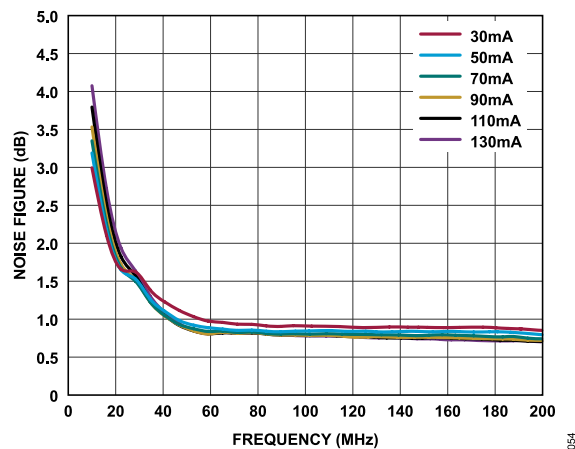


Figure 54. Noise Figure vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, $V_{DD} = 5V$

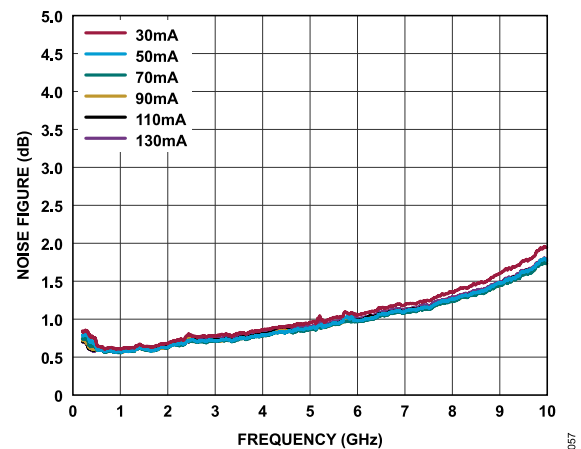


Figure 57. Noise Figure vs. Frequency for Various I_{DQ} Values, 200MHz to 10GHz, $V_{DD} = 5V$

TYPICAL PERFORMANCE CHARACTERISTICS

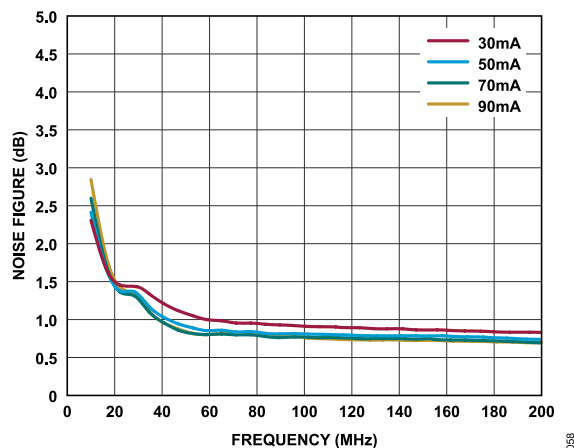


Figure 58. Noise Figure vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, $V_{DD} = 3.3V$

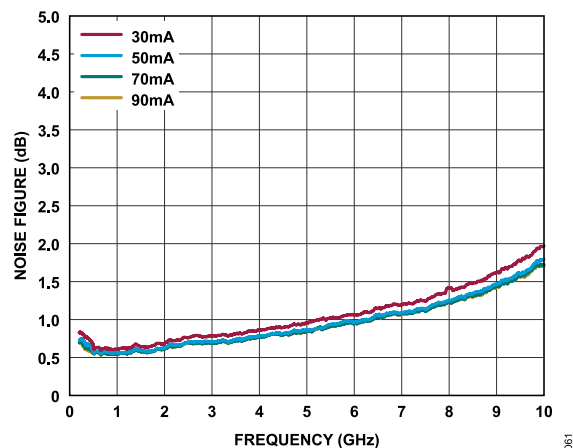


Figure 61. Noise Figure vs. Frequency for Various I_{DQ} Values, 200MHz to 10GHz, $V_{DD} = 3.3V$

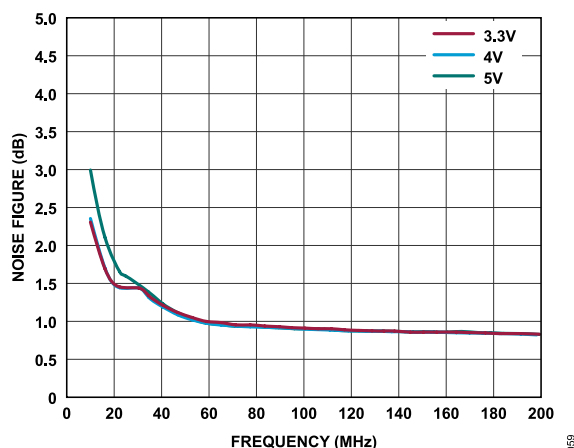


Figure 59. Noise Figure vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, $I_{DQ} = 30mA$

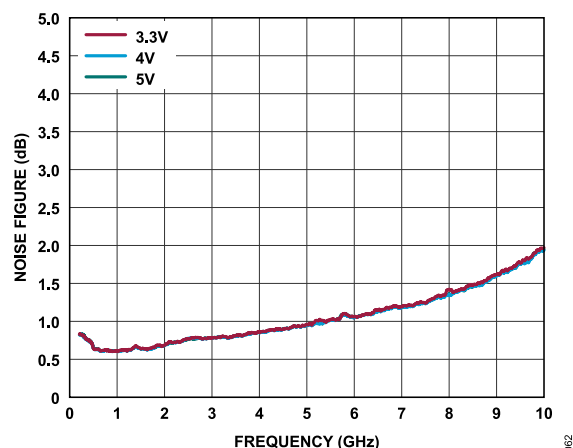


Figure 62. Noise Figure vs. Frequency for Various Supply Voltages, 200MHz to 10GHz, $I_{DQ} = 30mA$

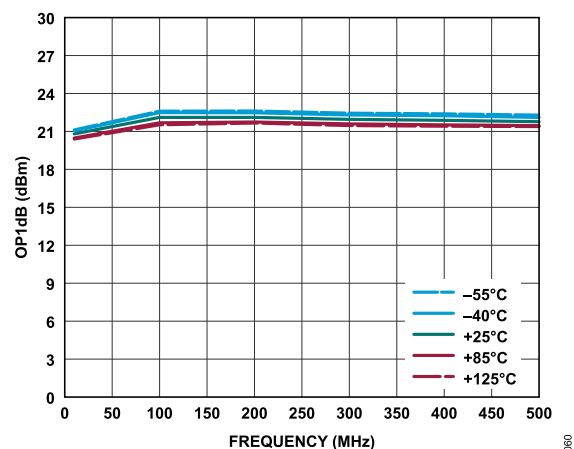


Figure 60. OP1dB vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

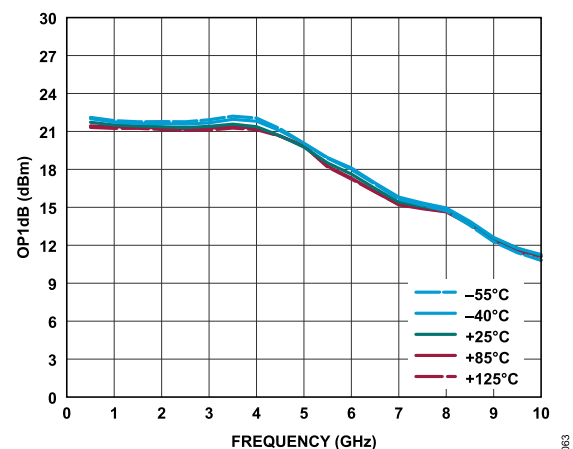


Figure 63. OP1dB vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

TYPICAL PERFORMANCE CHARACTERISTICS

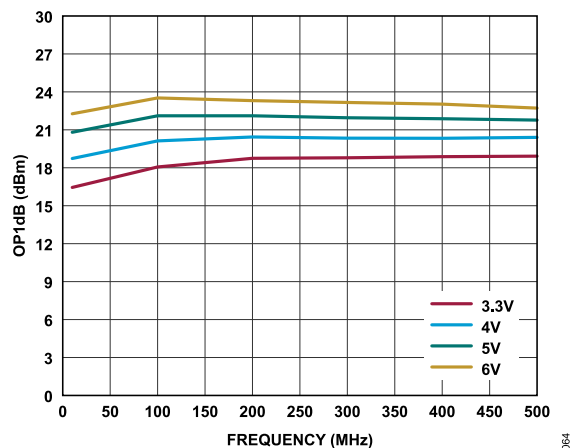


Figure 64. OP1dB vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90\text{mA}$

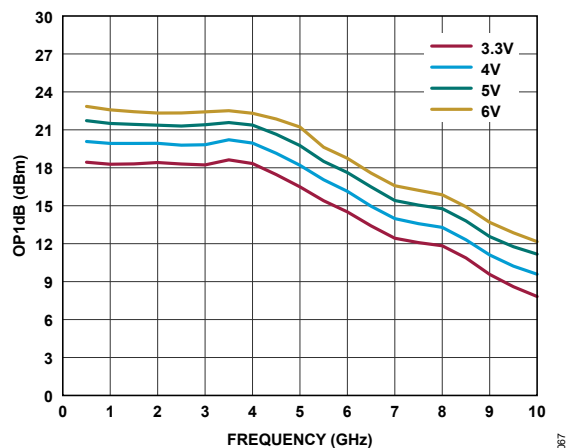


Figure 67. OP1dB vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90\text{mA}$

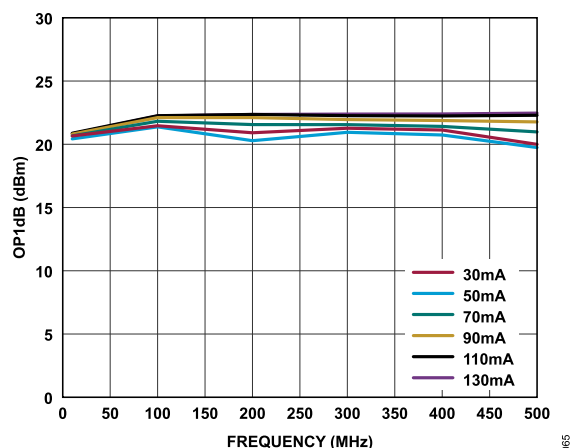


Figure 65. OP1dB vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5\text{V}$

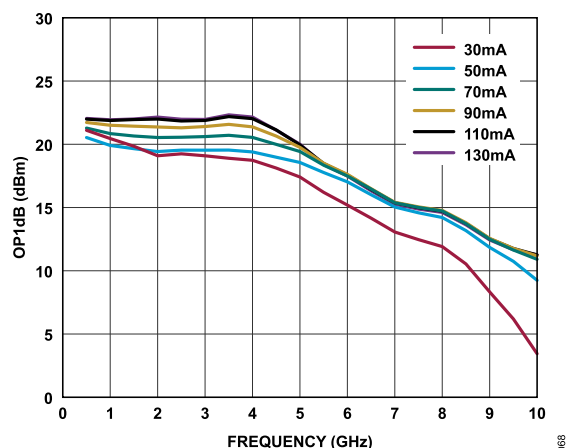


Figure 68. OP1dB vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5\text{V}$

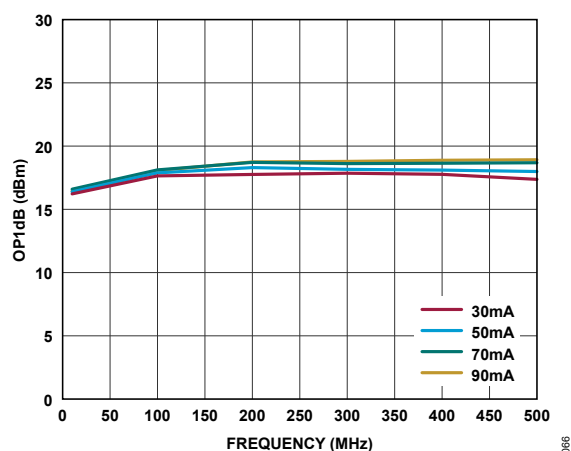


Figure 66. OP1dB vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3\text{V}$

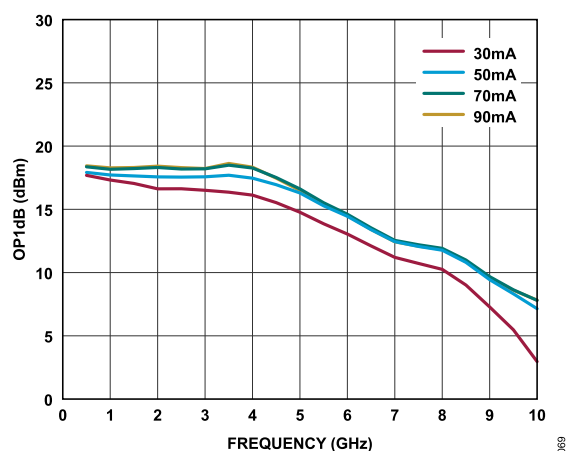


Figure 69. OP1dB vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3\text{V}$

TYPICAL PERFORMANCE CHARACTERISTICS

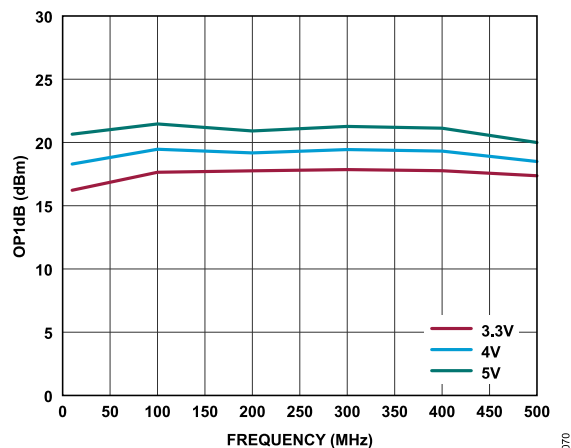


Figure 70. OP1dB vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30\text{mA}$

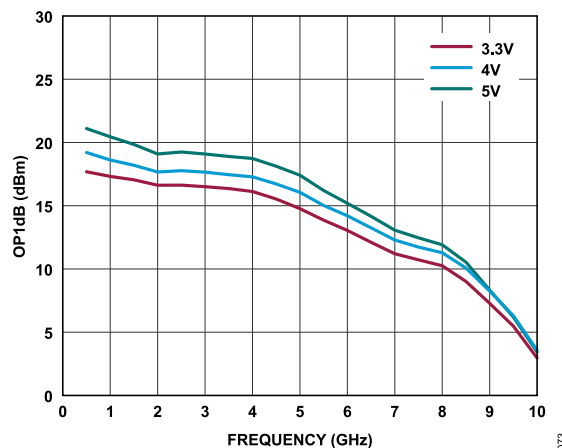


Figure 73. OP1dB vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30\text{mA}$

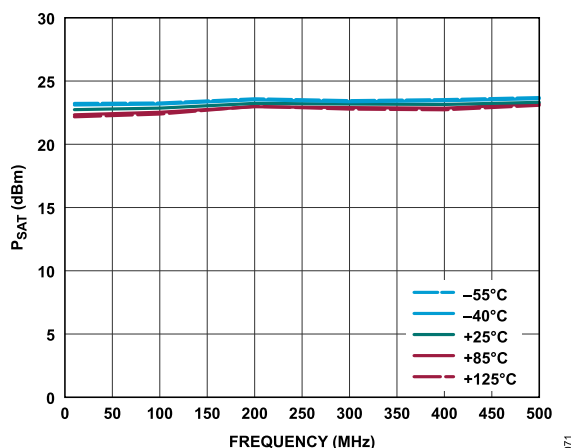


Figure 71. P_{SAT} vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5\text{V}$, $I_{DQ} = 90\text{mA}$

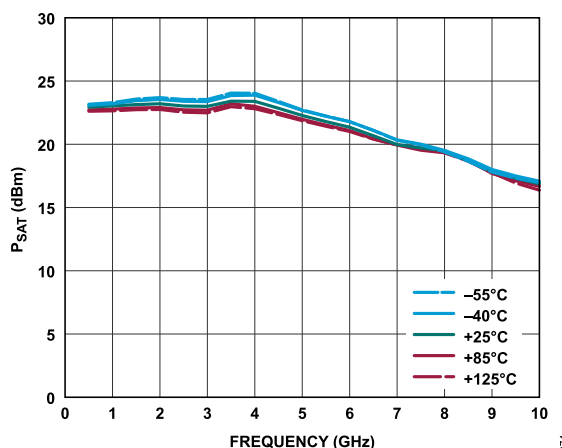


Figure 74. P_{SAT} vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5\text{V}$, $I_{DQ} = 90\text{mA}$

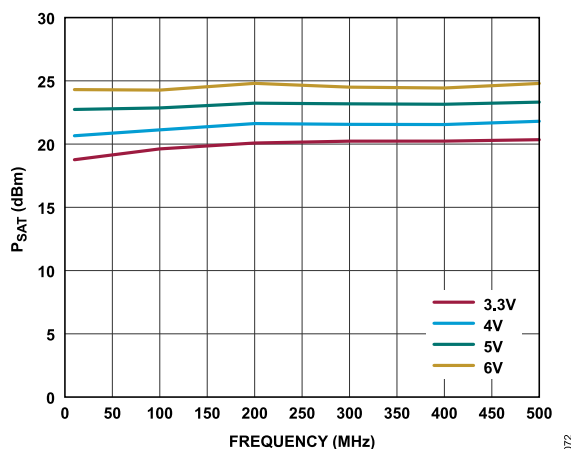


Figure 72. P_{SAT} vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90\text{mA}$

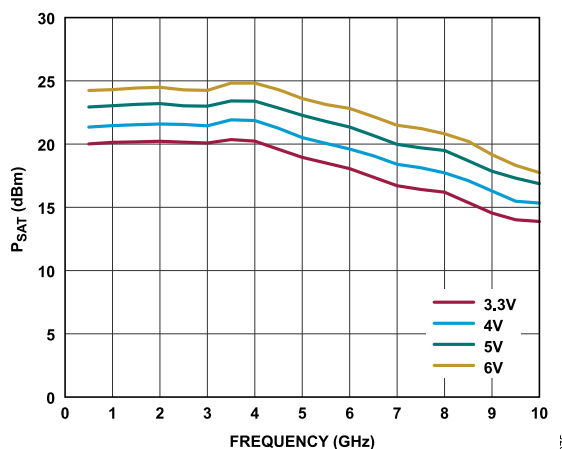


Figure 75. P_{SAT} vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90\text{mA}$

TYPICAL PERFORMANCE CHARACTERISTICS

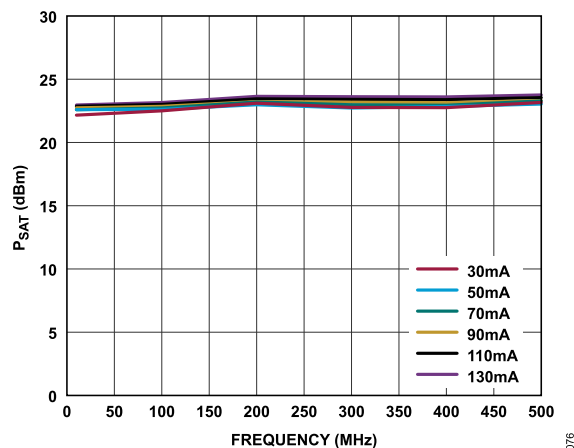


Figure 76. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5V$

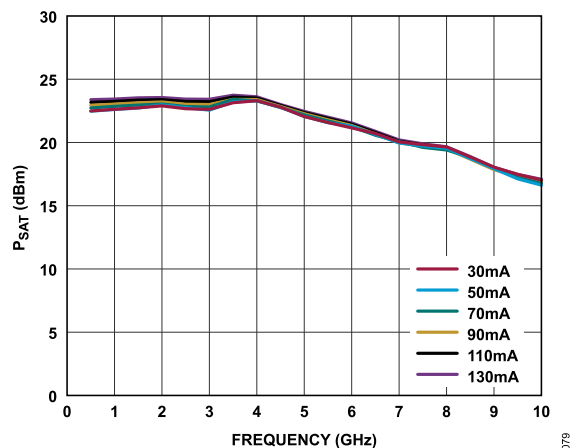


Figure 79. P_{SAT} vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5V$

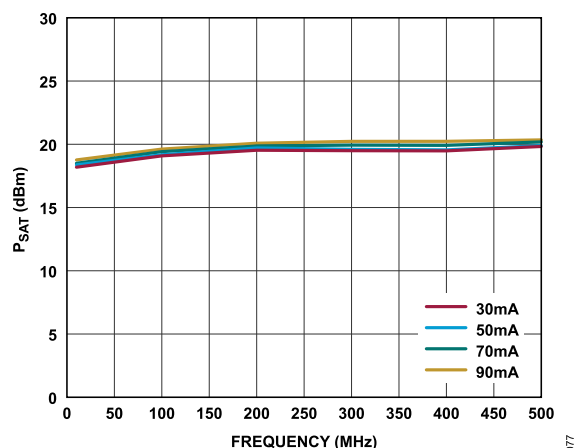


Figure 77. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3V$

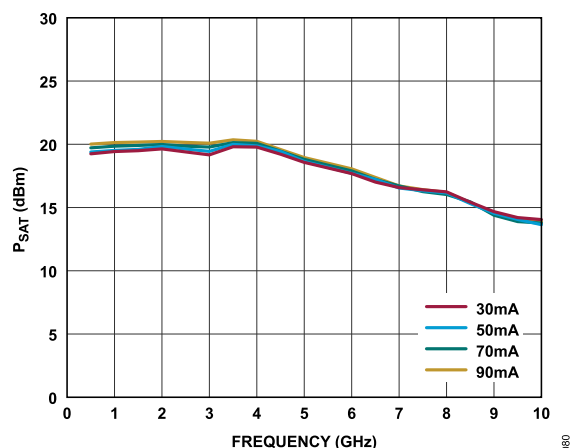


Figure 80. P_{SAT} vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3V$

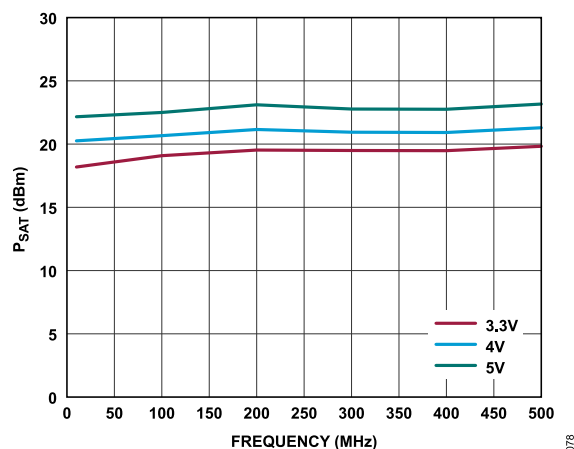


Figure 78. P_{SAT} vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30mA$

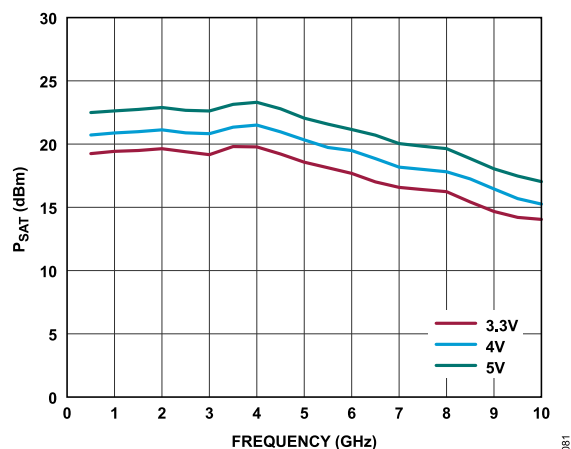


Figure 81. P_{SAT} vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30mA$

TYPICAL PERFORMANCE CHARACTERISTICS

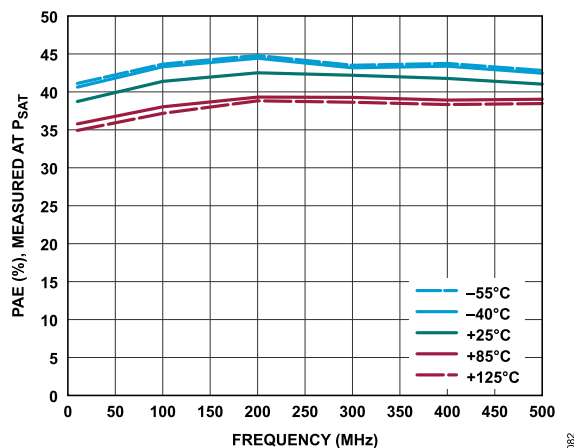


Figure 82. PAE, Measured at P_{SAT} vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

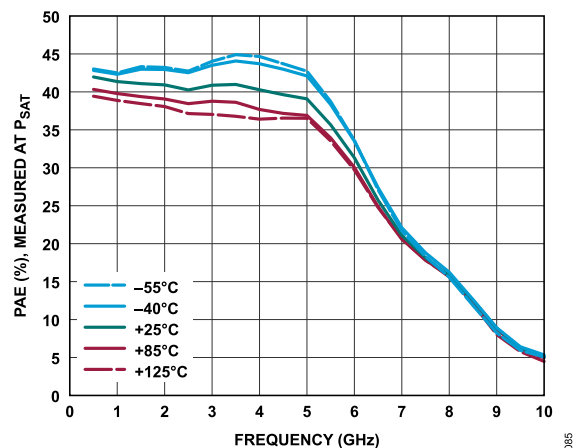


Figure 85. PAE, Measured at P_{SAT} vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

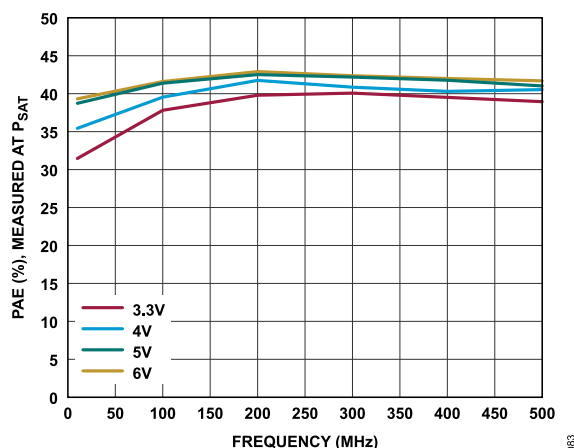


Figure 83. PAE, Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90mA$

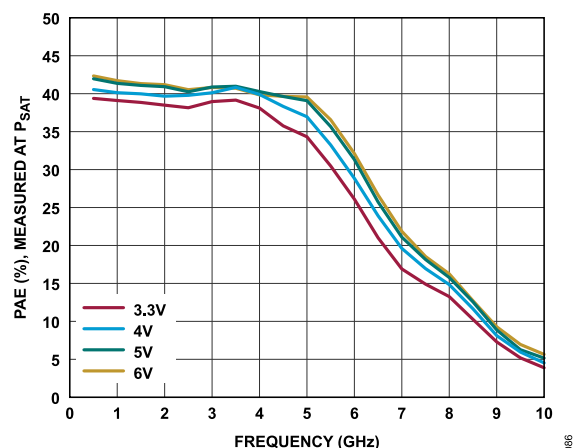


Figure 86. PAE, Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90mA$

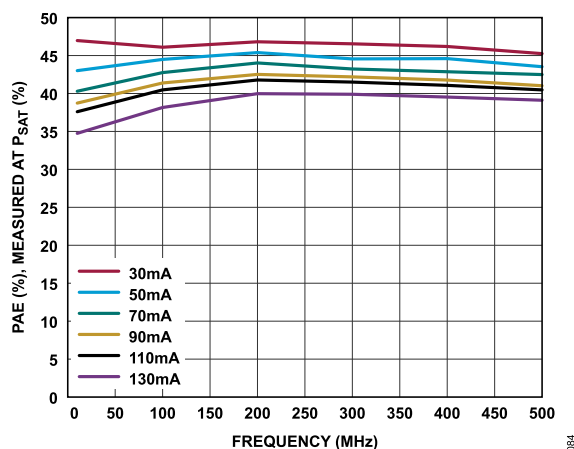


Figure 84. PAE, Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5V$

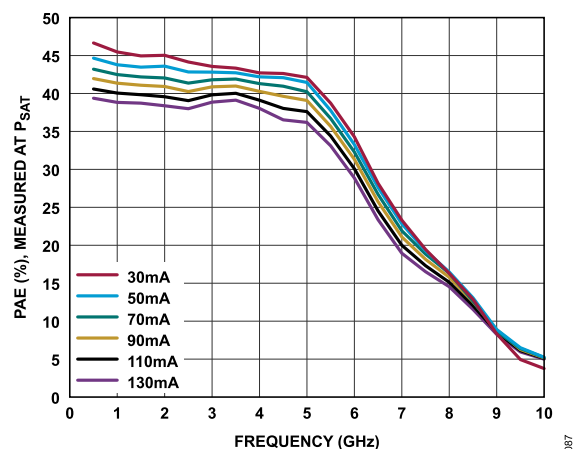


Figure 87. PAE, Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5V$

TYPICAL PERFORMANCE CHARACTERISTICS

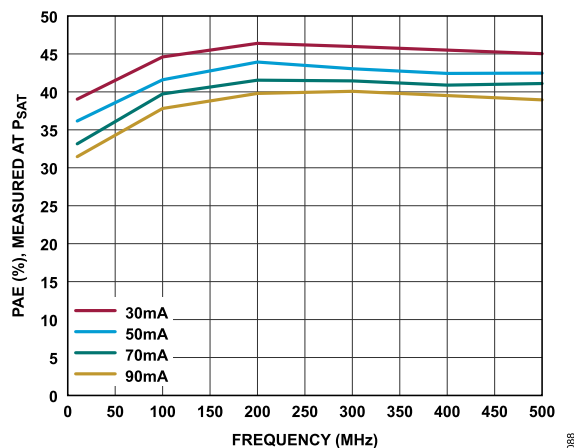


Figure 88. PAE, Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3V$

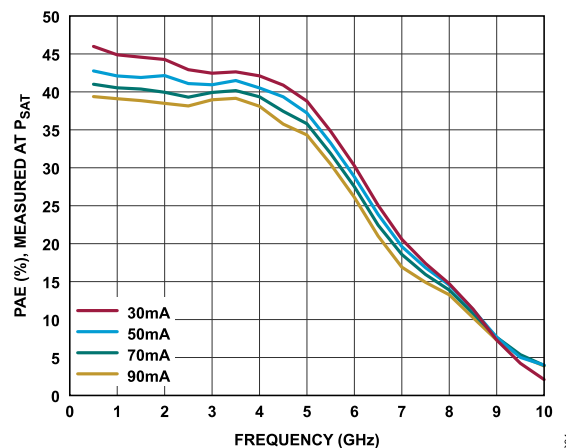


Figure 91. PAE, Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3V$

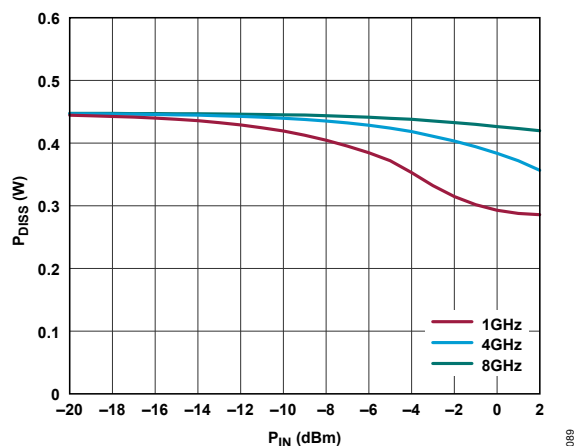


Figure 89. P_{DISS} vs. P_{IN} at Various Frequencies, $T_{CASE} = 85^{\circ}C$, and $V_{DD} = 5V$

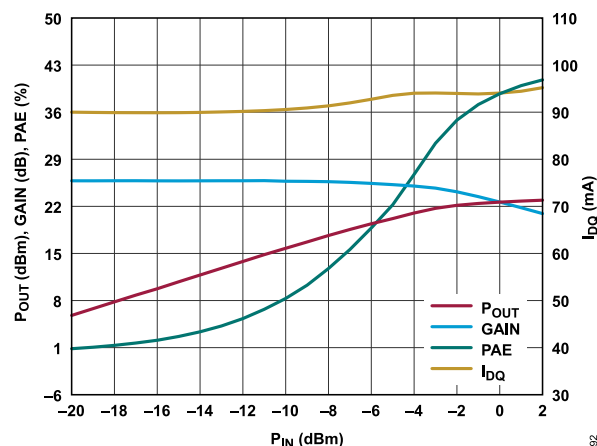


Figure 92. P_{OUT} , GAIN, PAE, and I_{DQ} vs. P_{IN} , Power Compression at 1GHz, $V_{DD} = 5V$

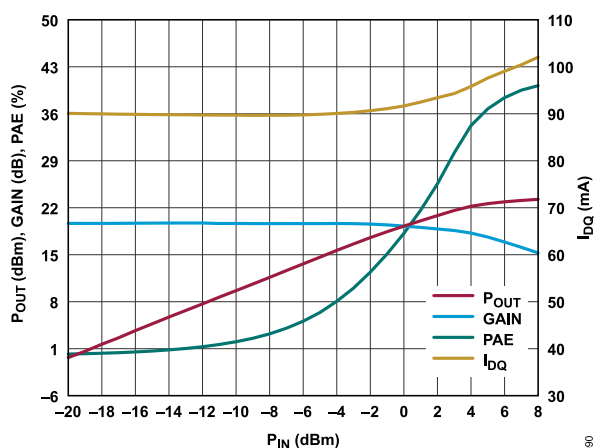


Figure 90. P_{OUT} , GAIN, PAE, and I_{DQ} vs. P_{IN} , Power Compression at 4GHz, $V_{DD} = 5V$

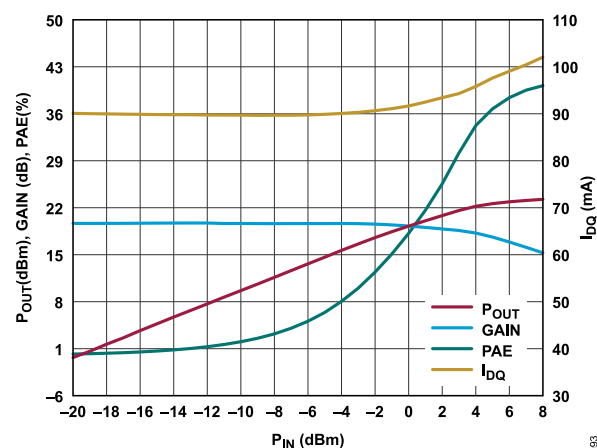


Figure 93. P_{OUT} , GAIN, PAE, and I_{DQ} vs. P_{IN} , Power Compression at 8GHz, $V_{DD} = 5V$

TYPICAL PERFORMANCE CHARACTERISTICS

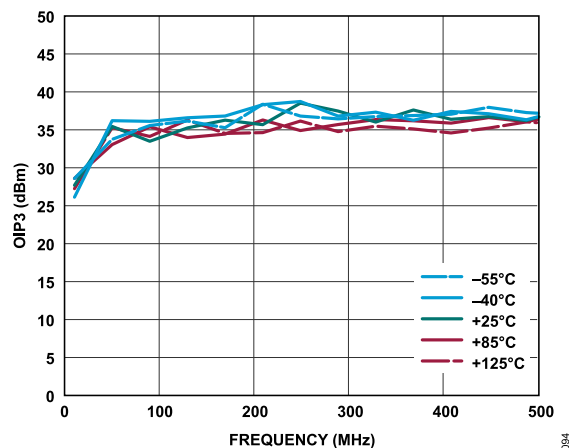


Figure 94. OIP3 vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

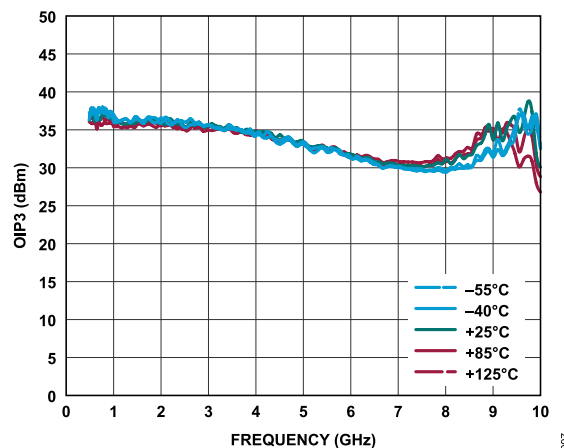


Figure 97. OIP3 vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

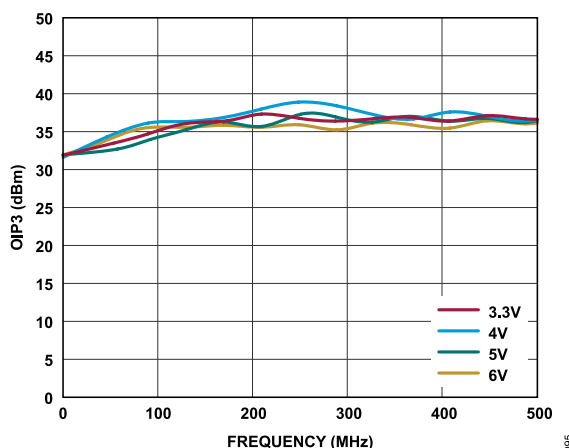


Figure 95. OIP3 vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90mA$

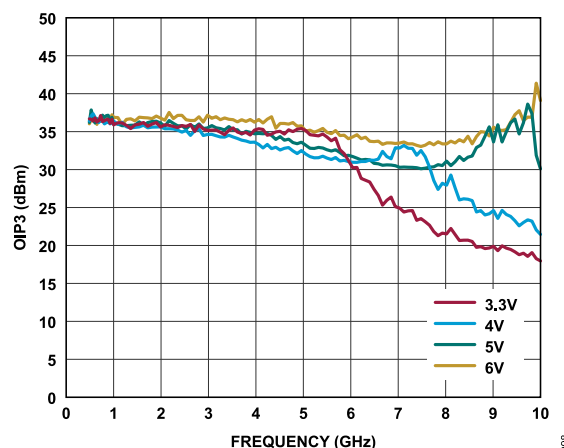


Figure 98. OIP3 vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90mA$

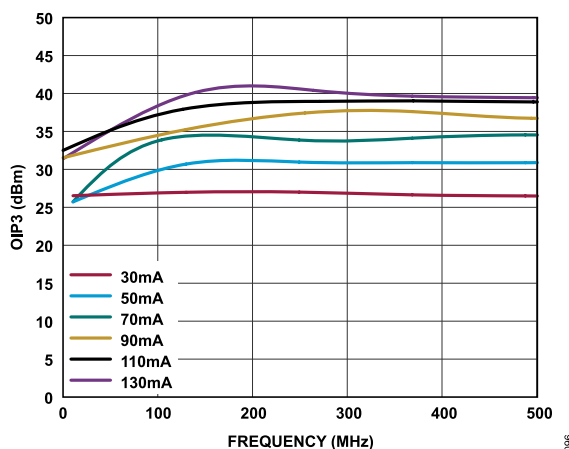


Figure 96. OIP3 vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5V$

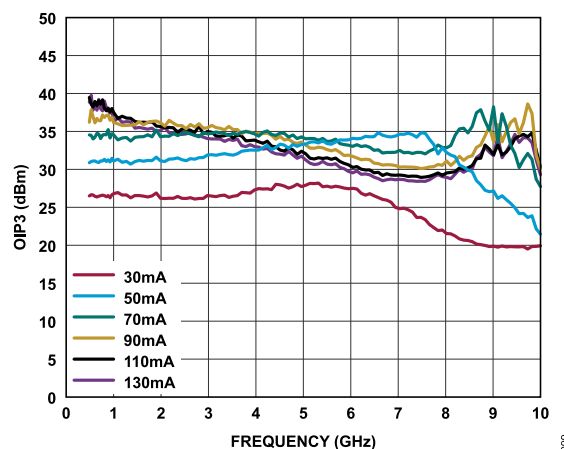


Figure 99. OIP3 vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5V$

TYPICAL PERFORMANCE CHARACTERISTICS

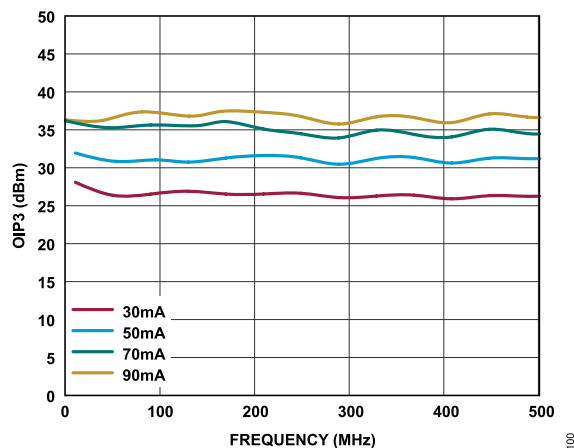


Figure 100. OIP3 vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3V$

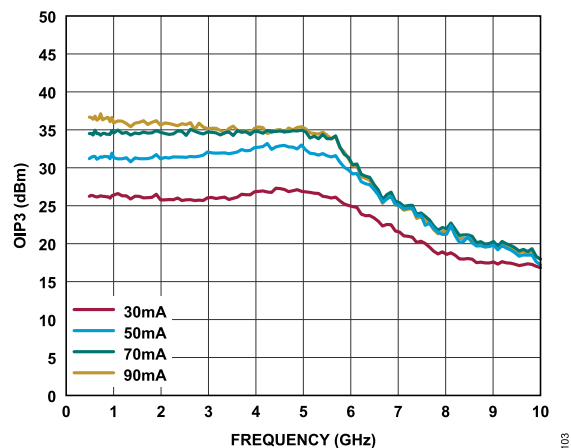


Figure 103. OIP3 vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3V$

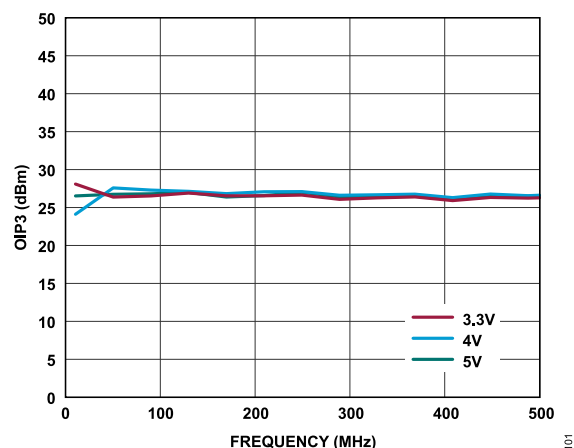


Figure 101. OIP3 vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30mA$

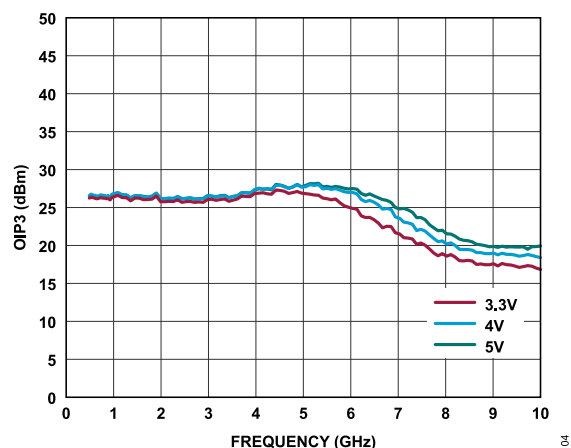


Figure 104. OIP3 vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30mA$

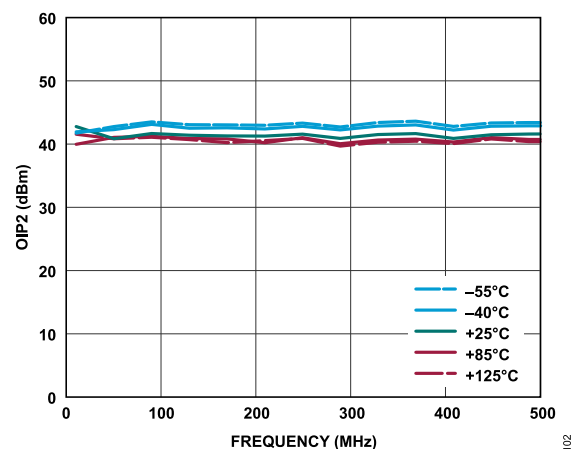


Figure 102. OIP2 vs. Frequency for Various Temperatures, 10MHz to 500MHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

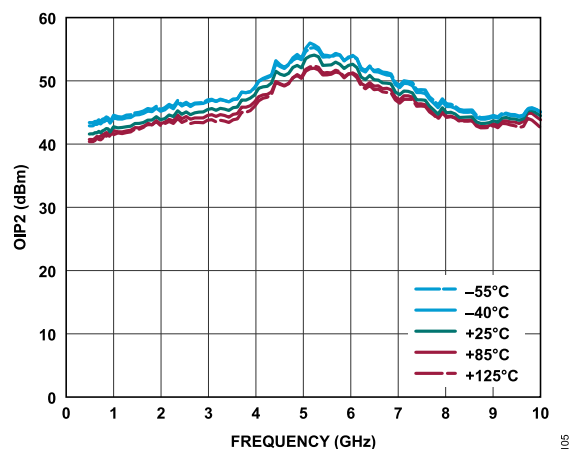


Figure 105. OIP2 vs. Frequency for Various Temperatures, 500MHz to 10GHz, $V_{DD} = 5V$, $I_{DQ} = 90mA$

TYPICAL PERFORMANCE CHARACTERISTICS

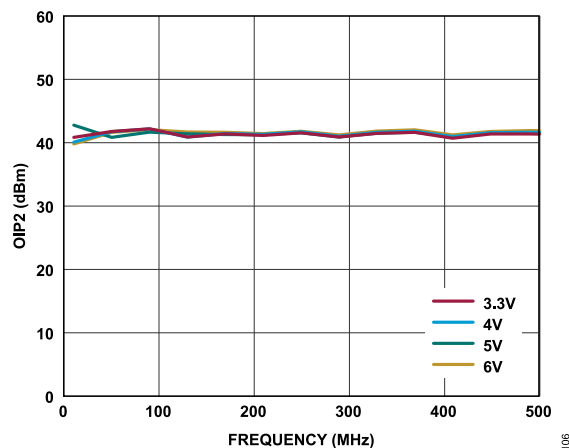


Figure 106. OIP2 vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 90\text{mA}$

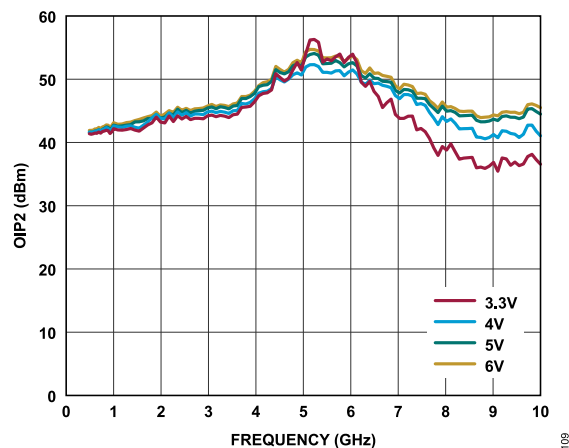


Figure 109. OIP2 vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 90\text{mA}$

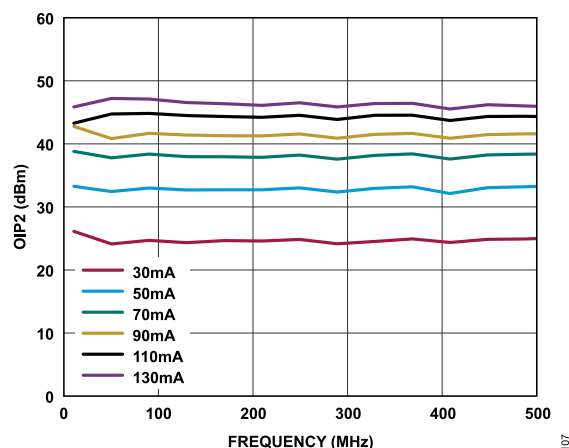


Figure 107. OIP2 vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 5\text{V}$

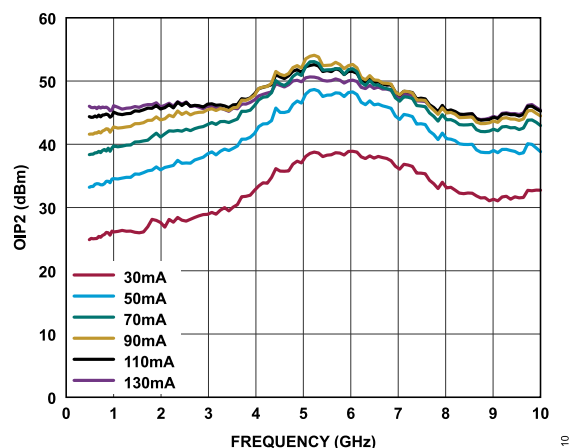


Figure 110. OIP2 vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 5\text{V}$

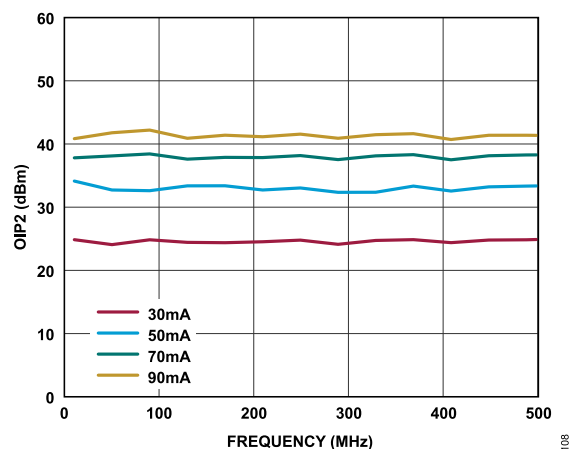


Figure 108. OIP2 vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, $V_{DD} = 3.3\text{V}$

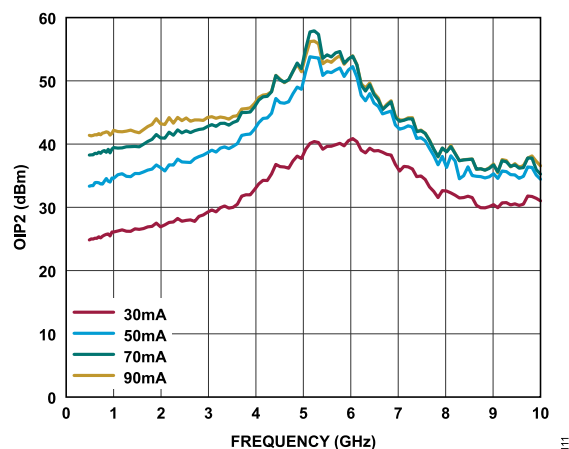


Figure 111. OIP2 vs. Frequency for Various I_{DQ} Values, 500MHz to 10GHz, $V_{DD} = 3.3\text{V}$

TYPICAL PERFORMANCE CHARACTERISTICS

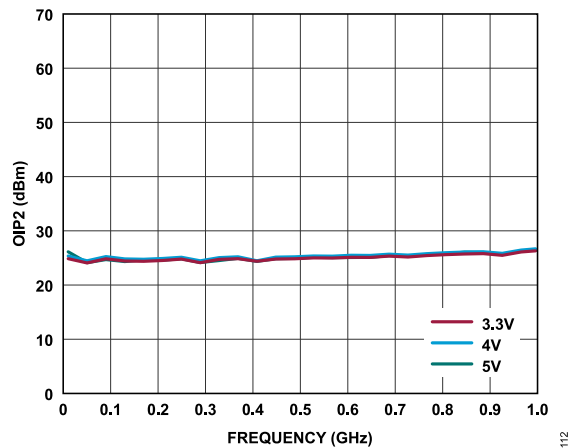


Figure 112. OIP2 vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, $I_{DQ} = 30\text{mA}$

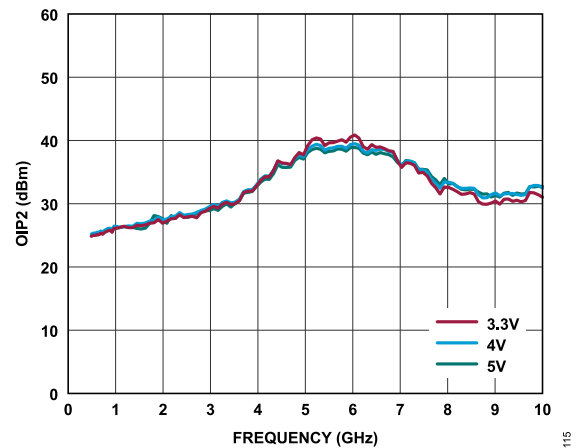


Figure 115. OIP2 vs. Frequency for Various Supply Voltages, 500MHz to 10GHz, $I_{DQ} = 30\text{mA}$

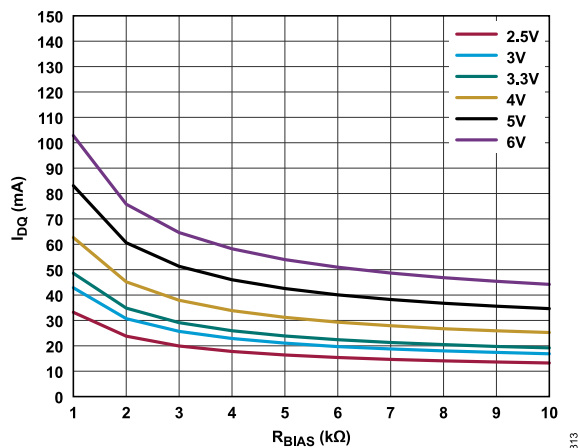


Figure 113. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 1kΩ to 10kΩ

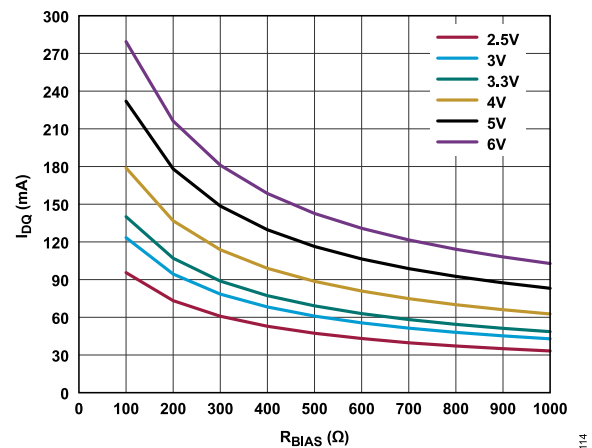


Figure 116. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0Ω to 1kΩ

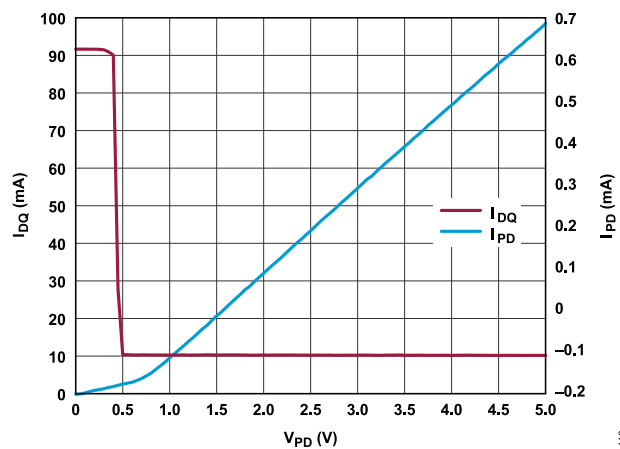


Figure 114. I_{DQ} and PD Current (I_{PD}) vs. V_{PD}

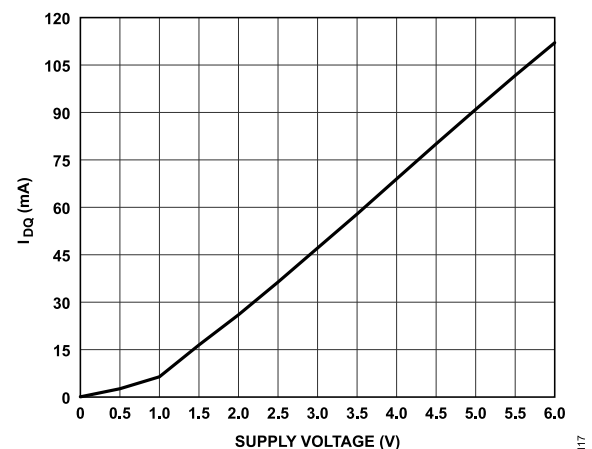


Figure 117. I_{DQ} vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

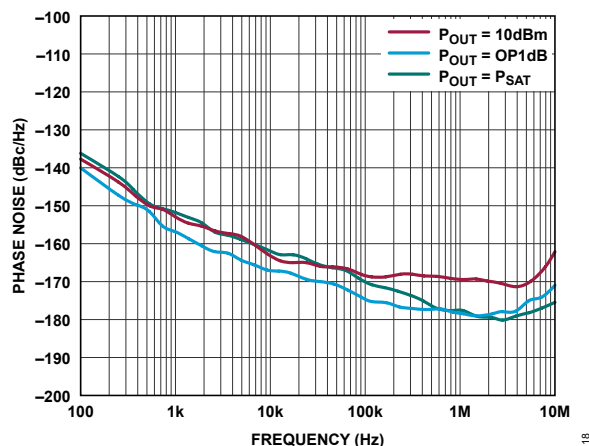


Figure 118. Residual Phase Noise vs. Frequency at 2GHz for Various P_{OUT} Values, $V_{DD} = 5V$

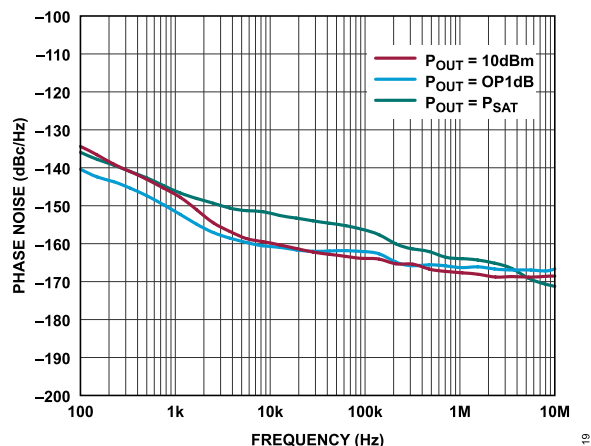


Figure 120. Residual Phase Noise vs. Frequency at 5GHz for Various P_{OUT} Values, $V_{DD} = 5V$

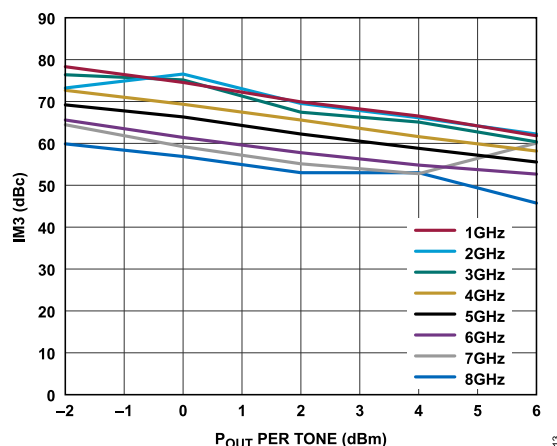


Figure 119. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, $V_{DD} = 5V$

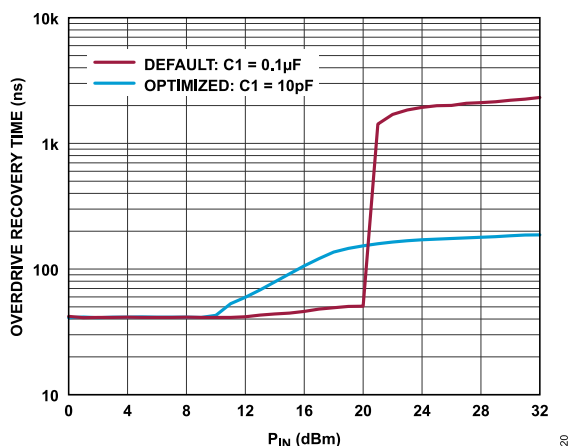


Figure 121. Overdrive Recovery Time vs. P_{IN} at 3GHz, Recovery Time to Within 90% of Small Signal Gain Value, $V_{DD} = 5V$, Blocking Signal at 4GHz

TYPICAL PERFORMANCE CHARACTERISTICS

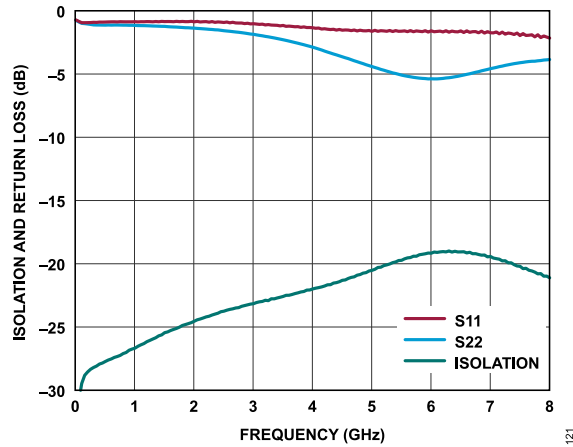
Amplifier Off State ($V_{PD} = V_{DD}$)

Figure 122. Isolation and Return Loss vs. Frequency, 10MHz to 8GHz, $V_{DD} = 5V$

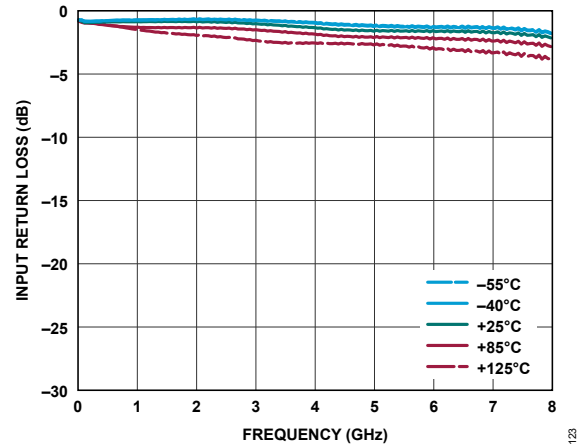


Figure 124. Input Return Loss vs. Frequency for Various Temperatures, 10MHz to 8GHz, $V_{DD} = 5V$

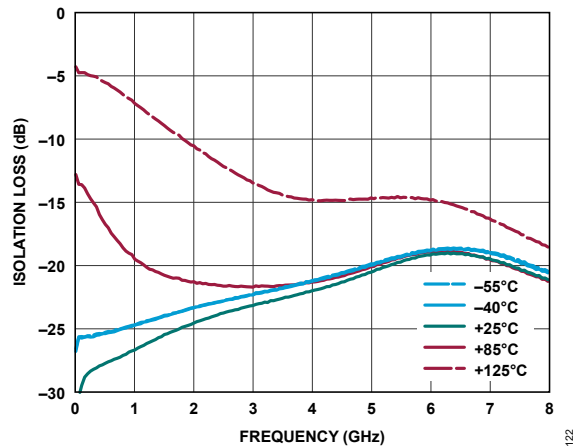


Figure 123. Isolation vs. Frequency for Various Temperatures, 10MHz to 8GHz, $V_{DD} = 5V$

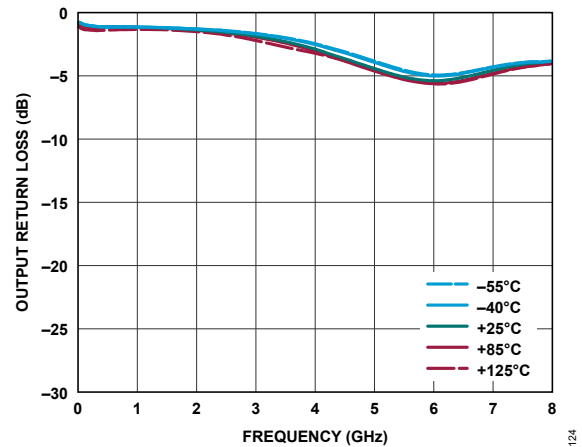


Figure 125. Output Return Loss vs. Frequency for Various Temperatures, 10MHz to 8GHz, $V_{DD} = 5V$

THEORY OF OPERATION

The ADL8130 is a wideband LNA with a bias inductor, and an enable or disable function. **Figure 126** shows the simplified architecture of the ADL8130.

The ADL8130 has DC-coupled, single-ended input and output ports with impedances that are nominally equal to 50Ω over the 0.01GHz to 8GHz frequency range. No external matching components are required. The value of the resistor connected between VDD2 and RBIAS controls the I_{DQ} .

The ADL8130 also has an enable or disable function. By pulling the VPD pin low or high, the ADL8130 can be enabled or disabled, respectively.

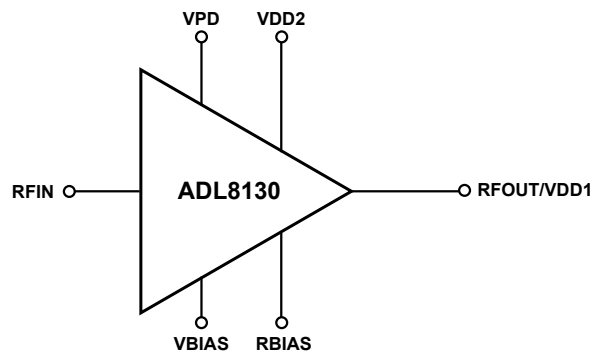


Figure 126. Simplified Schematic

131

APPLICATIONS INFORMATION

The basic connections for operating the ADL8130 over the specified frequency range are shown in **Figure 127**. Alternatively, 3.3V supply operation is also supported.

It is recommended to use 0.1μF power-supply decoupling capacitors. To set I_{DQ} , connect a resistor (R1) between the RBIAS and VDD2 pins. A default value of 835Ω is recommended, which results in a nominal I_{DQ} of 90mA. **Table 9** shows how I_{DQ} and I_{DQ_AMP} vary vs. R_{BIAS} . The RBIAS pin also draws a current that varies with the RBIAS value (see **Table 9**). Do not leave the RBIAS pin open. The VPD pin provides a convenient method to power up or power down the ADL8130. To enable the amplifier, connect the VPD pin to ground. To disable the amplifier, connect the VPD pin to a supply.

Figure 127 shows the typical application circuit.

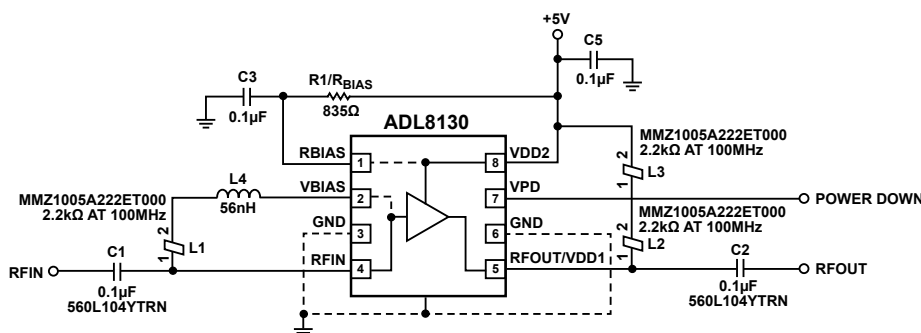


Figure 127. Typical Application Circuit

Recommended Bias Sequencing

Correct sequencing of the DC and RF power is required to safely operate the ADL8130. To power up the ADL8130, take the following bias sequencing steps:

1. Set V_{DD} to 5V.
2. Set V_{PD} to 0V.
3. Apply the RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence. **Table 9** through **Table 12** show alternate bias resistor options for different V_{DD} and I_{DQ} choices.

Table 9. Recommended Bias Resistor Values for $V_{DD} = 5V$

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
15000	30	29.3	0.7
2870	50	48.5	1.5
1330	70	67.3	2.7
835	90	85.5	4.5
536	110	118.4	1.6
383	130	127.3	2.7

Table 10. Recommended Bias Resistor Values for $V_{DD} = 3.3V$

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
2610	30	29.1	0.9
1400	40	38.4	1.6
887	50	47.6	2.4
619	60	56.7	3.3
464	70	65.9	4.1
357	80	75	5
280	90	83.9	6.1

APPLICATIONS INFORMATION

Table 11. Recommended Bias Resistor Values for Various Supply Voltages, $I_{DQ} = 90\text{mA}$

$R_{BIAS} (\Omega)$	$V_{DD} (V)$	$I_{DQ_AMP} (mA)$	$I_{RBIAS} (mA)$
215	3	83.8	6.2
280	3.3	84	6
464	4	84.9	5.1
835	5	85.5	4.5
1240	6	86.5	3.5

Table 12. Recommended Bias Resistor Values for Various Supply Voltages, $I_{DQ} = 70\text{mA}$

$R_{BIAS} (\Omega)$	$V_{DD} (V)$	$I_{DQ_AMP} (mA)$	$I_{RBIAS} (mA)$
357	3	65.6	4.4
464	3.3	65.9	4.1
750	4	66.6	3.4
1330	5	67.3	2.7
2210	6	67.9	2.1

Operation from 10kHz to 8GHz

Figure 129 shows the application circuit that was used to extend operation down to 10kHz. Note that additional components, $R2$ and $R3 = 300\Omega$, $L5$ and $L6 = 680\mu\text{H}$, $C2 = 1\mu\text{F}$, and $L4 = 2.2\text{k}\Omega$ at 100MHz, have been added to support low frequency operation. The gain and the return loss of this circuit are shown in **Figure 128**.

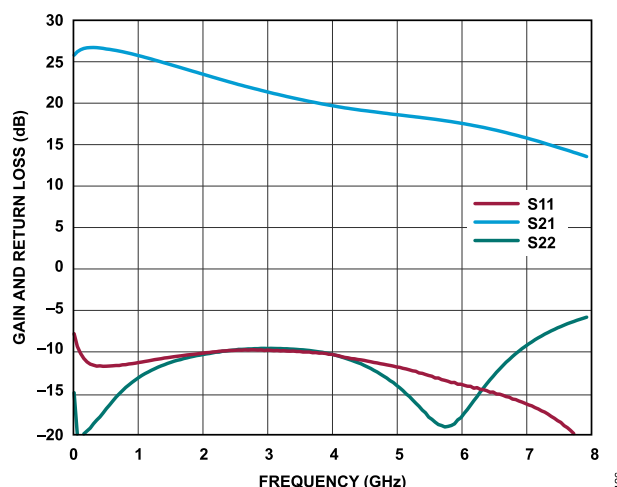


Figure 128. Gain and Return Loss vs. Frequency of 10kHz to 8GHz Application Circuit, $V_{DD} = 5V$, $I_{DQ} = 90\text{mA}$, and $R_{BIAS} = 835\Omega$

Further adjustments can be made to the external components of the device to operate at even lower frequencies. Specifically, the DC blocking capacitor values can be increased because these components are the limiting factor causing the low frequency cutoff.

APPLICATIONS INFORMATION

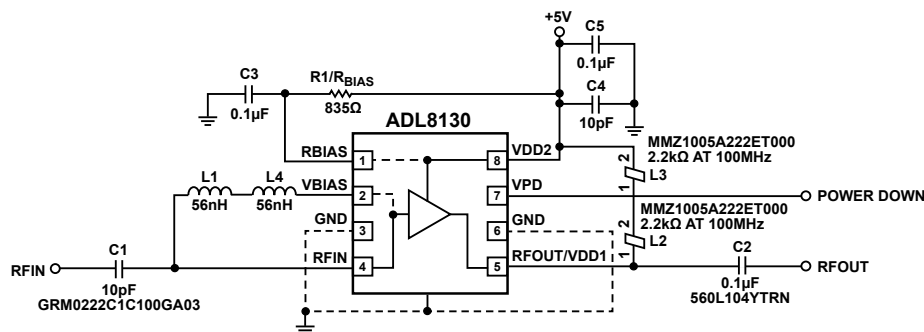


Figure 129. Typical Application Circuit for Operation from 10kHz to 8GHz

Overdrive Recovery Optimization

The overdrive recovery performance of the 10MHz to 8GHz circuit (see [Figure 130](#)) can be improved by adjusting the C1 value shown in [Figure 131](#). [Figure 121](#) is the overdrive recovery time performance comparison of the baseline [ADL8130-EVALZ](#) configuration vs. the optimized ADL8130-EVALZ. The reduced value of the input DC blocking capacitor, C1, has the most impact on the improved overdrive recovery.

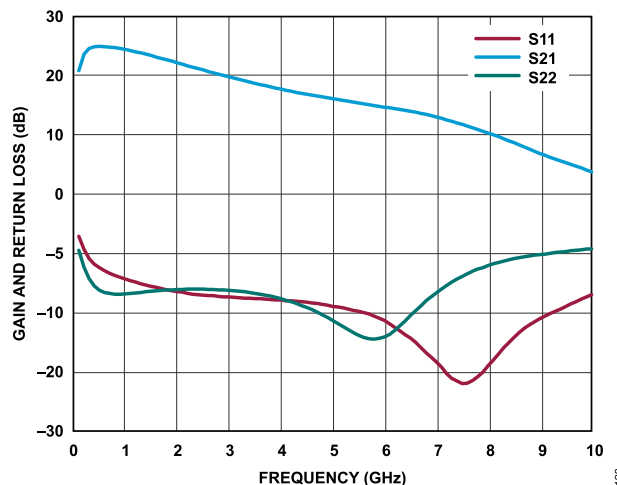
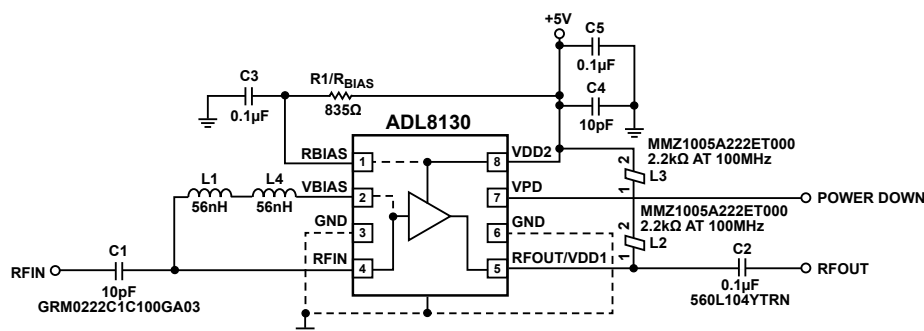
Figure 130. Gain and Return Loss vs. Frequency for Overdrive Recovery Time Optimized Circuit, 0.1GHz to 10GHz, $V_{DD} = 5V$, $R_{BIAS} = 835\Omega$ 

Figure 131. Application Circuit for Optimized Overdrive Recovery Time

APPLICATIONS INFORMATION

Recommended Power Management Circuit

Figure 132 shows a recommended power management circuit for the ADL8130. The **LT8607** step-down regulator is used to step down a 12V rail to 4.5V, which is then applied to the **LT3042** low dropout (LDO) linear regulator to generate a low noise 3.3V output. Even though the circuit shown in **Figure 132** has an input voltage (V_{IN}) of 12V, the input range to the LT8607 can be as high as 42V.

The 4.5V regulator output of the LT8607 is set by the R2 and R3 resistors, according to the following equation:

$$R2 = R3((V_{OUT}/0.778V) - 1), \text{ where } V_{OUT} \text{ is the output voltage.}$$

The switching frequency (f_{SW}) is set to 2MHz by the 18.2k Ω resistor (R1) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2MHz to 2.200MHz.

The V_{OUT} of the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$$V_{OUT} = 100\mu A \times R4$$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 3.3V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%). Therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 3.3V output to give a convenient 0V to 3.6V voltage range. **Table 13** provides the recommended resistor values for operation at 3.6V to 3V.

Table 13. Recommended Resistor Values for Operating at 3.6V to 3V

LDO V_{OUT} (V)	R4 (k Ω)	R7 (k Ω)	R8 (k Ω)
3.6	36.5	332	30.1
3.3	33.1	301	30.1
3	30.1	267	30.1

The LT8607 can source a maximum current of 750mA, and the LT3042 can source a maximum current of 200mA. If the 5V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The **LT8608** and **LT8609** step-down regulators can source a maximum current to 1.5A and 3A, respectively, and these devices are pin compatible with the LT8607. The **LT3045** linear regulator, which is pin compatible with LT3042, can source a maximum current to 500mA.

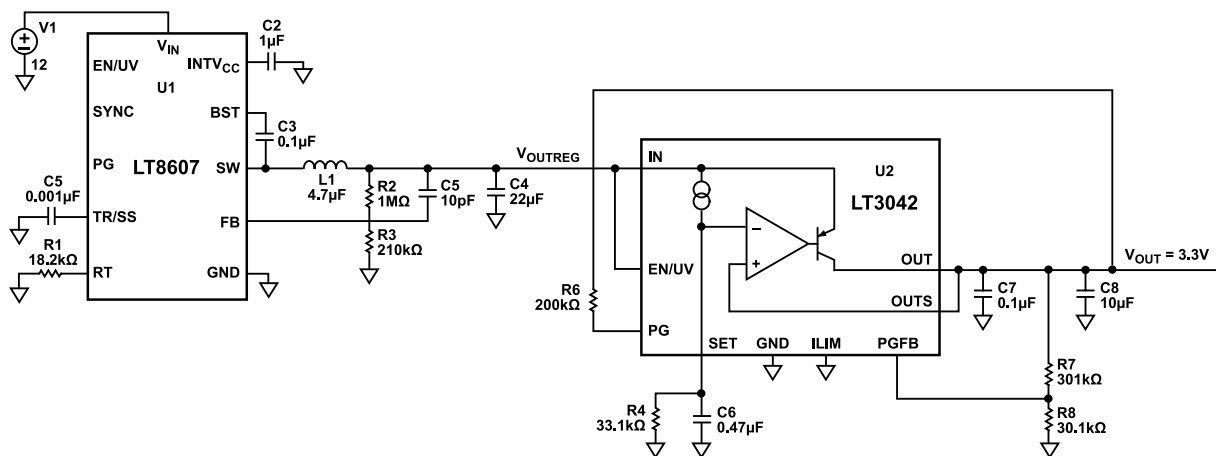


Figure 132. Recommended Power Management Circuit

OUTLINE DIMENSIONS

PACKAGE DRAWING (OPTION)	PACKAGE TYPE	PACKAGE DESCRIPTION
CP-8-30	LFCSP	8-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

Ordering Guide

MODEL ^{1, 2}	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE OPTION
ADL8130ACPZN	-55°C to +125°C	8-Lead LFCSP, 2mm × 2mm × 0.85mm	Tape, 1	CP-8-30
ADL8130ACPZN-R7	-55°C to +125°C	8-Lead LFCSP, 2mm × 2mm × 0.85mm	Reel, 3000	CP-8-30

- ¹ Z = RoHS-Compliant Part.
- ² The lead finish of this model is nickel palladium gold.

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