1GHz to 20GHz, Low Noise Amplifier with Integrated Temperature Sensor and Enable Function

FEATURES

- Single positive supply: 3.3V and I_{DQ} of 55mA
- RBIAS drain current adjustment pin
- Integrated temperature sensor
- Integrated enable and disable function
- Gain: 15dB typical from 10GHz to 17GHz
- OIP3: 29dBm typical from 10GHz to 17 GHz
- Noise figure: 2.1dB typical from 10GHz to 17GHz
- Extended operating temperature range: −55°C to +125°C
- RoHS-compliant, 2mm × 2mm, 8-lead LFCSP

APPLICATIONS

- Telecommunications
- Test instrumentation
- Military

GENERAL DESCRIPTION

The ADL8124 is a highly integrated, 1GHz to 20GHz, low noise amplifier (LNA). On-chip features include input and output AC coupling capacitors, an integrated bias inductor, an integrated temperature sensor, and an enable or disable pin (VENBL).

The typical gain and noise figure are 15dB and 2.1dB, respectively, from 10GHz to 17GHz. The output power for 1dB compression (OP1dB), output third-order intercept (OIP3), and output second-order intercept (OIP2) are 15dBm, 29dBm, and 43dBm, respectively, from 10GHz to 17GHz. The quiescent drain current (I_{DQ}), which can be adjusted, is 55mA operating from a 3.3V supply voltage (V_{DD}). Operation at 5V is also supported.

The ADL8124 is fabricated on a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT) process. This device is housed in an RoHS-compliant, 2mm × 2mm, 8-lead LFCSP package and is specified for operation over an extended temperature range of −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

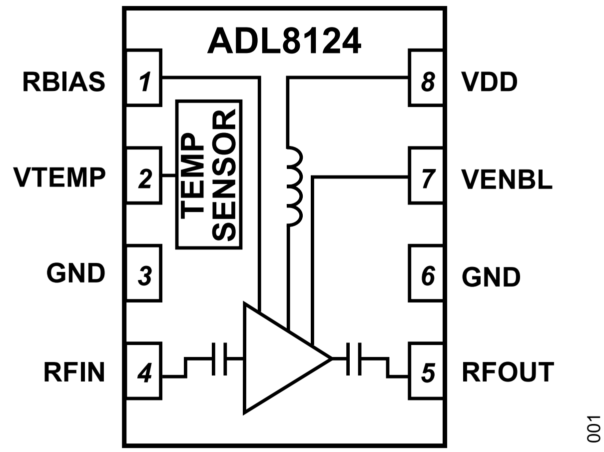

Figure 1. Functional Block Diagram

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

9/2025—Revision 0: Initial Version

SPECIFICATIONS

1GHz TO 2GHz FREQUENCY RANGE

V_{DD} = 3.3V, I_{DQ} = 55mA, bias resistance (R_{BIAS}) = 1540Ω, VENBL voltage (V_{ENBL}) = 3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 1GHz to 2GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	1		2	GHz	
GAIN (S21)	11	13		dB	
Gain Variation over Temperature		0.0077		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input (S11)		10		dB	
Output (S22)		8		dB	
OUTPUT					
OP1dB	12.5	14.5		dBm	
Saturated Power (P_{SAT})		15.5		dBm	
OIP3		28.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 0dBm
OIP2		33		dBm	Measurement taken at P_{OUT} per tone = 0dBm
POWER ADDED EFFICIENCY (PAE)		17.5		%	Measured at P_{SAT}

2GHz TO 10GHz FREQUENCY RANGE

V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω, V_{ENBL} = 3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 2GHz to 10GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2		10	GHz	
GAIN	11.5	13.5		dB	
Gain Variation over Temperature		0.0116		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input (S11)		11		dB	
Output (S22)		13.5		dB	
OUTPUT					
OP1dB	13.5	15.5		dBm	
Saturated Power (P_{SAT})		16		dBm	
OIP3		29.5		dBm	Measurement taken at P_{OUT} per tone = 0dBm
OIP2		28.5		dBm	Measurement taken at P_{OUT} per tone = 0dBm
POWER ADDED EFFICIENCY (PAE)		20.5		%	Measured at P_{SAT}

SPECIFICATIONS

10GHz TO 17GHz FREQUENCY RANGE

V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω, V_{ENBL} = 3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 10GHz to 17GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	10		17	GHz	
GAIN	13	15		dB	
Gain Variation over Temperature		0.0163		dB/°C	
NOISE FIGURE		2.1		dB	
RETURN LOSS					
Input (S11)		12		dB	
Output (S22)		13		dB	
OUTPUT					
OP1dB	13	15		dBm	
Saturated Power (P_{SAT})		16.5		dBm	
OIP3		29		dBm	Measurement taken at P_{OUT} per tone = 0dBm
OIP2		43		dBm	Measurement taken at P_{OUT} per tone = 0dBm
POWER ADDED EFFICIENCY (PAE)		21.5		%	Measured at P_{SAT}

17GHz TO 20GHz FREQUENCY RANGE

V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω, V_{ENBL} = 3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 4. 17GHz to 20GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	17		20	GHz	
GAIN	13	15		dB	
Gain Variation over Temperature		0.012		dB/°C	
NOISE FIGURE		2.5		dB	
RETURN LOSS					
Input		13.5		dB	
Output		11.5		dB	
OUTPUT					
OP1dB		11.5		dBm	
P_{SAT}		14		dBm	
OIP3		26		dBm	Measurement taken at P_{OUT} per tone = 0dBm
OIP2		60		dBm	Measurement taken at P_{OUT} per tone = 0dBm
PAE		14		%	Measured at P_{SAT}

SPECIFICATIONS

DC SPECIFICATIONS

Table 5. DC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					
Enable					
I_{DQ} = Amplifier Current (I_{DQ_AMP}) + RBIAS Current (I_{RBIAS})		55		mA	V_{ENBL} = 3.3V
I_{DQ_AMP}		53.6		mA	V_{ENBL} = 3.3V
I_{RBIAS}		1.4		mA	V_{ENBL} = 3.3V
Disable					
$I_{DQ} = I_{DQ\_AMP} + I_{RBIAS}$		6.6		mA	V_{ENBL} = 0V
I_{DQ_AMP}		6.6		mA	V_{ENBL} = 0V
I_{RBIAS}		0		mA	V_{ENBL} = 0V
SUPPLY VOLTAGE					
V_{DD}	2	3.3	6	V	

Table 6. Logic Control (V_{ENBL})

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL CONTROL INPUT					
Low, Amplifier Off State	0		1.1	V	
High, Amplifier On State	1.5		V_{DD}	V	
VENBL Input Current (I_{ENBL})		0.4		mA	V_{ENBL} = 3.3V
SWITCHING TIME					
Amplifier On State Time		29		ns	50% of the V_{ENBL} rising edge to the output envelope at 90%
Amplifier Off State Time		38		ns	50% of the V_{ENBL} falling edge to the output envelope at 10%

Table 7. Temperature Sensor

Parameter	Min	Typ	Max	Unit
VTEMP Voltage (V_{TEMP}) Output Voltage (V_{OUT}), T_{CASE} = 25°C		1.6		V
V_{TEMP} Temperature Coefficient, T_{CASE} = −55°C to +125°C		2.55		mV/°C

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	7.5V
V_{ENBL}	V_{DD}
RF Input Power Survivability (RFIN)	28dBm
Continuous Power Dissipation (P_{DISS})	
T_{CASE} = 85°C	0.9W
T_{CASE} = 125°C	0.46W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance.

Table 9. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-8-30		
T_{CASE} = 25°C	86.1	°C/W
T_{CASE} = 85°C	99.7	°C/W
T_{CASE} = 125°C	108.5	°C/W

1 Thermal resistance varies with operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8124

Table 10. ADL8124, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

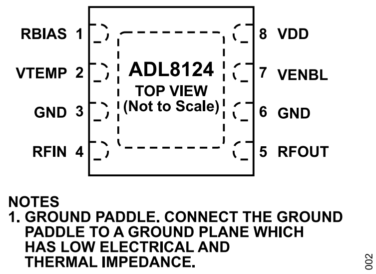

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set I_{DQ}. See the typical application circuit (see Figure 100) and Table 12 to Table 15 for more details. See Figure 7 for the interface schematic.
2	VTEMP	Temperature Sensor Output Voltage. See Figure 5 for the interface schematic.
3, 6	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 3 for the interface schematic.
4	RFIN	RF Input. RFIN is AC-coupled and matched to 50Ω. See Figure 4 for the interface schematic.
5	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50Ω. See Figure 6 for the interface schematic.
7	VENBL	Device Enable. An active high digital signal enables the device, and an active low digital signal disables the device. See Figure 8 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 6 for the interface schematic.
	GROUND PADDLE	Ground Paddle. Connect the ground paddle to a ground plane which has a low electrical and thermal impedance.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

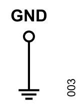

Figure 3. GND Interface Schematic

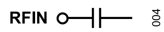

Figure 4. RFIN Interface Schematic

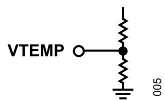

Figure 5. VTEMP Interface Schematic

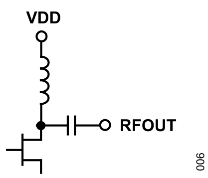

Figure 6. RFOUT and VDD Interface Schematic

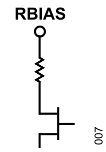

Figure 7. RBIAS Interface Schematic

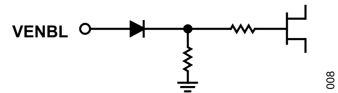

Figure 8. VENBL Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

AMPLIFIER ON STATE (V_{ENBL} = 3.3V)

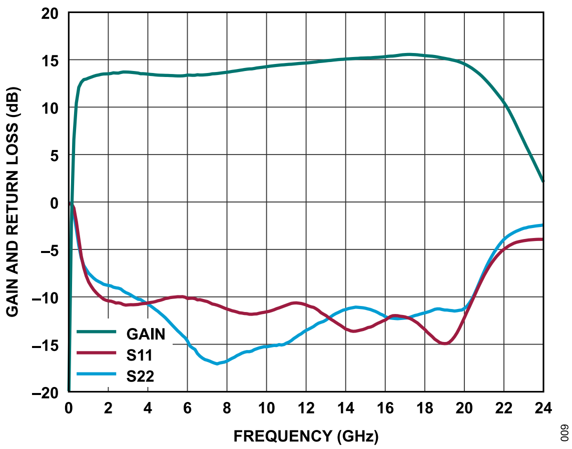

Figure 9. Broadband Gain and Return Loss vs. Frequency, 10MHz to 24GHz, V_{DD} = 3.3V, I_{DQ} = 55mA

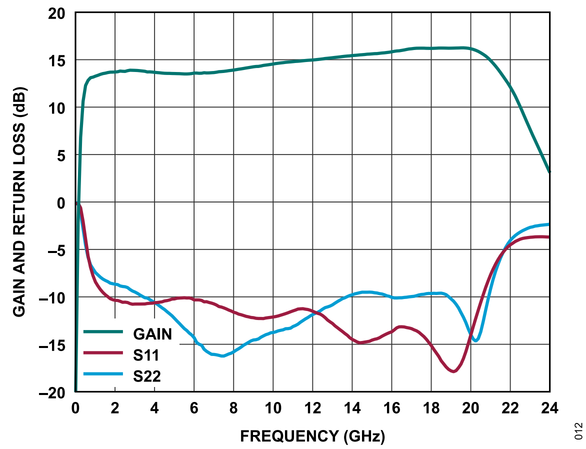

Figure 12. Broadband Gain and Return Loss vs. Frequency, 10MHz to 24GHz, V_{DD} = 5V, I_{DQ} = 85mA

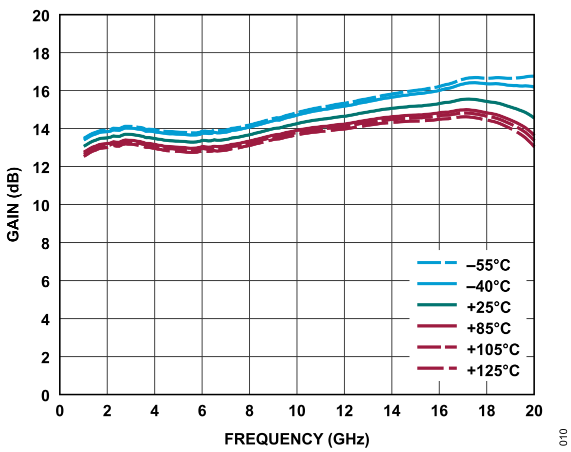

Figure 10. Gain vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

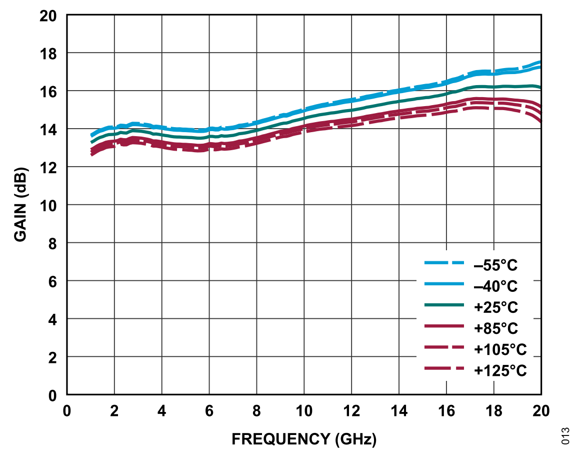

Figure 13. Gain vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

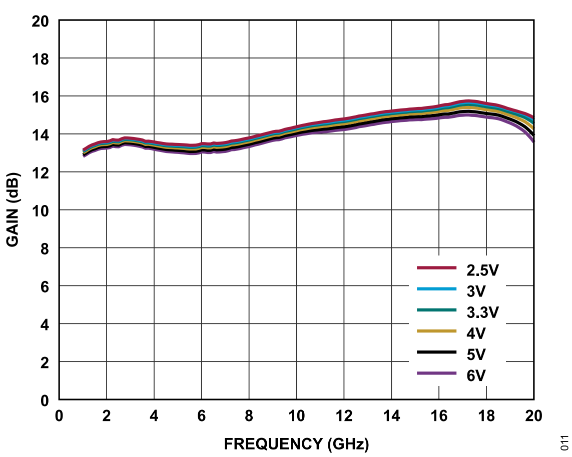

Figure 11. Gain vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

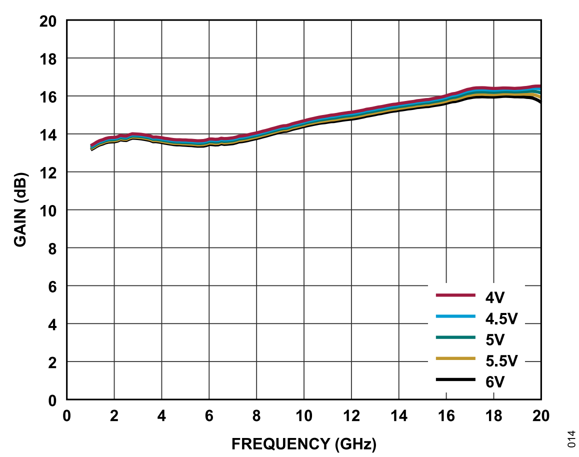

Figure 14. Gain vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

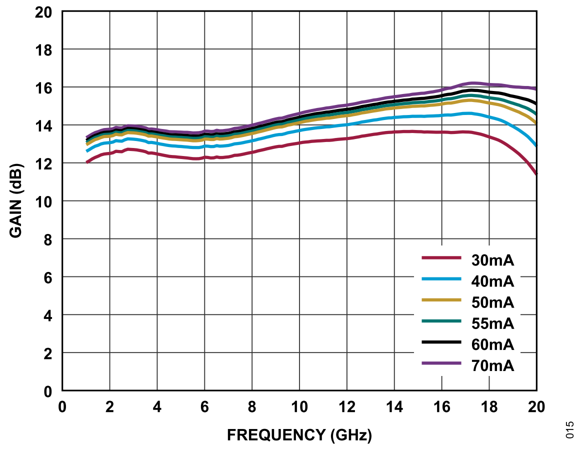

Figure 15. Gain vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

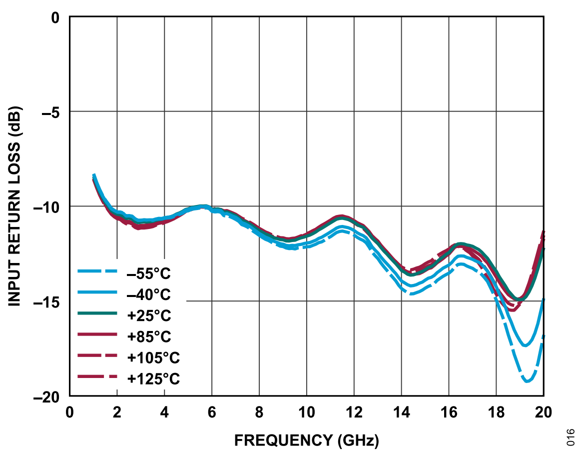

Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

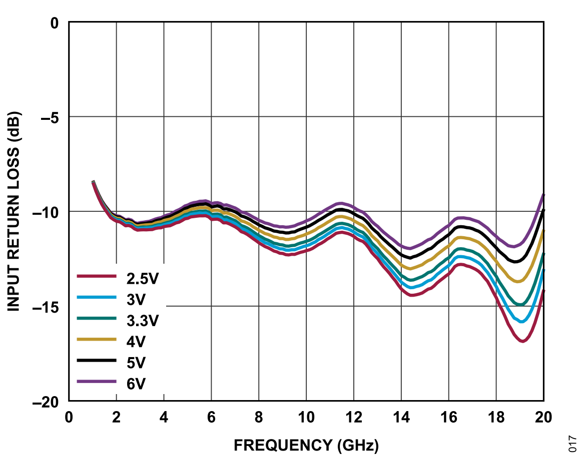

Figure 17. Input Return Loss vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

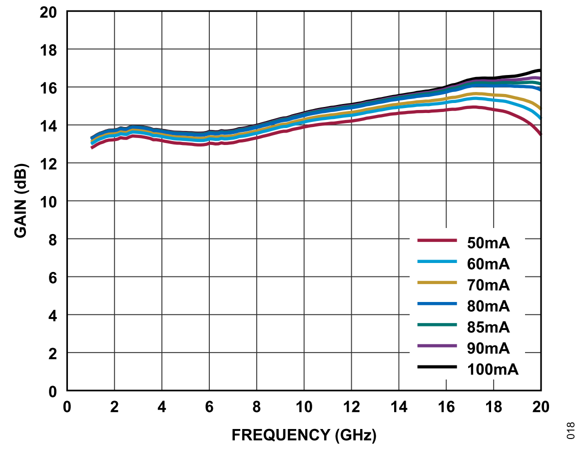

Figure 18. Gain vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

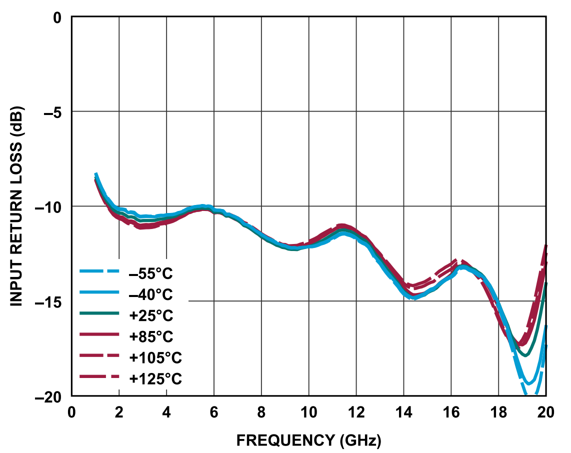

Figure 19. Input Return Loss vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

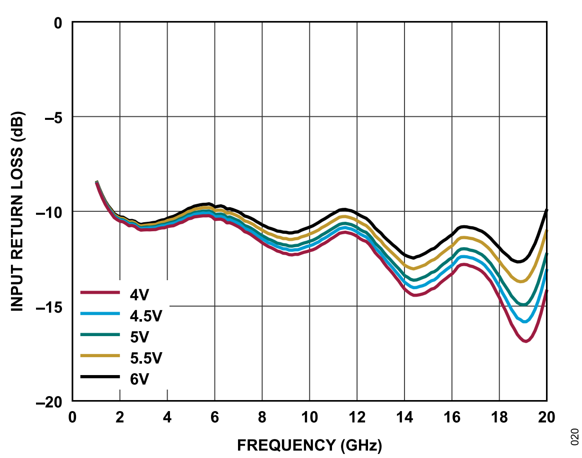

Figure 20. Input Return Loss vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

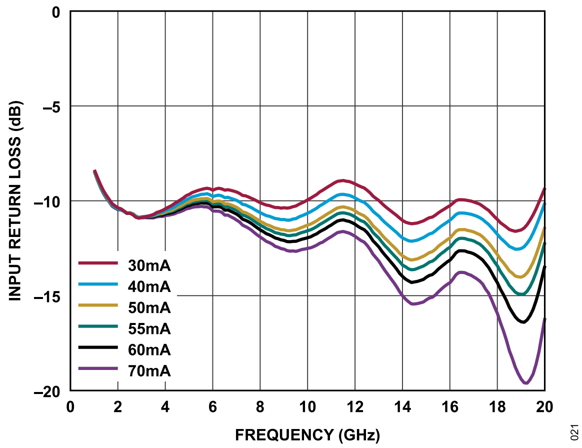

Figure 21. Input Return Loss vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

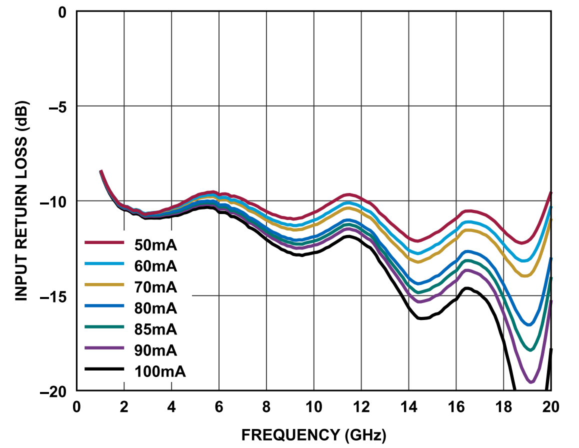

Figure 24. Input Return Loss vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

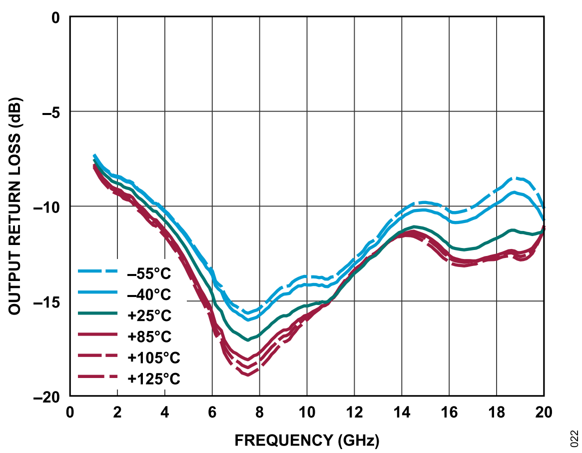

Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

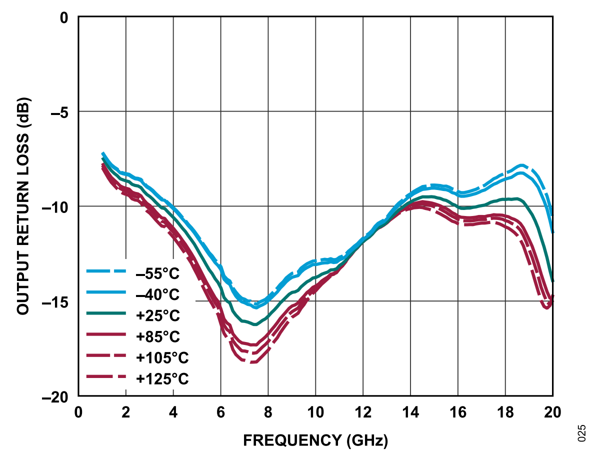

Figure 25. Output Return Loss vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

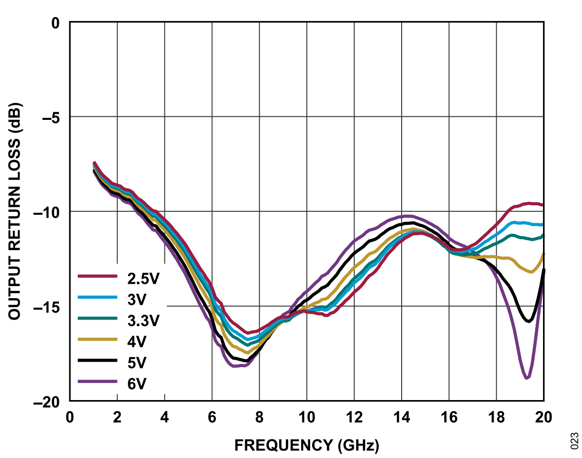

Figure 23. Output Return Loss vs Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

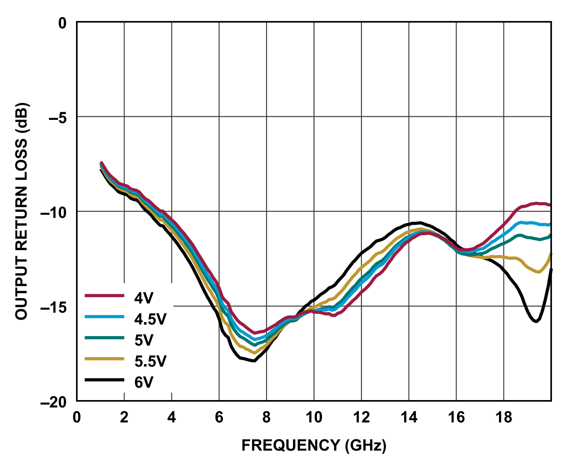

Figure 26. Output Return Loss vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

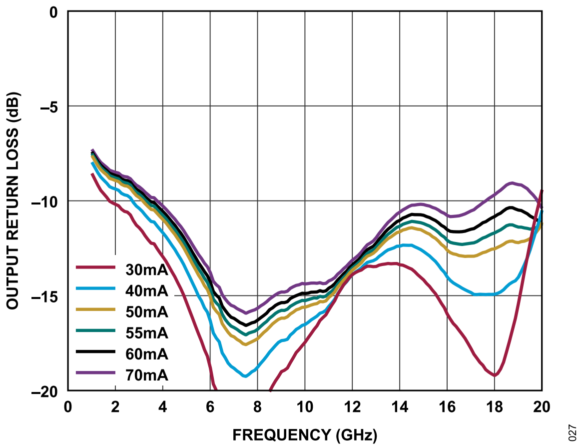

Figure 27. Output Return Loss vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

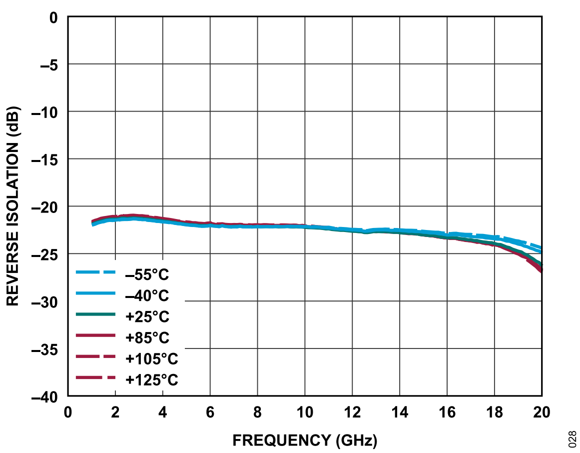

Figure 28. Reverse Isolation vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

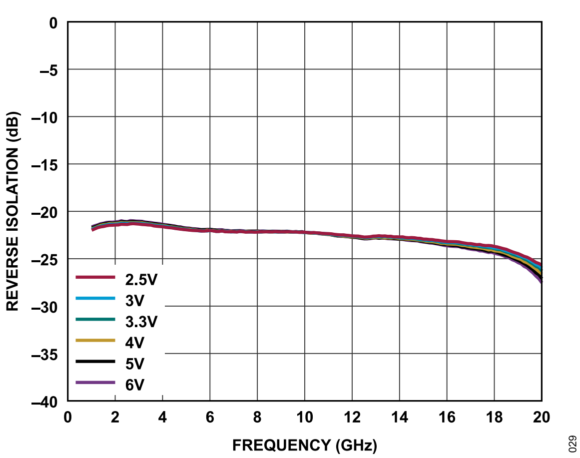

Figure 29. Reverse Isolation vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

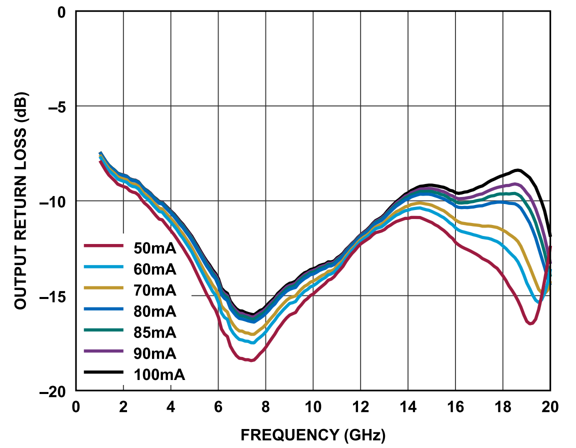

Figure 30. Output Return Loss vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, and V_{DD} = 5V

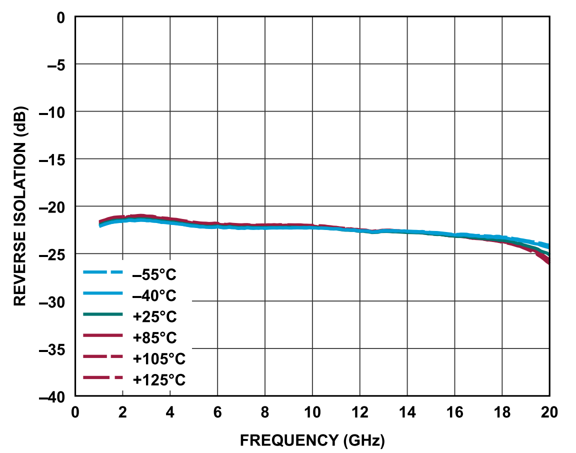

Figure 31. Reverse Isolation vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

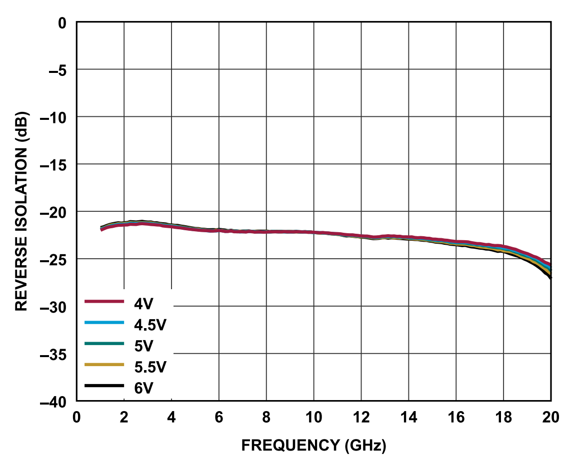

Figure 32. Reverse Isolation vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

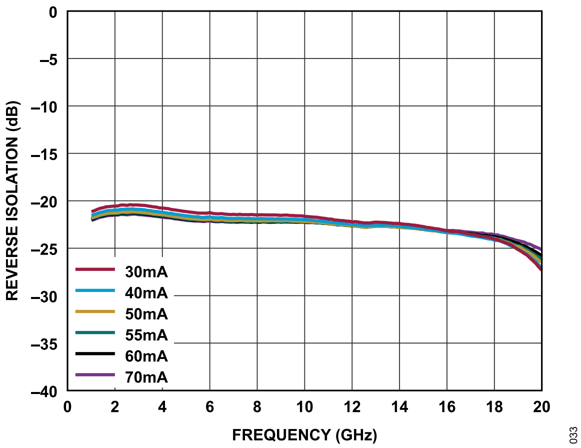

Figure 33. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

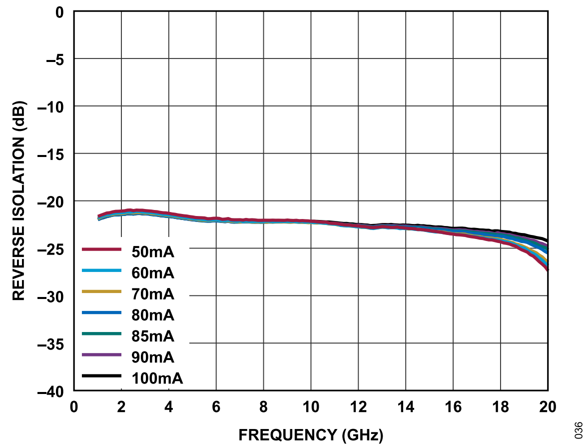

Figure 36. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

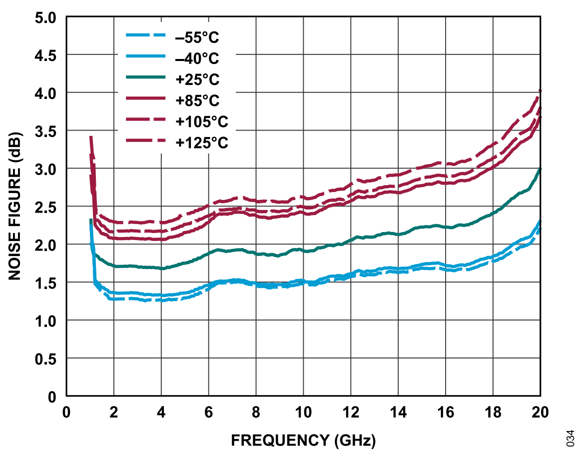

Figure 34. Noise Figure vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

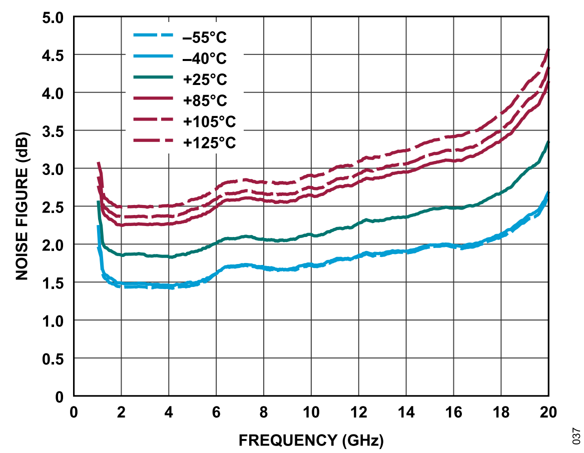

Figure 37. Noise Figure vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

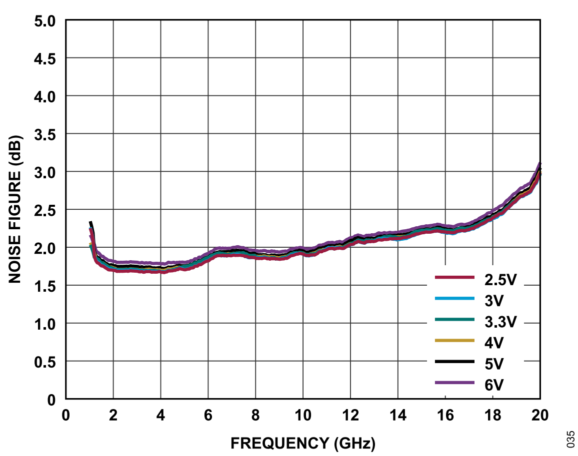

Figure 35. Noise Figure vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

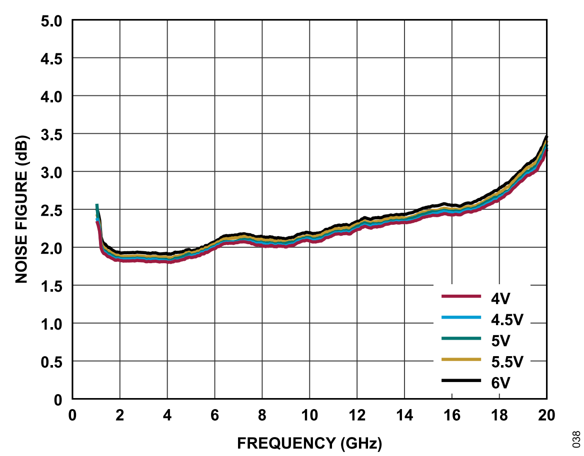

Figure 38. Noise Figure vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

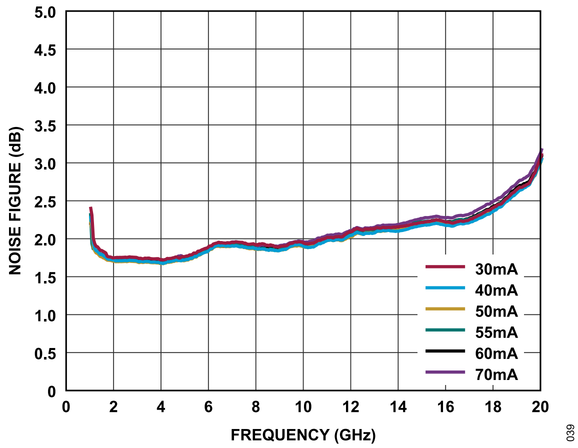

Figure 39. Noise Figure vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

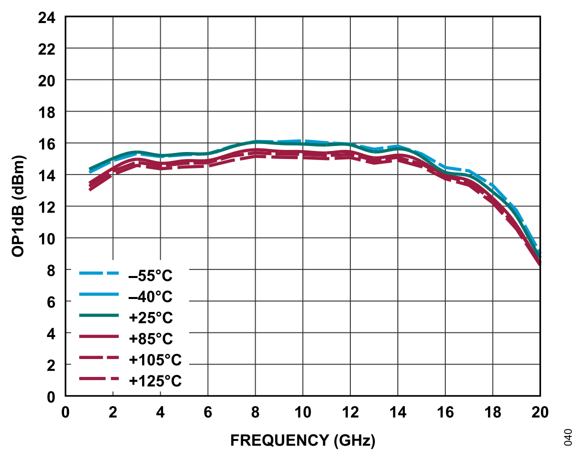

Figure 40. OP1dB vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

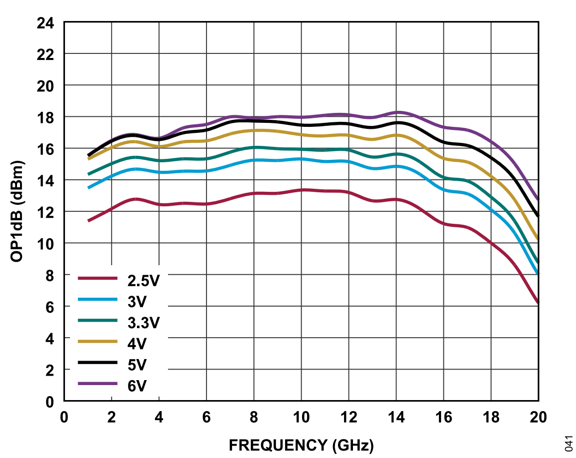

Figure 41. OP1dB vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

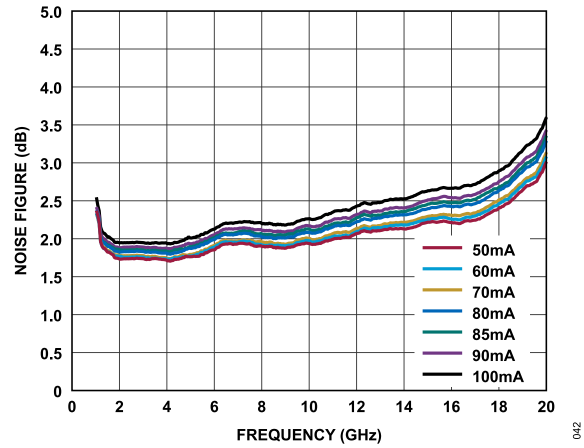

Figure 42. Noise Figure vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

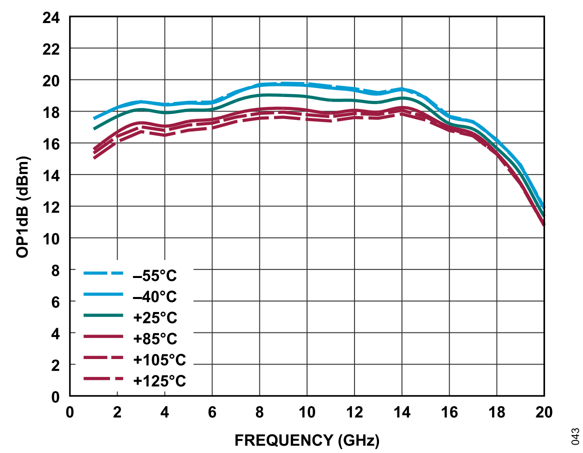

Figure 43. OP1dB vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

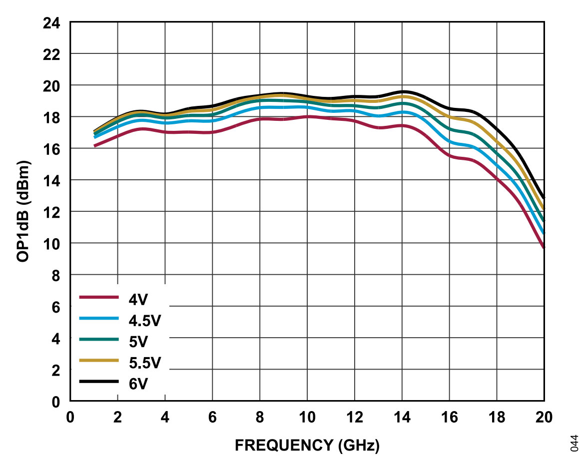

Figure 44. OP1dB vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

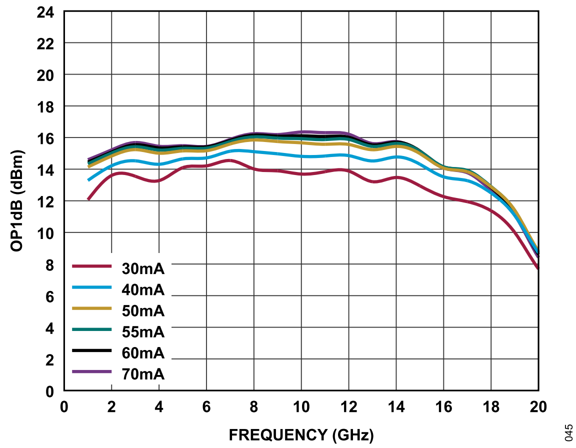

Figure 45. OP1dB vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

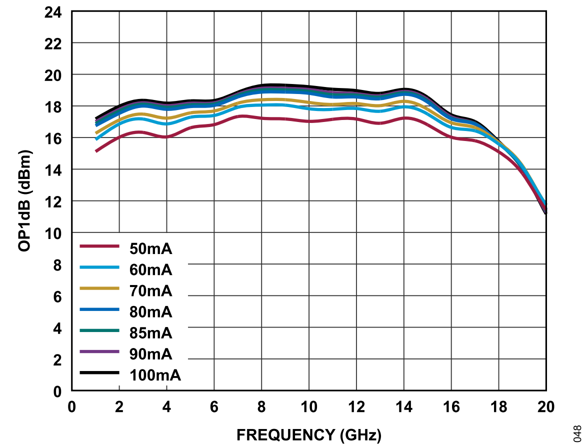

Figure 48. OP1dB vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

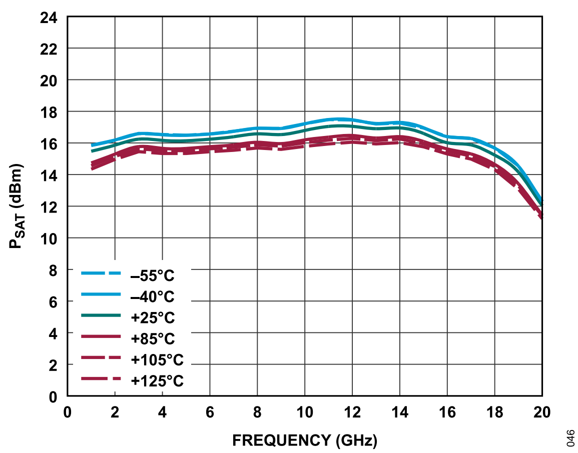

Figure 46. P_{SAT} vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

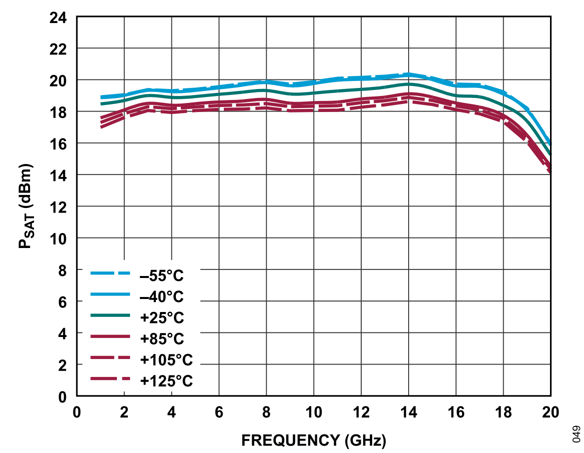

Figure 49. P_{SAT} vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

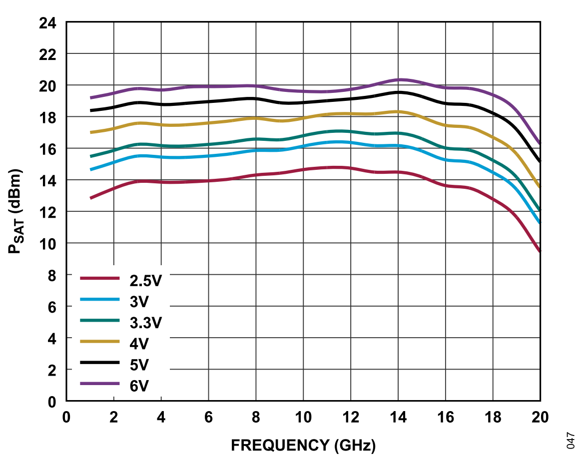

Figure 47. P_{SAT} vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

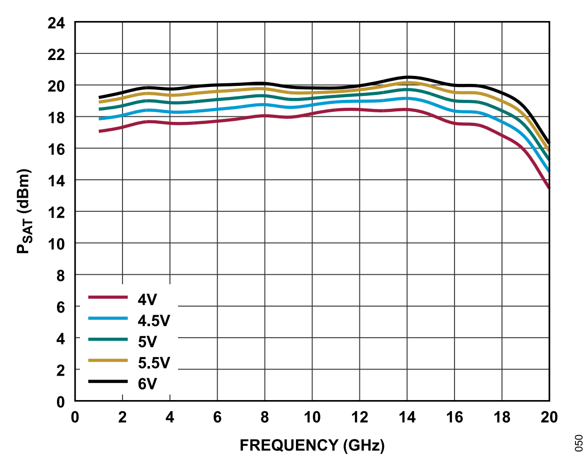

Figure 50. P_{SAT} vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

TYPICAL PERFORMANCE CHARACTERISTICS

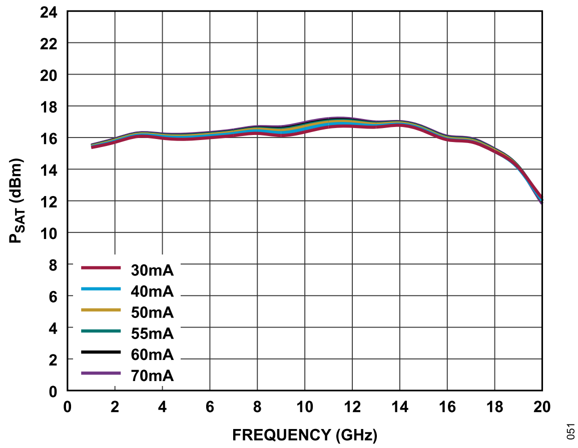

Figure 51. P_{SAT} vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

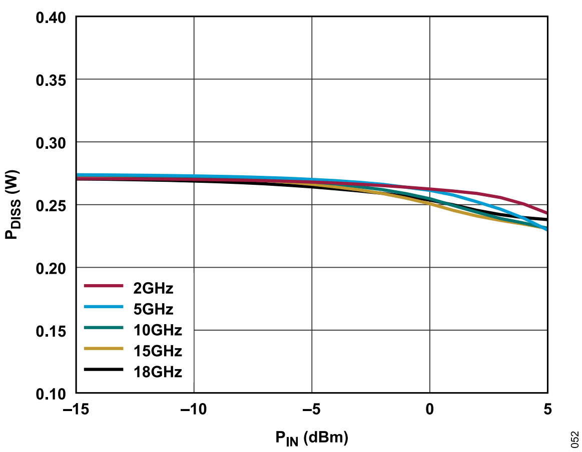

Figure 52. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 3.3V, R_{BIAS} = 1540Ω

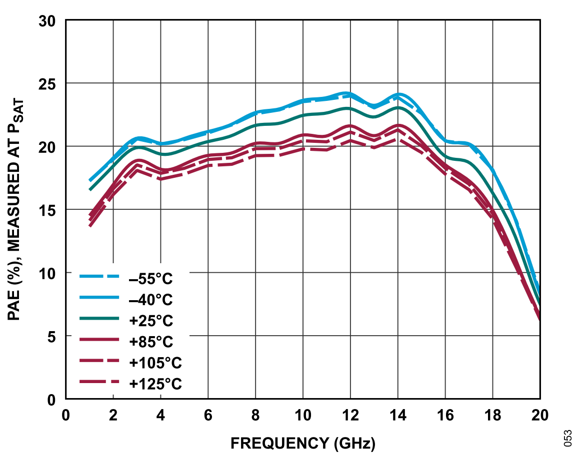

Figure 53. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

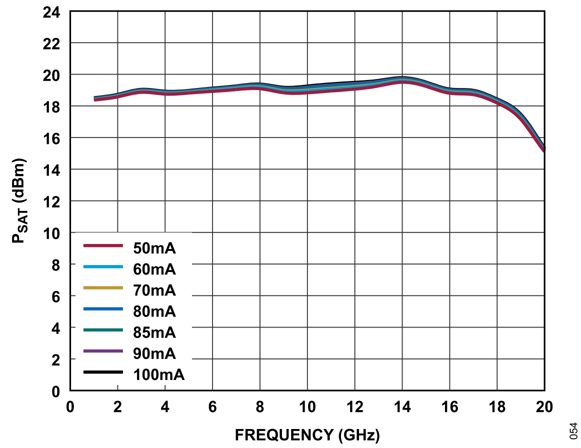

Figure 54. P_{SAT} vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

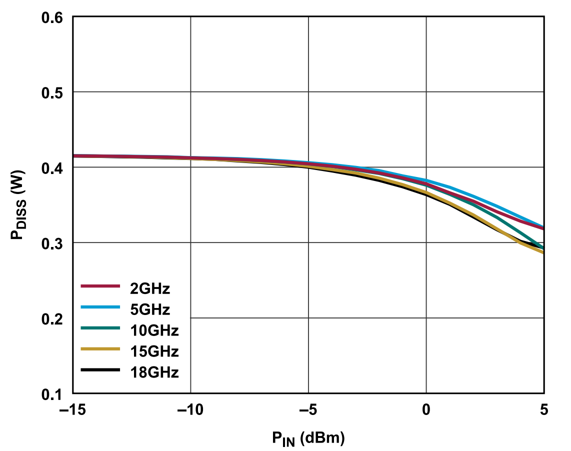

Figure 55. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 5V, R_{BIAS} = 1731Ω

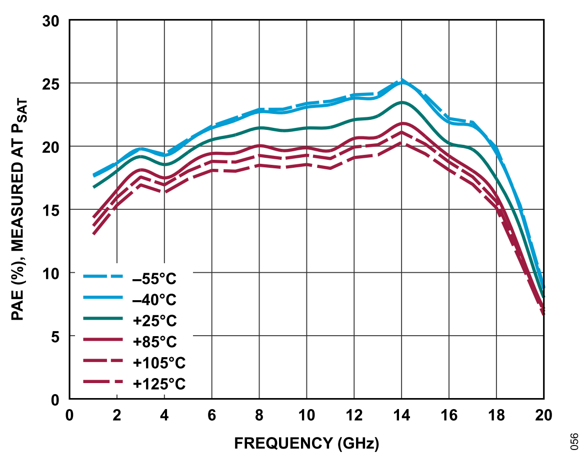

Figure 56. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

TYPICAL PERFORMANCE CHARACTERISTICS

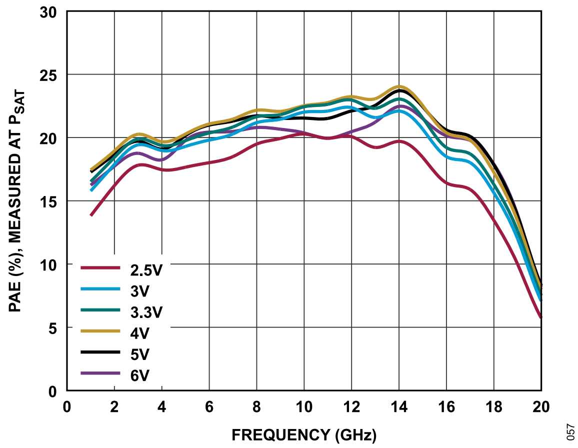

Figure 57. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 55mA

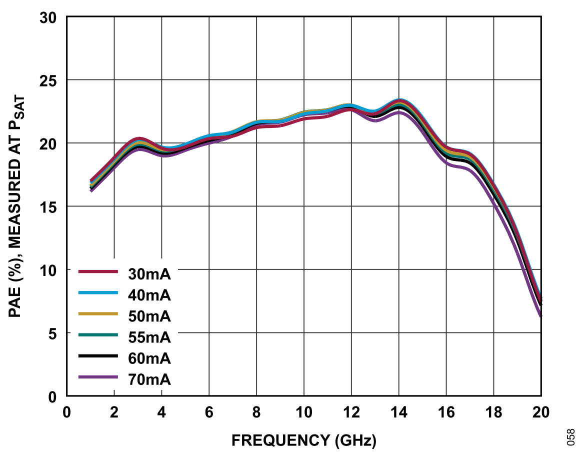

Figure 58. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 3.3V

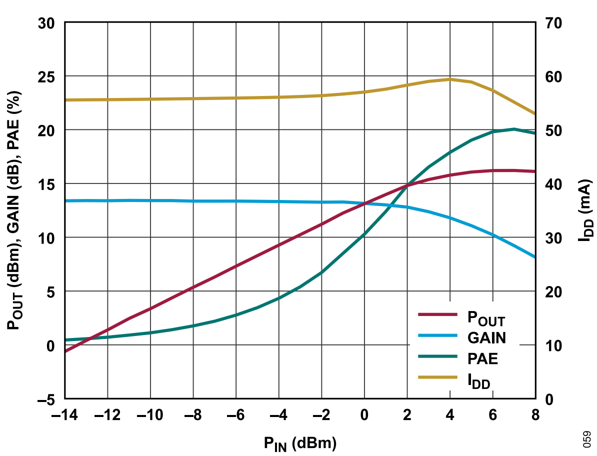

Figure 59. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. P_{IN}, Power Compression at 5GHz, V_{DD} = 3.3V, R_{BIAS} = 1540Ω

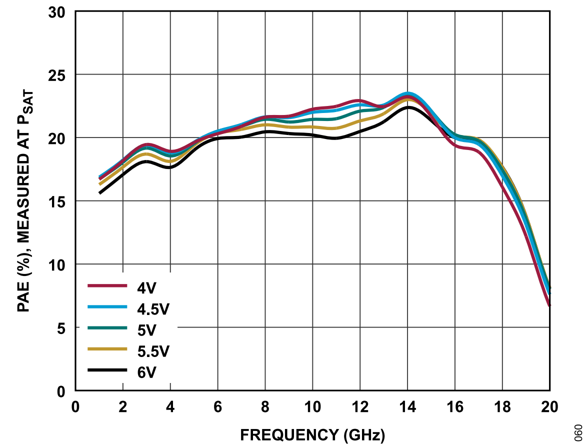

Figure 60. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 1GHz to 20GHz, I_{DQ} = 85mA

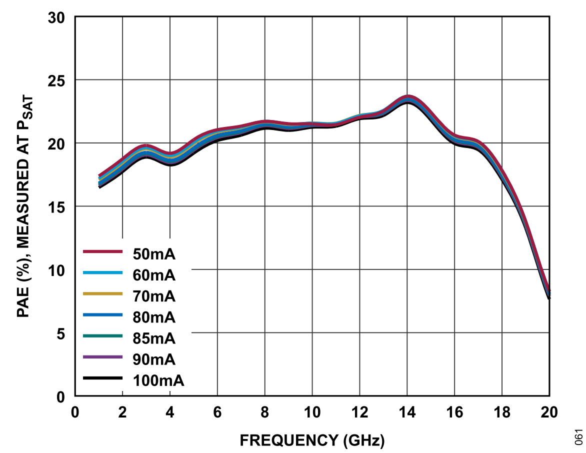

Figure 61. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 1GHz to 20GHz, V_{DD} = 5V

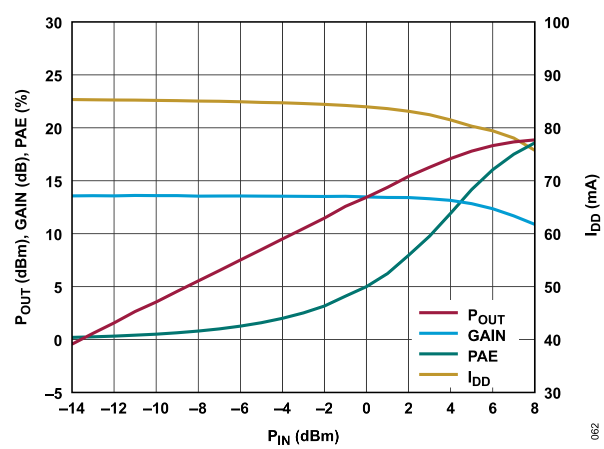

Figure 62. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 5GHz, V_{DD} = 5V, R_{BIAS} = 1731Ω

TYPICAL PERFORMANCE CHARACTERISTICS

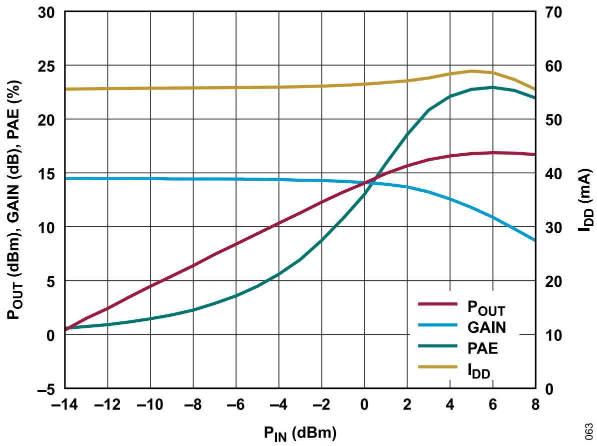

Figure 63. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10GHz, V_{DD} = 3.3V, R_{BIAS} = 1540Ω

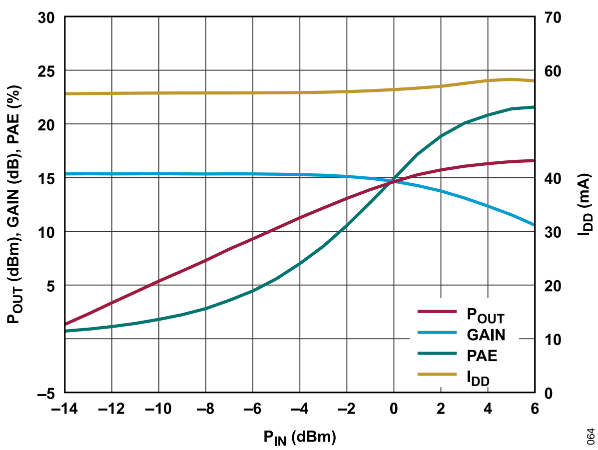

Figure 64. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 15GHz, V_{DD} = 3.3V, R_{BIAS} = 1540Ω

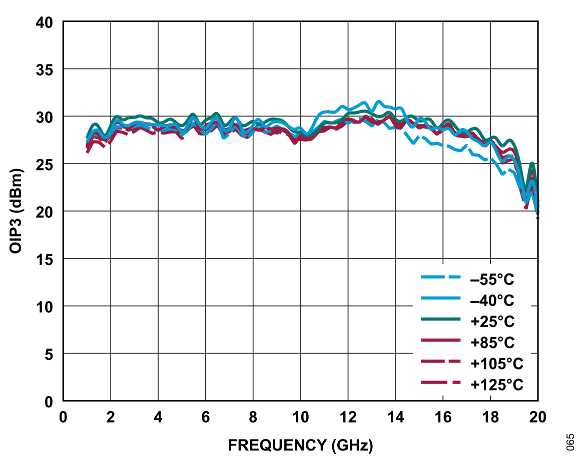

Figure 65. OIP3 vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω, P_{OUT} per Tone = 0dBm

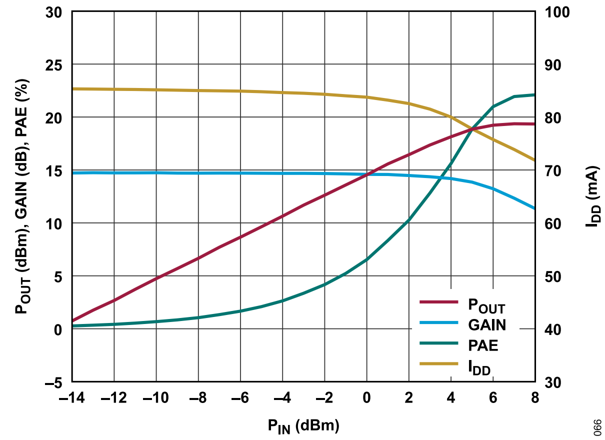

Figure 66. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10GHz, V_{DD} = 5V, R_{BIAS} = 1731Ω

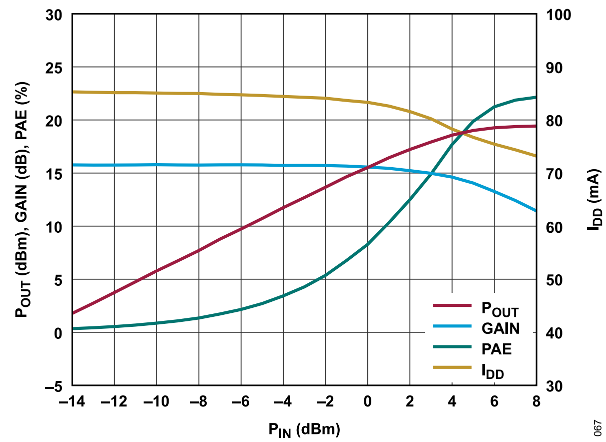

Figure 67. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 15GHz, V_{DD} = 5V, R_{BIAS} = 1731Ω

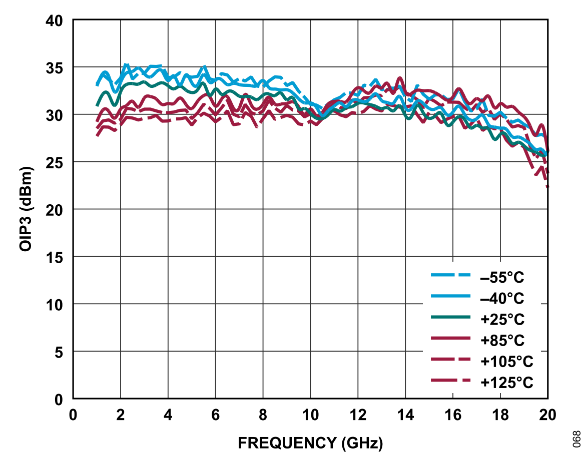

Figure 68. OIP3 vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω, P_{OUT} per Tone = 0dBm

TYPICAL PERFORMANCE CHARACTERISTICS

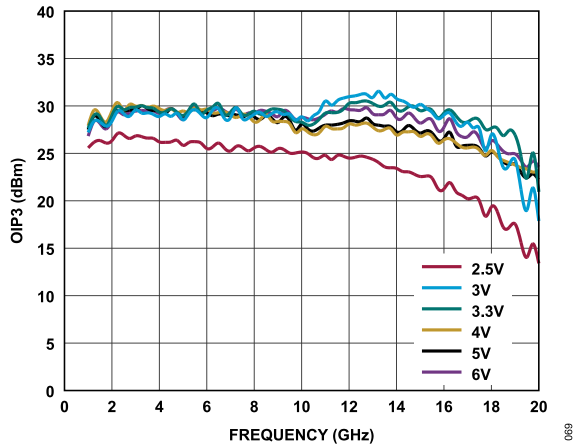

Figure 69. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 55mA, P_{OUT} per Tone = 0dBm

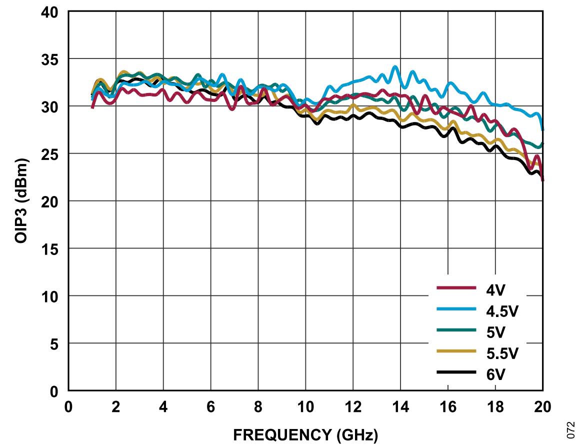

Figure 72. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 85mA, P_{OUT} per Tone = 0dBm

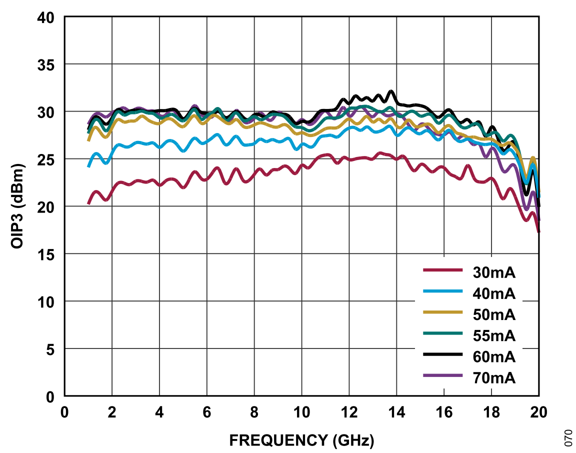

Figure 70. OIP3 vs. Frequency for Various I_{DQ} Values, V_{DD} = 3.3V, P_{OUT} per Tone = 0dBm

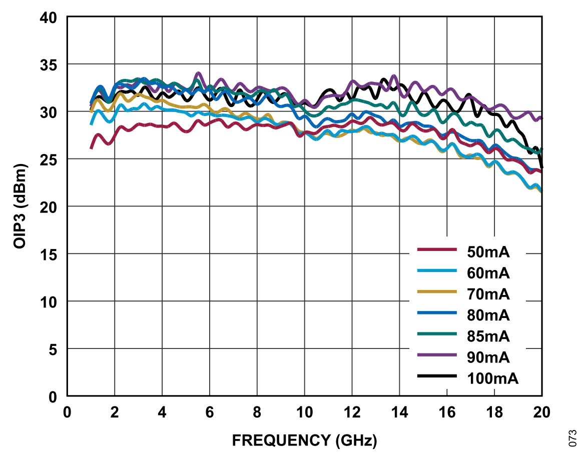

Figure 73. OIP3 vs. Frequency for Various I_{DQ} Values, V_{DD} = 5V, P_{OUT} per Tone = 0dBm

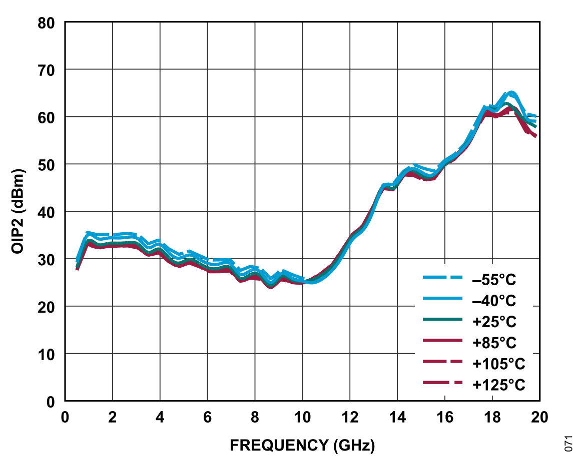

Figure 71. OIP2 vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω, P_{OUT} per Tone = 0dBm

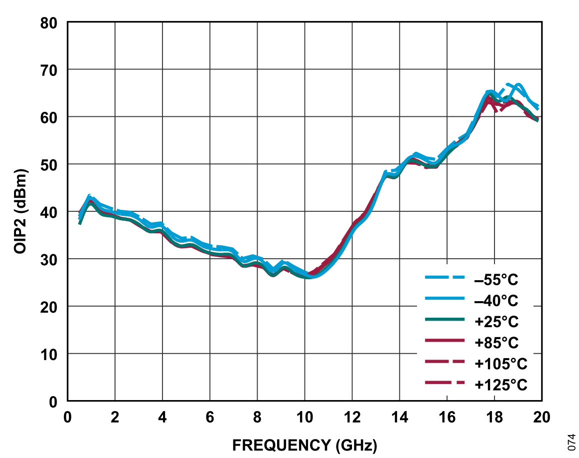

Figure 74. OIP2 vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω, P_{OUT} per Tone = 0dBm

TYPICAL PERFORMANCE CHARACTERISTICS

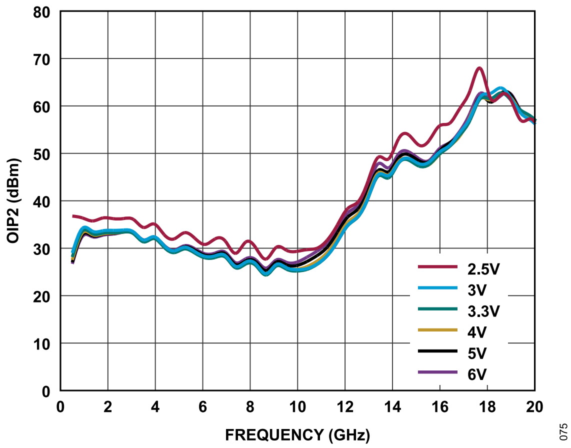

Figure 75. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 55mA, P_{OUT} per Tone = 0dBm

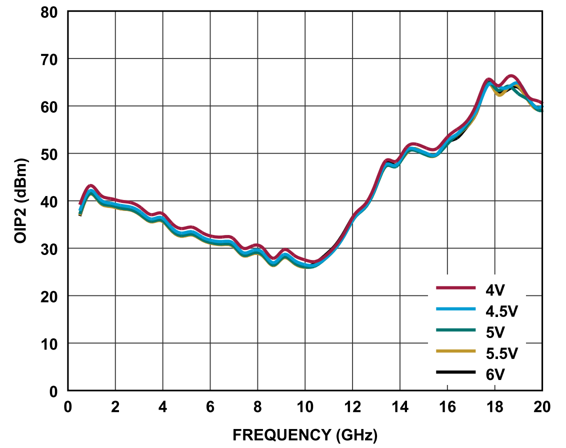

Figure 78. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 85mA, P_{OUT} per Tone = 0dBm

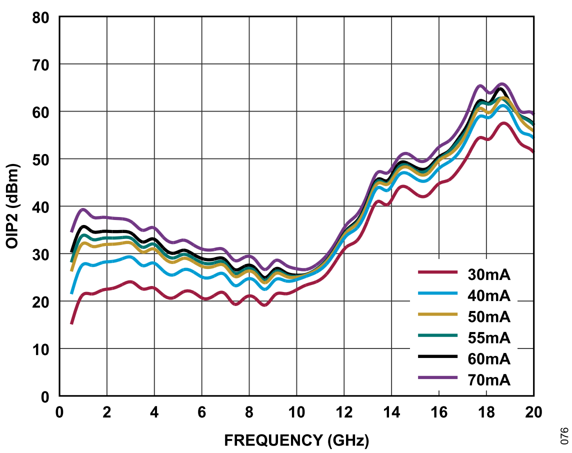

Figure 76. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 3.3V, P_{OUT} per Tone = 0dBm

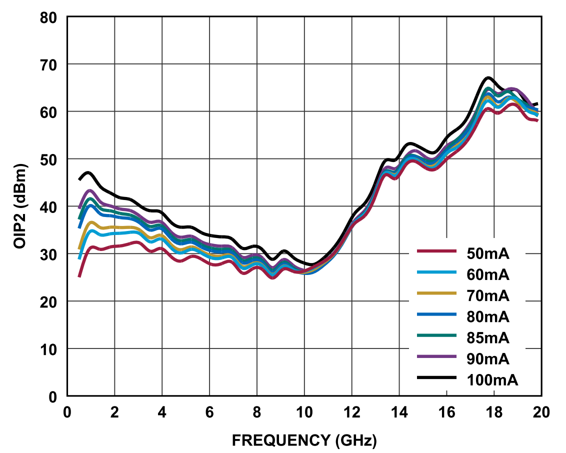

Figure 79. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 5V, P_{OUT} per Tone = 0dBm

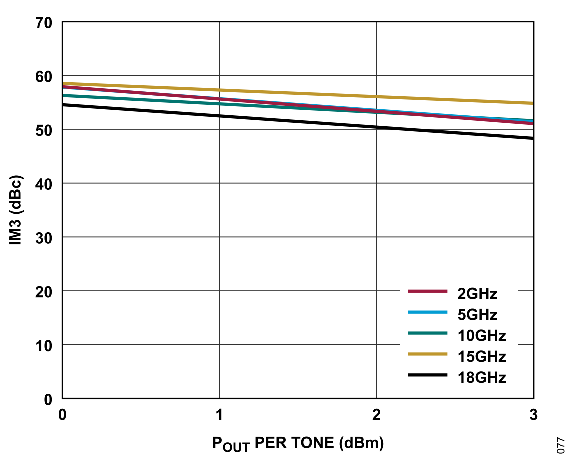

Figure 77. Output IM3 vs P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.3V, R_{BIAS} = 1540Ω

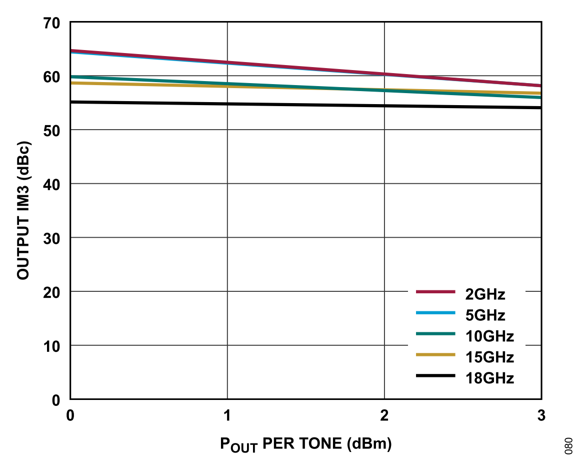

Figure 80. Output IM3 vs P_{OUT} per Tone for Various Frequencies, V_{DD} = 5V, R_{BIAS} = 1731Ω

TYPICAL PERFORMANCE CHARACTERISTICS

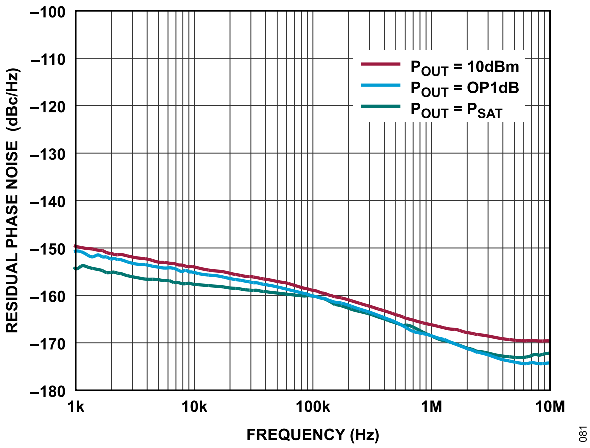

Figure 81. Residual Phase Noise vs. Frequency at 5GHz for Various P_{OUT} Values, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

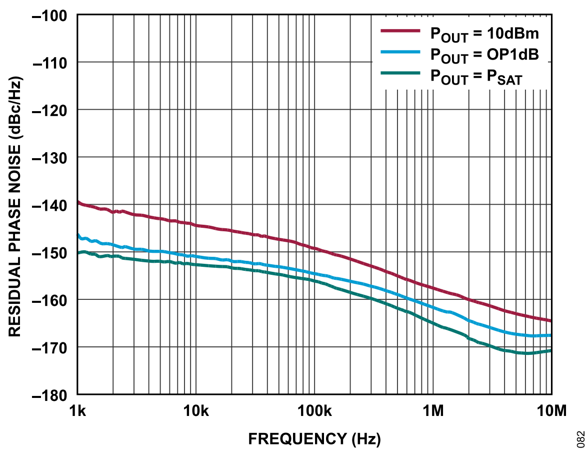

Figure 82. Residual Phase Noise vs. Frequency at 15GHz for Various P_{OUT} Values, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

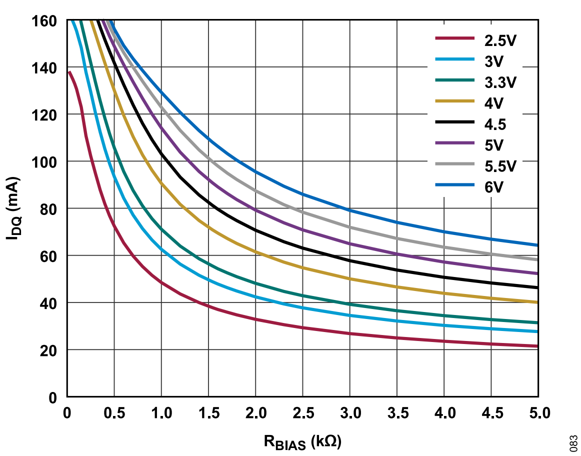

Figure 83. I_{DQ} vs. R_{BIAS} for Various Supply Voltages, 0Ω to 5kΩ

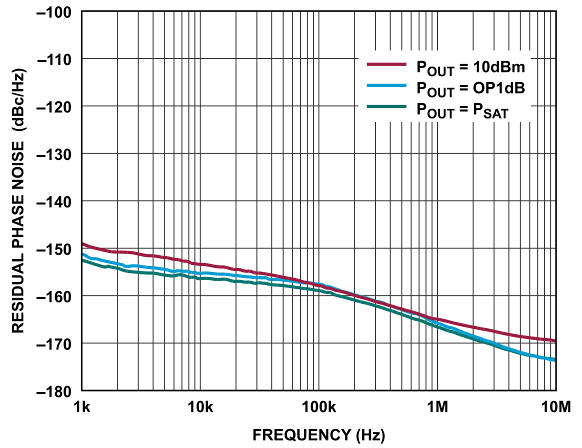

Figure 84. Residual Phase Noise vs. Frequency at 10GHz for Various P_{OUT} Values, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

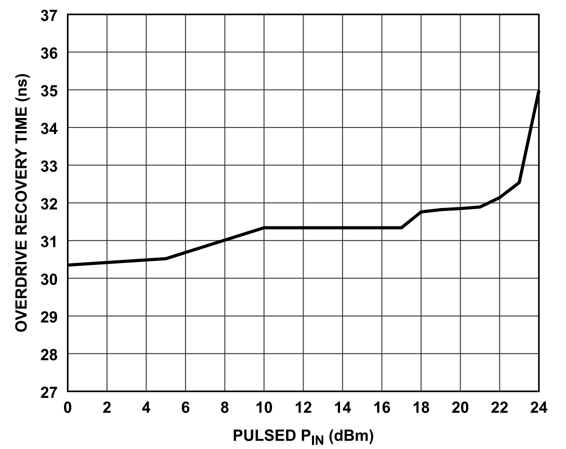

Figure 85. Overdrive Recovery Time vs. Pulsed P_{IN} at 8GHz, Recovery to Within 90% of Small Signal Gain Value, V_{DD} = 5V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

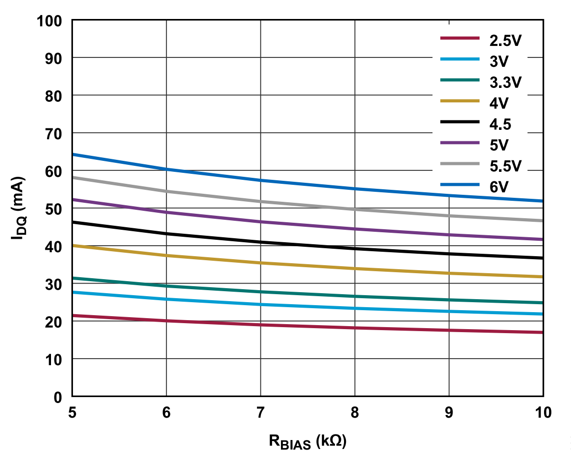

Figure 86. I_{DQ} vs. R_{BIAS} for Various Supply Voltages, 5kΩ to 10kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

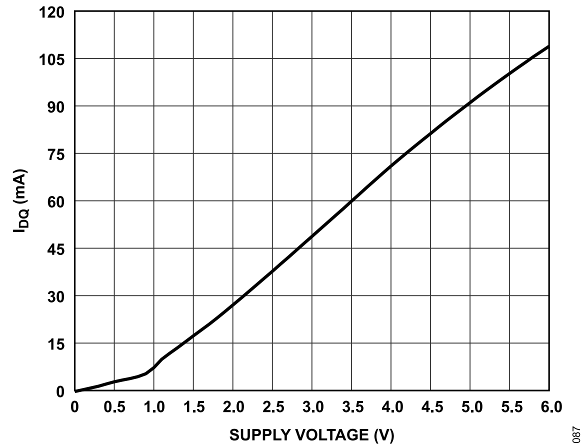

Figure 87. I_{DQ} vs. Supply Voltage, R_{BIAS} = 1540Ω

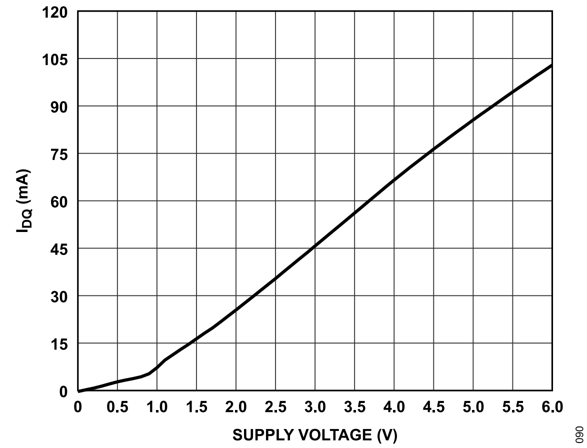

Figure 90. I_{DQ} vs. Supply Voltage, R_{BIAS} = 1731Ω

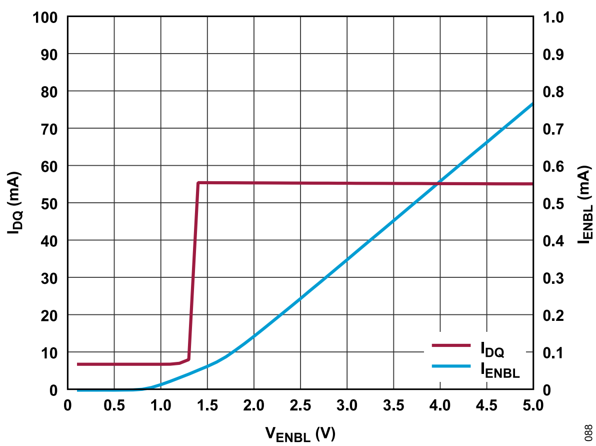

Figure 88. I_{DQ} and I_{ENBL} vs. V_{ENBL}, R_{BIAS} = 1540Ω

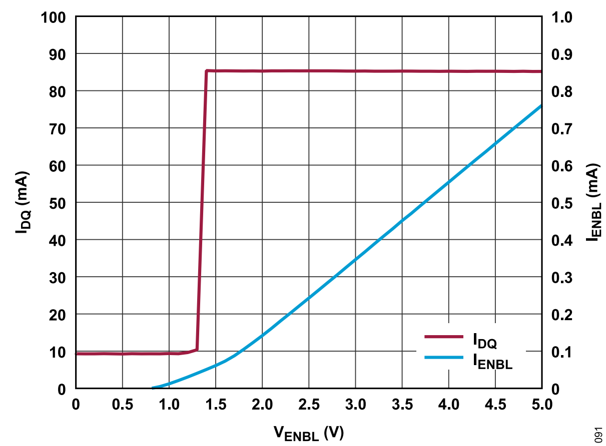

Figure 91. I_{DQ} and I_{ENBL} vs. V_{ENBL}, R_{BIAS} = 1731Ω

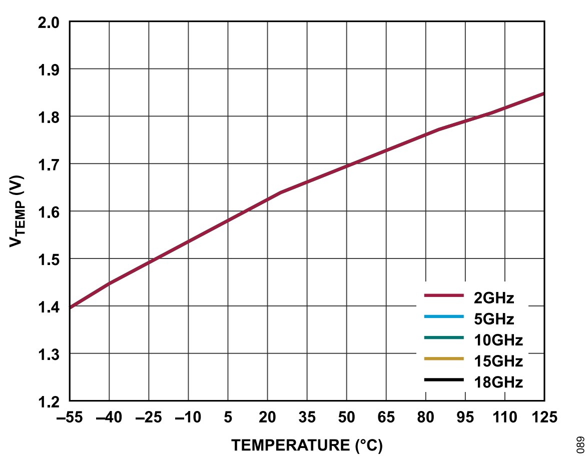

Figure 89. V_{TEMP} vs. Temperature for Various Frequencies at OP1dB, V_{DD} = 3.3V, I_{DQ} = 55mA, R_{BIAS} = 1540Ω

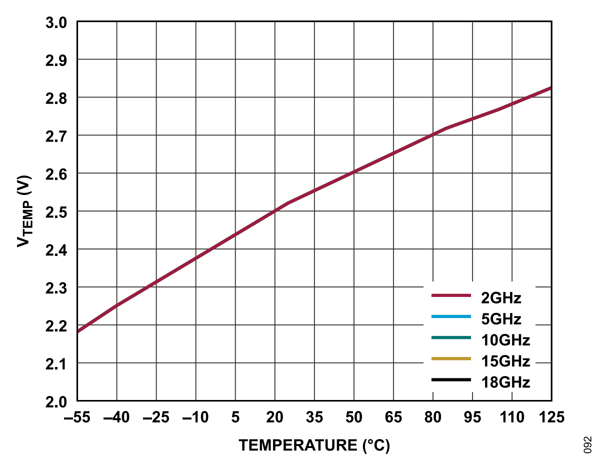

Figure 92. V_{TEMP} vs. Temperature for Various Frequencies at OP1dB, V_{DD} = 5V V, I_{DQ} = 85mA, R_{BIAS} = 1731Ω

TYPICAL PERFORMANCE CHARACTERISTICS

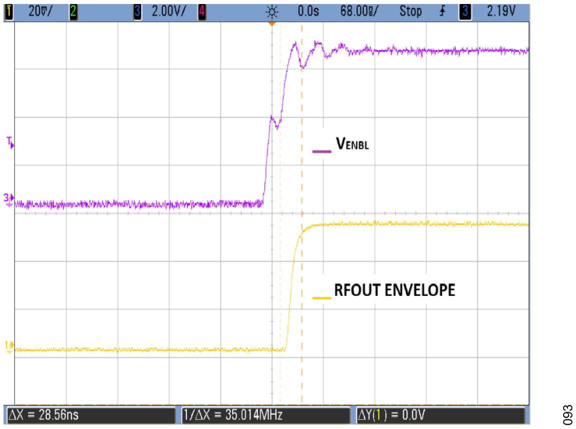

Figure 93. On Response of the RFOUT Envelope Timing When the VENBL Pin Is Toggled

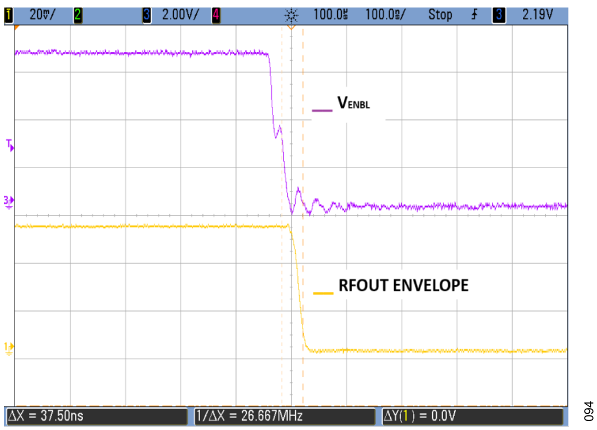

Figure 94. Off Response of the RFOUT Envelope Timing When the VENBL Pin Is Toggled

TYPICAL PERFORMANCE CHARACTERISTICS

AMPLIFIER OFF STATE (V_{ENBL} = 0V)

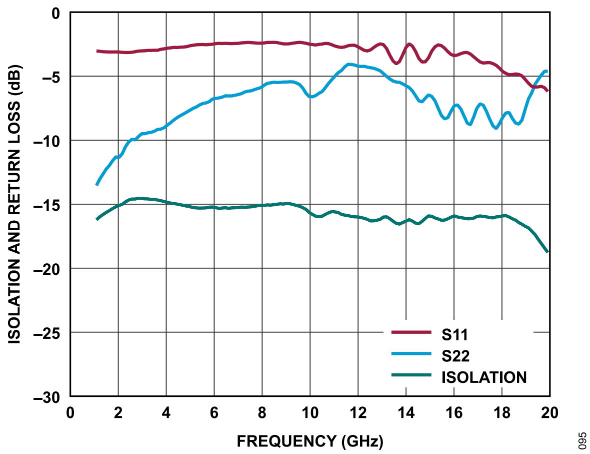

Figure 95. Isolation and Return Loss vs. Frequency, 1GHz to 20GHz, V_{DD} = 3.3V

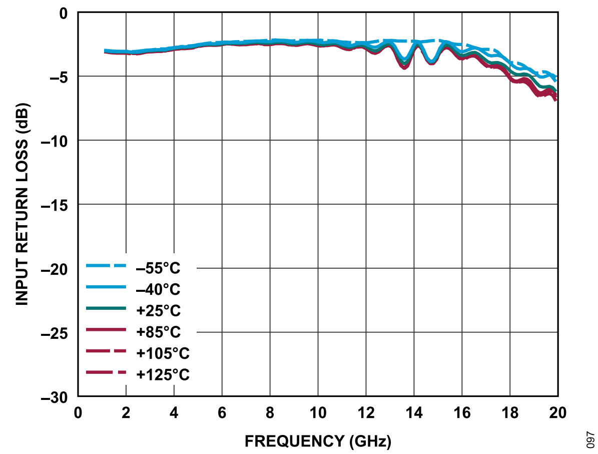

Figure 97. Input Return Loss vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V

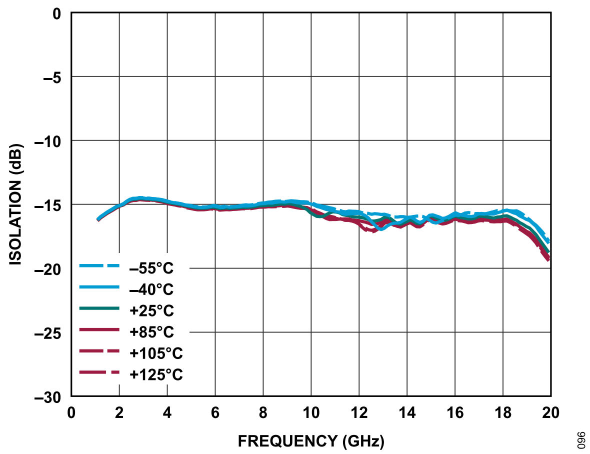

Figure 96. Isolation vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V

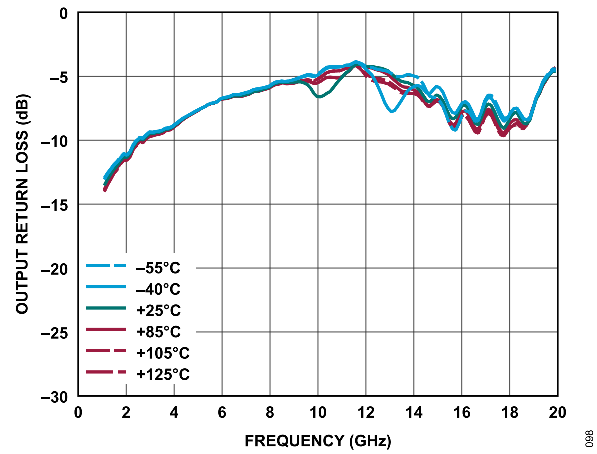

Figure 98. Output Return Loss vs. Frequency for Various Temperatures, 1GHz to 20GHz, V_{DD} = 3.3V

THEORY OF OPERATION

The ADL8124 is a wideband LNA with integrated AC-coupling capacitors, a bias inductor, a temperature sensor, and an enable or disable function. Figure 99 shows the simplified architecture of the ADL8124.

The ADL8124 has AC-coupled, single-ended input and output ports with impedances that are nominally equal to 50Ω over the 1GHz to 20GHz frequency range. No external matching components are required. The value of the resistor connected between VDD and RBIAS controls the I_{DQ}.

The ADL8124 contains an integrated temperature sensor. The temperature sensor is biased internally through the VDD pin. The voltage that is proportional to the device temperature can be measured on the VTEMP pin.

The ADL8124 also has an enable or disable function. By pulling the VENBL pin high or low, the ADL8124 can be enabled or disabled, respectively.

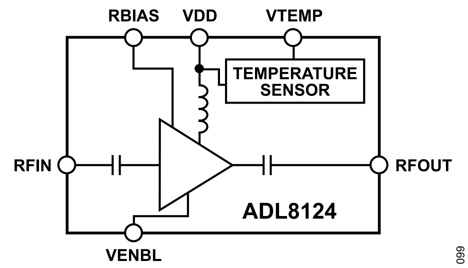

Figure 99. Simplified Architecture

APPLICATIONS INFORMATION

The basic connections for operating the ADL8124 over the specified frequency range are shown in Figure 100 . No external biasing inductor is required, which allows the 3.3V supply to be connected to the VDD pin. Alternatively, 5V supply operation is also supported. It is recommended to use 100pF power-supply decoupling capacitor. The power-supply decoupling capacitor shown in Figure 100 represents the configuration used to characterize and qualify the ADL8124.

To set I_{DQ}, connect a resistor (R3) between the RBIAS and VDD pins. A default value of 1540Ω is recommended, which results in a nominal I_{DQ} of 55mA. Table 12 shows how I_{DQ} and I_{DQ_AMP} vary vs. R_{BIAS}. The RBIAS pin also draws a current that varies with the R_{BIAS} value (see Table 12). Do not leave the RBIAS pin open.

The VTEMP pin provides an output voltage that is proportional to the die temperature. The VTEMP pin has a high output resistance that must be buffered using an op amp. The temperature sensor is internally supplied through the VDD pin.

The VENBL pin provides a convenient method to power up or power down the ADL8124. To enable the amplifier, connect the VENBL pin to a supply. To disable the amplifier, connect the VENBL pin to ground.

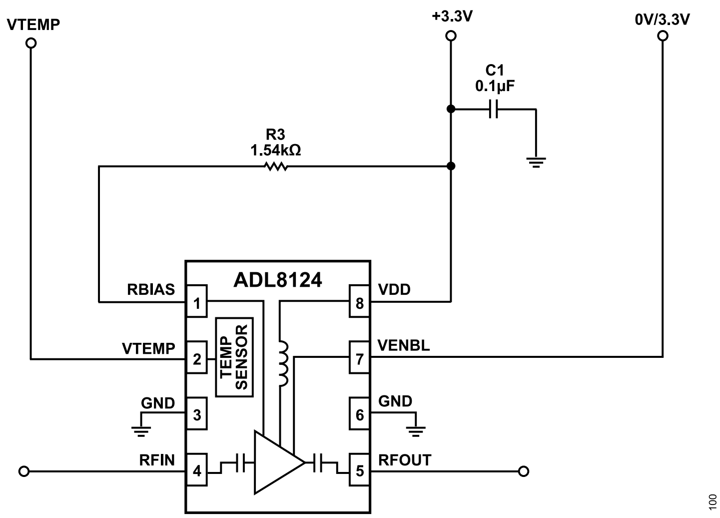

Figure 100. Typical Application Circuit

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

Correct sequencing of the DC and RF power is required to safely operate the ADL8124. To power up the ADL8124, take the following bias sequencing steps:

1. Set VDD to 3.3V.
2. Set VENBL to VDD.
3. Apply the RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence. Table 12 , Table 13 , Table 14, and Table 15 show alternate bias resistor options for different V_{DD} and I_{DQ} choices.

Table 12. Recommended Bias Resistor Values for V_{DD} = 3.3V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
5540	30	29.6	0.4
2836	40	39.2	8
1836	50	48.8	1.2
1540	55	53.6	1.4
1322	60	58.4	1.6
1015	70	68	2

Table 13. Recommended Bias Resistor Values for V_{DD} = 5V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
5539	50	49.3	0.7
3531	60	58.8	1.2
2532	70	68.5	1.5
1945	80	78	2
1731	85	82.8	2.2
1555	90	87.6	2.4
1275	100	97.2	2.8

Table 14. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 55mA

R_{BIAS} (Ω)	V_{DD} (V)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
776	2.5	53.3	1.7
1222	3	53.4	1.6
1540	3.3	53.6	1.4
2456	4	53.8	1.2
4312	5	54.1	0.9
7780	6	54.4	0.6

Table 15. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 85mA

R_{BIAS} (Ω)	V_{DD} (V)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
1103	4	82.6	2.4
1399	4.5	82.7	2.3
1731	5	82.8	2.2
2102	5.5	82.9	2.1
2534	6	83	2

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 101 shows a recommended power management circuit for the ADL8124. The LT8607 step-down regulator is used to step down a 12V rail to 4.5V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 3.3V output. Even though the circuit shown in Figure 101 has an input voltage (V_{IN}) of 12V, the input range to the LT8607 can be as high as 42V.

The 4.5V regulator output of the LT8607 is set by the R2 and R3 resistors, according to the following equation:

$R2 = R3((V_{OUT}/0.778V) – 1)$, where V_{OUT} is the output voltage.

The switching frequency (f_{SW}) is set to 2MHz by the 18.2kΩ resistor (R1) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2MHz to 2.200MHz.

The V_{OUT} of the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$V_{OUT} = 100µA × R4$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 3.3V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%). Therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 3.3V output to give a convenient 0V to 3.6V voltage range. Table 16 provides the recommended resistor values for operation at 3.6V to 3V.

Table 16. Recommended Resistor Values for Operating at 3.6V to 3V

LDO V_{OUT} (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
3.6	36.5	332	30.1
3.3	33.1	301	30.1
3	30.1	267	30.1

The LT8607 can source a maximum current of 750mA, and the LT3042 can source a maximum current of 200mA. If the 5V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5A and 3A, respectively, and these devices are pin compatible with the LT8607. The LT3045 linear regulator, which is pin compatible with LT3042, can source a maximum current to 500mA.

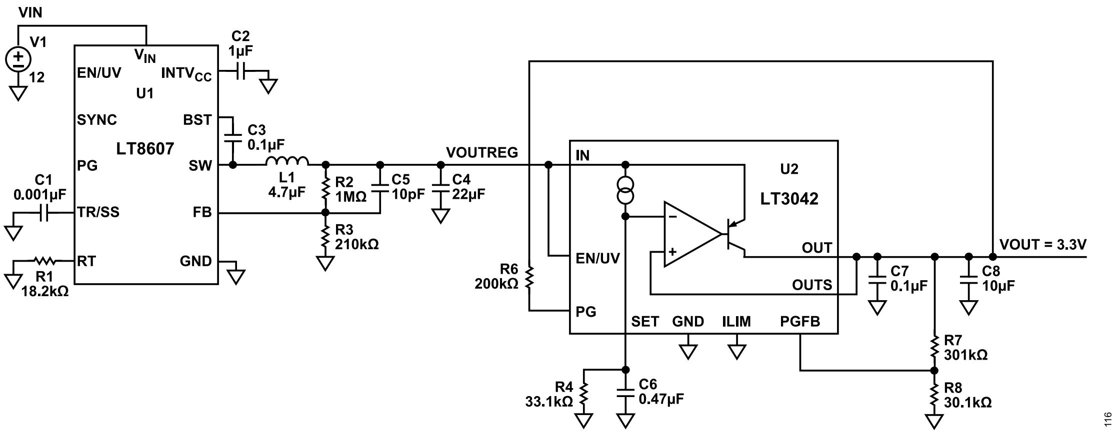

Figure 101. Recommended Power Management Circuit

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CP-8-30	LFCSP	8-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8124ACPZN	−55°C to +125°C	8-Lead LFCSP, 2mm × 2mm × 0.85mm	Tape, 1	CP-8-30
ADL8124ACPZN-R7	−55°C to +125°C	8-Lead LFCSP, 2mm × 2mm × 0.85mm	Reel, 3000	CP-8-30

1 Z = RoHS Compliant Part.

2 The lead finish of the ADL8124ACPZN and ADL8124ACPZN-R7 is nickel palladium gold.