Data Sheet

ADL7075

100MHz to 31GHz, High Survivability, Low Noise Amplifier

FEATURES

- Wideband operation: 100MHz to 31GHz
- Single positive supply (self biased) typical: 5V and 90mA
- RBIAS drain current adjustment pin
- Gain: 14.5dB typical from 100MHz to 18GHz
- Noise figure: 3.5dB typical from 100MHz to 18GHz
- Typical OP1dB of 17dBm and P_{SAT} of 18dBm from 100MHz to 18GHz
- Extended operating temperature range: −55°C to +125°C
- **RoHS-compliant, 2mm × 2mm, 8-lead LFCSP**

APPLICATIONS

- Telecommunications
- Instrumentation
- Radars
- Electronic warfare

FUNCTIONAL BLOCK DIAGRAM

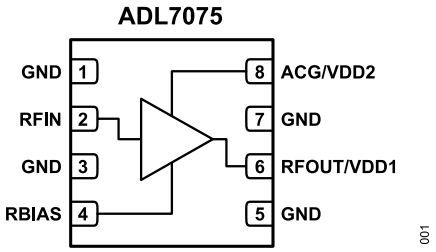

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADL7075 is an ultrawideband, low noise amplifier (LNA) that operates from 100MHz to 31GHz. The typical gain and noise figure are 14.5dB and 3.5dB, respectively, from 100MHz to 18GHz. The output power for 1dB compression (OP1dB), output third-order intercept (OIP3), and output second-order intercept (OIP2) are 17dBm, 29dBm, and 30dBm, respectively, from 100MHz to 18GHz. The nominal quiescent current (I_{DQ}), which can be adjusted, is 90mA from a 5V supply voltage (V_{DD}). The internally matched, DC-coupled RF input and output pins require external AC coupling capacitors along with a bias inductor on RFOUT.

The ADL7075 is fabricated on a pseudomorphic high electron mobility transistor (pHEMT) process. It is housed in an RoHS-compliant, 2mm × 2mm, 8-lead LFCSP and is specified for operation from −55°C to +125°C.

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REVISION HISTORY

7/2026—Revision 0: Initial Version

SPECIFICATIONS

100MHz to 18GHz Frequency Range

V_{DD} = 5V, I_{DQ} = 90mA, bias resistance (R_{BIAS}) = 665Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 100MHz to 18GHz Frequency Range

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
FREQUENCY RANGE			0.1		18	GHz
GAIN	S21		12	14.5		dB
Gain Variation Over Temperature				0.0168		dB/°C
NOISE FIGURE				3.5		dB
RETURN LOSS						
Input	S11			8		dB
Output	S22			12		dB
OUTPUT						
Output Power For 1dB Compression	OP1dB		14	17		dBm
Saturated Output Power	P_{SAT}			18		dBm
Output Third-Order Intercept	OIP3	Measurement taken at output power (P_{OUT}) per tone = 0dBm		29		dBm
Output Second-Order Intercept	OIP2	Measurement taken at P_{OUT} per tone = 0dBm		30		dBm
POWER ADDED EFFICIENCY	PAE	Measured at P_{SAT}		13		%

18GHz to 28GHz Frequency Range

V_{DD} = 5V, I_{DQ} = 90mA, R_{BIAS} = 665Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 18GHz to 22GHz Frequency Range

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
FREQUENCY RANGE			18		28	GHz
GAIN	S21		12	14		dB
Gain Variation Over Temperature				0.0205		dB/°C
NOISE FIGURE				4.1		dB
RETURN LOSS						
Input	S11			12		dB
Output	S22			11		dB
OUTPUT						
Output Power For 1dB Compression	OP1dB		12	15.5		dBm
Saturated Output Power	P_{SAT}			19		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 0dBm		27		dBm
Output Second-Order Intercept	OIP2	Measurement taken at P_{OUT} per tone = 0dBm		40		dBm
POWER ADDED EFFICIENCY	PAE	Measured at P_{SAT}		12.83		%

SPECIFICATIONS

28GHz to 31GHz Frequency Range

V_{DD} = 5V, I_{DQ} = 90mA, R_{BIAS} = 665Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 28GHz to 31GHz Frequency Range

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
FREQUENCY RANGE			28		31	GHz
GAIN	S21		14	16		dB
Gain Variation Over Temperature				0.0282		dB/°C
NOISE FIGURE				5.4		dB
RETURN LOSS						
Input	S11			15		dB
Output	S22			15.5		dB
OUTPUT						
Output Power For 1dB Compression	OP1dB		11	13.5		dBm
Saturated Output Power	P_{SAT}			17.5		dBm
Output Third-Order Intercept	OIP3	Measurement taken at P_{OUT} per tone = 0dBm		25		dBm
POWER ADDED EFFICIENCY	PAE	Measured at P_{SAT}		9.2		%

DC Specifications

Table 4. DC Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CURRENT					
Supply	I_{DQ}		90		mA
Amplifier	I_{DQ_AMP}		84.5		mA
R_{BIAS}	I_{RBIAS}		5.5		mA
SUPPLY VOLTAGE	V_{DD}	3	5	6	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

PARAMETER	RATING
VDD1	7V
VDD2	10.5V
RF Input Power (RFIN)	See **Figure 2**
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 13.28mW/°C Above 85°C)	1.195W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 5V, I_{DQ} = 90mA, Input Power (P_{IN}) = Off)	118.9°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

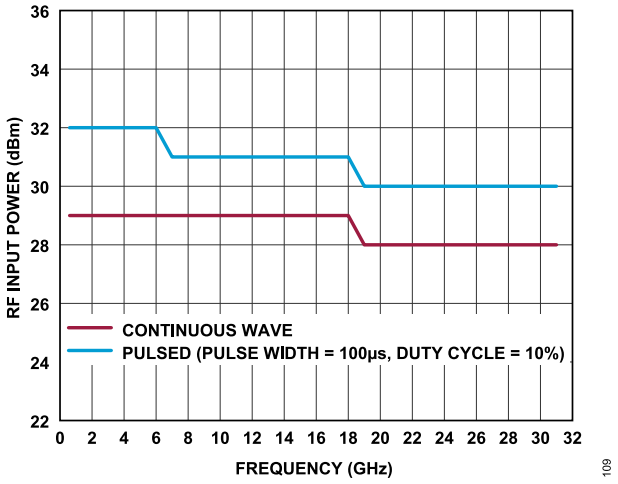

Figure 2. RF Input Power Absolute Maximum Ratings for Continuous Wave and Pulsed vs. Frequency, T_{CASE} = 85°C

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance.

Table 6. Thermal Resistance[1]

PACKAGE TYPE	θ_{JC}	UNIT
CP-8-30		
Quiescent, T_{CASE} = 25°C	62	°C/W
Worst Case,[2] T_{CASE} = 85°C	75.3	°C/W

[1] Thermal resistance varies with operating conditions.

[2] Across all specified operating conditions.

ABSOLUTE MAXIMUM RATINGS

Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL7075

Table 7. ADL7075, 8-Lead LFCSP

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±250	1A

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

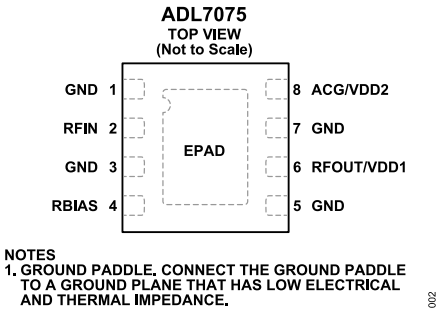

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

PIN NO.	MNEMONIC	DESCRIPTION
1, 3, 5, 7	GND	Grounds. Connect these pins to a ground plane that has low electrical and thermal impedance. See **Figure 4** for the interface schematic.
2	RFIN	RF Input. The RFIN pin is DC-coupled and matched to 50Ω. See **Figure 5** for the interface schematic.
4	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDDx to set I_{DQ}. See **Table 9** and **Table 10** for additional information. See **Figure 6** for the interface schematic.
6	RFOUT/VDD1	RF Output (RFOUT) and Drain Bias Voltage (VDD1). The RF output is DC-coupled and also serves as the drain biasing node. For the drain bias voltage, connect a DC bias network to provide the drain current and AC-couple the RF output path. See **Figure 7** for the interface schematic.
8	ACG/VDD2	AC Ground (ACG) and Optional Alternative Drain Bias (VDD2). Connect a capacitor between the ACG/VDD2 pin and ground. The ACG/VDD2 pin can also be used as the drain biasing node through an internal resistor. Do not use the ACG/VDD2 pin simultaneously with the RFOUT/VDD1 pin. See **Figure 7** for the interface schematic.
	EPAD	Ground Paddle. Connect the ground paddle to a ground plane that has low electrical and thermal impedance.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Interface Schematics

Figure 4. GND Interface Schematic

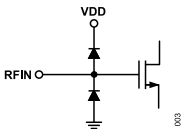

Figure 5. RFIN Interface Schematic

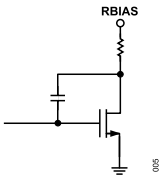

Figure 6. RBIAS Interface Schematic

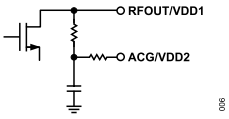

Figure 7. RFOUT/VDD1 and ACG/VDD2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

100MHz to 31GHz

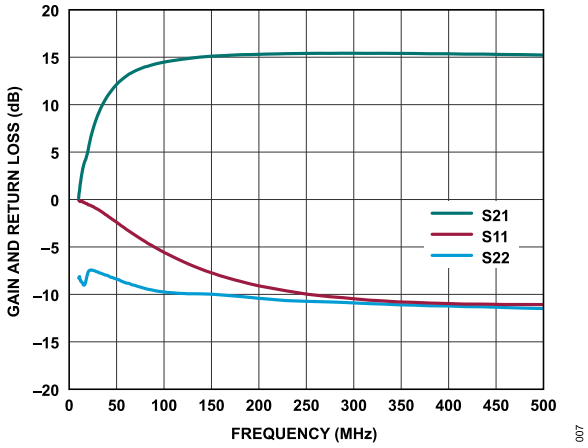

Figure 8. Gain and Return Loss vs. Frequency, 10MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

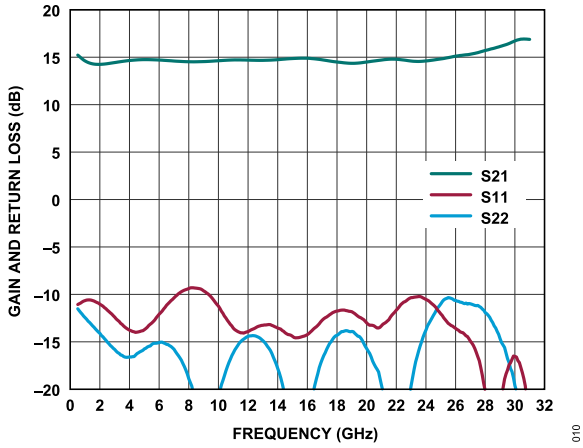

Figure 11. Gain and Return Loss vs. Frequency, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

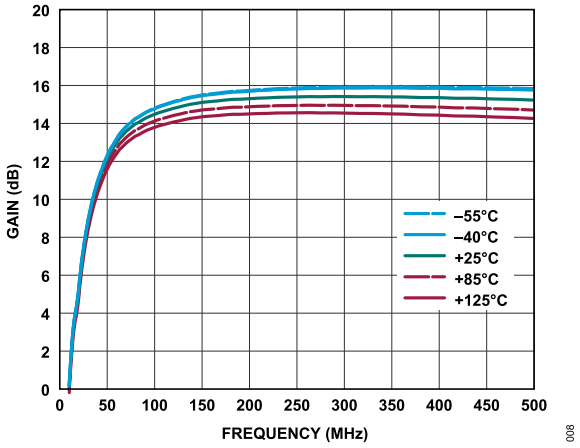

Figure 9. Gain vs. Frequency for Various Temperatures, 10MHz to 500MHz,V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

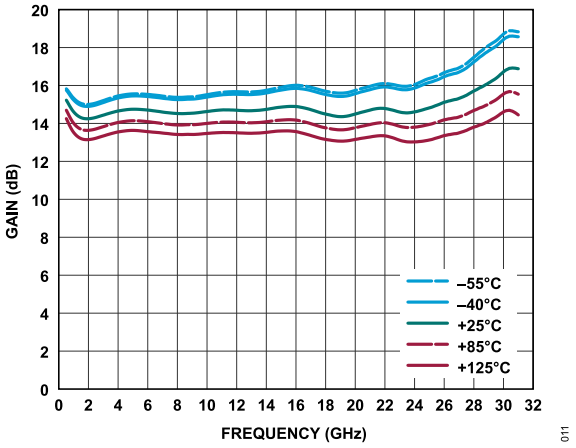

Figure 12. Gain vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

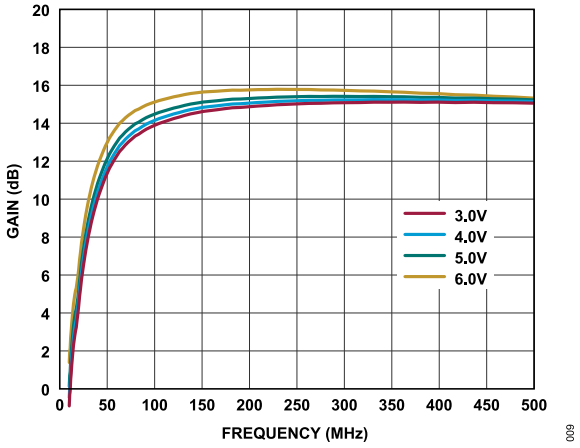

Figure 10. Gain vs. Frequency for Various Supply Voltages, 10MHz to 500MHz and I_{DQ} = 90mA

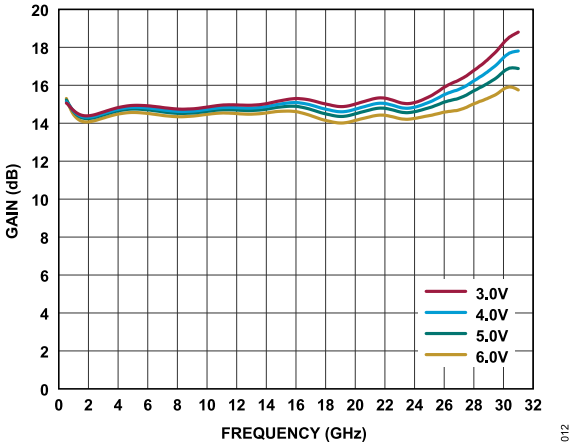

Figure 13. Gain vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

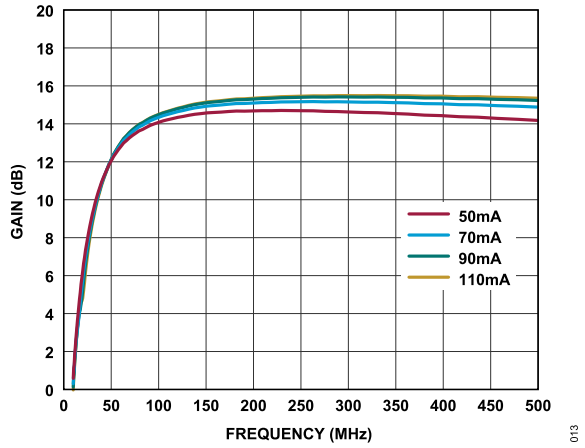

Figure 14. Gain vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, and V_{DD} = 5V

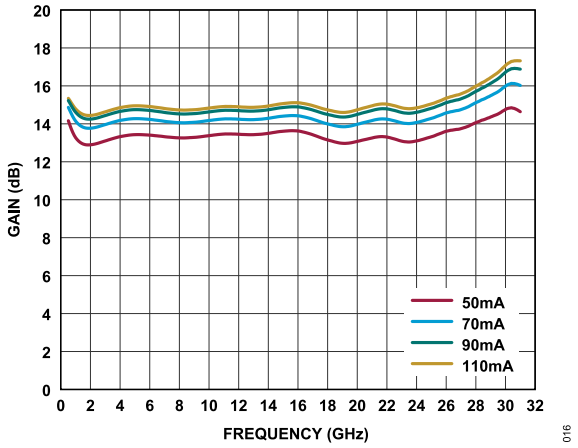

Figure 17. Gain vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and V_{DD} = 5V

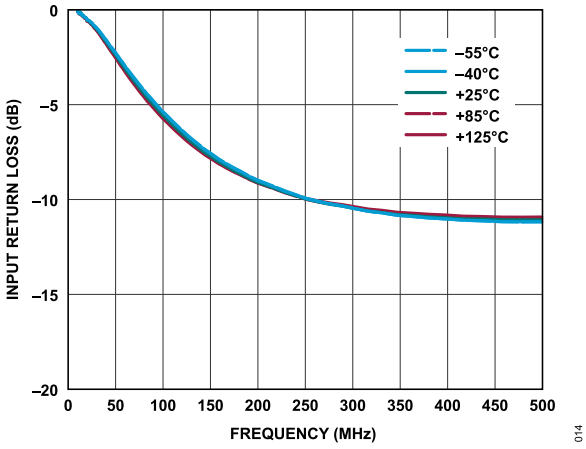

Figure 15. Input Return Loss vs. Frequency for Various Temperatures, 10MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

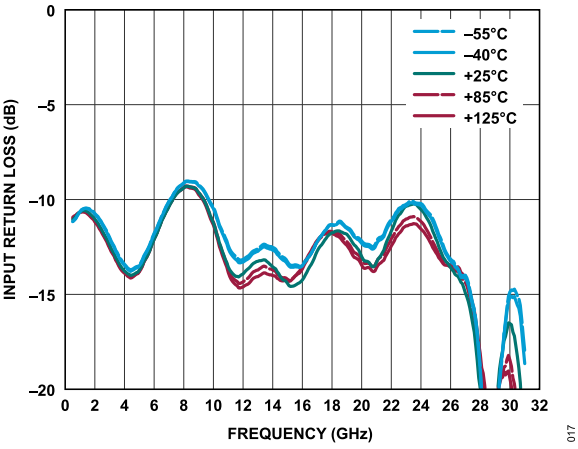

Figure 18. Input Return Loss vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

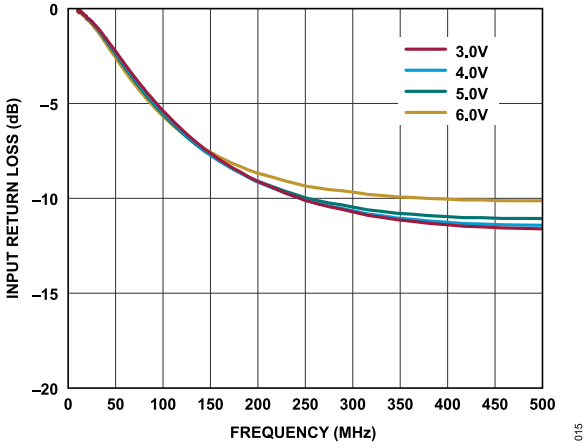

Figure 16. Input Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, and I_{DQ} = 90mA

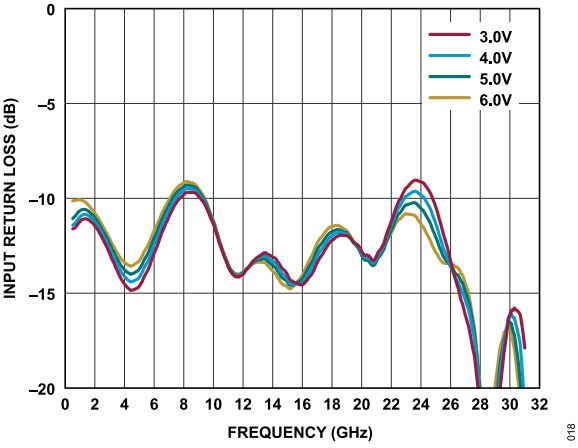

Figure 19. Input Return Loss vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

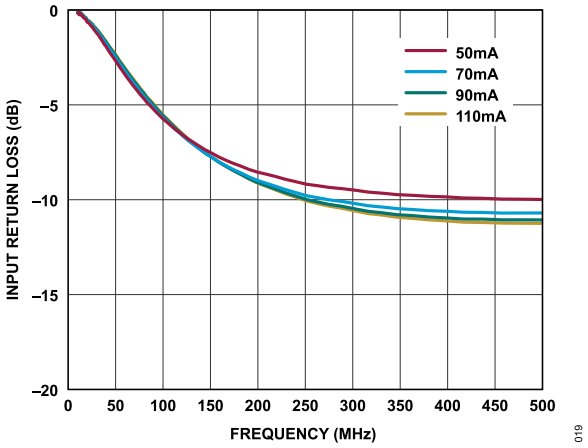

Figure 20. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, and V_{DD} = 5V

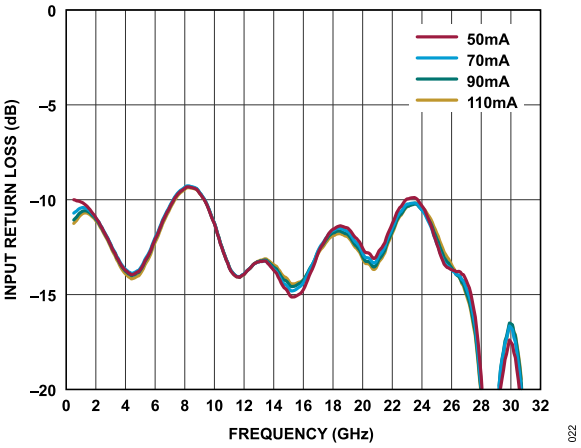

Figure 23. Input Return Loss vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and V_{DD} = 5V

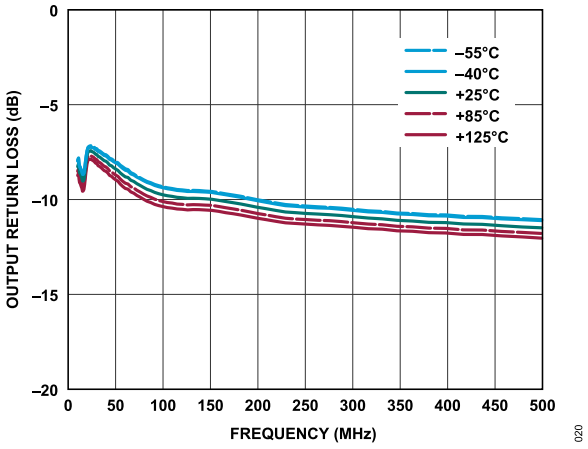

Figure 21. Output Return Loss vs. Frequency for Various Temperatures, 10MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

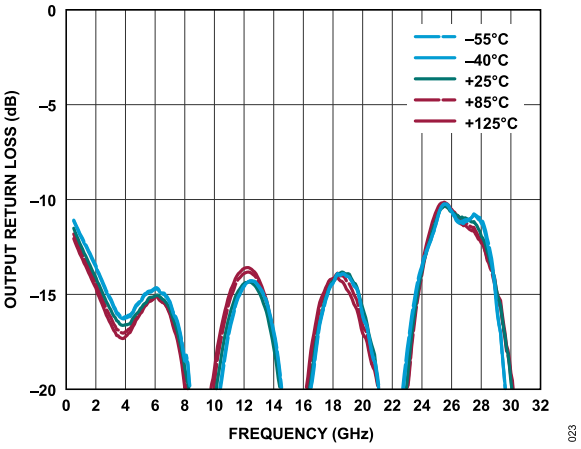

Figure 24. Output Return Loss vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

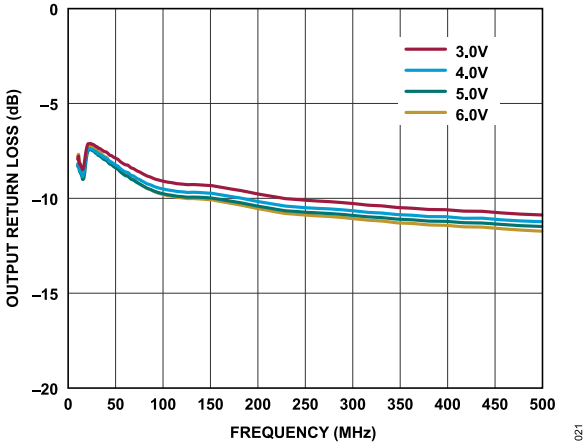

Figure 22. Output Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, and I_{DQ} = 90mA

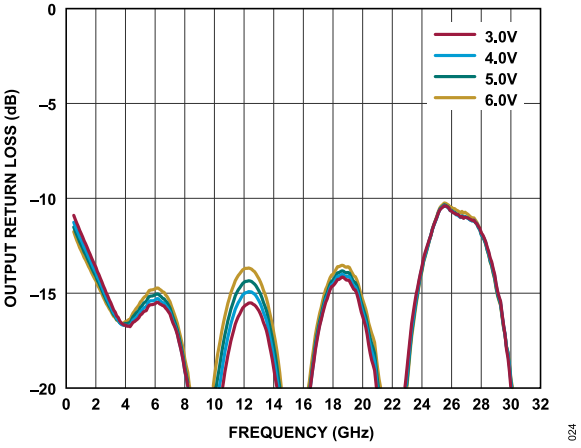

Figure 25. Output Return Loss vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

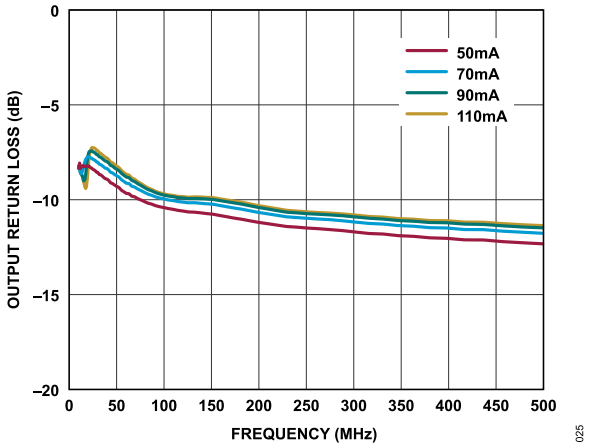

Figure 26. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, and V_{DD} = 5V

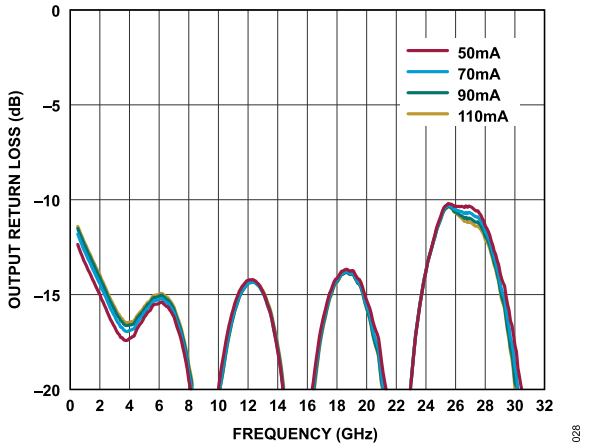

Figure 29. Output Return Loss vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and V_{DD} = 5V

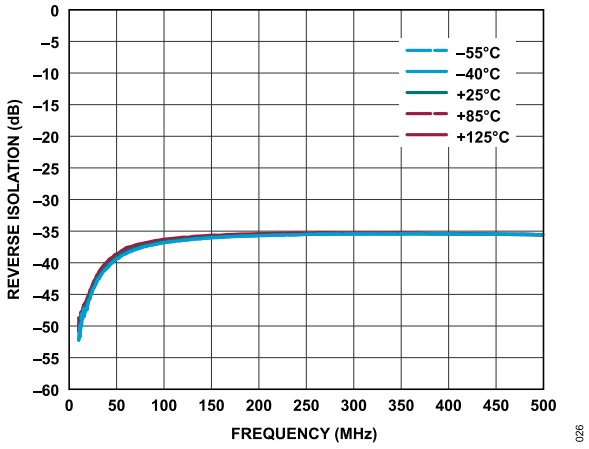

Figure 27. Reverse Isolation vs. Frequency for Various Temperatures, 10MHz to 500MHz,V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

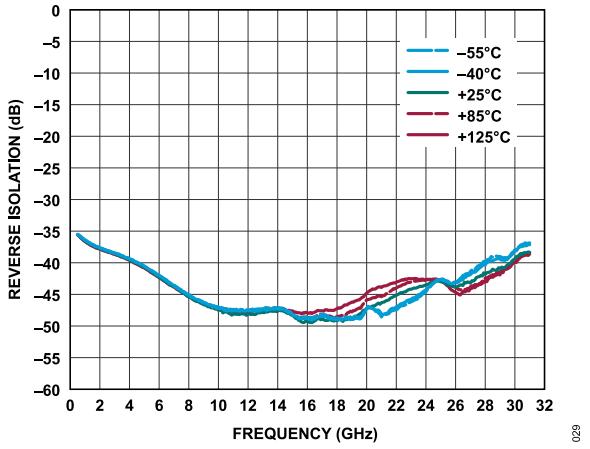

Figure 30. Reverse Isolation vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

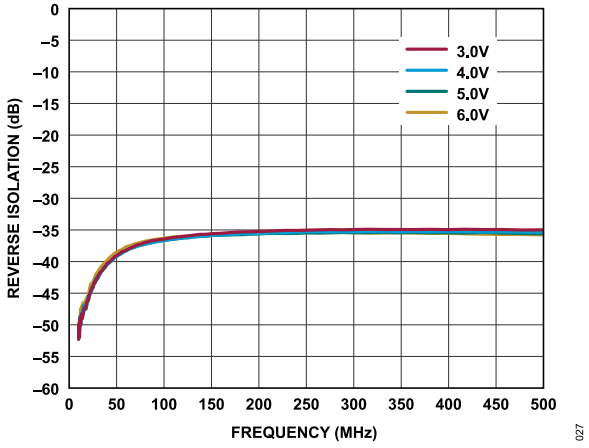

Figure 28. Reverse Isolation vs. Frequency for Various Supply Voltages, 10MHz to 500MHz, and I_{DQ} = 90mA

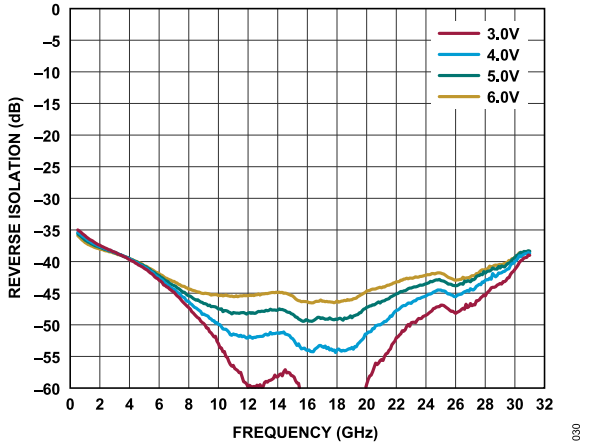

Figure 31. Reverse Isolation vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

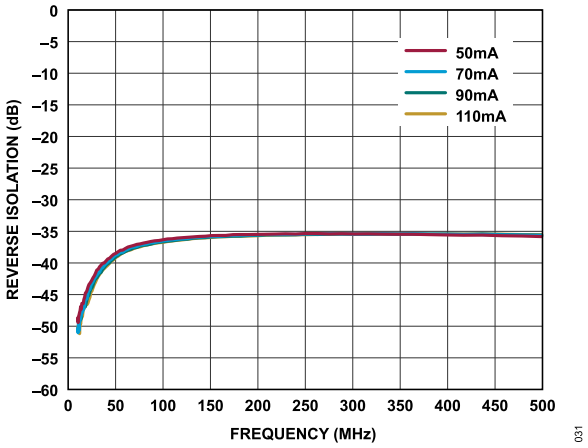

Figure 32. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 10MHz to 500MHz, and V_{DD} = 5V

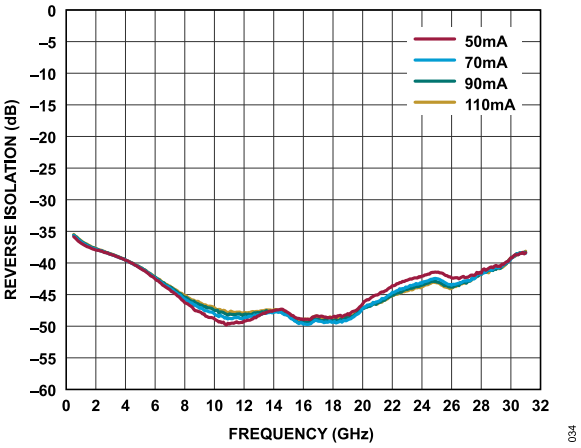

Figure 35. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and V_{DD} = 5V

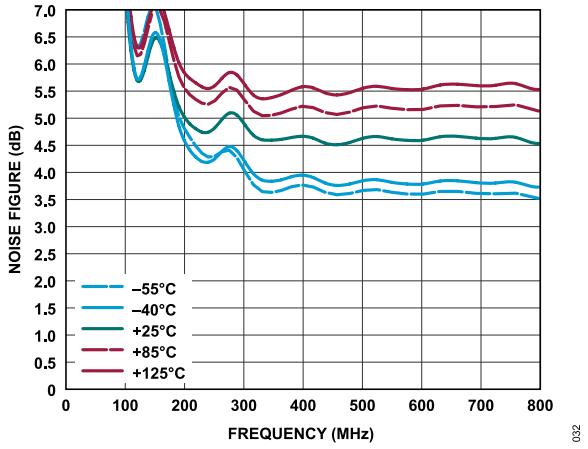

Figure 33. Noise Figure vs. Frequency for Various Temperatures, 10MHz to 800MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

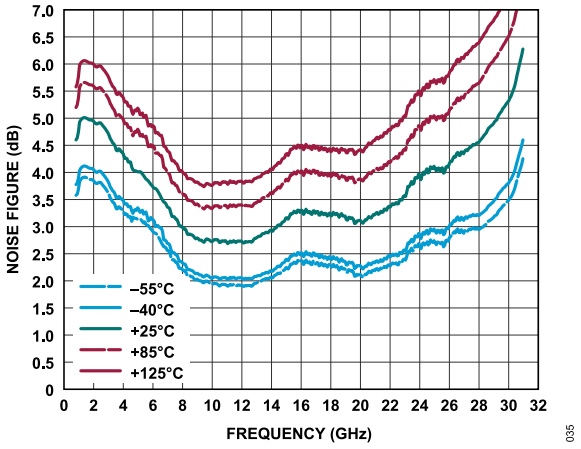

Figure 36. Noise Figure vs. Frequency for Various Temperatures, 800MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

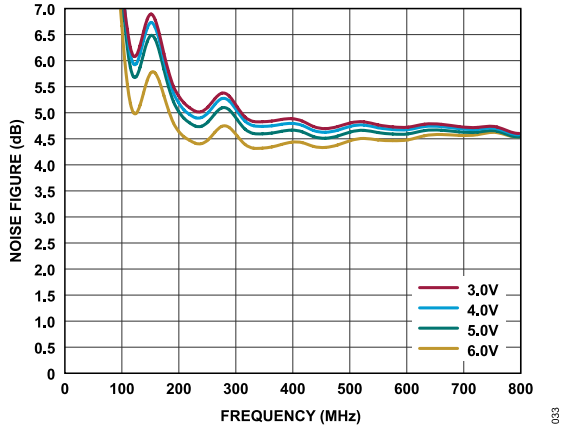

Figure 34. Noise Figure vs. Frequency for Various Supply Voltages, 10MHz to 800MHz, and I_{DQ} = 90mA

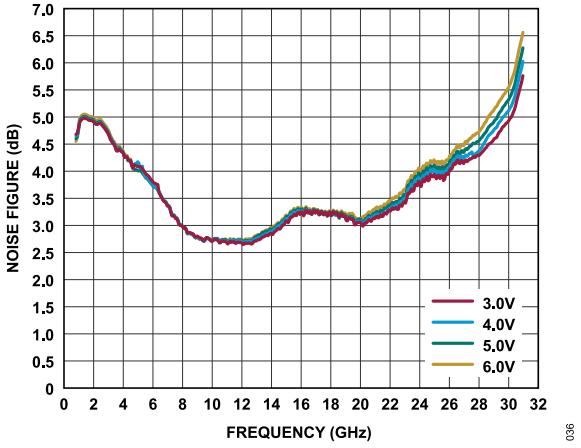

Figure 37. Noise Figure vs. Frequency for Various Supply Voltages, 800MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

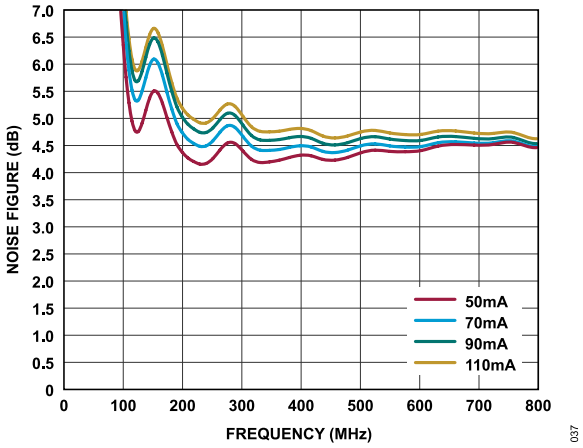

Figure 38. Noise Figure vs. Frequency for Various I_{DQ} Values, 10MHz to 800MHz, and V_{DD} = 5V

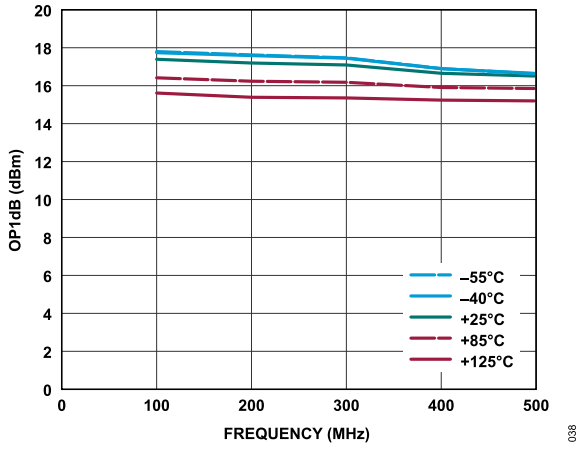

Figure 39. OP1dB vs. Frequency for Various Temperatures, 100MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

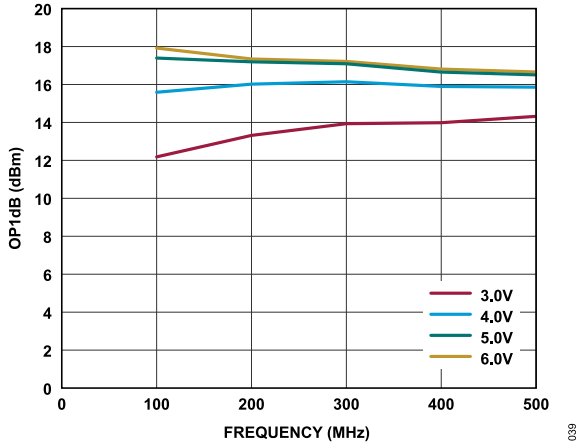

Figure 40. OP1dB vs. Frequency for Various Supply Voltages, 100MHz to 500MHz, and I_{DQ} = 90mA

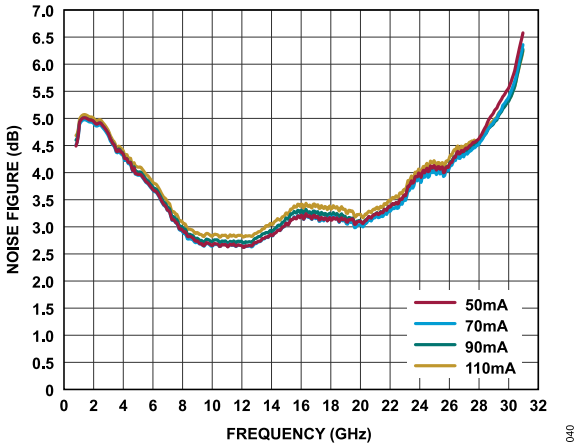

Figure 41. Noise Figure vs. Frequency for Various I_{DQ} Values, 800MHz to 31GHz, and V_{DD} = 5V

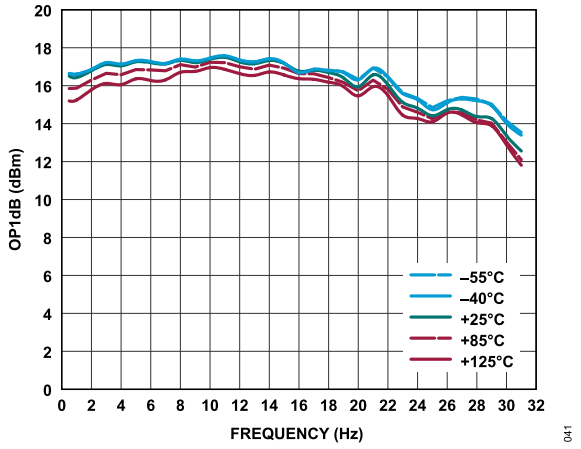

Figure 42. OP1dB vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

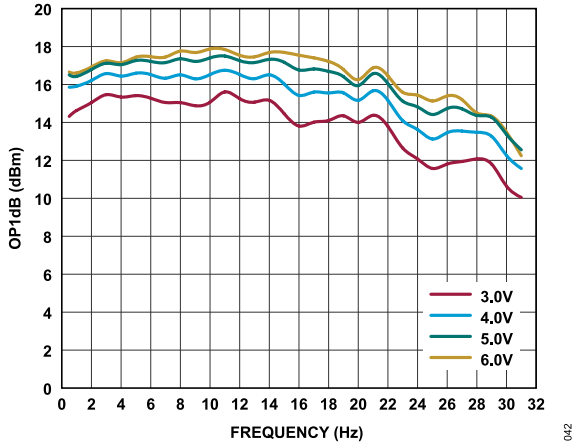

Figure 43. OP1dB vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

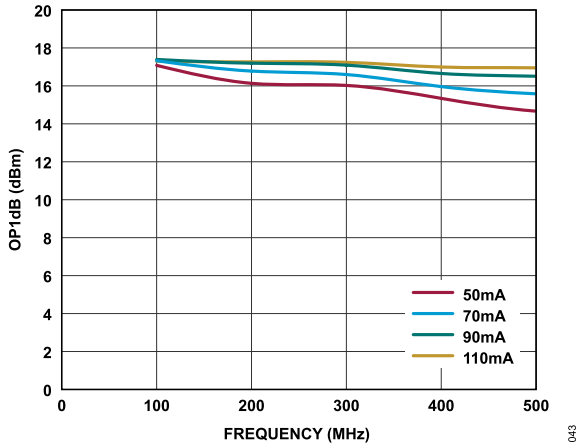

Figure 44. OP1dB vs. Frequency for Various I_{DQ} Values, 100MHz to 500MHz, and V_{DD} = 5V

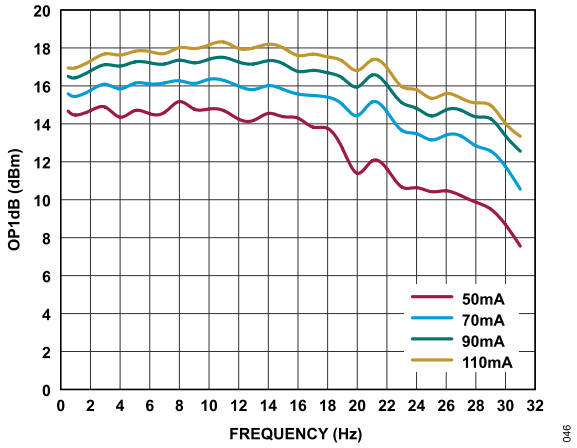

Figure 47. OP1dB vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and V_{DD} = 5V

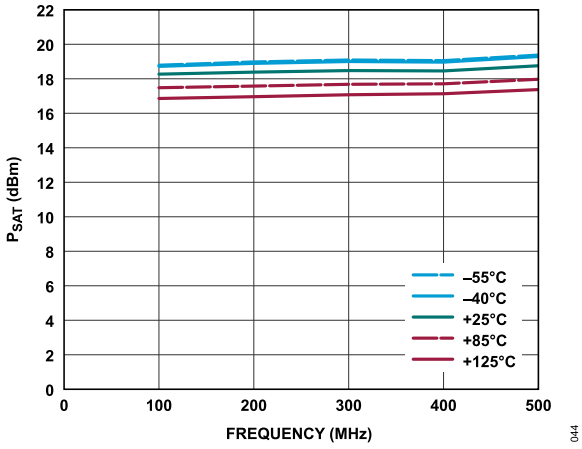

Figure 45. P_{SAT} vs. Frequency for Various Temperatures, 100MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

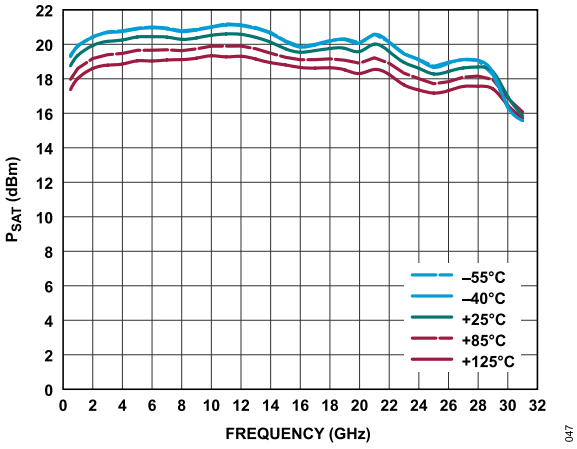

Figure 48. P_{SAT} vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

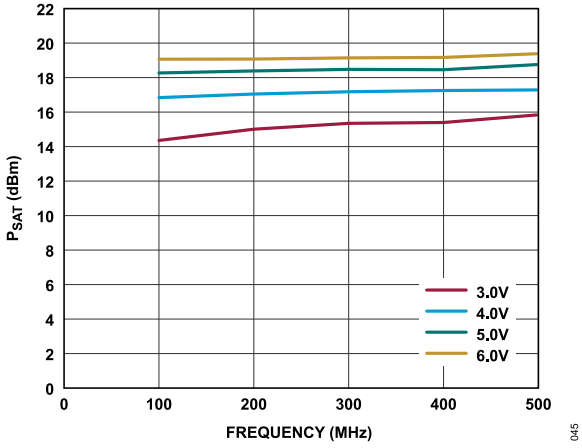

Figure 46. P_{SAT} vs. Frequency for Various Supply Voltages, 100MHz to 500MHz, and I_{DQ} = 90mA

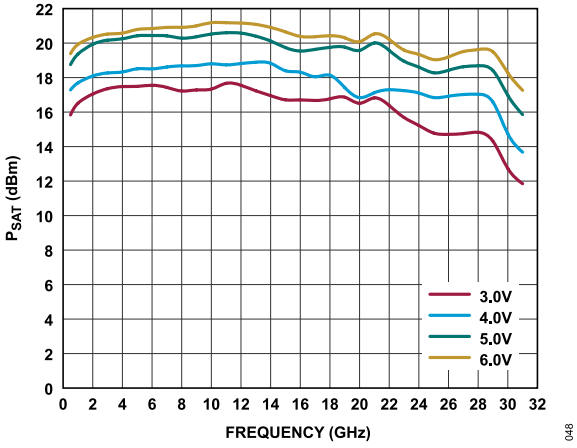

Figure 49. P_{SAT} vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

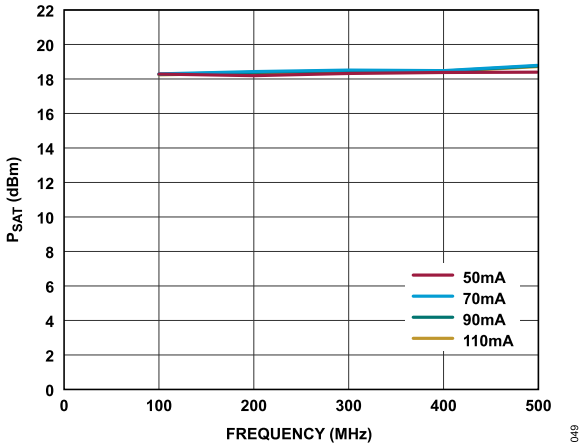

Figure 50. P_{SAT} vs. Frequency for Various I_{DQ} Values, 100MHz to 500MHz, and I_{DQ} = 90mA

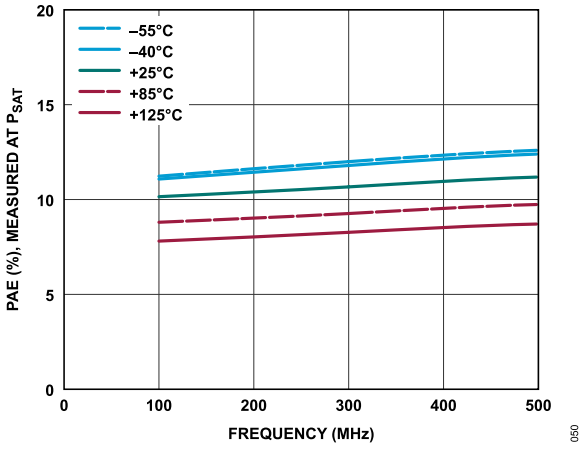

Figure 51. PAE, Measured at P_{SAT} vs. Frequency for Various Temperatures, 100MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

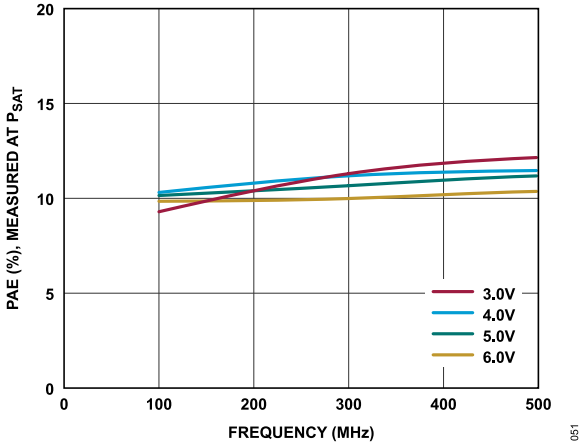

Figure 52. PAE, Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 100MHz to 500MHz, and I_{DQ} = 90mA

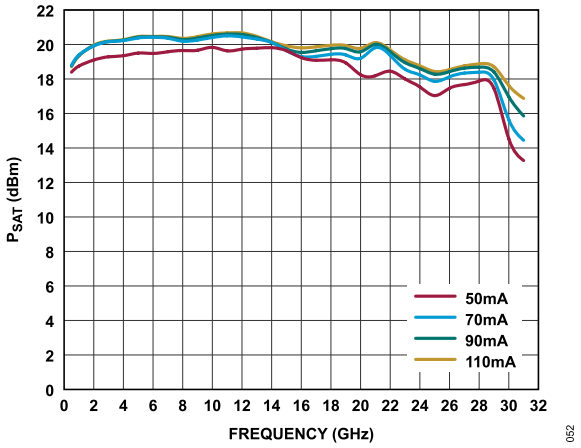

Figure 53. P_{SAT} vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and I_{DQ} = 90mA

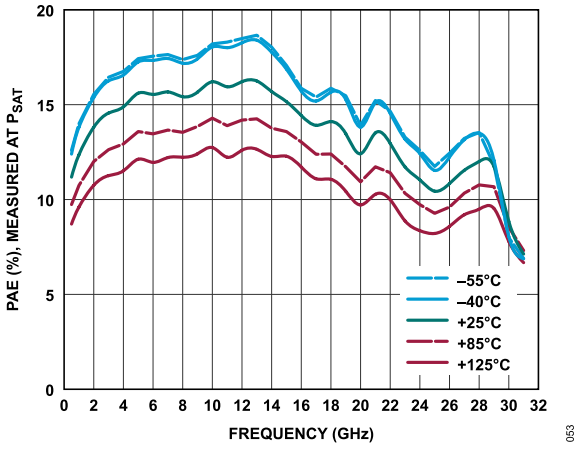

Figure 54. PAE, Measured at P_{SAT} vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

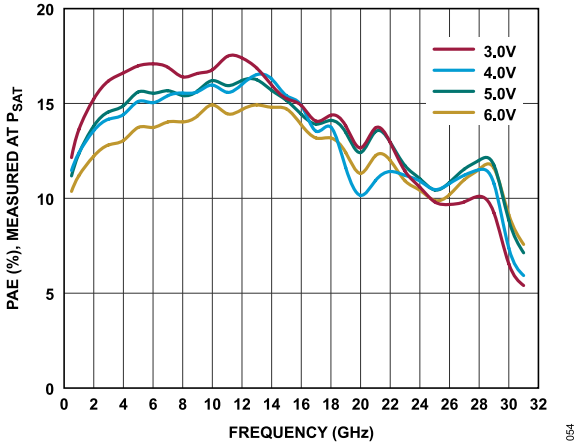

Figure 55. PAE, Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, and I_{DQ} = 90mA

TYPICAL PERFORMANCE CHARACTERISTICS

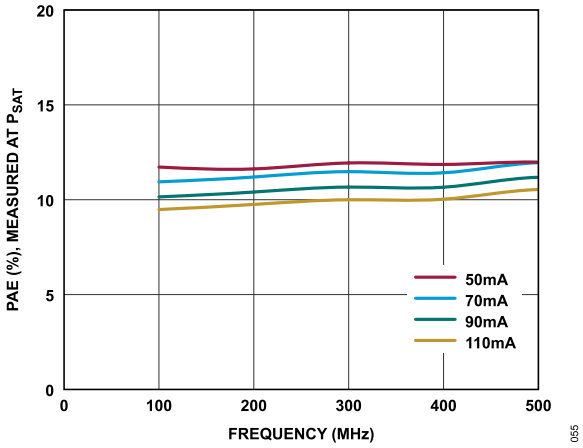

Figure 56. PAE, Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 100MHz to 500MHz, and I_{DQ} = 90mA

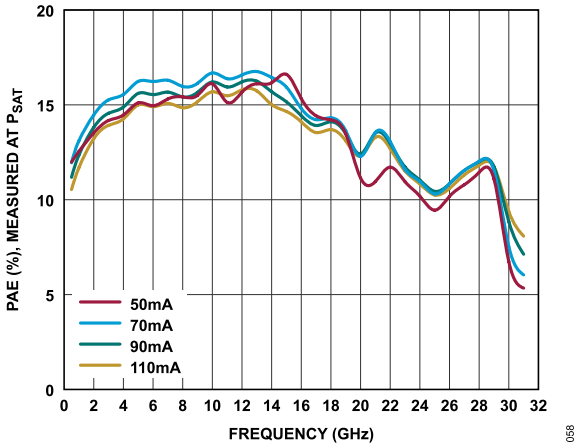

Figure 59. PAE, Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, and I_{DQ} = 90mA

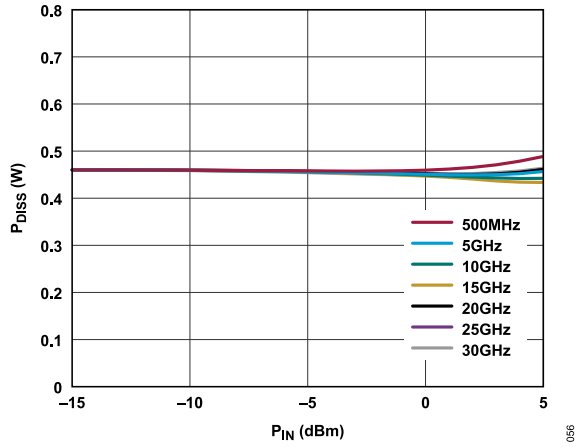

Figure 57. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, and V_{DD} = 5V

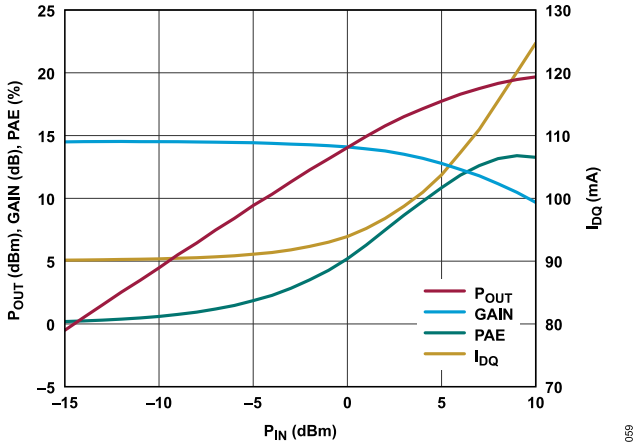

Figure 60. P_{OUT}, GAIN, PAE, and I_{DQ} vs. P_{IN}, Power Compression at 2GHz, V_{DD} = 5V, and R_{BIAS} = 665Ω

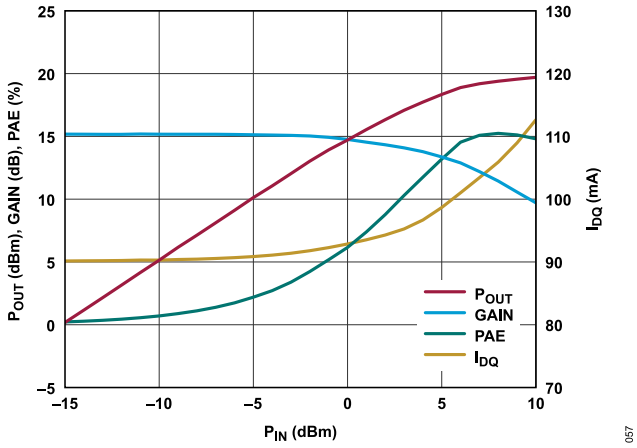

Figure 58. P_{OUT}, GAIN, PAE, and I_{DQ} vs. P_{IN}, Power Compression at 15GHz, V_{DD} = 5V, and R_{BIAS} = 665Ω

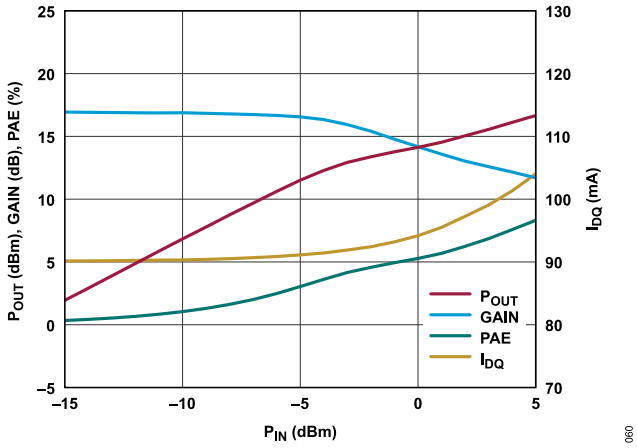

Figure 61. P_{OUT}, GAIN, PAE, and I_{DQ} vs. P_{IN}, Power Compression at 30GHz, V_{DD} = 5V, and R_{BIAS} = 665Ω

TYPICAL PERFORMANCE CHARACTERISTICS

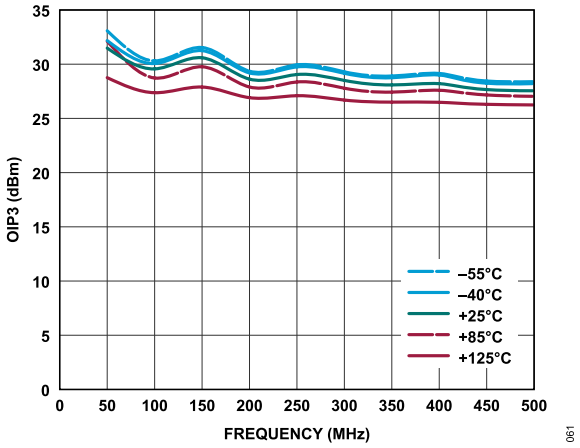

Figure 62. OIP3 vs. Frequency for Various Temperatures, 50MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

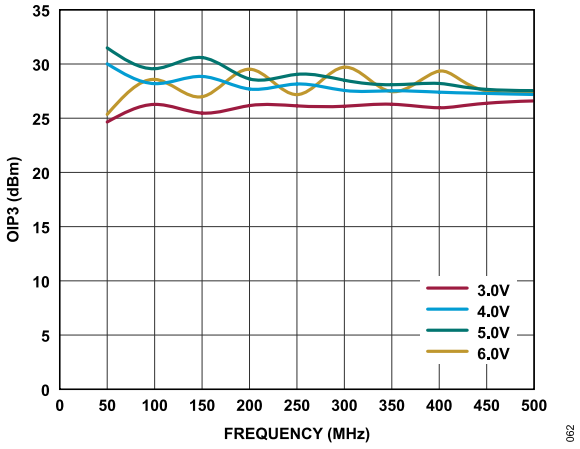

Figure 63. OIP3 vs. Frequency for Various Supply Voltages, 50MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

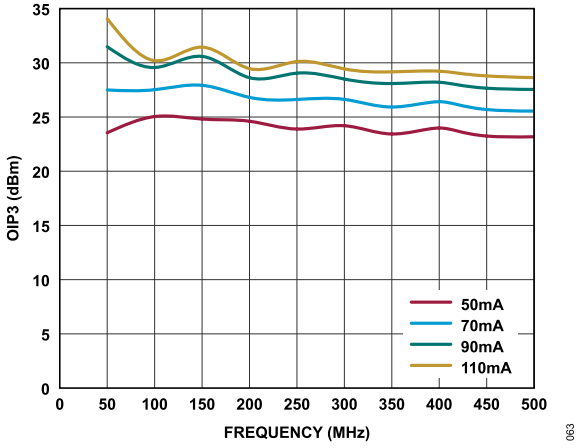

Figure 64. OIP3 vs. Frequency for Various I_{DQ} Values, 50MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

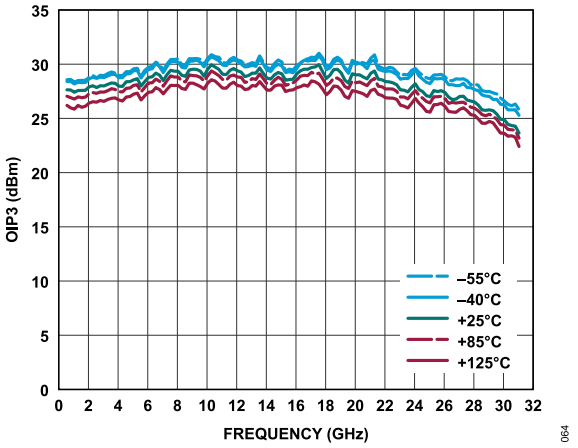

Figure 65. OIP3 vs. Frequency for Various Temperatures, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

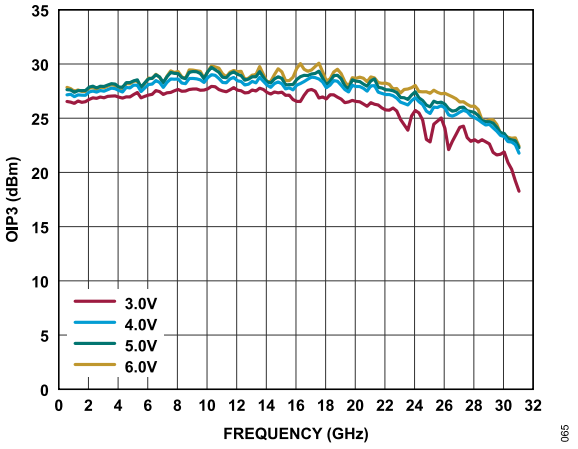

Figure 66. OIP3 vs. Frequency for Various Supply Voltages, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

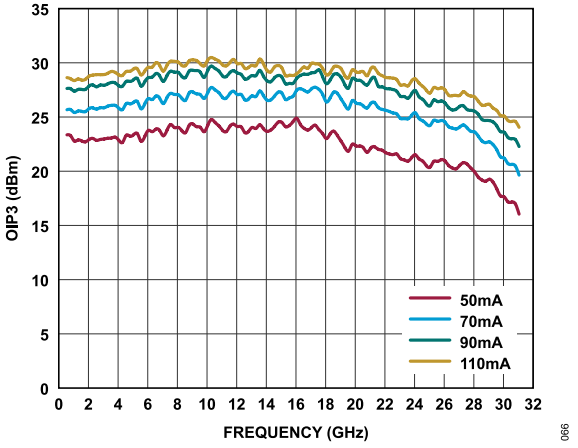

Figure 67. OIP3 vs. Frequency for Various I_{DQ} Values, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

TYPICAL PERFORMANCE CHARACTERISTICS

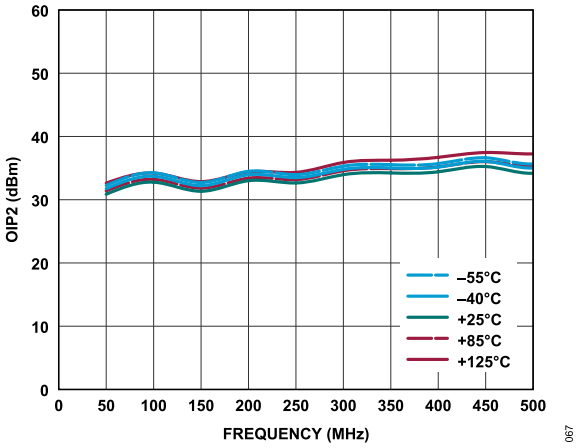

Figure 68. OIP2 vs. Frequency for Various Temperatures, 100MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

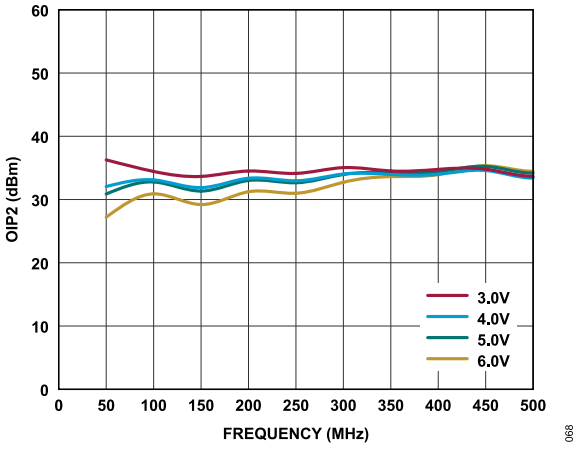

Figure 69. OIP2 vs. Frequency for Various Supply Voltages, 100MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

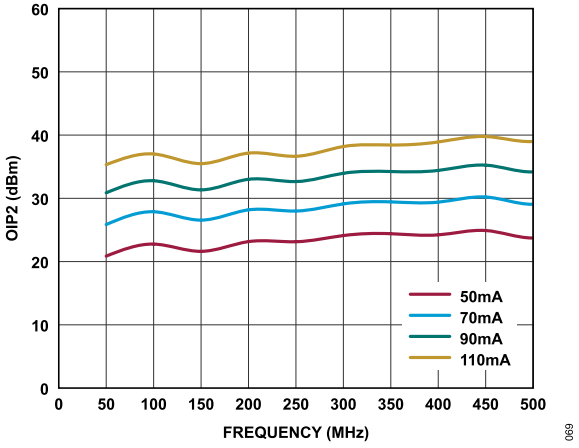

Figure 70. OIP2 vs. Frequency for I_{DQ} Values, 100MHz to 500MHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

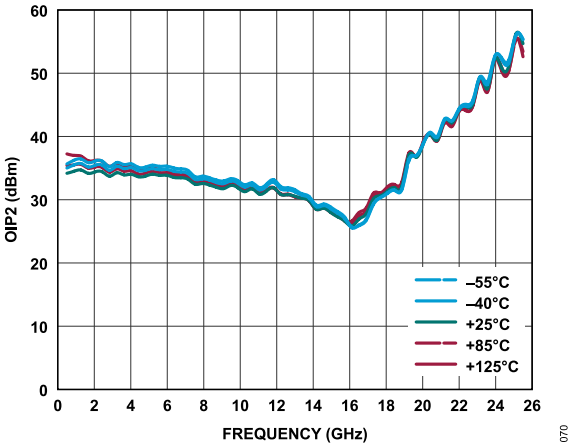

Figure 71. OIP2 vs. Frequency for Various Temperatures, 500MHz to 25.5GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

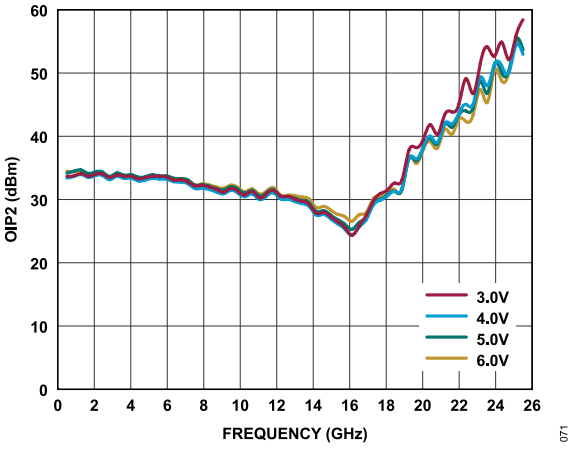

Figure 72. OIP2 vs. Frequency for Various Supply Voltages, 500MHz to 25.5GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

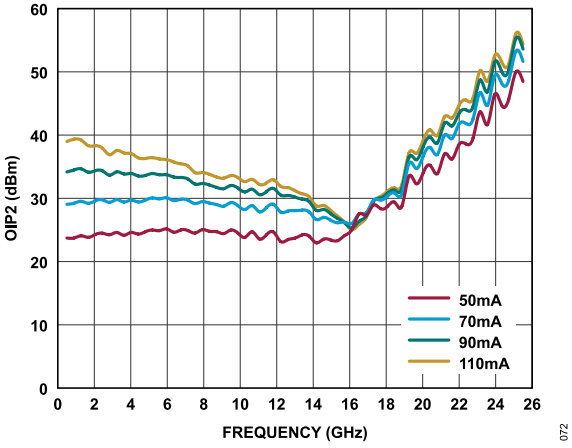

Figure 73. OIP2 vs. Frequency for I_{DQ} Values, 500MHz to 25.5GHz, V_{DD} = 5V, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

TYPICAL PERFORMANCE CHARACTERISTICS

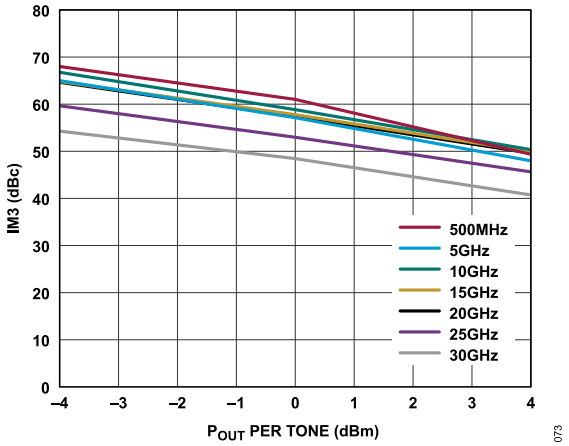

Figure 74. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5V, and R_{BIAS} = 665Ω

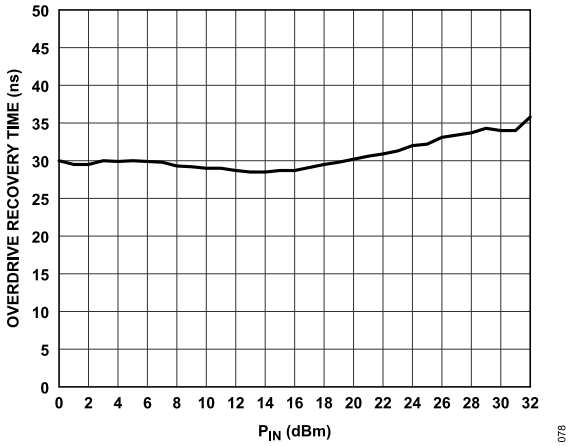

Figure 77. Overdrive Recovery Time vs. P_{IN} at 10GHz, Recovery Time to Within 90% of Small Signal Gain Value, V_{DD} = 5V, and R_{BIAS} = 665Ω, Blocking Signal at 11GHz

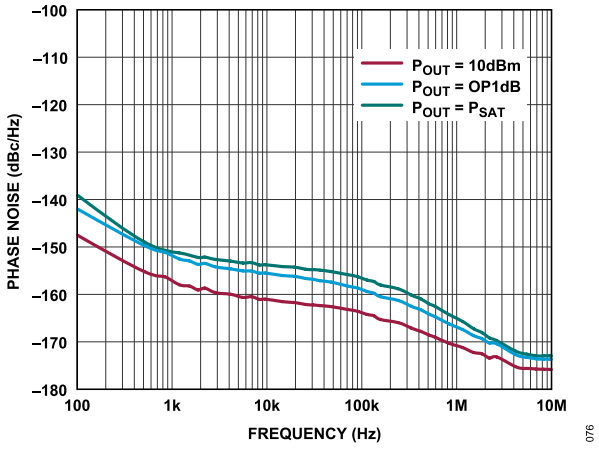

Figure 75. Phase Noise vs. Frequency at 10GHz for Various P_{OUT} Values

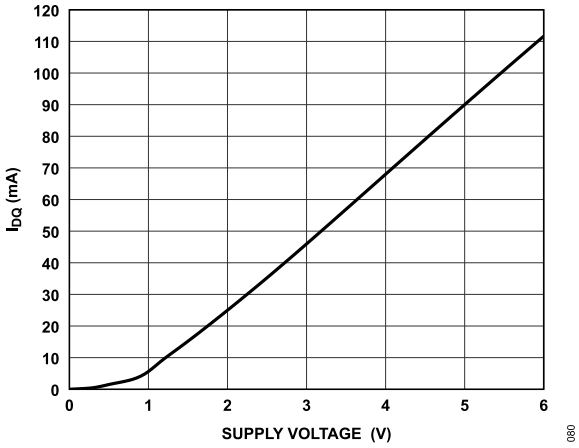

Figure 78. I_{DQ} vs. Supply Voltage, R_{BIAS} = 665Ω

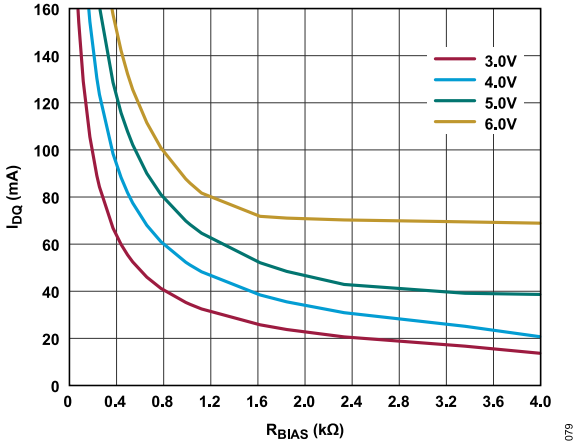

Figure 76. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0Ω to 4kΩ

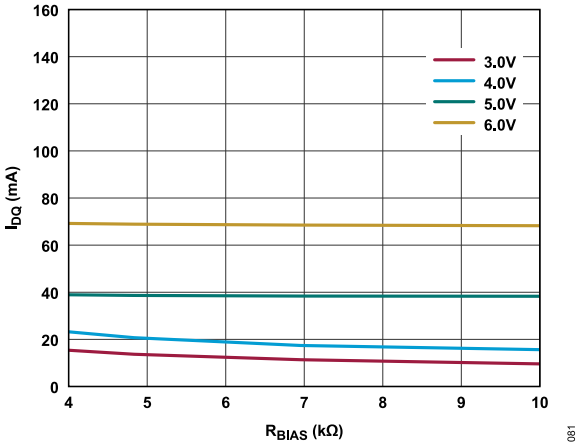

Figure 79. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 4kΩ to 10kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

100MHz to 31GHz, Biasing Through the ACG/VDD2 Pin

VDD2 = 8.5V, and bias voltage (V_{BIAS}) = 5V.

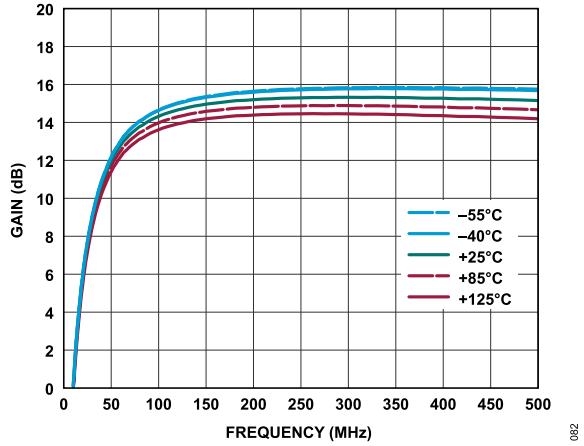

Figure 80. Gain vs. Frequency for Various Temperatures, 10MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

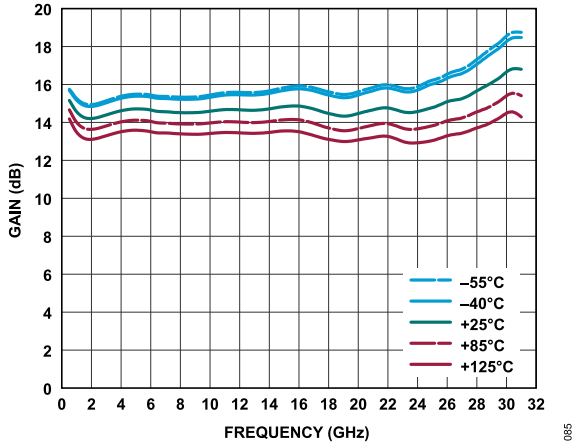

Figure 83. Gain vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

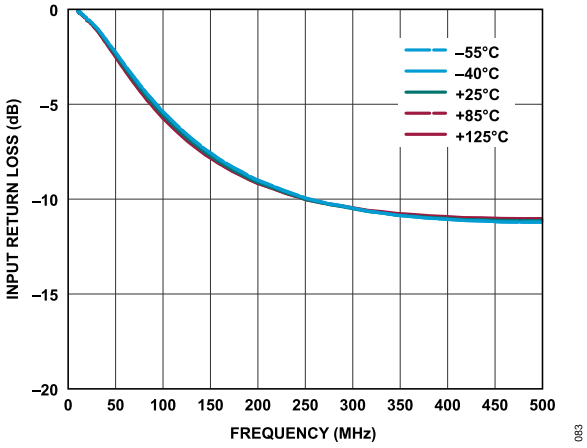

Figure 81. Input Return Loss vs. Frequency for Various Temperatures, 10MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

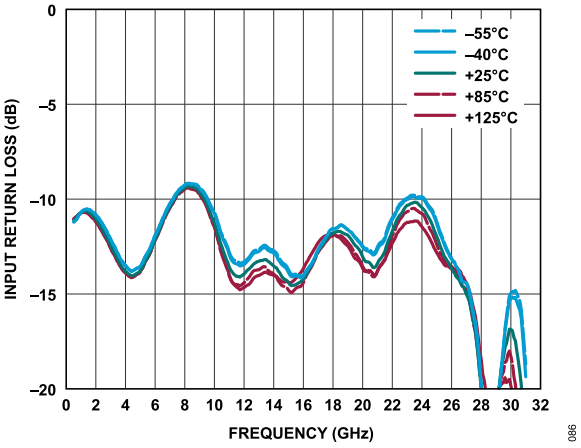

Figure 84. Input Return Loss vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

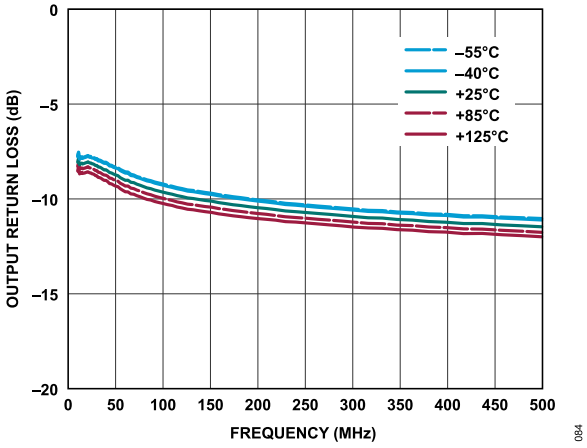

Figure 82. Output Return Loss vs. Frequency for Various Temperatures, 10MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

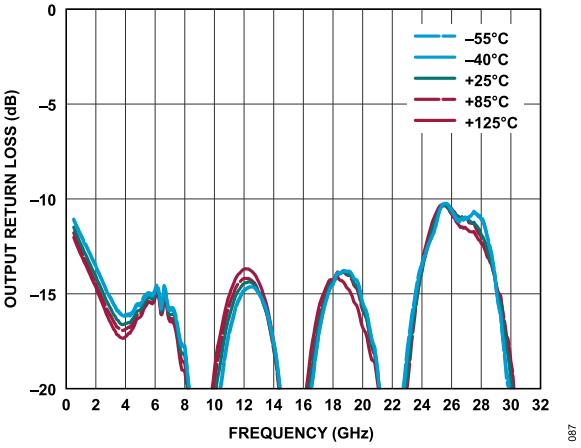

Figure 85. Output Return Loss vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

TYPICAL PERFORMANCE CHARACTERISTICS

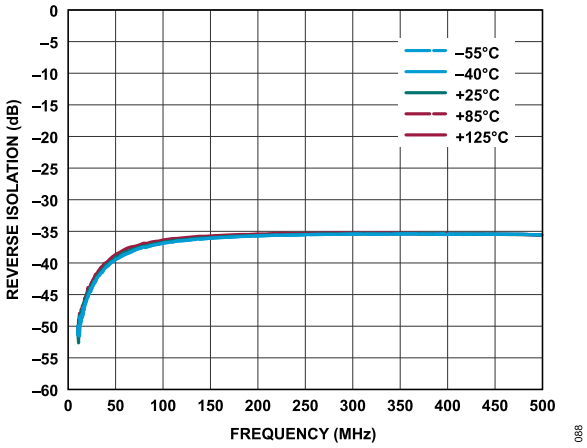

Figure 86. Reverse Isolation vs. Frequency for Various Temperatures, 10MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

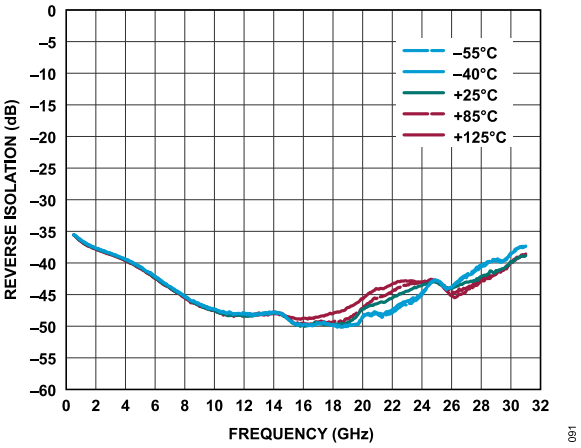

Figure 89. Reverse Isolation vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

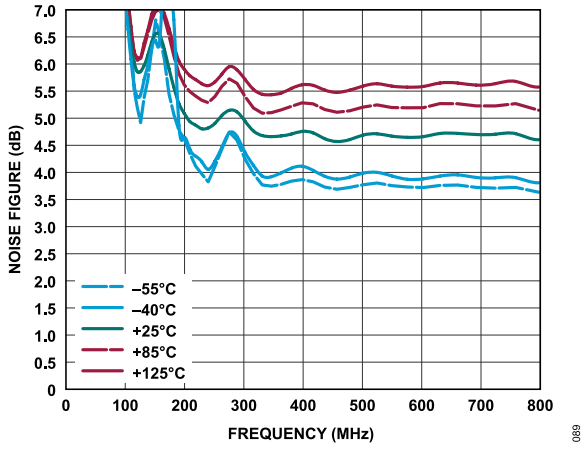

Figure 87. Noise Figure vs. Frequency for Various Temperatures, 10MHz to 800MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

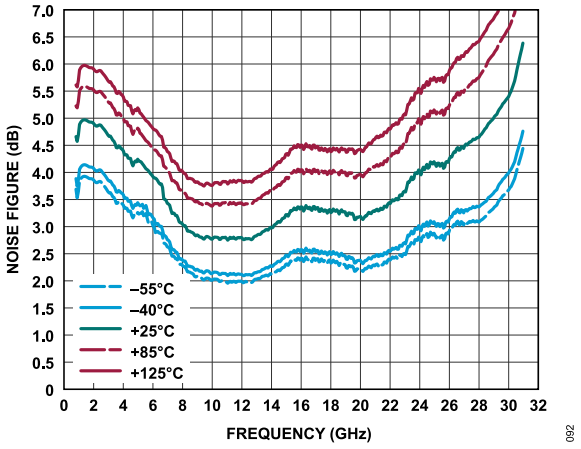

Figure 90. Noise Figure vs. Frequency for Various Temperatures, 800MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

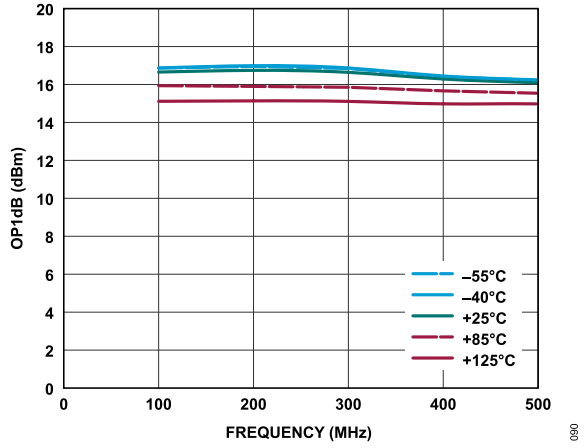

Figure 88. OP1dB vs. Frequency for Various Temperatures, 100MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

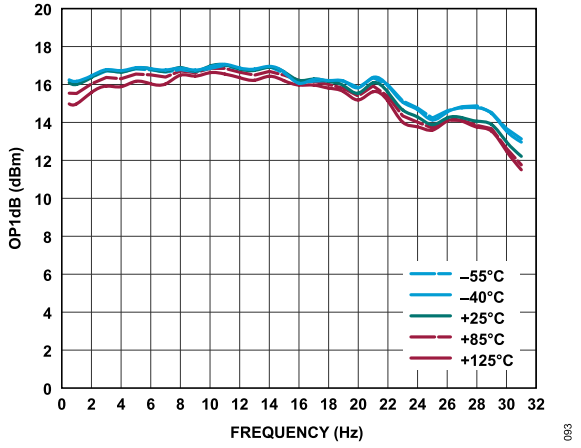

Figure 91. OP1dB vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

TYPICAL PERFORMANCE CHARACTERISTICS

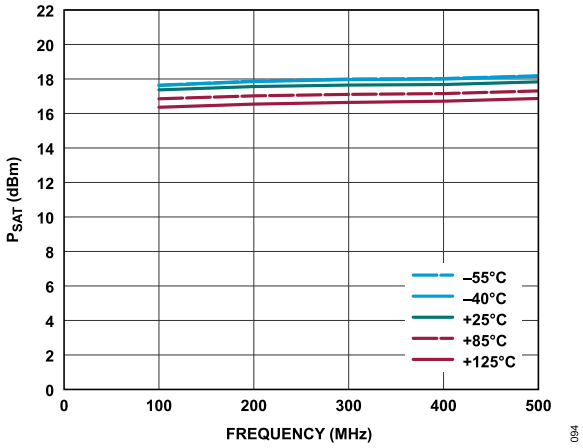

Figure 92. P_{SAT} vs. Frequency for Various Temperatures, 100MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

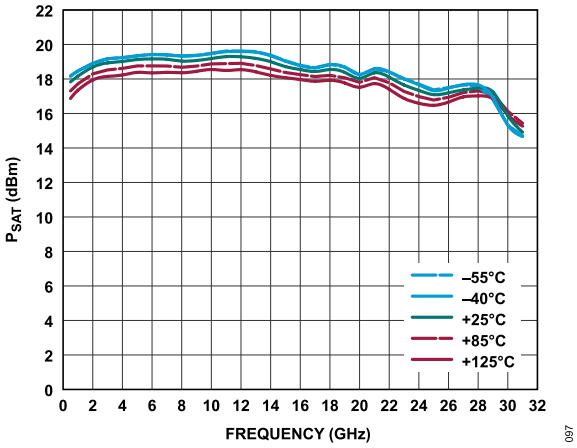

Figure 95. P_{SAT} vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

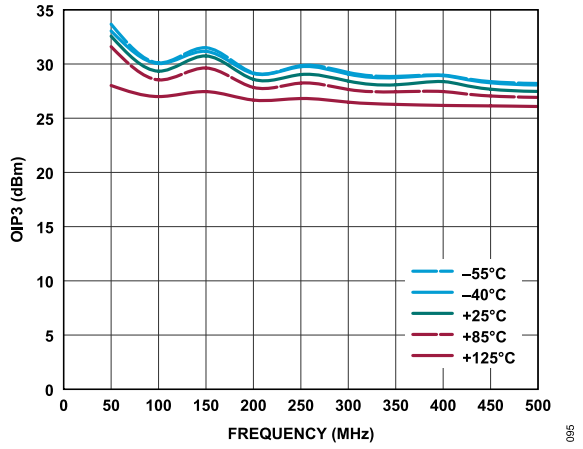

Figure 93. OIP3 vs. Frequency for Various Temperatures, 50MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

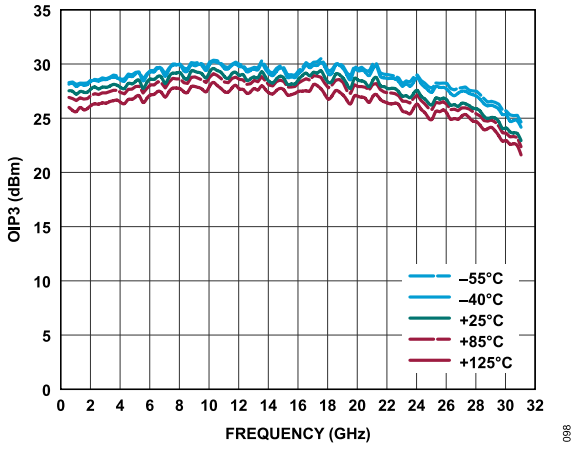

Figure 96. OIP3 vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

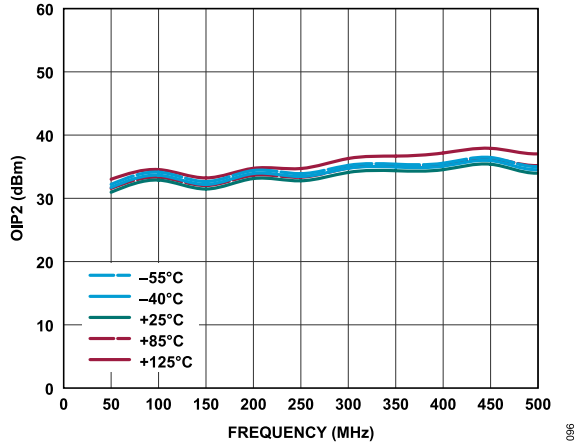

Figure 94. OIP2 vs. Frequency for Various Temperatures, 50MHz to 500MHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

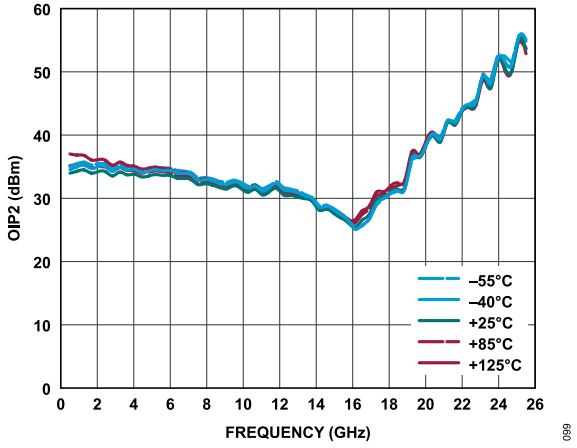

Figure 97. OIP2 vs. Frequency for Various Temperatures, 500MHz to 31GHz, I_{DQ} = 90mA, and R_{BIAS} = 665Ω

TYPICAL PERFORMANCE CHARACTERISTICS

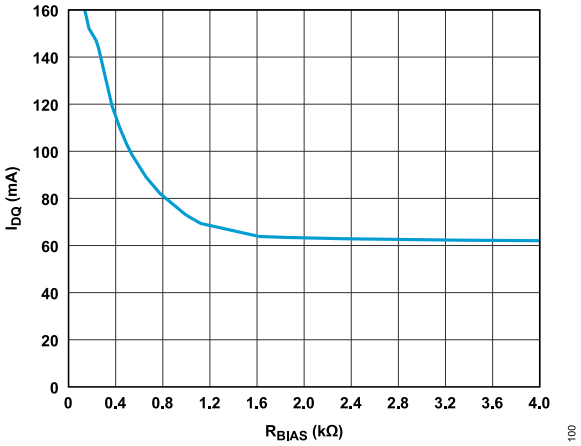

Figure 98. I_{DQ} vs. R_{BIAS}, 0Ω to 4kΩ, Biasing Through the ACG/VDD2 Pin

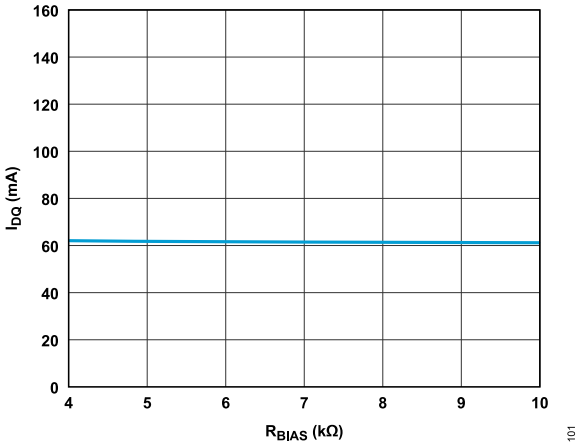

Figure 99. I_{DQ} vs. R_{BIAS}, 4kΩ to 10kΩ, Biasing Through the ACG/VDD2 Pin

THEORY OF OPERATION

The ADL7075 is a wideband LNA that operates from 100MHz to 31GHz. A simplified block diagram is shown in **Figure 100**.

The ADL7075 has DC-coupled, single-ended input and output ports with impedance that is nominally equal to 50Ω over the specified frequency range. AC input and output coupling capacitors and a bias inductor are the only external matching components required. To adjust I_{DQ}, connect an external resistor between the RBIAS and VDDx pins. The RFOUT/VDD1 pin provides the drain current. However, the drain bias voltage can also be resistively biased by connecting the ACG/VDD2 pin to an external supply.

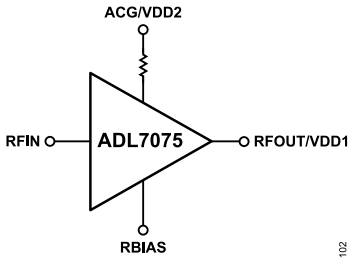

Figure 100. Simplified Schematic

APPLICATIONS INFORMATION

Operation from 10MHz to 31GHz

The basic connections for operating the ADL7075 from 10MHz to 31GHz are shown in **Figure 101**. VDD must be supplied to the RFOUT/VDD pin through a broadband bias tee or external bias network. An external DC block is required at the RF input and output.

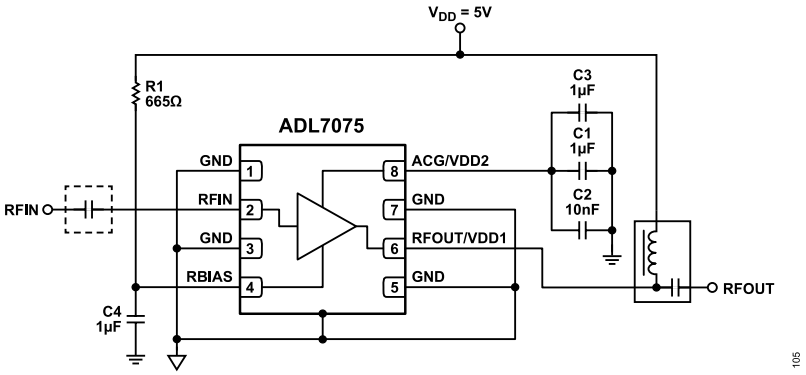

Figure 101. Typical Application Circuit for Operation from 10MHz to 31GHz

The bias conditions, V_{DD} = 5V and I_{DQ} = 90mA, are the recommended operating point to achieve the specified performance. The gain and return loss of this circuit are shown in **Figure 102** and **Figure 103** across frequencies. To set other bias conditions, adjust the R_{BIAS} value. **Table 9** shows the recommended R_{BIAS} values and their associated I_{DQ} values.

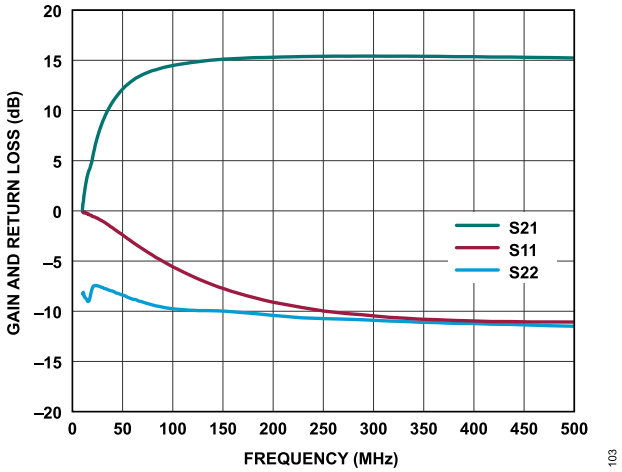

Figure 102. Gain and Return Loss vs. Frequency of 10MHz to 500MHz Application Circuit, V_{DD} = 5V, I_{DQ} = 90mA, R_{BIAS} = 665Ω

APPLICATIONS INFORMATION

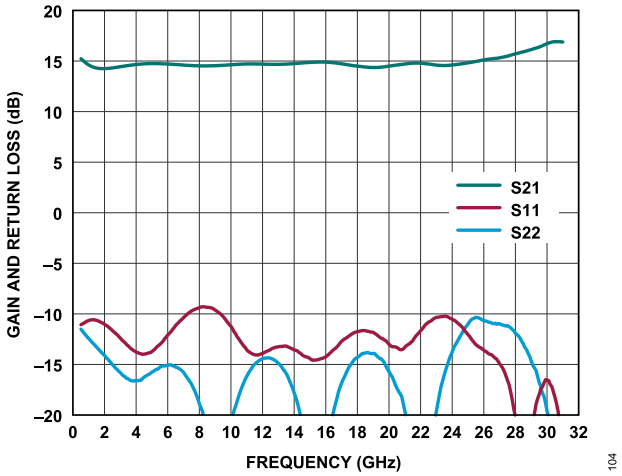

Figure 103. Gain and Return Loss vs. Frequency of 100MHz to 31GHz Application Circuit, 500MHz to 31GHz, V_{DD} = 5V, I_{DQ} = 90mA, R_{BIAS} = 665Ω

Recommended Bias Sequencing

The correct sequencing of the DC and RF power is required to safely operate the ADL7075. During power-up, apply V_{DD} before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before V_{DD} is powered off.

For more information on using the evaluation board, refer to the **EVAL-ADL7075** user guide.

Table 9. Recommended Bias Resistor Values for Various I_{DQ} Values, V_{DD} = 5V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
1850	50	47.8	2.3
1032	70	66	4
665	90	84.5	5.5
502	110	102.6	7.2

Table 10. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 90mA

R_{BIAS} (Ω)	V_{DD} (V)
242	3.0
447	4.0
665	5.0
995	6.0

APPLICATIONS INFORMATION

Providing Drain Bias Through the ACG/VDD2 Pin

An alternative way to bias the ADL7075 is through the ACG/VDD2 pin (Pin 8), which is shown in **Figure 104**. Because of the voltage drop across the internal bias resistor, a higher V_{DD} is required. If a 665Ω bias resistor (R1) is used and connected to the 8.5V power supply, resulting total current is 90mA.

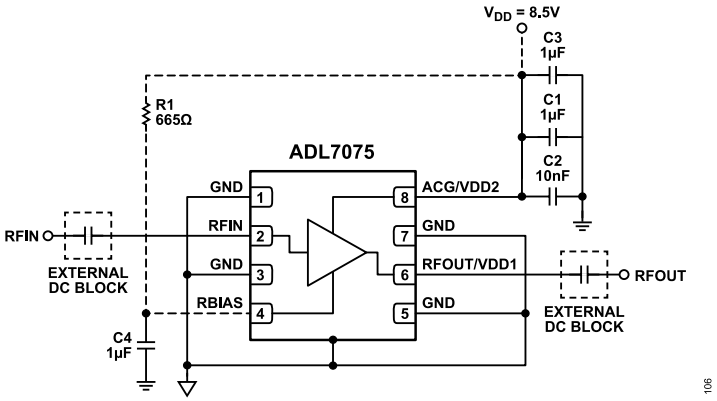

Figure 104. Providing Resistive Drain Bias Through the ACG/VDD2 Pin

Overdrive Recovery Optimization

The overdrive recovery performance of the 100MHz to 31GHz shown in **Figure 77** is the overdrive recovery time performance comparison of the baseline **ADL7075-EVALZ** configuration. External DC blocking capacitor were used during validation, the performance shown in **Figure 105** shows the gain and return loss of that calibrated setup. Main component that effects this metric is the input capacitance on RFIN trace. To reduce the overdrive recovery time, select a smaller value for this capacitor.

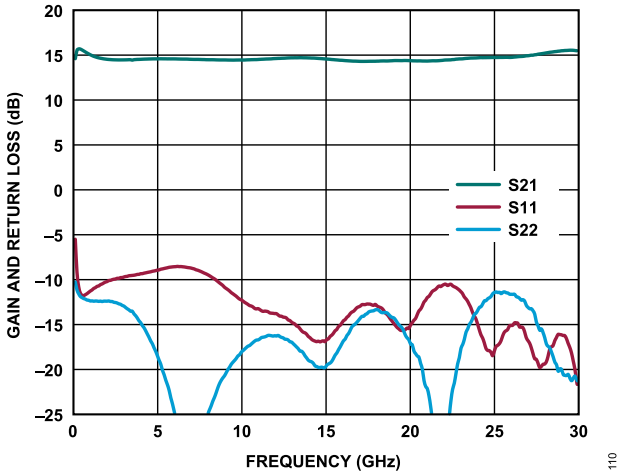

Figure 105. Gain and Return Loss vs. Frequency for ADL7075-EVALZ Overdrive Recovery Time Optimized Circuit, 100MHz to 31GHz, V_{DD} = 5V, R_{BIAS} = 665Ω

APPLICATIONS INFORMATION

Recommended Power Management Circuit

Figure 106 shows a recommended power management circuit for the ADL7075. The **LT8607** step-down regulator is used to step down a 12V rail to 4.5V that is then applied to the **LT3042** low dropout (LDO) linear regulator to generate a low noise 3.3V output. Even though the circuit shown in **Figure 106** has an input voltage (V_{IN}) of 12V, the input range to the LT8607 can be as high as 42V.

The 4.5V regulator output of the LT8607 is set by the R2 and R3 resistors, according to the following equation:

$R2 = R3((V_{OUT}/0.778V) - 1)$
where V_{OUT} is the output voltage.

The switching frequency (f_{SW}) is set to 2MHz by the 18.2kΩ resistor (R1) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2MHz to 2.200MHz.

The V_{OUT} of the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$V_{OUT} = 100\mu A \times R4$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 3.3V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more tolerance (5%). Therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 3.3V output to give a convenient 0V to 3.6V voltage range. **Table 11** provides the recommended resistor values for operation at 3.6V to 3V.

Table 11. Recommended Resistor Values for Operating at 3.6V to 3V

LDO V_{OUT} (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
3.6	36.5	332	30.1
3.3	33.1	301	30.1
3	30.1	267	30.1

The LT8607 can source a maximum current of 750mA, and the LT3042 can source a maximum current of 200mA. If the 5V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The **LT8608** and **LT8609** step-down regulators can source a maximum current to 1.5A and 3A, respectively, and these devices are pin compatible with the LT8607. The **LT3045** linear regulator, which is pin compatible with LT3042, can source a maximum current to 500mA.

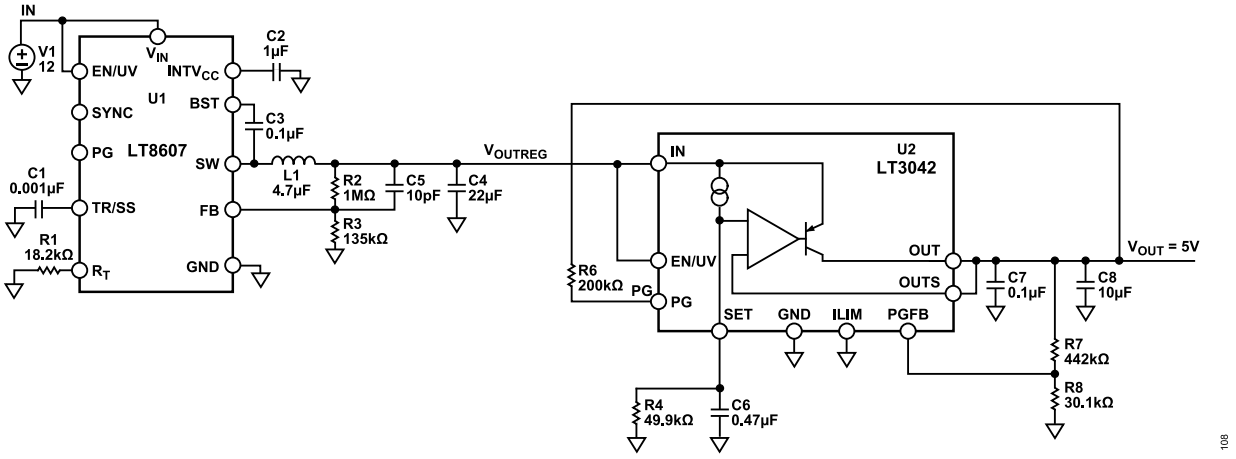

Figure 106. Recommended Power Management Circuit

OUTLINE DIMENSIONS

PACKAGE DRAWING (OPTION)	PACKAGE TYPE	PACKAGE DESCRIPTION
CP-8-30	LFCSP	8-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to **Package Index**.

Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE OPTION
ADL7075ACPZ	−55°C to +125°C	8-lead LFCSP, 2mm × 2mm × 0.85mm	Tape, 1	CP-8-30
ADL7075ACPZ-R7	−55°C to +125°C	8-lead LFCSP, 2mm × 2mm × 0.85mm	Reel, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

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