40dB Gain, 1500MHz to 2700MHz Transmit Amplifier

FEATURES

- 2-stage, high-linearity transmit amplifier for RF DACs, transceivers, and SoCs to power amplifier interfaces
- Excellent gain stability and flatness over temperature
- Single 5.0V supply
- Power gain: 40.0dB
- OIP3: 40.0dBm
- OIP2: 50.0dBm
- Noise figure: 4.0dB
- OP1dB: 26.0dBm
- ENP pin enables and disables within 50ns
- 100Ω and 50Ω differential inputs and 50Ω single-ended output
- DC current can be adjusted by external resistors
- 16-lead, 3mm × 3mm LFCSP

APPLICATIONS

- 4G, LTE, and 5G in frequency division duplex (FDD) and time division duplex (TDD) broadband
- Macro, micro, remote radio head (RRH) and massive, multiple-input and multiple-output (mMIMO) communication systems

FUNCTIONAL BLOCK DIAGRAM

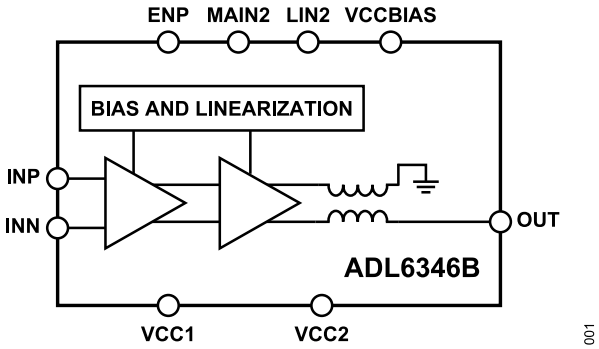

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADL6346B is a transmit two-stage differential amplifier that provides an interface from RF digital-to-analog converters (DACs), RF transceivers, and systems on a chip (SoC) to power amplifiers. The ADL6346B also includes an integrated impedance matching and an integrated RF balun so that it can be configured as a differential input, single-ended output to allow high-performance RF capabilities in desired frequency ranges.

To optimize performance vs. power level, the ADL6346B includes the ability to adjust the DC operating and linearization currents using external resistors.

The ADL6346B is manufactured on an advanced silicon germanium (SiGe), bipolar complementary metal-oxide semiconductor (BiCMOS) process.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

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REVISION HISTORY

3/2026—Revision 0: Initial Version

SPECIFICATIONS

VCC1 voltage (V_{CC1}) = VCC2 voltage (V_{CC2}) = VCCBIAS voltage (V_{CCBIAS}) = 5.0V, T_{CASE} = 50°C, input power (P_{IN}) = −24dBm (–27dBm per tone for two tones), source resistance (R_S) = 100Ω, load resistance (R_L) = 50 Ω, bias resistor (R_{BIAS}) = 150Ω, and linearizer resistor (R_{LIN}) = 1kΩ, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		1500		2700	MHz
Power Gain			40.0		dB
NOISE AND LINEARITY PERFORMANCE					
Output 1dB Compression Point (OP1dB)			26.0		dBm
Output Second-Order Intercept (OIP2)			50.0		dBm
Output Third-Order Intercept (OIP3)			40.0		dBm
Noise Figure			4.0		dB
RF INPUT AND OUTPUT CHARACTERISTICS					
Input					
Impedance	Differential		100		Ω
Return Loss	In-band, see the RF Input and Output section		15		dB
Output					
Impedance	Single-ended		50		Ω
Return Loss	In-band		13		dB
GAIN FLATNESS					
Over ±200MHz Bandwidth			±0.1		dB
Over ±400MHz Bandwidth			±0.2		dB
SETTLING TIME					
Disable to Enable			50		ns
Enable to Disable			50		ns
POWER SUPPLY					
Voltage		4.75	5.0	5.25	V
Supply Current			440		mA
Power-Down Current			2		mA
DIGITAL LOGIC					
Input Voltage	ENP				
High (V_{IH})		1.07			V
Low (V_{IL})				0.68	V
Input Current					
High (I_{IH})				−100	µA
Low (I_{IL})				100	µA

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
V_{CC1}, V_{CC2}, V_{CCBIAS}	−0.3V to +5.6V
ENP	−0.3V to +3.6V
RF Input Power (INN and INP) at 100Ω	10dBm
Temperature	
Operating Range for Continuous Operation (Measured at Exposed Pad)	−40°C to +115°C
Operating Range[1] (Measured at Exposed Pad)	−40°C to +125°C
Storage Range	−65°C to +150°C

[1] Operation up to 125°C is supported but can impact the operating lifetime of the device. To avoid a reduction in operating lifetime when operating at more than 115°C, the device must operate at a paddle temperature at less than 115°C for a period. Contact Analog Devices, Inc., Support for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the conduction thermal resistance from junction to case where the T_{CASE} is measured at the bottom of the package.

The thermal resistance value specified in Table 3 is simulated based on JEDEC specifications and must be used in compliance with JESD51-12.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CR-16-1	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

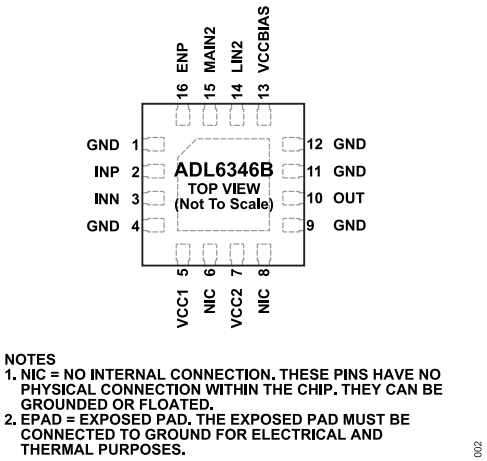

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4, 9, 11, 12	GND	Input and output	Ground.
2	INP	Input	Positive RF Input.
3	INN	Input	Negative RF Input.
5	VCC1	Input	Amplifier 1 Analog Power Supply (5.0V).
6, 8	NIC		No Internal Connection. These pins have no physical connection within the chip. They can be grounded or floated.
7	VCC2	Input	Amplifier 2 Analog Power Supply (5.0V).
10	OUT	Output	Single-Ended RF Output.
13	VCCBIAS	Input	Bias Circuitry Analog Power Supply (5.0V).
14	LIN2	Input	Linearizer Bias Set Resistor.
15	MAIN2	Input	Main Amplifier Bias Set Resistor.
16	ENP	Input	Amplifier Enable.
	EPAD	Input and output	Exposed Pad. The exposed pad must be connected to ground for electrical and thermal purposes.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC1} = V_{CC2} = V_{CCBIAS} = 5.0V, T_{CASE} = 50°C, P_{IN} = −24dBm (−27dBm per tone for two tones), R_S = 100Ω, R_L = 50Ω, R_{BIAS} = 150Ω, and R_{LIN} = 1kΩ, unless otherwise noted.

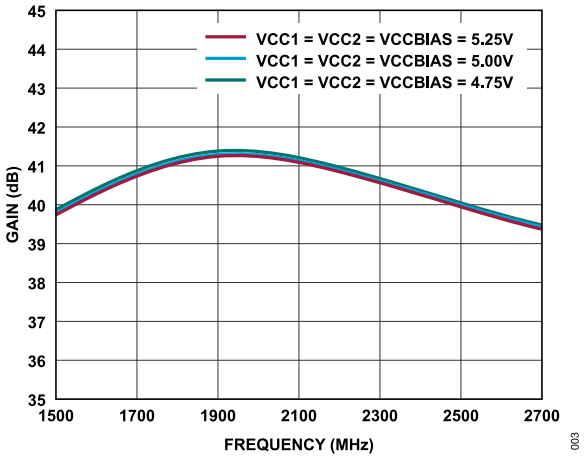

Figure 3. Gain vs. Frequency for Various Supplies

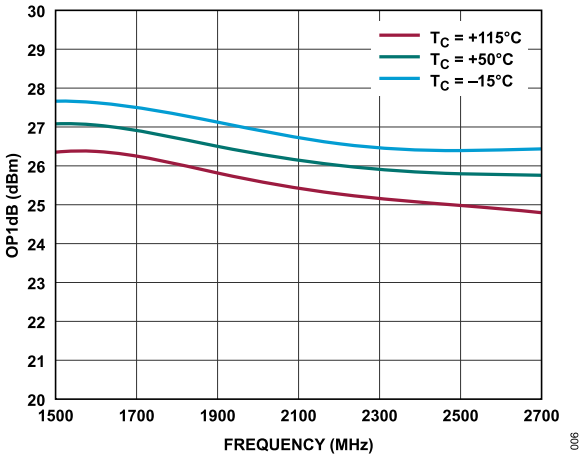

Figure 6. OP1dB vs. Frequency for Various Temperatures

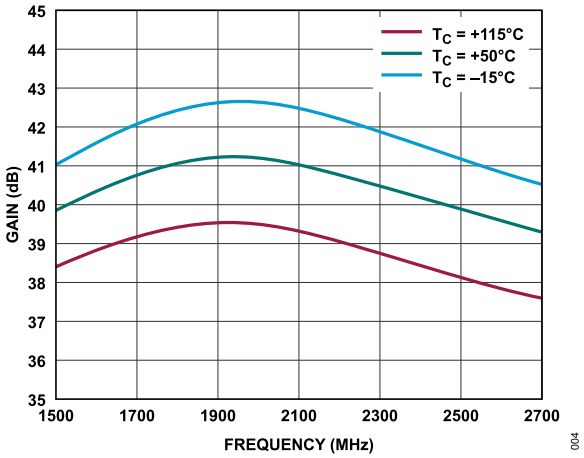

Figure 4. Gain vs. Frequency for Various Temperatures

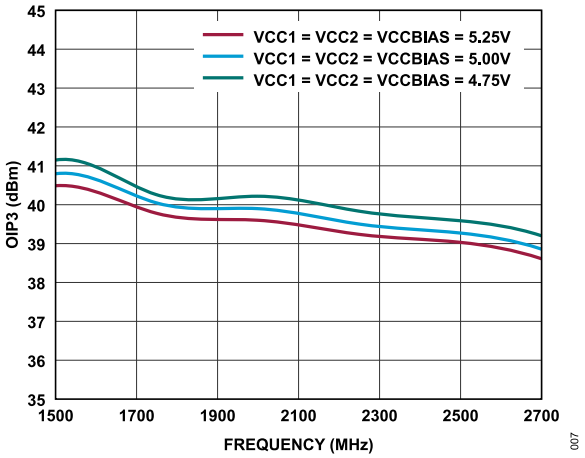

Figure 7. OIP3 vs. Frequency for Various Supplies

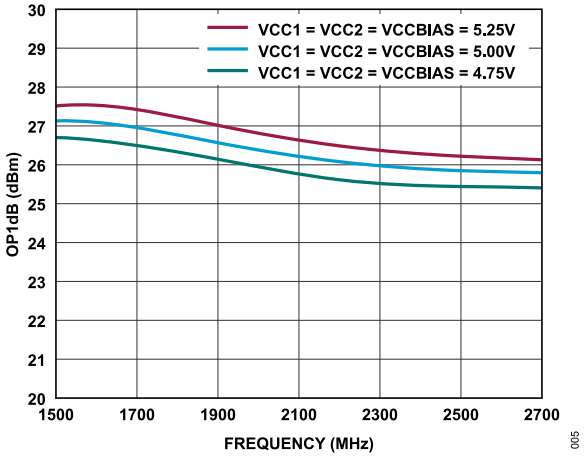

Figure 5. OP1dB vs. Frequency for Various Supplies

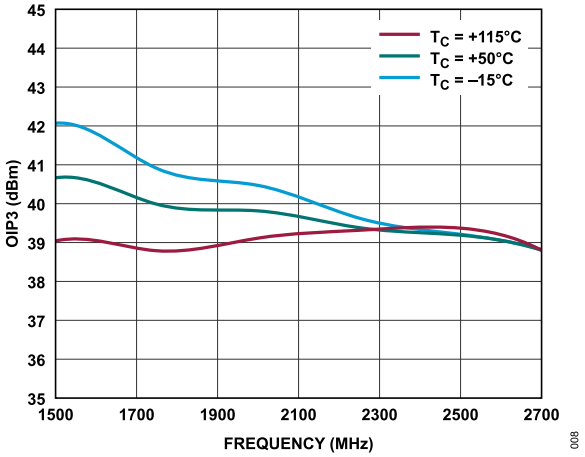

Figure 8. OIP3 vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

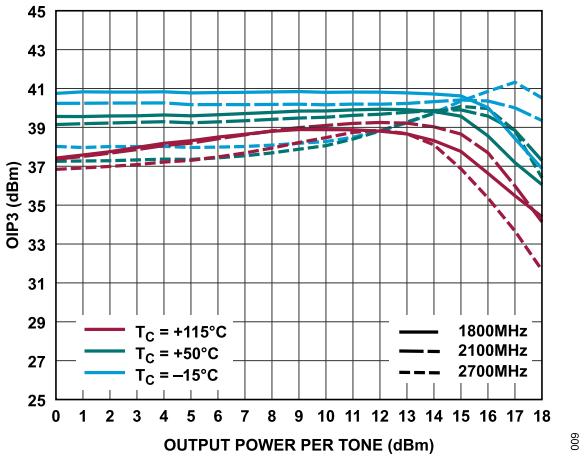

Figure 9. OIP3 vs. Output Power Per Tone for Various Temperatures at 1800MHz, 2100MHz, and 2700MHz

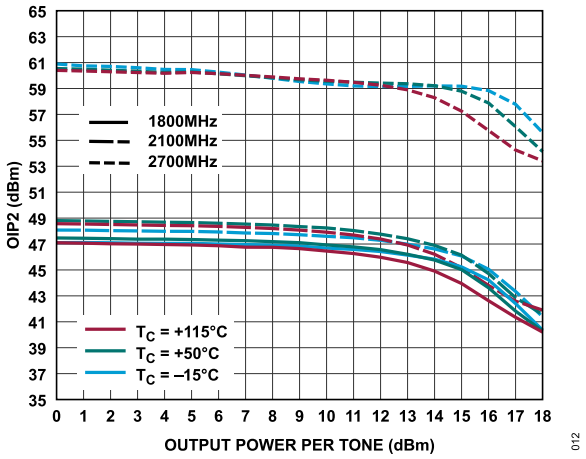

Figure 12. OIP2 vs. Output Power per Tone for Various Temperatures at 1800MHz, 2100MHz, and 2700MHz

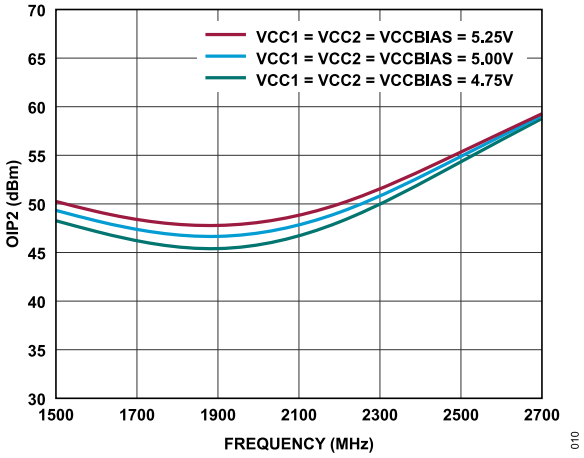

Figure 10. OIP2 vs. Frequency for Various Supplies

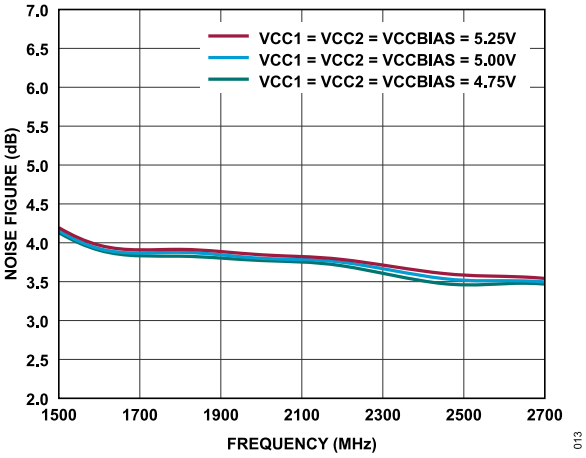

Figure 13. Noise Figure vs. Frequency for Various Supplies

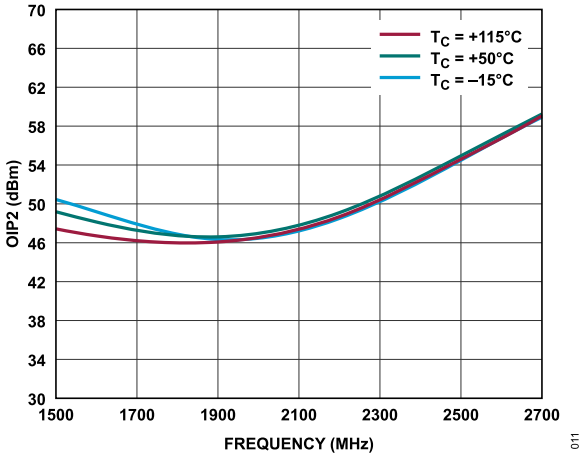

Figure 11. OIP2 vs. Frequency for Various Temperatures

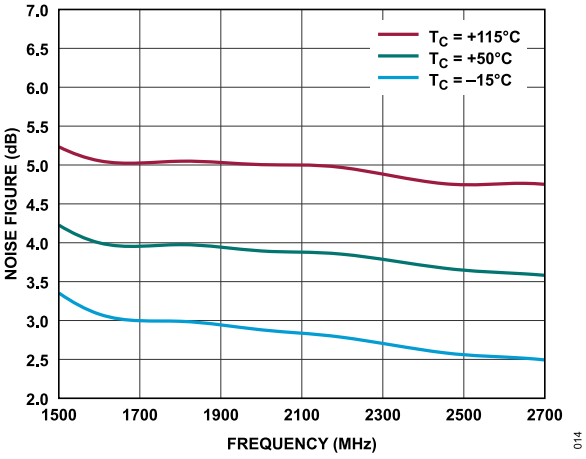

Figure 14. Noise Figure vs. Frequency for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

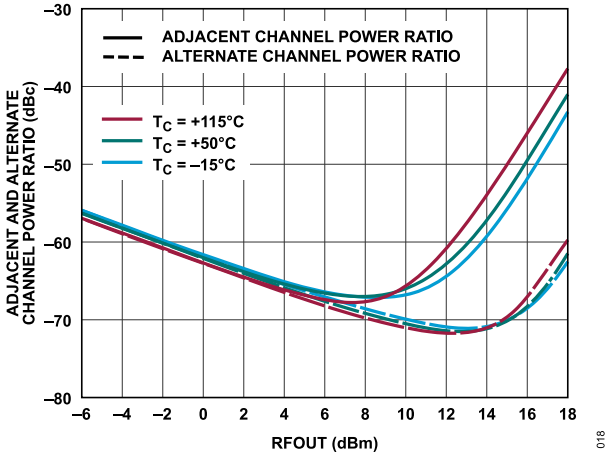

Figure 15. Adjacent and Alternate Channel Power Ratio vs. RF Output Power (RFOUT) over Temperature at 1800MHz, Long-Term Evolution (LTE) Test Model 1.1 (TM1.1), 5MHz

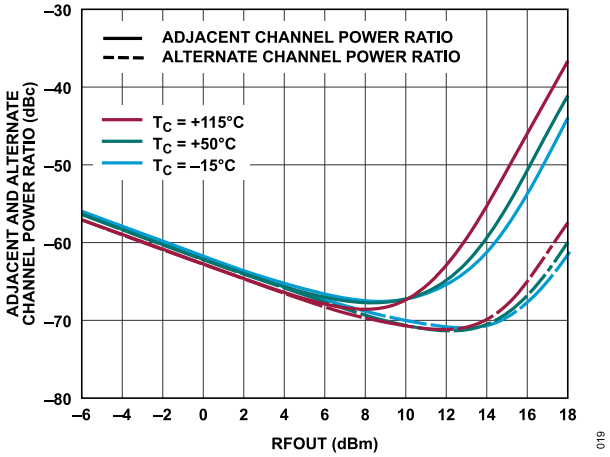

Figure 16. Adjacent and Alternate Channel Power Ratio vs. RF Output Power (RFOUT) over Temperature at 2100MHz, LTE Test Model 1.1 (TM1.1), 5MHz

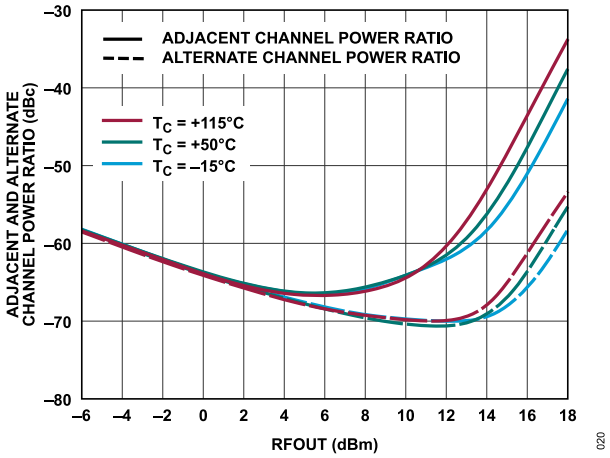

Figure 17. Adjacent and Alternate Channel Power Ratio vs. RF Output Power (RFOUT) over Temperature at 2700MHz, LTE Test Model 1.1 (TM1.1), 5MHz

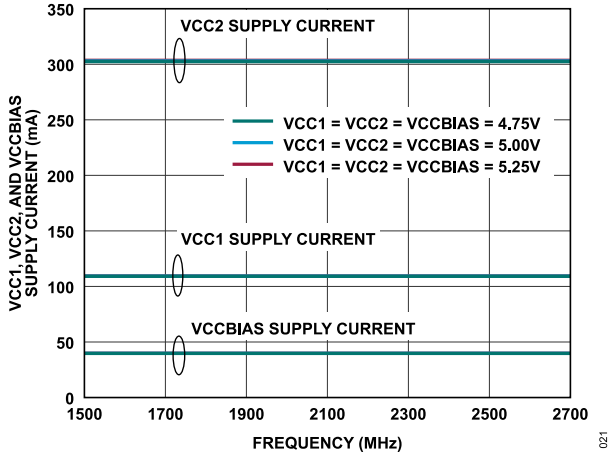

Figure 18. VCC1, VCC2, and VCCBIAS Supply Current vs. Frequency for Various Supplies

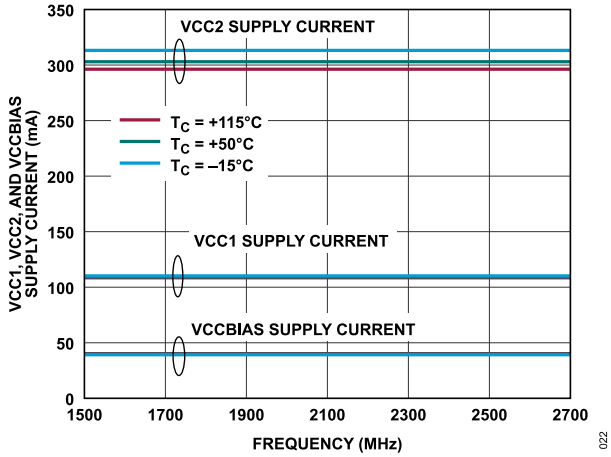

Figure 19. VCC1, VCC2, and VCCBIAS Supply Current vs. Frequency for Various Temperatures

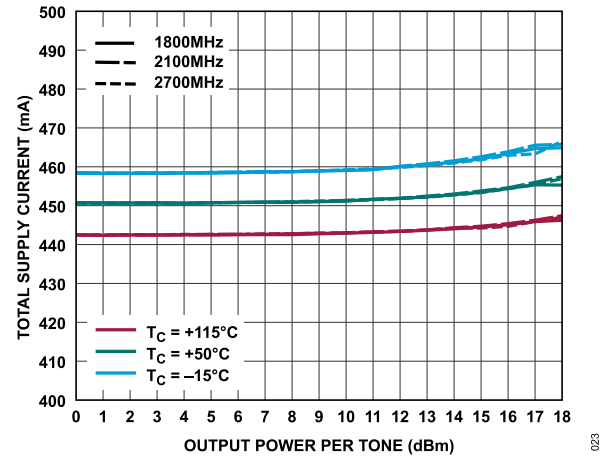

Figure 20. Total Supply Current vs. Output Power per Tone for Various Temperatures at 1800MHz, 2100MHz, and 2700MHz

TYPICAL PERFORMANCE CHARACTERISTICS

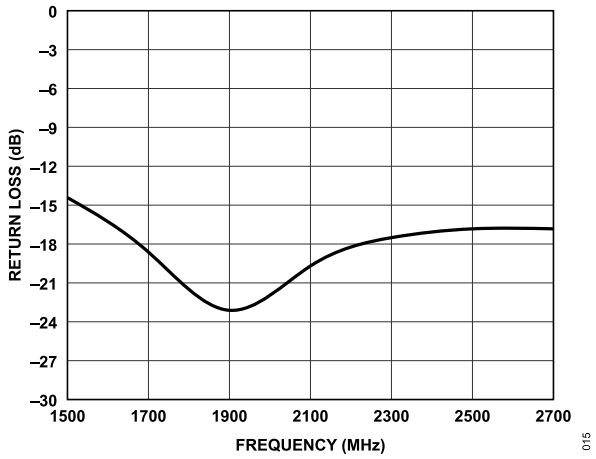

Figure 21. Return Loss of Differential RF Input S11 at 100Ω Match

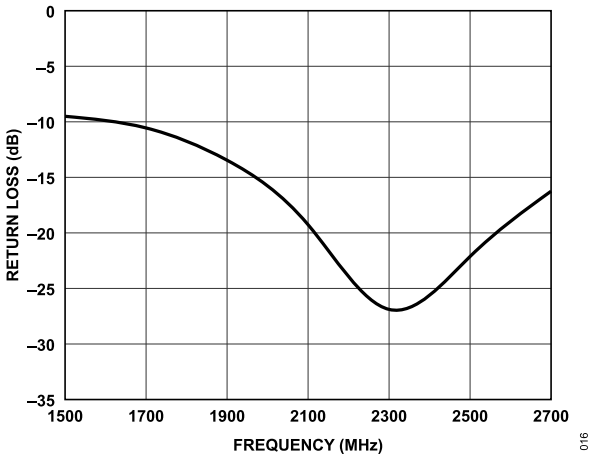

Figure 22. Return Loss of Single-Ended RF Output S22 at 50Ω Match

THEORY OF OPERATION

The ADL6346B is a highly integrated transmit amplifier used to interface an RF transceiver, RF DAC, or RF SoC to the power amplifier in a transmitter.

The ADL6346B requires only three pairs of bypass capacitors and two current set resistors. All impedance matching components are internal. Additionally, the balun is also integrated within the package.

The ADL6346B targets high-dynamic range, multicarrier transmitter designs. The signal path through the device starts with differential inputs, which are nominally at 100Ω; however, the inputs can be easily matched to 50Ω differential systems, if desired. The input signals are connected to a pair of fully differential, linearized amplifiers. The first stage is fixed biased, but the main current to the second stage can be adjusted by changing the value of the off-chip, surface-mounted device (SMD) resistor on the PCB. Additionally, the linearization can be optimized for a specific range of frequencies using another SMD resistor. After amplification, the output signal is applied to a low-loss integrated balun to provide a single-ended 50Ω output. The integrated output saves substantial board space, reduces the total bill of materials (BOM) cost, and eliminates another potential source of radiation or channel-to-channel isolation degradation. The integrated balun is shielded and results in minimum coupling to adjacent amplifiers. When implementing the ADL6346B in a multiple transceiver system, the channel-to-channel isolation is usually limited by the PCB routing rather than the proximity of these amplifiers.

RF INPUT AND OUTPUT

The input impedance is 100Ω differential, and the output impedance is 50Ω single-ended, to allow the ADL6346B to be driven by the DAC. In addition, the 50Ω differential inputs can be achieved with external matching networks. See the Input Port Matching section for additional information.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 23 shows the basic connections, and Table 5 gives uses additional details on these connections.

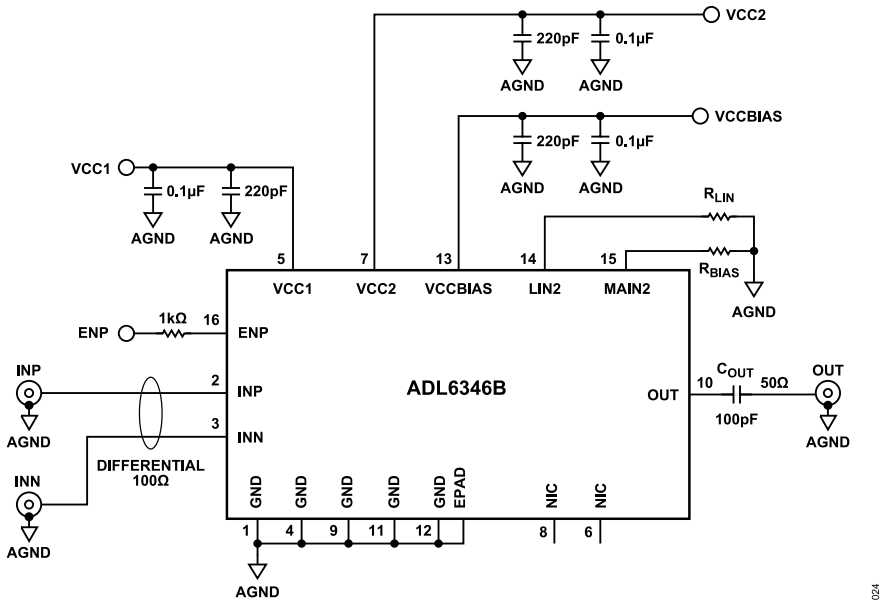

Figure 23. Basic Connections

Table 5. Basic Connections

Functional Blocks	Pin No.	Mnemonic	Description	Basic Connection
5V	5, 7	VCC1, VCC2	Amplifiers, analog supply voltage, 5V.	Decouple these pins via 220pF and 0.1µF capacitors to ground. Ensure that the decoupling capacitors are located close to these pins.
	13	VCCBIAS	Bias circuitry power supply (5.0V).	Decouple this pin via 220pF and 0.1µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
RF Inputs	2, 3	INP, INN	RF inputs.	Differential RF inputs.
RF Output	10	OUT	RF output.	RF output, single-ended.
Device Enable	16	ENP	Active high for normal operation.	Connect this pin with a series 1kΩ resistor.
Linearizer, Main Bias	14, 15	LIN2, MAIN2	Current set resistors R_{LIN} and R_{BIAS}.	Connect a resistor from each of these pins to ground to set the quiescent DC current and optimize the linearization current.
Ground	1, 4, 9, 11, 12	GND	Ground.	Connect these pins to the ground of the printed circuit board.
Exposed Pad	EPAD	EPAD	Exposed pad.	Exposed Pad 1. The exposed pad must be connected to ground for electrical and thermal purposes.
NIC	6, 8	NIC	No internal connection.	These pins have no physical connection within the chip. They can be grounded or floated.

APPLICATIONS INFORMATION

INPUT PORT MATCHING

The ADL6346B does not require external matching components for a 100Ω input impedance to achieve the return loss specification. However, external matching components are required for 50Ω source matching, if desired (see Figure 24). The input return loss with and without the matching circuit is shown in Figure 25. Note that the matching components can be changed due to the board structures and materials.

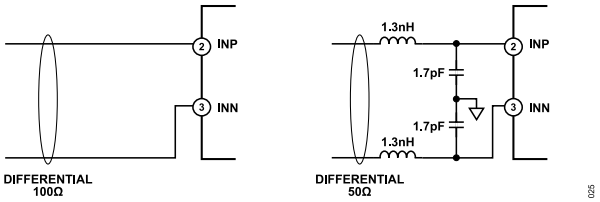

Figure 24. Input Matching Components for the ADL6346B

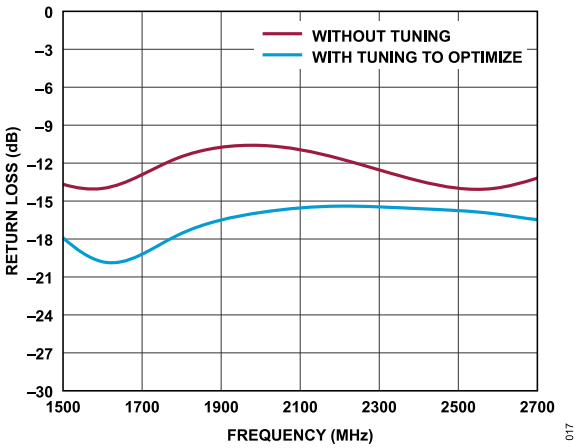

Figure 25. Return Loss of Differential RF Input S11 at 50Ω Match; 1.3nH in Series and 1.7pF in Shunt on Each Input

OUTPUT PORT CONNECTION

The RF output port is DC-coupled so that an external DC blocking capacitor (C_{OUT}) is required, see Figure 23.

APPLICATIONS INFORMATION

PERFORMANCE AND POWER OPTIMIZATION

The DC power consumption of the ADL6346B can be optimized with the power dissipation settings, see Figure 26. The OIP3 and the OP1dB performance can be adjusted accordingly, see Figure 27 and Figure 28.

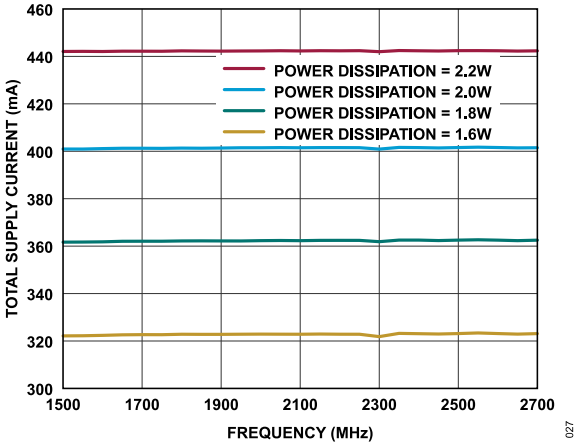

Figure 26. Total Supply Current vs. Frequency for Various Power Dissipation Settings

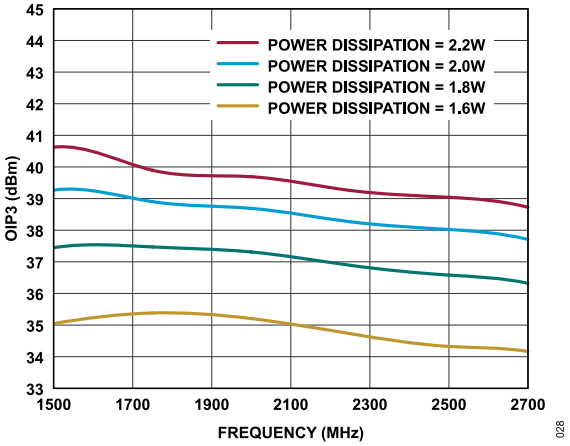

Figure 27. OIP3 vs. Frequency for Various Power Dissipation Settings

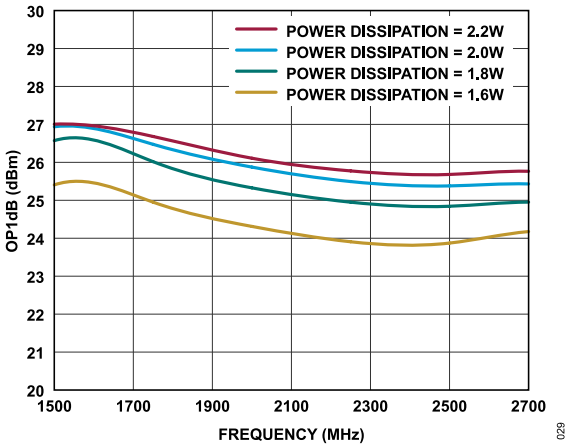

Figure 28. OP1dB vs. Frequency for Various Power Dissipation Settings

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CR-16-1	LFCSP_RT	16-Lead Lead Frame Chip Scale Package, Routable

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL6346ACRZB	−40°C to +115°C	16-Lead LFCSP_RT (3mm × 3mm × 0.65mm)	Cut-Tape, 750	CR-16-1
ADL6346ACRZB-R7	−40°C to +115°C	16-Lead LFCSP_RT (3mm × 3mm × 0.65mm)	Reel, 750	CR-16-1
ADL6346ACRZB-RL	−40°C to +115°C	16-Lead LFCSP_RT (3mm × 3mm × 0.65mm)	Reel, 2500	CR-16-1

[1] Z = RoHS Compliant Part.