FEATURES

- Broadband TxVGA interfacing RF-DAC to beamformer and PA
- Operating frequency range: 0.38 GHz to 12 GHz, 2 product variants
  - ADL6331-A: 0.38 GHz to 8 GHz
  - ADL6331-B: 1.0 GHz to 12 GHz
- Optimizes common-mode rejection of RF-DAC, even-order harmonics, and intermodulation
- 50 Ω differential inputs and 50 Ω single-ended outputs
- Integrated broadband RF output balun
- 70 dB of gain control range in 1 dB step
- RF DSA range: 24.0 dB with 1.0 dB step
- Amplifier bypass loss of 12 dB each
- Asynchronous toggle between multiple pre-defined attenuation values and bypass amplifier stages
- Power gain at 4 GHz: 15.1 dB (ADL6331-A), 15.4 dB (ADL6331-B)
- Noise figure at 4 GHz: 7.5 dB (ADL6331-A), 7.5 dB (ADL6331-B)
- OIP3 at 4GHz: 31.0 dBm (ADL6331-A), 31.0 dBm (ADL6331-B)
- OIP2 at 4GHz: 58 dBm (ADL6331-A), 56 dBm (ADL6331-B)
- OP1dB at 4GHz: 12.4 dBm (ADL6331-A), 12.0 dBm (ADL6331-B)
- Fully programmable through a 3-/4-wire SPI
- Single 3.3 V supply
- 24-terminal, 4.0 mm x 4.0 mm LGA

APPLICATIONS

- Aerospace and defense
- Instrumentation and test equipment
- Communication system

GENERAL DESCRIPTION

The ADL6331 transmit variable gain amplifier (TxVGA) provides an interface from RF digital-to-analog converters (RF-DACs) to a single-ended power amplifier (PA) signal chain. Each ADL6331 IC is composed of a balun, two differential RF amplifiers with bypass attenuators, and a digital step attenuator (DSA) to provide suitable transmitter performance in a 24-terminal, 4.0 mm x 4.0 mm LGA package.

Serial-port interface (SPI) control is available to configure RF signal path or to optimize supply current vs. performance.

An integrated RF balun is used to provide a single-ended output over 0.38 GHz to 8.0 GHz (ADL6331-A) or 1.0 GHz to 12.0 GHz (ADL6331-B) with good impedance match.

Table 1. ADL6331 Frequency Ranges

<table>
<thead>
<tr>
<th>ADL6331 Variant</th>
<th>Frequency Range (GHz)</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>0.38 to 8.0</td>
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<tr>
<td>B</td>
<td>1.0 to 12.0</td>
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</tbody>
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FUNCTIONAL BLOCK DIAGRAM

![Figure 1. Functional Block Diagram](image-url)