# Robust, Industrial, Low Latency and Low Power 10/100/1000 Mbps Ethernet PHY with Copper and Fiber Interface

## FEATURES

- 1 Gb Ethernet PHY IEEE 802.3 compliant
  - Support Copper and Fiber Interface
  - 10BASE-T/100BASE-TX/1000BASE-T
  - 100BASE-FX/1000BASE-X, and 1000BASE-KX
  - Media converter mode between Copper and Fiber
  - Bridge mode between RGMII and SGMII
- MII, RMII, RGMII, and SGMII MAC interfaces
- Low latency performance
  - 1000BASE-T RGMII latency transmit <70 ns, receive <230 ns
  - 100BASE-TX MII latency transmit <55 ns, receive <250 ns
- Wake-on-LAN (WoL)
- EEE in accordance with IEEE 802.3az
- EMC tests standards
  - IEC 61000-4-5 surge
  - IEC 61000-4-4 electrical fast transient (EFT)
  - IEC 61000-4-2 ESD
  - IEC 61000-4-6 conducted immunity
  - IEC 61000-4-3 radiated immunity
  - EN55032 radiated and conducted emissions
- Unmanaged configuration using multilevel pin strapping
- MDIO/MDC management interface and interrupt pin
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Voltage mode MDI drivers, eliminates termination resistors
- Automatic polarity and pair swap correction
- Cable diagnostics (TDR and signal analysis)
- Frame generator and checker, multiple loopback modes
- 3 × Configurable LEDs
- 48-lead, 7 mm × 7 mm LFCSP small package, at −40°C to +105°C ambient operation
- Low power consumption
  - 91.5 mW for 1000BASE-X
  - 336.5 mW for 1000BASE-T
  - 3.3 V/2.5 V/1.8 V MDIO and MAC interface VDDIO supply
  - Integrated power supply monitoring and POR

## APPLICATIONS

- Energy Distribution and Energy Automation
- Robotics/Motion Control
- Factory Automation and Industrial Automation
- Test and measurement

## GENERAL DESCRIPTION

The ADIN1320 is a low-power, single-port Gigabit Ethernet transceiver that supports copper, fiber, and backplane Ethernet connectivity. Its key features include low latency and energy-efficient operation, making it an excellent choice for a wide range of industrial Ethernet applications where performance and power efficiency are critical.

It integrates a high-performance Energy Efficient Ethernet (EEE) PHY core along with a robust SerDes subsystem, enabling operation over 10BASE-T, 100BASE-TX, 1000BASE-T, 100BASE-FX, 1000BASE-X, and 1000BASE-KX physical layers. The device supports multiple MAC-side interfaces including SGMII, RGMII, RMII, and MII; and enables a variety of operating modes such as SGMII/RGMII/RMII/MII to Copper, RGMII/RMII/MII to Fiber, RGMII/RMII/MII to copper-or-fiber automatic media selection Copper to Fiber media conversion, and SGMII to RGMII bridging. This versatility allows the ADIN1320 to function as a copper PHY, fiber PHY, mixed-media PHY, media converter, or MAC-interface bridge depending on system requirements.

The MII management interface (MDIO) provides a 2-wire serial connection between a host processor or MAC and the ADIN1320, enabling access to control and status registers within the PHY Core, SerDes subsystem, and GE subsystem. It supports both IEEE 802.3 Clause 22 and Clause 45 frame structures, ensuring compatibility with a wide range of Ethernet controllers and systems.

The ADIN1320 is offered in a compact 7 mm x 7 mm, 48-lead lead frame chip scale package (LFCSP) making it suitable for space-constrained designs. It operates from two power supplies (0.9 V and 3.3 V), with flexible VDDIO options (1.8 V, 2.5 V, or 3.3 V) for MDIO and MAC interfaces. On power-up, the device remains in hardware reset until all supply voltages exceed their required thresholds. Integrated brown-out protection holds the device in reset if supply voltages fall below minimum levels, and it resumes operation automatically once conditions are restored.

The ADIN1320 supports copper cables up to 150m at 1 Gbps and 180m at 100 or 10 Mbps. Note that throughout this data sheet, multifunction pins, such as XTAL_I/CLK_IN/REF_CLK, are referred to either by the entire pin name or by a single function of the pin, for example, XTAL_I/CLK_IN, when only that function is relevant.

For up to date information on the production release timelines, contact your local Analog Devices, Inc., sales representatives or send an email to adin1320@analog.com.


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## FUNCTIONAL BLOCK DIAGRAM

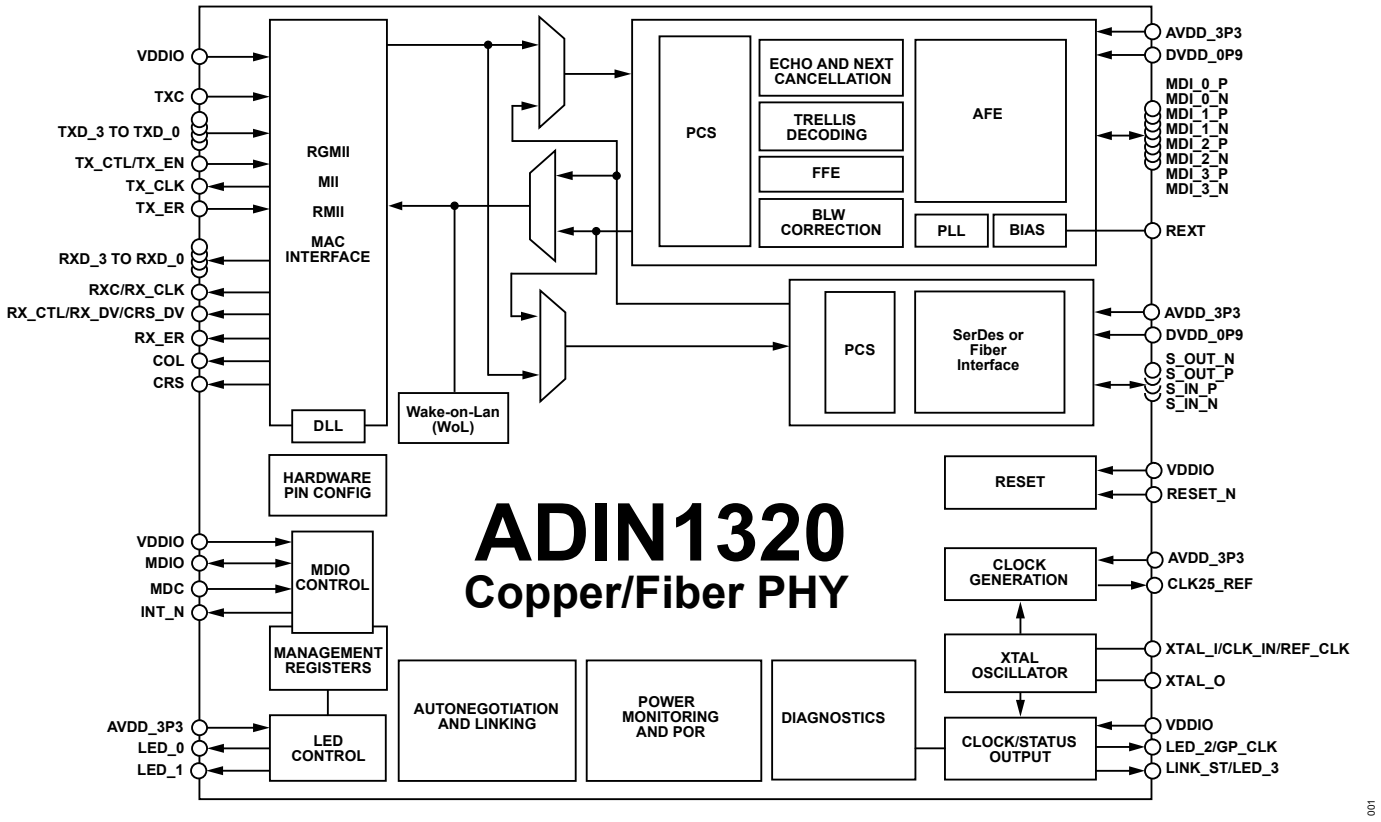


*Figure 1. ADIN1320 Functional Block Diagram.*

## OPERATING MODES

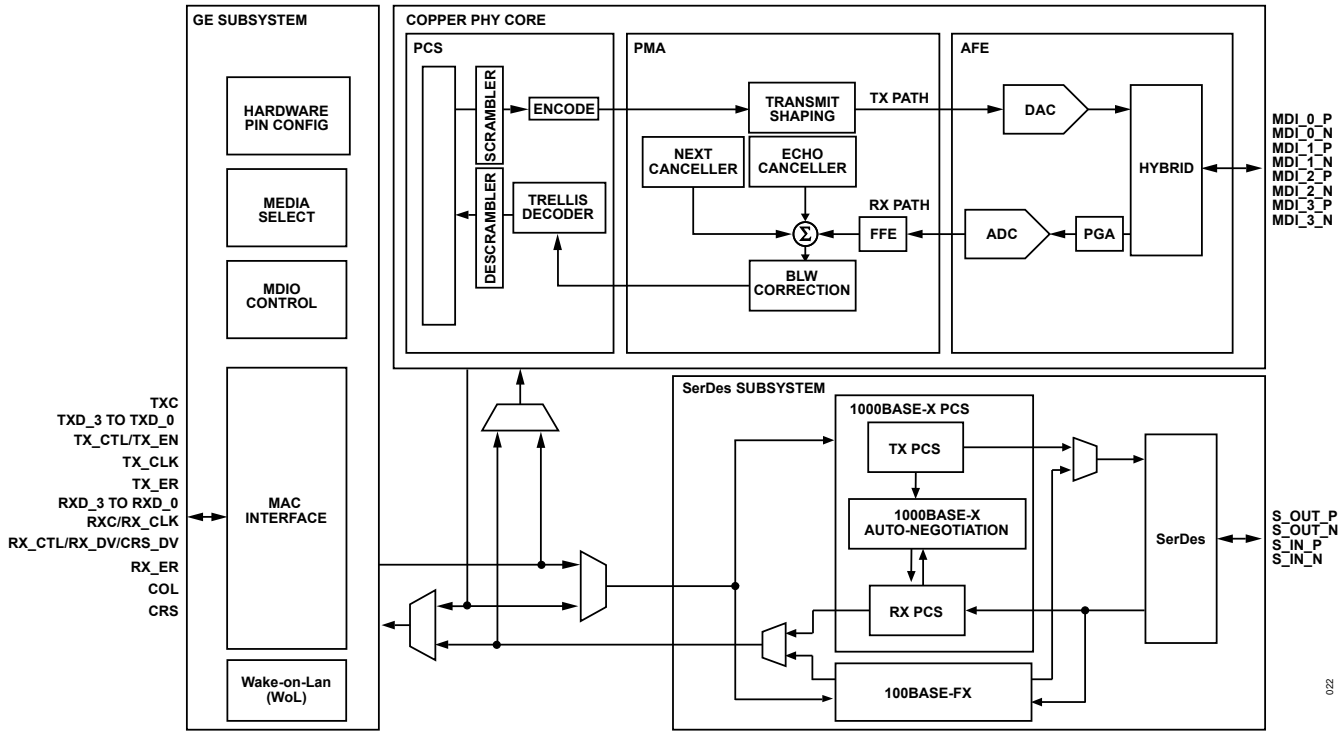


*Figure 2. Simplified Channel Block Diagram (Copper or Fiber Auto-Media Detect)*

## FUNCTIONAL BLOCK DIAGRAM

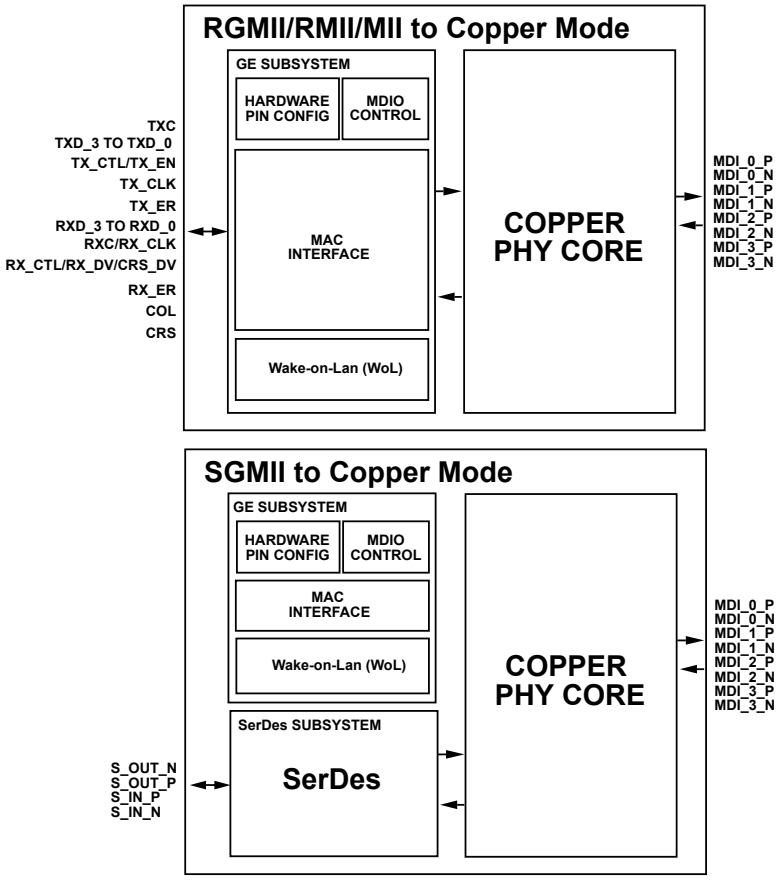


*Figure 3. SGMII/RGMII/RMII/MII to Copper Modes*

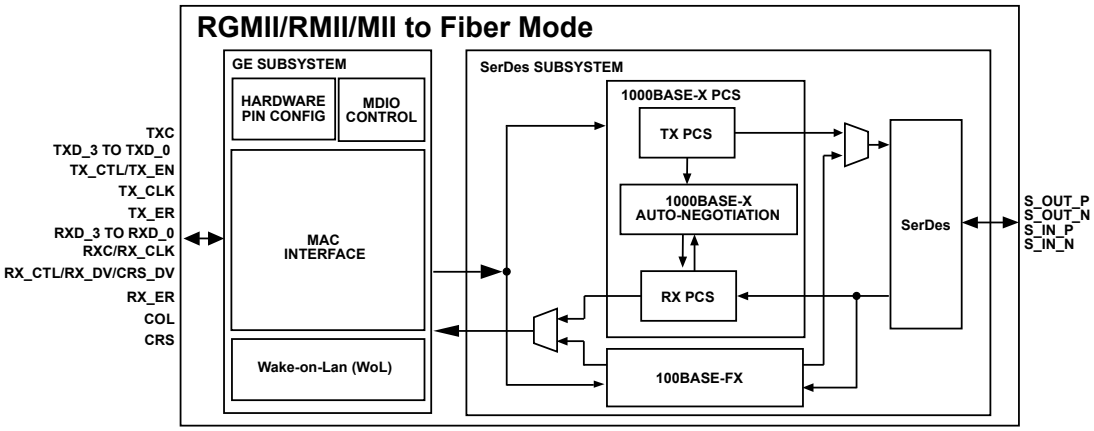


*Figure 4. RGMII/RMII/MII to Fiber Modes*

## FUNCTIONAL BLOCK DIAGRAM

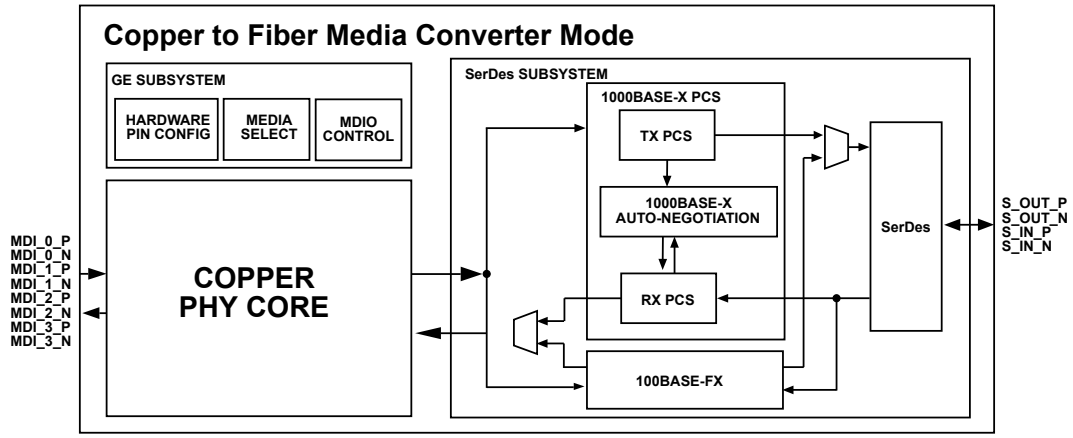


*Figure 5. Copper-Fiber Media Converter Mode*

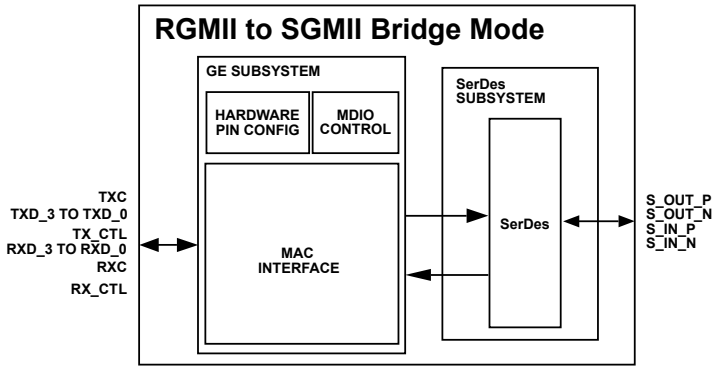


*Figure 6. SGMII-RGMII Bridge Mode*

## OUTLINE DIMENSIONS

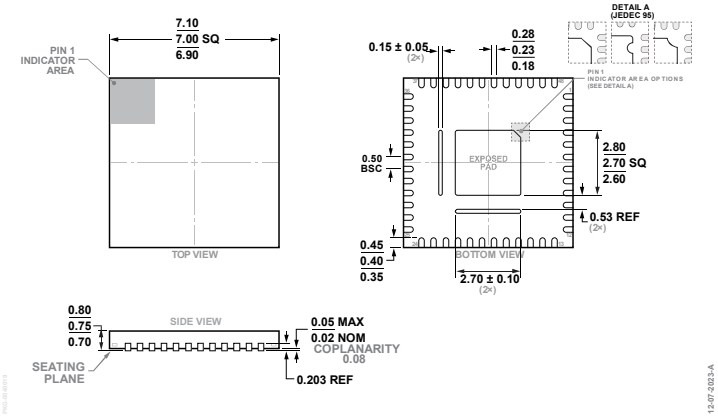


*Figure 7. 48-Lead Lead Frame Chip Scale Package [LFCSP]*
*7 mm × 7 mm Body and 0.75 mm Package Height*
*(CP-48-29)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| ADIN1320CCPZ | -40°C to +105°C | 48-Lead LFCSP (7mm x mm x 0.75mm w/ EP) | | CP-48-29 |

[1] Z = RoHS Compliant Part.