Robust, Industrial, Low Power 10BASE-T1S MAC-PHY

FEATURES

- 10BASE-T1S IEEE Standard 802.3-2022 Compliant
- 10BASE-T1S PHY operating modes
  - Point-to-point half-duplex (up to 200m)
  - Multidrop configuration half-duplex (≥25m, ≥40 nodes)
- PLCA features: PLCA coordinator, burst mode, precedence mode, and multiple PLCA IDs
- MAC features
  - OPEN Alliance 10BASE-T1x MAC-PHY SPI interface with cut through or store and forward operation
  - Transmit priority queues with total size of 28k bytes
  - 16 MAC address filters, VLAN, and EtherType filtering
- IEEE 802.1AS/IEEE 1588 support
- OPEN Alliance features topology discovery, and advanced diagnostics including PLCA diagnostics
- Safe state controller (SSC) for handling fault conditions
- Compatible with power delivery over data line
- Provides robust EMC/EMI performance
  - Low cost bus interface network with no external ESD components required
  - Enhanced noise immunity providing additional performance for noisy environments
- Low power consumption: maximum current of 50mA in functional modes of operation and 40µA in sleep mode
- 1.8V to 3.3V I/O logic levels with support for 5V inputs
- Junction temperature range: −40°C to +150°C
- Small package: 4mm × 4mm 24-lead LFCSP (QFN)

APPLICATIONS

- Industrial cabinet applications
- Building automation and control
- Energy control panels
- Ethernet based zonal architectures
- Robotics connectivity

FUNCTIONAL BLOCK DIAGRAM

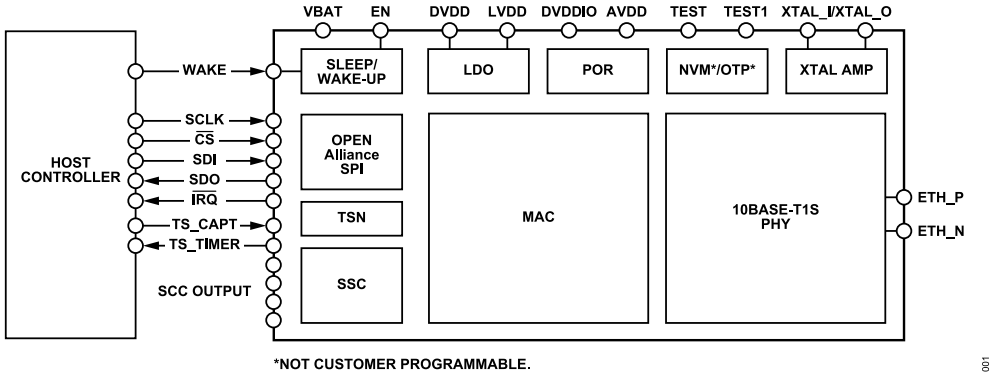

Figure 1. ADIN1140 Functional Block Diagram

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REVISION HISTORY

3/2026—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADIN1140 is a low power, high performance, single port 10BASE-T1S MAC-PHY designed for multidrop Ethernet connectivity applications.

The PHY complies with the IEEE 802.3™-2022 Ethernet standard for 10Mbps single-pair Ethernet. For point-to-point (half-duplex) configurations, the standard specifies up to 15m, but the ADIN1140 has been tested up to 200m[1]. For multidrop configurations, the standard allows up to at least 8 nodes over 25m, while the ADIN1140 has been validated in setups with more than 40 nodes[2].

Physical layer collision avoidance (PLCA) is supported for improving latency and throughput performance in a half-duplex communication system. The PLCA block includes PLCA coordinator mode, burst mode, and precedence mode. Multiple PLCA IDs reduce latency as certain nodes can be prioritized using more than one transmit opportunity within a PLCA cycle.

OPEN Alliance TC10/TC14 features include:

- Sleep/Wake-up
- Topology discovery
- Advanced diagnostics including dynamic channel quality (DCQ) and signal quality index (SQI)

The ADIN1140 contains an integrated media access control (MAC) interface with 16 MAC address filters. It also supports VLAN and EtherType filtering.

The OPEN Alliance 10BASE-T1x MAC-PHY SPI Interface (OA-SPI) enables direct connectivity of the ADIN1140 with a host controller. This SPI enables the use of lower power processors without an integrated MAC, which provides the lowest overall system level power consumption. Incoming Ethernet frames can be assigned to different transmit priority queues.

Microcontrollers without time-sensitive networking (TSN) support can use the IEEE 802.1AS™/IEEE 1588™ engine to synchronize with a generalized precision time protocol (gPTP) grandmaster. The gPTP enables high-precision clock recovery with ultra-low jitter for synchronization to a common network time and timestamping of sensor data.

The ADIN1140 features overvoltage (OV) and undervoltage (UV) detection when monitoring the VBAT pin using programmable overvoltage and undervoltage thresholds.

The integrated safe state controller (SSC) can monitor fault detection mechanisms and place the device in a safely defined mode of operation in the event of a fault condition. This ensures that the 10BASE-T1S node enters a predefined state in the event of a local fault.

It also includes transaction interrupt controller (TIC), which provides configurable interrupt management with flexible sensitivity, debug ports, and OA-SPI signaling for system events and diagnostics.

[1] Tested under typical conditions using 18AWG solid copper twisted pair cable.
[2] Tested under typical lab conditions without noise injection.

SPECIFICATIONS

STANDARDS COMPLIANCE

The ADIN1140 10BASE-T1S transceivers conform to the following specifications:

- IEEE Standard 802.3-2022 for 10BASE-T1S
- IEEE 802.3 Clause 148 PLCA Reconciliation Sublayer (RS)
- OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface V1.1
- OPEN Alliance TC10/TC14 10BASE-T1S Sleep/Wake-up version 1.0
- OPEN Alliance TC14 10BASE-T1S Topology Discovery Specification version 1.0
- OPEN Alliance TC14 Advanced diagnostic features for 10BASE-T1S version 1.1

OPERATING CONDITIONS

AVDD = 4.75V to 5.25V, DVDDIO = 1.71V to 3.47V, DVDD and LVDD from internal LDO. All specifications at −40°C to +150°C junction temperature, unless otherwise noted.

Table 1. Operating Conditions

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS						
Digital Core Power Supply	V_{DVDD}	Power supply output, generated from internal LDO		1.1		V
Low-Voltage Supply	V_{LVDD}[1]	Power supply output, generated from internal LDO	3.05	3.3	3.45	V
Digital Input and Output Power Supply	V_{DVDDIO}	Power supply input, can be supplied from LVDD[1]	1.71		3.47	V
Analog Power Supply	V_{AVDD}	Power supply input	4.75	5	5.25	V
Always-On Domain Supply	V_{VBAT}	Power supply input	4.5		70	V
POWER ON RESET						
Exit From Reset	V_{VBAT}	Always-on domain functional	3.2		3.9	V
	V_{AVDD}	All other IC domains functional	4.2		4.7	V
Entry Into Reset	V_{VBAT}	Independent from AVDD: complete IC in reset	3.2		3.9	V
	V_{AVDD}	Complete IC in reset excluding always-on domain	4.2		4.7	V
TEMPERATURE						
Junction Temperature	T_J		−40		+150	°C
REFERENCE CLOCK INPUT						
Transconductance	g_M			6.25		mS
External Crystal (XTAL)		Requirements for an external crystal used on XTAL_I/CLK_IN pin and XTAL_O pin				
Crystal Frequency				25		MHz
Crystal Frequency Tolerance		Over full temperature range and life-time	−100		+100	ppm
Crystal Shunt Capacitance	C_{SHUNT}				3	pF
Crystal Load Capacitance[2]	C_{LOAD}				12	pF
Crystal Equivalent Series Resistance (ESR)	R_s				100	Ω
External Clock Input (CLK_IN)		When driving XTAL_I with an oscillator				
Clock Input Frequency				25		MHz
Clock Input Frequency Tolerance		Over full temperature range and lifetime	−100		+100	ppm
Clock Input Voltage Range		DC-coupled sine or square wave at XTAL_I/CLK_IN pin	0.8		1.1	Vp-p
Clock Input Duty Cycle			40		60	%
Clock Input Jitter					±300	ps

[1] Maximum 10mA DC current.

[2] Load capacitance C_{LOAD} = *(C1 x C2)/(C1 + C2)* + C_{STRAY}, where C_{STRAY} is the stray capacitance including routing and package parasitics. C1 and C2 are the capacitors loaded on printed circuit board (PCB).

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ELECTRICAL CHARACTERISTICS

All digital inputs are 5V tolerant.

Table 2. Electrical Characteristics

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS		OA-SPI/SAIFx				
Input High Voltage[1]	V_{IH}	DVDDIO: 2.5V to 3.3V	DVDDIO × 0.7		5.5	V
		DVDDIO: 1.8V to < 2.5V	DVDDIO × 0.7		4.5	V
Input Low Voltage	V_{IL}		−0.3		+DVDDIO × 0.3	V
Input Pull-up Resistance	R_{PU}	DVDDIO = 3.63V, V_{PAD} = 0V	15		30	kΩ
Input Pull-down Resistance	R_{PD}	DVDDIO = 3.63V, V_{PAD} = 3.63V	15		30	kΩ
		DVDDIO = 3.63V, V_{PAD} = 5.5V	22		40	kΩ
Input Leakage Current	I_{IN}		−2		+2	µA
DIGITAL INPUTS		WAKE[2]				
WAKE Input Threshold		Active high	0.95	1	1.05	V
		Active low[3]	0.9		1	V
Input Leakage Current	I_{IN}	WAKE: 0V to 70V	−1		+1	µA
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	OA-SPI, SAIFx				
		Load condition = 2mA	DVDDIO – 0.4			V
		EN				
		Load condition = 25µA	2.5		3.6	V
Output Low Voltage	V_{OL}	OA-SPI, SAIFx				
		Load condition = 2mA			0.4	V
		EN				
		Load condition = 250µA			0.4	V
High-Impedance Leakage Current	I_{LEAK}		−2		+5	µA
DIGITAL I/O		OA-SPI, SAIFx				
Pin Capacitance	C_{PIN}				7	pF
10BASE-T1S PHY		ETHP, ETHN				
Differential Capacitance		Measurement frequency = 10MHz		4[4]	7[5]	pF
Output Signal Swing		Driving the 50Ω differential load	0.8	1	1.2	V_{P-P}

[1] All digital inputs are 5V tolerant.

[2] Conforms with OPEN Alliance TC10/TC14 10BASE-T1S Sleep/Wake-up version 1.0 glitch requirements.

[3] 40mV to 50mV hysteresis on the WAKE input pin.

[4] V_{CM} = 2.5V, Temp. = +25°C, IC powered.

[5] V_{CM} = −5V to +10V, Temp. = −40°C to +150°C, IC powered and unpowered.

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POWER CONSUMPTION CHARACTERISTICS

Table 3. Power Consumption Characteristics

Parameter	Symbol	Conditions / Comments	Min	Typ	Max	Unit
Battery Power Supply	I_{VBAT}			28	40	µA
DVDDIO Current Consumption[1]	I_{DVDDIO}	The DVDDIO current is determined by a number of external factors[2]				
Analog Power Supply Standby Mode	I_{AVDD}			2.3	3	mA
Analog Power Supply Active Mode[3]	I_{AVDD}				48	mA
Battery Power Supply Sleep Mode	$I_{VBATSleep}$			28	40	µA
Analog Power Supply Sleep Mode[4, 5]	$I_{AVDDSleep}$				50	µA

1 When sourcing from LVDD, do not exceed the DC current limit of 10mA.

2 For more details, see the DVDDIO Current section.

3 MAC-PHY with 10Mbps Ethernet transmission throughput, 15MHz OA-SPI clock.

4 Typically AVDD supply is turned off using EN pin function saving AVDD current when in sleep mode.

5 Internal LDOs turned off in sleep mode.

DVDDIO Current

I_{DVDDIO} is application specific, but is typically dominated by the sum of Output Dynamic Current and Input Dynamic Current:

$$I_{DVDDIO} = I_{OD} + I_{ID}$$

The on-chip I/O current I_{DVDDIO} is based on dynamic switching currents on the digital I/O pins.

The dynamic current, due to switching activity on an output pin, is calculated using the following equation:

$$I_{OD} = (C_{PIN} + C_L) \times V_{DVDDIO} \times f$$

where:

I_{OD} = Output Dynamic Current.

C_{PIN} = dynamic, transient power dissipation capacitance internal to the transceiver output pins (see Table 2).

C_L = total load capacitance that an output pin sees outside the transceiver.

V_{DVDDIO} = DVDDIO supply voltage.

f = frequency of switching on the pin.

The dynamic current, due to switching activity on an input pin, is calculated using the following equation:

$$I_{ID} = C_{PIN} \times V_{DVDDIO} \times f$$

where:

I_{ID} = Input Dynamic Current.

C_{PIN} = dynamic, transient power dissipation capacitance internal to the transceiver input pins (see Table 2).

V_{DVDDIO} = DVDDIO supply voltage.

f = frequency of switching on the pin.

Further aspects that may need to be taken into account include the contributions due to additional resistive loads (either internal or external pull-up/pull-down).

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OPEN ALLIANCE SPI I/O TIMING SPECIFICATIONS

Table 4. OA-SPI Timing Specifications

			DVDDIO = 1.8V		DVDDIO = 3.3V		
Parameter	**Symbol**	**Conditions/Comments**	**Min**	**Max**	**Min**	**Max**	**Unit**
OPEN Alliance Compliant SPI (OA-SPI)		OPEN Alliance SPI pins (SCLK, $\overline{IRQ}$, $\overline{CS}$, SDO, and SDI)					
SCLK Frequency			8	22.5	8	25	MHz
SCLK Duty Cycle			25/75	75/25	25/75	75/25	%
$\overline{CS}$ High Time	t_1		120		120		ns
$\overline{CS}$ Setup Time	t_2		17		17		ns
$\overline{CS}$ Hold Time	t_3		17		17		ns
SDI Input Setup Time Before Sample Edge	t_4		5		5		ns
SDI Input Hold Time After Sample Edge	t_5		5		5		ns
SDO Output Valid (Delay After Drive Edge)	t_6			14		12	ns
SDO Output Hold Time After Drive Edge	t_7		5		4		ns
SDO Output Disable Time	t_8			20		20	ns
SDO Output Valid (Delay After $\overline{CS}$ Edge)	t_9			15		12	ns

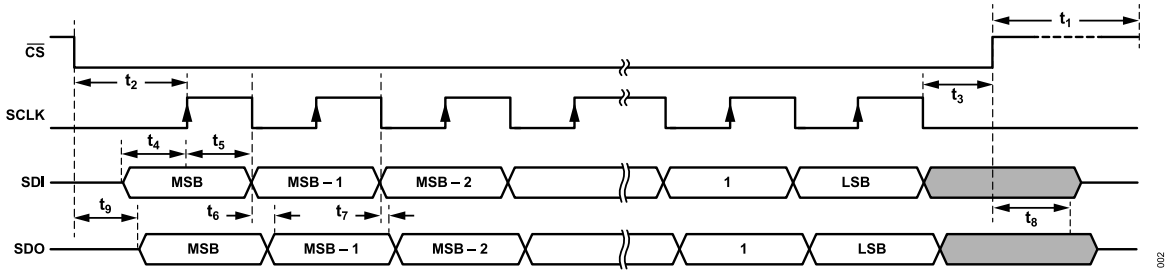

Figure 2. OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface Timing

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I/O TIMING SPECIFICATIONS

Note that the higher frequencies may require the highest drive strength setting depending on the system design.

TS_TIMER and TS_CAPT Interfaces Timing Specifications

Table 5. TS_TIMER and TS_CAPT Timing Specifications

Parameter	Conditions/Comments	Min	Typ	Max	Unit
TS_CAPT					
Pulse Width		80			ns
TS_TIMER[1, 2]					
Period		32		8,589,934,560	ns
Period Error[3]	Either QE_CORR = 0 or the sum of TS_TIMER_HI and TS_TIMER_LO must be ≥ 64		0		ns
Period Error[3]	gPTP locked	−10		+10	ns
Period Jitter[3]	QE_CORR equal to 0	−12		+12	ns
Period Jitter[3]	QE_CORR not equal to 0	−27		+27	ns
Period Jitter[3]	gPTP not used QE_CORR equal to 0 and the sum of TS_TIMER_HI and TS_TIMER_LO is a multiple of 80[4]	−2		+2	ns
Period Jitter[3]	QE_CORR equal to 0	−12		+12	ns
Period Jitter[3]	QE_CORR not equal to 0	−27		+27	ns

1 Setting of TS_TIMER_HI and TS_TIMER_LO must always be a multiple of 16.

2 Linked to gPTP grandmaster clock when gPTP functionality is used.

3 Period error/jitter measured from positive edge to positive edge.

4 For example, TS_TIMER_HI + TS_TIMER_LO = 80, 160, 320.

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
DVDDIO to GND	3.63V
AVDD to GND	5.5V
VBAT to GND	70V
WAKE to GND	70V
XTAL_I/CLKIN to GND	−0.3V to +1.8V
XTAL_O to GND	−0.3V to +1.35V
ETH_P/ETH_N (Common Mode)[1]	±20V
Temperature	
Storage Range	−60°C to +150°C
Solder Reflow, per JEDEC J-STD-020	260°C
Junction while Biased	−40°C to +150°C

[1] Maximum ETH_P/ETH_N receiver common mode DC offset. The ETH_P/ETH_N transmitter should not be enabled if driving into a low-impedance DC load. This can result in device damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 7. Tolerant Voltage on Digital I/O Pins for Different Power Supplies

Voltage Operation (V)	Minimum DVDDIO (V)	Maximum Digital I/O Voltage (V)
3.3	2.97	5.5
	0	3.63
2.5	2.25	5.5
	0	3.63
1.8[1]	1.62	4.5
	0	3.63

[1] Not tolerant to 5V input voltage.

THERMAL RESISTANCE

Thermal performance is directly linked to the PCB design and operating environment. Careful attention to PCB thermal design is required.

The thermal characteristics mentioned in this section are provided for package comparison and estimation purposes only. They are not intended for accurate system temperature calculation. Thermal simulation is required for accurate temperature analysis that accounts for all the impacts of each specific 3D system design, including, but not limited to other heat sources, the use of heat-sinks, and the system enclosure.

Thermal data is generated according to the JEDEC JESD51 series of specifications:

- θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.
- θ_{JMA} is the junction-to-ambient thermal resistance in moving air.
- θ_{JB} is the junction-to-board thermal resistance.
- θ_{JC} is the junction-to-case thermal resistance.
- Ψ_{JT} is the junction-to-top thermal characterization parameter.
- Ψ_{JB} is the junction-to-board thermal characterization parameter.

Table 8. Thermal Resistance

		Air Flow Conditions			
Parameter	Unit	No airflow	1m/s	2m/s	3m/s
θ_{JA}	(°C/W)	70.8[1]	-	-	-
θ_{JMA}	(°C/W)	-	56.1[2]	53.6[1]	52.0[1]
Ψ_{JT}[1]	(°C/W)	2.4	-	-	-
Ψ_{JB}[1]	(°C/W)	37.6	-	-	-
θ_{JB}[3]	(°C/W)	38.9	-	-	-
θ_{JC}[4]	(°C/W)	51.7	-	-	-

[1] Simulated data based on JEDEC 2s2p thermal test board with 4 thermal vias under the exposed paddle in a JEDEC Natural Convection environment.

[2] Simulated data based on JEDEC 2s2p thermal test board with 4 thermal vias under the exposed paddle in a JEDEC Forced Convection environment.

[3] Simulated data based on JEDEC 2s2p thermal test board with 4 thermal vias under the exposed paddle in a JEDEC Junction-to-Board environment.

[4] Simulated using a JEDEC 1s thermal test board with a cold plate attached to the package top and measured at the package top surface.

When using the device, the T_{JMAX} must not go above 150°C. The following equation calculates the junction temperature using the measured package surface temperature and applies only when not using a heat sink on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_J is the junction temperature of the DUT.
T_S is the package surface temperature (°C).
W_{TOTAL} is the total power consumption of the DUT.

$$W_{TOTAL} = ((VBAT \times I_{VBAT}) + (DVDDIO \times I_{DVDDIO}) + (AVDD \times I_{AVDD})$$

Values of θ_{JA} are provided for package comparison and PCB design considerations. Use θ_{JA} for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times W_{TOTAL})$$

where T_A = ambient temperature (°C).

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) ratings are per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) ratings are per ANSI/ESDA/JEDEC JS-002.

Table 9. ADIN1140, 24-Lead [LFCSP] – ETH_P, ETH_N Pins

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±8k	2

[1] HBM level is relative to GND paddle reference.

Table 10. ADIN1140, 24-Lead [LFCSP]

ESD Model	Withstand Threshold (V)	Class
HBM	±2.5k	2
FICDM	±500	C2a

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

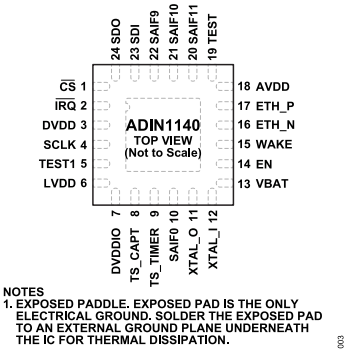

Figure 3. ADIN1140 MAC-PHY Pin Configuration

Table 11. ADIN1140 Pin Function Descriptions

Pin Number	Mnemonic[1]	Type	Description
1	$\overline{CS}$	Digital input	OA-SPI Interface SPI Chip-Select ($\overline{CS}$) Input (Active Low). Optional: 10kΩ pull-up resistor.
2	$\overline{IRQ}$	Digital output	OA-SPI Interface Interrupt Output. External 10kΩ pull-up is required if host controller pull-up is not available.
3	DVDD	Power	Decoupling for the internally generated digital core power supply (1.1V). Requires a 10nF and 1µF decoupling capacitor.
4	SCLK	Digital input	OA-SPI Interface SPI Serial Clock (SCLK) Input. External 10kΩ pull-down is required if host controller pull-down is not available.
5	TEST1	Digital input/output	DNC or 10kΩ pull-down resistor.
6	LVDD	Power	Decoupling for the internally generated 3.3V, regulated from AVDD, and used to power the analog logic. LVDD can be used to drive DVDDIO at 3.3V and/or to source an off-chip supply if required. The DC current in total (DVDDIO + off-chip) that can be supplied from this pin is 10mA. Requires a 100nF and 2.2µF decoupling capacitor.
7	DVDDIO	Power	Separate supply for the I/O circuitry, to allow the digital I/O level to be controlled as suits the application. It can run from 1.8V to 3.3V. Requires a 100nF and 4.7µF decoupling capacitor.
8	TS_CAPT	Digital input	Input for the synchronized timer to trigger the capture of a timestamp (optional). Do not connect (DNC) when not used.
9	TS_TIMER	Digital output	Output of the synchronized timer (optional). DNC when not used.
10	SAIF0	Digital output	Output pin used for the safe state controller (SSC).
11	XTAL_O	Analog output	Crystal Amplifier (25MHz) Output Pin.
12	XTAL_I	Analog input	Crystal Amplifier (25MHz) Input Pin. Direct clock reference (25MHz) input pin.
13	VBAT	Power	Always-On Domain Supply Input. Connect to 5V or battery supply. Requires a filter network (100Ω resistor and 10µF capacitor) that prevents damage or malfunction during electrical events or electrical event testing. An additional 100nF capacitor can be used for improved noise immunity.
14	EN	Digital output	An output pin is asserted when the 10BASE-T1S transceiver is in a wake-up mode, DNC or connect to a test point when not used.
15	WAKE	Digital input	Input that can be used for an external device to trigger the 10BASE-T1S transceiver to exit the sleep mode. WAKE is triggered by a voltage threshold (see Table 2). Default: disabled. Optional: 10kΩ pull-down resistor. Do not leave floating/unconnected. Short to GND when not used. When connecting externally (off-PCB), the pin needs an off-chip filter for EMI protection.
16	ETH_N	Analog input/output	10BASE-T1S Transmit/Receive Negative Pin. Differential and Symmetric Signal.
17	ETH_P	Analog input/output	10BASE-T1S Transmit/Receive Positive Pin. Same as ETH_N.
18	AVDD	Power	5V Supply Input.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 11. ADIN1140 Pin Function Descriptions (Continued)

Pin Number	Mnemonic[1]	Type	Description
			Requires a 100nF and 4.7µF decoupling capacitor.
19	TEST	Digital input	Short to GND. Do not leave floating/unconnected.
20	SAIF11	Digital output	Output pin used for the safe state controller (SSC).
21	SAIF10	Digital output	Output pin used for the safe state controller (SSC).
22	SAIF9	Digital output	Output pin used for the safe state controller (SSC).
23	SDI	Digital input	Serial Data Input (SDI). Data is clocked in on the SDI pin on each rising edge. Optional: 10kΩ pull-down resistor.
24	SDO	Digital output	Serial Data Output (SDO). Data is clocked out on the SDO pin on each falling edge. Optional: 33Ω series resistor at the source side of the signal.
EXP_PAD	GND	Ground	Exposed paddle. Exposed pad is the only electrical ground. Solder the exposed pad to an external ground plane underneath the IC for thermal dissipation.

[1] Any SAIF can be left unconnected. The pins are three-stated when not enabled in pin multiplexing. All other pins must be connected as per the description.

THEORY OF OPERATION

The ADIN1140 is an IEEE 802.3-2022 10BASE-T1S compliant Ethernet transceiver capable of 10Mbps half-duplex point-to-point or multidrop operation over a single-balanced pair of conductors. The ADIN1140 supports both PLCA and CSMA/CD modes for multidrop networks. PLCA achieves bounded latencies and fair transmit opportunities, while maintaining high throughput.

PHYSICAL LAYER COLLISION AVOIDANCE (PLCA)

The PLCA is an optional generic reconciliation sublayer (gRS) for 10BASE-T1SPHYs operating in half-duplex mode and is defined in clause 148 of the IEEE 802.3-2022 specification. The PLCA is an enhancement to CSMA/CD and controls the carrier sense and collision detect signals to add functionality without requiring any change to the MAC layer. The PLCA is not a replacement for CSMA/CD, as media access is still handled by existing CSMA/CD functions. The 10BASE-T1S network can be seamlessly switched between the two methods of medium access control when required.

The PLCA operates by granting a transmit opportunity to each node on the network in a round-robin fashion based on a node ID, which is unique to each node. During each transmit opportunity, only the node with the corresponding node ID is permitted to transmit.

PLCA Operation

The node with ID = 0 is known as the PLCA coordinator. A PLCA cycle begins when this node transmits a BEACON onto the network to indicate the beginning of a new cycle of transmit opportunities. All PHYs on the network use the BEACON to synchronize their transmit opportunity timers (TO_TIMER). Nodes detect their assigned transmit opportunity by comparing the number of transmit opportunities that have passed since the BEACON, with their internally assigned node ID. When a programmed number of transmit opportunities have occurred, the PLCA coordinator node issues another BEACON to start the cycle again. If the PLCA coordinator node fails, the network falls back to CSMA/CD for medium access control when no beacons are detected. This time-out is calculated as 2 × (max_to_timer × max_plca_node_count + beacon_timer) bit-times which is 2 × (255 × 255 + 20) = 130,090 bit-times = 13.009ms. This is mandated by IEEE 802.3-2022 Clause 148.4.6.4. The nodes switch back to PLCA mode when the first beacon is again detected on the network.

For a network with node IDs [0, N], a PLCA cycle consists of one BEACON and N+1 transmit opportunities .When a node wishes to use its transmit opportunity to send a packet, it transmits COMMIT symbols to inform all other nodes that it is sending a packet. The PLCA cycle moves to the next transmission opportunity at the end of the packet transmission or if nothing is transmitted within the TO_TIMER period.

The PLCA comes with many advantages. The round-robin scheme ensures that access to the medium is fair. The PLCA cycle results in a bounded maximum link latency, which means that a 10BASE-T1S network with PLCA is deterministic. The TO_TIMER ensures that if nodes have nothing to transmit, the PLCA cycle moves to the next node ID and causes the active nodes to use the majority of the cycle time, which maximizes the throughput. Figure 4 shows an example of a PLCA cycle.

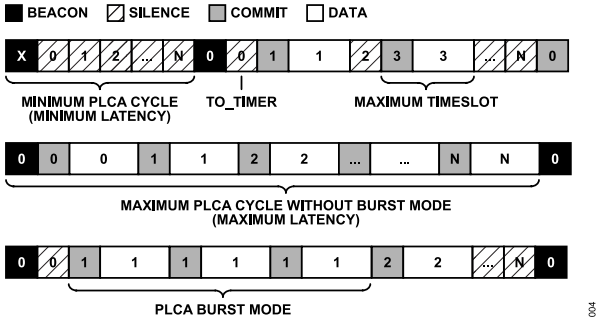

Figure 4. PLCA Cycle Overview

PLCA Features

Beside the normal PLCA operation described in the PLCA Operation section, the ADIN1140 supports the following different PLCA features that can be enabled based on the user's use case:

- Burst Mode:
  - In the PLCA burst mode, specific nodes are configured to allow the transmission of multiple frames during a single transmit opportunity up to a configured limit. During burst mode, after sending each frame, the node sends COMMIT symbols to inform other nodes that it has more frames to transmit.
- Precedence Mode:
  - The PLCA precedence mode is a feature that enables prioritization such as a traditional CAN bus. The priority of the nodes is based on PLCA node ID in ascending order (ID = 0 is the highest priority). To use this feature, all PLCA nodes on the network must have precedence mode enabled. This feature can work alongside PLCA burst mode. Precedence mode works by restarting the PLCA cycle after any packet is sent by any node. This means that the PLCA cycle only moves to the next node if all previous nodes had nothing to transmit.
- Leader Mode:
  - The PLCA leader mode allows any node to be the PLCA coordinator node, regardless of PLCA ID. When enabled, any node can be configured to set itself as the PLCA coordinator node, even if it is not assigned PLCA ID = 0. This can be used to elect a back-up PLCA coordinator when the node with PLCA ID = 0 is non-functional. When leader mode is enabled, the node transmits beacons on the network. The system must ensure this is done only when the coordinator node has failed. Once the coordinator node is back functional, two nodes transmit beacons on the network. This condition must be detected by the node that has enabled leader mode and must turn off the leader mode option. Note that this causes a temporary disruption to the traffic on the bus.

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Multiple PLCA ID Support

The ADIN1140 supports the assignment of multiple PLCA IDs to a single node. This is used to adjust the frequency of transmit opportunities available, to achieve ultra-low latencies for specific nodes in a system. A single node can have up to eight unique PLCA IDs.

MEDIA ACCESS CONTROLLER (MAC)

The transceiver combines an IEEE802.3-2022 Ethernet PHY and an 802.3 Clause 4 compliant media access controller (MAC), which includes an OA-SPI.

This interface allows the MAC to connect to low-cost microcontrollers without requiring a microcontroller with MAC interface. Ethernet packets and control/status commands are transferred over OA-SPI. An OA-SPI also requires only five pins, which enable a simpler hardware interface with fewer pins than MII or RMII. The MAC has one receive first in, first out (FIFO), and two transmit FIFOs, one low priority and one high priority. The data is transferred over the OA-SPI full duplex.

The MAC layer in the ADIN1140 also supports, but not limited to, the following features: frame filtering, MAC statistics counters, transmit priority queues, and carrier sense multiple access with collision detection (CSMA/CD) operation.

CSMA/CD

The transceiver implements PLCA in the PHY for deterministic, collision free transmission. However, if (for example) the PLCA head node fails or the PLCA is disabled, the node defaults to CSMA/CD. The CSMA/CD is implemented in the MAC as per the IEEE 802.3 Standard.

The CSMA/CD media access method can enable two or more stations to share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message. If, after initiating a transmission, the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (back-off) before attempting to transmit again. If the maximum configured retry count is reached, the transmit frame is dropped. The retry limit count can be configured from 0 to 15 attempts as per the IEEE 802.3 Standard.

Frame Filtering on Receive

Received frames filtering requires configuration of the address filtering table. The ADIN1140 supports different methods for filtering the received frames.

MAC Address Filtering

The MAC can be configured to filter up to 16 different MAC addresses based on the destination MAC address (DA). For the configuration details, refer to the device manual.

VLAN Filtering

The MAC supports VLAN Identifier based filtering for IEEE 802.1Q tagged Ethernet frames to the host. The VID table can store two VID (VLAN ID) entries.

The device supports decoding of one VLAN tag of C-TAG type, any subsequent VLAN tags are not supported and the second VLAN tag is considered as the EtherType of the frame. Frames without VLAN tag is not filtered also if VLAN filtering is enabled.

EtherType Filtering

The MAC also supports EtherType (Ethernet type) based filtering for all the received Ethernet frames. The EtherType filter table can store two EtherType entries.

Transmit Priority Queues

The transmit frame priority feature enables the use of two different FIFOs on transmit: a high priority FIFO and a low priority FIFO. The FIFO sizes are configurable up to total size of 28k bytes.

The priority queues can be used in two ways:

- The two FIFOs are used as two different queues, which allow two different parts of an application to send information using a certain split in the throughput allocation.
- One queue is used as a high priority bypass queue. In this way, most of the traffic is sent through the low priority queue, and then any traffic that must be sent immediately is sent through the high priority queue.

Frames must be sent to one queue at a time, as sending frame to both the queues at same time can cause the MAC entering unrecoverable state and no frames get through until the part is reset.

OPEN Alliance SPI Protocol

The OPEN Alliance SPI protocol version 1.1 can transfer data over the SPI using full duplex operation, which achieves bidirectional frame transfer.

The ADIN1140 supports the following OPEN Alliance SPI capabilities:

- Validation of frame check sequence (FCS) appended by and received from the SPI host.
- Supported chunk payload of 8, 16, 32, and 64 bytes.
- IEEE 1588 time stamp capture on transmit and receive.

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The OPEN Alliance SPI protocol defines two types of transactions: data transactions for Ethernet frame transfers and control transactions for register read/write operations.

A chunk is the basic element of data transactions, and they are composed of 4 bytes of overhead plus the configured payload size.

Data transactions consist of an equal number of transmit and receive chunks. Chunks in both transmit and receive directions may or may not contain valid frame data independent from each other, allowing for the simultaneous transmission and reception of different length frames. The data header of the chunk in the transmit frames, and the data footer in the receive frames, indicate which bytes of the payload contain the valid frame data. For more details on the OPEN Alliance SPI protocol used by the ADIN1140, refer to OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface v1.1.

Note that $\overline{CS}$ can be continuously asserted for multiple transactions of the same type. When changing between control and data transactions, $\overline{CS}$ must be deasserted for the minimum high time period, as shown in Figure 5. The minimum $\overline{CS}$ high time is stated in Table 4.

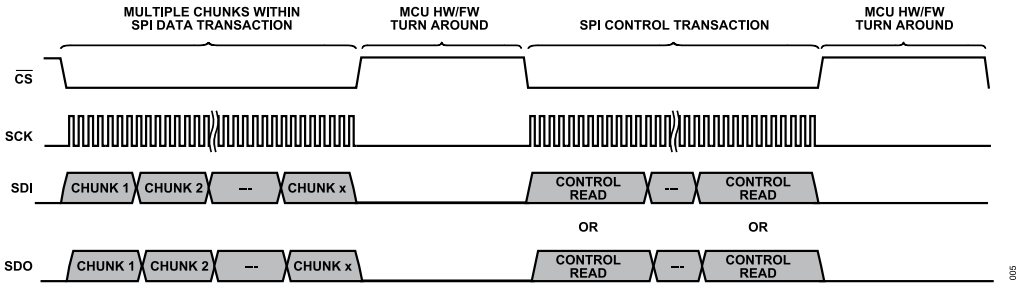

Figure 5. Ethernet Data Frame Transfer Followed by Control Transfer

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Data Chunks

Transmit data chunks consist of a 4-byte header followed by the transmit data chunk payload, as shown in Figure 6.

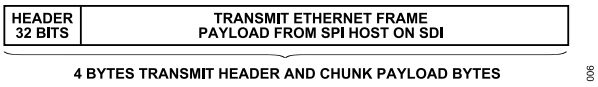

Figure 6. Transmit Data Chunk

Receive data chunks consist of the receive data chunk payload followed by a 4-byte footer, as shown in Figure 7

Figure 7. Receive Data Chunk

The default size of the data chunk payload is 64 bytes. This size can be configured to 8 bytes, 16 bytes, 32 bytes, or 64 bytes via the chunk payload selector bits. The data chunk size must be configured before enabling data transmission or reception. Therefore, when the data chunk size is configured, it must not be changed without resetting the MAC-PHY.

OPEN Alliance SPI Cut Through Mode

If cut through mode from or to the host is enabled, the method to transfer frames remains the same as when using store and forward mode. However, the frame receive starts when sufficient frame data to fill a chunk is received, and the frame transmit starts when a configured transmit threshold is reached.

The cut through mode can be enabled via the receive cut through enable bits and transmit cut through enable bits.

On receive, the MAC returns data as it becomes available. Unlike in store and forward mode, there may be empty chunks (DV = 0) between a start of frame (SOF) chunk and an end of frame (EOF) chunk.

If the host does not read frames fast enough to keep the receive FIFO empty, the frames are then buffered in the receive FIFO as if it is operating in store and forward mode. When all the frames are read, the FIFO returns to operating in cut through mode.

On transmit, the host must provide frame data at a rate fast enough (>10Mbps) to ensure that the frame does not under run on transmit. If the MAC under runs, it asserts the equivalent bit in the status register and the MAC stops transmitting the frame in progress and appends a bad CRC to the frame.

Cut Through Transmit Latency

The time interval between the start of an SPI data transaction with a transmit header SWO of 0 (frame starts immediately in the chunk), and the time TX_EN rises with an SPI frequency of 20MHz and transmit threshold set to one half-word = 4µs. The PHY transmit latency is 0.44µs. This makes a total transmit latency of 4.44µs.

Cut Through Receive Latency

The receive latency varies based on the chunk size and the SPI frequency. Table 12 indicates the latency for a SPI frequency of 20MHz and all supported chunk sizes.

Table 12. Receive Latency for 16MHz for All Supported Chunk Sizes

Chunk Size (Bytes)	Time to Receive a Chunk of Data Over xMII (µs)[1]	Time for Chunk Transfer over SPI (µs)[2]	Total Rx Latency (µs)
64	57.6	26.11	70.66
32	32	13.82	38.91
16	19.2	7.68	23.04
8	12.8	4.61	15.10

[1] Enough frame data to fill a chunk must be received before a transfer starts on the SPI. The time to receive the frame preamble is also included in this.

[2] Assuming that the µC is not waiting for an interrupt and that it is providing back-to-back OPEN Alliance data transactions on the SPI. The frame transfers start in the middle of the chunk on average.

Control Transactions

Control transactions consist of one or more control commands. These commands are used by the SPI host to read and write registers within the MAC-PHY, and each one is composed of a 32-bit control command header followed by register data. See Table 13.

Table 13. Control Command Header

D31	D30	D29	D28	D27 to D24	D23 to D8	D7 to D1	D0
0	HDRB	WNR	AID	MMS	ADDR [15:0]	LEN	P

See the following definitions:

- HDRB: received header bad. When set by the MAC-PHY, HDRB indicates that a header is received with a parity error. The SPI host must always clear this bit. The MAC-PHY ignores this value.
- WNR: write not read. If 1, data is to be written to registers. Otherwise, data is to be read.
- AID: address increment disable. When clear, the address is automatically post-incremented by one following each register read or write.
- MMS: memory map selector. This field selects the specific register memory map to access. See Table 14.
- ADDR: address of the first register within the selected memory map to access.
- LEN: length. Specifies the number of registers to read/write. This field is interpreted as the number of registers − 1. Therefore, a length of 0 reads or writes a single register.
- P: parity. Parity bit calculated over the control command header. Method used is odd parity.

For more details, refer to the OPEN Alliance TC6 and the device manual.

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Table 14. Register Memory Maps (MMS)

MMS	Memory Map Description
0	Standard control and status (SPI Address 0x00 to Address 0x20).
1	MAC (from SPI Address 0x30).

TOPOLOGY DISCOVERY

Network topology refers to the arrangement of nodes and connections within a network. In some cases, it is necessary to correlate the logical topology of a network with the physical location of nodes in the real world. A 10BASE-T1S network may contain multiple identical devices on the same bus, whose specific function depends on the physical location of the device. Topology discovery allows a 10BASE-T1S network to relate the MAC address of a node to its physical location, thereby, allowing otherwise identical modules to be differentiated from each other easily.

A 10BASE-T1S uses a multidrop topology where every node is at a different position along the cable. Topology discovery allows any node to determine the distance between itself and another node on the bus. The end node can determine the distance to each node one by one to reveal the entire topology.

The OPEN Alliance TC14 10BASE-T1S topology discovery specification outlines a mechanism to measure the distance between the nodes and the normative requirements for state machines, timing, and voltage levels associated with this measurement.

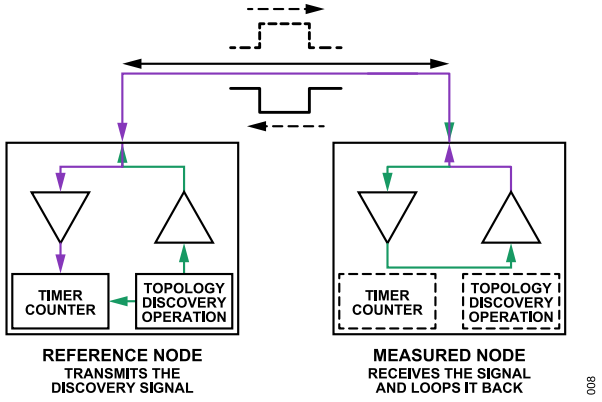

Figure 8. Topology Discovery Operation

Distance Measurement

The distance between any two nodes is determined by measuring the propagation delay of a pulse sent back and forth between the two nodes. The number of pulses received during a known time window are counted to determine the average propagation delay. Additionally, each node performs a measurement of their own internal delays, which are subtracted from the total propagation delay to determine the nominal propagation delay (NVP) of the cable. The propagation delay per meter of a pulse through single pair cable is typically (~5ns/m), so the length of single pair cable between the nodes is determined from the measured cable propagation delay.

For higher accuracy, the exact nominal velocity of propagation (NVP) of used cable is considered.

Other components such as PCB traces and common mode chokes can also add signal delays. These additional delays depend on the circuit implementation and must be subtracted to obtain a more accurate distance measurement.

The measurement time window is programmable and lengthened to increase the resolution of the acquired distance measurement.

Before the measurement procedure is started, select a reference node and a measured node. Prevent all the other nodes connected to the same line from any transmission. It is also recommended to disable the PLCA at all the nodes to avoid periodic BEACON transmissions.

This distance measurement process can be used for other applications where knowing the cable length between nodes is useful. For example, it is used to determine the link latency between the nodes for time sensitive networking (TSN) with gPTP.

TIME SYNCHRONIZATION

The ADIN1140 transceiver integrates a full IEEE 802.1AS (gPTP) engine, which removes the need for a microcontroller for gPTP.

Along with the engine, the ADIN1140 provides hardware counters and waveform generation.

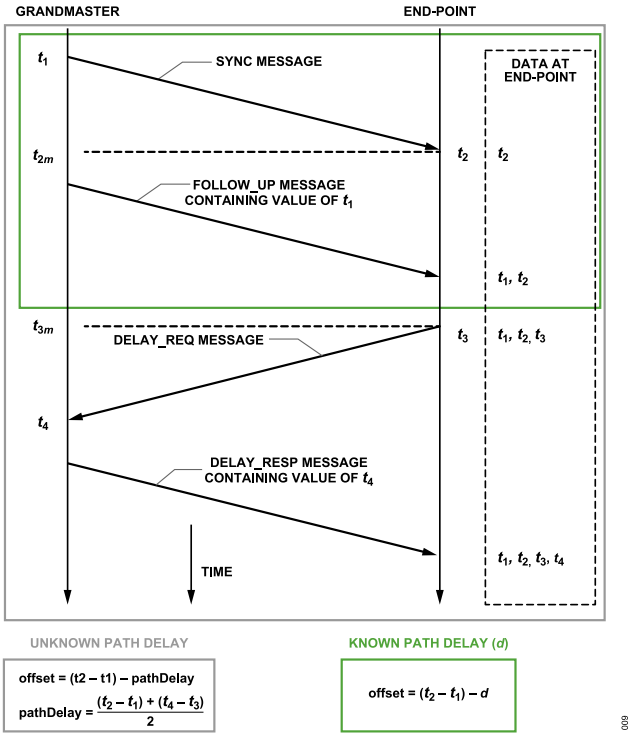

Figure 9. PTP Messages Exchange for Time Synchronization

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gPTP Grandmaster

The transceiver operating in an IEEE 802.1AS-2020 network can operate as a gPTP grandmaster and transmit sync and follow-up messages generated by the microcontroller software. The transceiver sends back the exact timestamp when the sync message is transmitted on the 10BASE-T1S bus. The hardware time-stamping is done in the PHY, therefore accounting for all the variable factors, including the PLCA elastic buffer.

gPTP End Point

The transceiver operating in an 802.1AS network can operate as a gPTP end point and receive and process synchronization frames. The transceiver can behave as an 802.1AS target and lock to a grandmaster present on the network. The transceiver provides the following gPTP features:

- Internal free-running counter and syntonized counter
- Capturing timestamps of received and transmitted frames
- Grandmaster redundancy

Timestamp Counters and Capture

The transceiver has two counters for timestamping, the internal free-running counter and the syntonized IEEE 1588 counter. The free-running counter is a 32-bit counter based on the local clock and increments in 10ns steps. The syntonized counter is the one which adjusts towards the gPTP time when gPTP messages are processed. The syntonized counter is a 64-bit counter in which the lower 32 bits represent nanoseconds with 1 LSB = 1ns.

The device can capture timestamps of both received and transmitted frames using either the free-running counter or the syntonized counter.

Also, asserting the TS_CAPT pin captures and stores a timestamp of both the syntonized counter and the free-running counter in dedicated registers.

Waveform Generation on TS_TIMER Output

The transceiver can generate an output signal (TS_TIMER) that uses two configurable counters to generate repeating waveforms driven by the syntonized time.

SAFE STATE CONTROLLER (SSC)

The SSC is a block that monitors fault detection mechanisms and place the device into a defined state if fault conditions are detected. This ensures that the transceiver device enters a defined state in the event of a local fault. The SSC has the following two modes of operation:

1. Functional Mode: The transceiver is operating as normal with the SSC monitoring the fault detection mechanisms.
2. Safe State Mode: The transceiver halts normal operation and enters a defined state.

The safe state mode places the transceiver in a safely defined mode of operation in the event of a fault condition. The safe state mode is considered an emergency situation and the automated safety actions are applied immediately. This can disturb functional mode operations that are in progress. The transceiver maintains the 10BASE-T1S network access in safe state mode, provided no detected safety fault degrades the 10BASE-T1S network. This enables safety faults to be read and resolved over the 10BASE-T1S network. A 32-bit status register is available that provides the live status of all the available fault detection events. This allows the system software to monitor all currently active fault conditions. The SSC also stores an index value that identifies the earliest fault detection mechanism that triggered entry to safe state mode. When in safe state mode, the transceiver can configure the SAIF interfaces into a benign state or set output pin levels to control external devices. The configurable parameters are pin direction, pin value, and pull-up/pull-down. There are six different pad configurations (outside of no change-keep functional mode configuration) that are selectable for each SAIF pin:

1. Disable input and output. Three-state.
2. Enable input and output. Drive 0 (low).
3. Enable input and output. Drive 1 (high).
4. Enable input, disable output. Regular input mode.
5. Enable input, disable output. Pull-down enabled.
6. Enable input, disable output. Pull-up enabled.

Entry Into Safe State Mode

There are six safety fault detection mechanisms available to trigger entry into safe state mode. Each fault detection mechanism is enabled or disabled individually. The SSC monitors the enabled fault detection mechanisms when in functional mode. While in safe state mode, the SSC continues to monitor the fault detection mechanisms. The fault detection mechanisms are:

- Manual: The SSC supports manual entry into safe state mode using a register write.
- gPTP unlocked: The gPTP lock status is monitored by the SSC to trigger entry to safe state mode when the gPTP target is unlocked.
- Ethernet frame timeout: Ethernet traffic is monitored by the SSC to trigger entry to safe state mode when no Ethernet frames have been received within a user programmed time window. The timer is a 16-bit counter with a counter interval of 81.92µs. (Max timeout = 5.368sec.)
- Device unattended timeout: The SSC has an Alive bit (self-clearing) that is used by the SSC to monitor if the device is left unattended. The system software must periodically set this bit before a user programmed timeout is reached to prevent the device from entering safe state mode. Setting the bit restarts the timer. The timer is a 16-bit counter with a counter interval of 81.92µs. (Max timeout = 5.368sec.)

- SQI degradation: The received signal quality indicator (SQI) level is used to trigger entry to safe state mode if it transitions below a user programmed threshold.
- OTP configuration error: The SSC can trigger entry to safe state mode if any ECC errors are detected in the OTP memory.

Exit From Safe State Mode

Exit from the safe state mode by the following methods (manually or automatically):

- Manual Exit: System software can read the SSC status flags for the fault detection mechanisms and choose to manually exit safe state mode using a register write, if all fault conditions are resolved. If all faults are not resolved, an interrupt may be triggered when attempting to exit safe mode.
- Automatic Exit: Automatic exit from safe sate mode is a configurable option for many fault detection mechanisms. However, not all fault detection mechanisms support automatic exit. If used, the SSC can automatically exit safe state mode if all automatic exit enabled SSC fault detection mechanisms are resolved and there are no other faults detected.

Table 15 details the exit mode available for each safety fault detection mechanism. Upon exiting safe state mode, if any entry condition is active or becomes active, a new entry to safe state mode triggers.

Table 15. Fault Detection Mechanisms − Safe State Mode Exit

Fault Detection Mechanism	Description
Manual	Manual exit required.
gPTP Unlocked	Supports automatic exit. The SSC monitors the gPTP target lock status and exit safe state mode when the gPTP target regains lock.
Ethernet Frame Timeout	Supports automatic exit. The SSC monitors incoming Ethernet traffic and exit the safe state mode if valid Ethernet frames are detected.
Device Unattended Timeout	Manual exit required.
SQI Degradation	Manual exit required.
OTP Configuration Error	Manual exit required.

SYSTEM DEBUG AND DIAGNOSTICS

The transceiver devices support diagnostics at the Physical and MAC layer. In addition, device diagnostics are available to readback.

Physical Layer Diagnostics

The following diagnostics are supported in accordance with the Open Alliance TC14 Advanced Diagnostics v1.1 specification:

- **Dynamic channel quality (DCQ):** Signal quality index (SQI) is computed and reported for received packets on the 10BASE-T1S network.
- **PLCA diagnostics:** The PLCA diagnostics supported by the device and can be read from the PLCA diagnostics register are listed below:
  - **PLCA beacon received before transmit opportunity (BCNBFTO):** This occurs when a PLCA beacon is received before a node's transmit opportunity. It can indicate multiple PLCA coordinator nodes on the mixing segment, or one PLCA coordinator node incorrectly configured with a node count smaller than the number of nodes on the mixing segment.
  - **PLCA unexpected beacon (UNEXPB):** This condition occurs on a PLCA coordinator node when it receives a beacon that it did not transmit. This indicates the presence of another PLCA coordinator node on the mixing segment.
  - **PLCA receive in assigned transmit opportunity (RXINTO):** This condition occurs when the PHY detects the beginning of a packet in its assigned transmit opportunity. This indicates another node on the mixing segment with the same PLCA ID.
- **PRBS generator:** The device also has a pseudorandom binary sequence generator (PRBS) to output. When PMA test mode 3 is enabled, the PHY outputs a pseudorandom binary sequence (PRBS) from the PHY.

MAC Layer Diagnostics

MAC layer diagnostics include all the mandatory diagnostics from the IEEE 802.3 standard and also several optional ones listed below:

- aFramesTransmittedOK
- aSingleCollisionFrames
- aMultipleCollisionFrames
- aFramesReceivedOK
- aFrameCheckSequenceErrors
- aAlignmentErrors
- aFramesWithDeferredXmissions
- aLateCollisions
- aFramesAbortedDueToXSColls
- aFramesLostDueToIntMACXmitError
- aFramesLostDueToIntMACRcvError
- aMulticastFramesXmittedOK
- aBroadcastFramesXmittedOK
- aMulticastFramesReceivedOK
- aBroadcastFramesReceivedOK
- aInRangeLengthErrors
- aFrameTooLongErrors

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Device Diagnostics

The device diagnostics supported specifically by the transceiver are listed in Table 16.

Table 16. Device Diagnostics

Diagnostic	Description
MAC Loopback Test	Within the MAC, MII Tx is connected to MII Rx.
PHY Loopback Test	PMA test modes and PCS Loopback.
gPTP Status and Counters	The gPTP engine statistics counters for gPTP event tracking.
Signal Timeout Monitor	Configurable timeout monitor reset by frame reception. Trigger may cause transition into.
Config Validation	Software can verify bootloader has run successfully – checks DONE and status flags.

Transaction Interrupt Controller (TIC)

The transceiver manages various interrupt events related to the operation of the device using the TIC. The TIC monitors the state of various input signals from other blocks and generates interrupts based on changes to those input signals. These events are flagged through the OA-SPI interface.

The transaction interrupt controller supports the following features:

- Configurable number of interrupts.
- Configurable sensitivity. Interrupts can be sensitive to low level, high level, rising edge, and falling edge of the input signal.
- Two output debug ports that can mux to any input signal and any interrupt sensitivity state.
- Interrupt resend functionality.

The transaction interrupt controller supports a range of input signals related to: MAC, PHY, gPTP, Bootloader, SQI, SSC, and Sleep/Wake. For more details, refer to the device manual.

APPLICATIONS INFORMATION

TYPICAL CONNECTION DIAGRAM

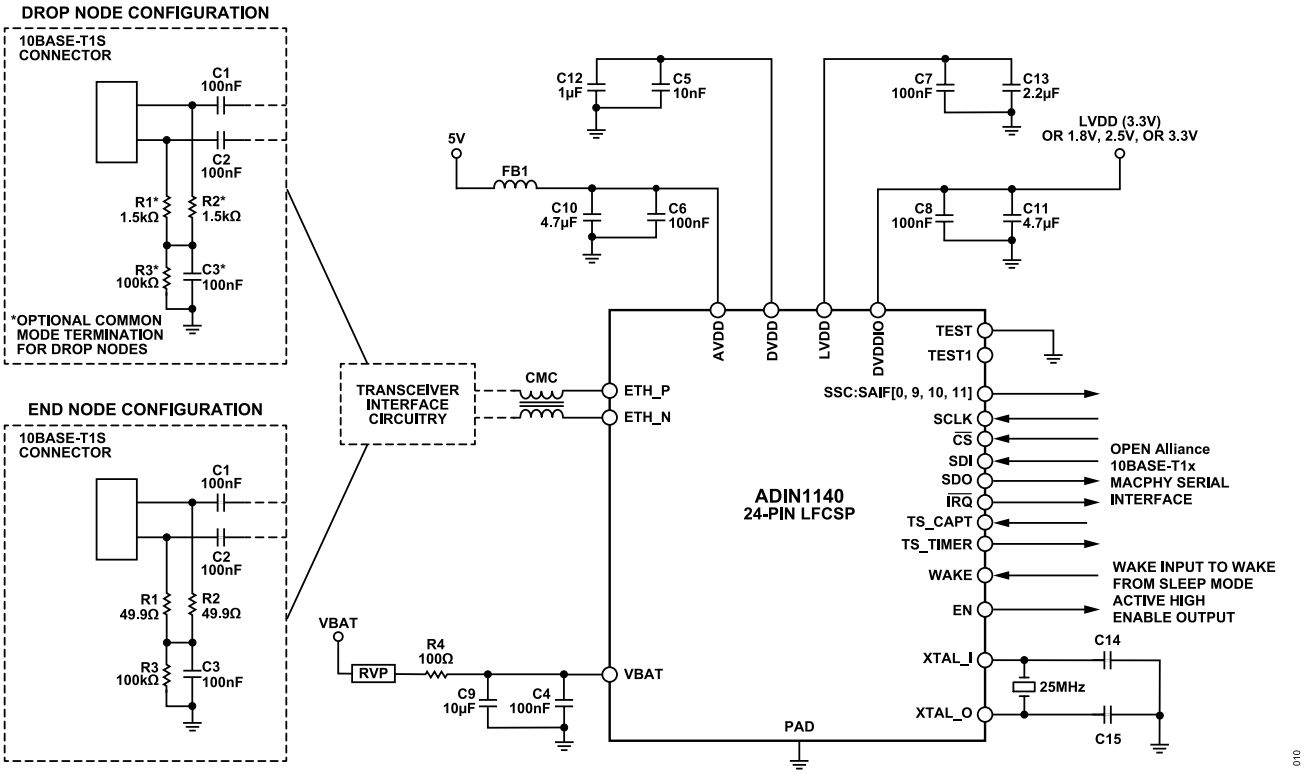

Figure 10. Typical Connection Diagram with 10BASE-T1S MAC-PHY

APPLICATIONS INFORMATION

EXTERNAL CLOCK INPUT

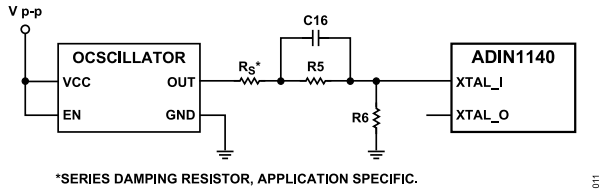

Figure 11. Typical Oscillator Connection Diagram

Table 17. Oscillator Circuit Component Selection[1]

Clock V_{P-P} (V)	R5 (kΩ)	R6 (kΩ)	C16 (pF)	R_S (Ω)[2]
3.3	3.6	1.8	5	100
2.5	3.6	2.4	7	100
1.8	3.6	4.5	15	100

[1] Assumes a parasitic input capacitance (PCB + Pin) of ~10pF.

[2] R_S: Recommended series damping resistor value is application specific.

POWER SUPPLY REQUIREMENTS

Power-Up Sequence

There are no power-up sequence requirements between the VBAT, AVDD, and DVDDIO supply when using up to 3.3V I/O supply.

When using 5V I/O logic, the DVDDIO supply must be >2.5V before any 5V logic signal is driven into the ADIN1140 device. This also applies when the DVDDIO supply is being powered from LVDD 3.3V supply. Failure to do this exceeds the absolute maximum ratings of the ADIN1140 device.

XTAL_I input must be present no later than 0.5s after power-on. Otherwise, the HV die goes into auto sleep mode (requires power cycle to recover) and internal LDOs are turned off.

Note: Make sure AVDD supply can handle 120mA of in-rush current on start-up.

Power-Down Sequence

There are no power-down sequence requirements between the VBAT, AVDD, and DVDDIO supply. DVDDIO supply must remain >2.5V as long as 5V I/O signals are driven into the ADIN1140 digital inputs.

PCB LAYOUT RECOMMENDATIONS

This section details the key areas of interest for the placement and layout of the device and corresponding support components.

LAYOUT GUIDELINES

The layout of the ADIN1140 10BASE-T1S transceiver devices must be executed in line with the following specific requirements. These requirements are critical for systems aiming to achieve compliance with EMC standards along with achieving lowest node capacitance to enhance the overall 10BASE-T1S bus performance. Further to these specific requirements, best layout practices must always be followed.

10BASE-T1S Interface Layout

The 10BASE-T1S interface layout requires attention to routing practices that preserve signal integrity and minimize noise coupling. The following guidelines outline the key considerations to ensure reliable communication performance and reduces the risk of signal degradation across the physical layer:

- Ethernet P and Ethernet N: Reduce stub length as much as possible.
- Ethernet P and Ethernet N: On the trace routing, try to minimize single ended and differential capacitance.
- Length match Ethernet P and Ethernet N. Try not to introduce imbalance in length and also imbalance in coupling to neighboring nets/potentials. To match the trace lengths, different routing techniques can be used. It is recommended to apply those techniques on the same end of the length-matched pair.
- Match any vias in the signal route with the same impedance of the signal line.
- When placing signal vias, it is recommended to place ground, or return, vias close by to provide a short path to ground.

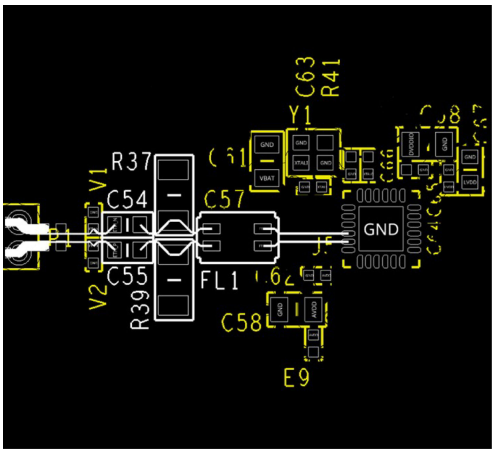

Figure 12. T1S Termination Network and Connectors (Combined View)

Decoupling Capacitors Placement and Layout

Place decoupling capacitors for any power pin on the same side of the PCB as the transceiver with the smaller capacitor closest to the respective pin. Figure 13 shows the placement of the ADIN1140 power decoupling components.

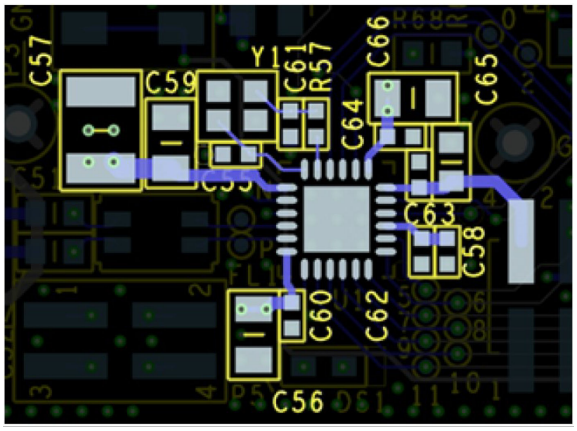

Figure 13. Power Decoupling Components

Common-Mode Choke (CMC) Parasitic Capacitance

Not all applications require a CMC, but when required, the following points should be considered for the board design:

- Refer to Open Alliance CMC specification.
- Optimal CMC parasitic capacitance must be less than 10pF.
- The parasitic capacitance between the CMC and adjacent ground planes must be minimized to ensure that the CMC rejects common-mode noise across the specified frequency range.
- High-speed layout techniques must be used to minimize the parasitic capacitance of the landing pads and the CMC body to the ground plane below the component.
- Minimizing parasitic capacitance supports the goal of maximizing the differential bandwidth with minimum insertion loss, and more importantly, reducing signal reflections on the bus.
- Use ground relief in the ground plane underneath the CMC for reducing parasitic capacitance to ground.

Power Supply Requirements

For specific power supply values, see the Power Consumption Characteristics section. The general rules for managing the power supply are:

- For the requirements of the ADIN1140 power supply pin filtering, refer to the bill of material (BOM) of reference designs. The passive components (termination resistors and AC-coupling capacitors) must be sized to adequately handle BCI events.
- Ensure that the digital and analog power supplies are isolated to minimize potential coupling paths between the noisy and sensitive power supplies.
- Employ double vias if possible, when connecting ADIN1140 supplies to minimize the supply inductance. In situations where this is not possible, analog supplies take priority.

PCB LAYOUT RECOMMENDATIONS

General Layout Guidelines

General Requirements

Following are the general requirements for the PCB layout:

- The ADIN1140 contains a common ground thermal exposed pad. The exposed pad must be connected directly to a solid, contiguous ground plane through a thermal via array.
- Carefully consider the return currents for signals on the PCB and simplify their path using techniques such as employing planar capacitors and using stitching vias.

Component Placement and Routing

Following are the component placement and routing requirements for the PCB layout:

- Ideally, place common mode choke, AC coupling caps and termination on the same side of the PCB as the ADIN1140 device.
- Keep decoupling caps close and on same the side of the PCB as the ADIN1140 device.
- Keep crystal resonator close and on the same side of the PCB as the ADIN1140 device.

DUT Area

Following are the DUT area requirements for the PCB layout:

- For proper thermal management, the ADIN1140 device must have its ground paddle connected to a continuous PCB ground plane.
- Use stitching into internal layers to sink heat (9 vias – 3 × 3).

Performance Requirement

Following is the performance requirement for the PCB layout:

- The preferred option for optimal EMC performance is stripline routing but microstrip routing may also be used. For additional details, refer to the industry-standard PCB layout design guidelines.

Plane Notes

Following are the plane notes for the PCB layout:

- The ADIN1140 reference hardware has implemented a copper ground plane void underneath the common-mode choke (three layers deep).
- The internal ground layer reference immediately below the common-mode choke, which is on an external layer must have an area of ground cut-out that matches the dimension of the courtyard of the common-mode choke.

OUTLINE DIMENSIONS

For the latest package outline information and land patterns (footprints), go to Package Index.

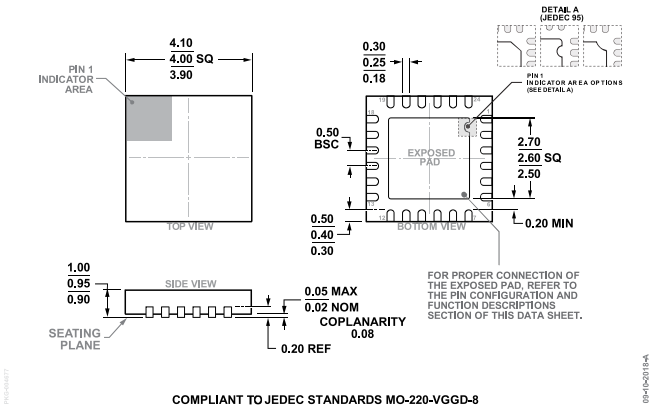

Figure 14. 24-Lead Lead Frame Chip-Scale Package [LFCSP]
4mm × 4mm Body and 0.95mm Package Height
(CP-24-17)
Dimensions are shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADIN1140BCPZ	−40°C to +150°C	24-Lead LFSCP (4mm × 4mm × 0.95mm w/ EP)	Tray, 490	CP-24-17
ADIN1140BCPZ-RL	−40°C to +150°C	24-Lead LFSCP (4mm × 4mm × 0.95mm w/ EP)	Reel, 5000	CP-24-17

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADIN1140D1Z	10BASE-T1S and 10BASE-T1L MAC-PHY multimode platform board: USB-T1S, T1L-T1S, and MQTT drop node
DEMO-ADIN114XAZ	ADIN1140 10BASE-T1S MAC-PHY MCU-less with feather connectivity

[1] Z = RoHS Compliant Part.