3mm × 3mm SP4T MEMS Switch, 0Hz/DC to 30GHz

FEATURES

- Operational frequency range:
  - −3dB bandwidth:
    - DC to 19GHz (typical) for RF1, RF4
    - DC to 17GHz (typical) for RF2, RF3
  - −6dB bandwidth:
    - DC to 29GHz (typical) for RF1, RF4
    - DC to 22GHz (typical) for RF2, RF3
- High bit rate capability up to 64Gbps
- Low insertion loss:
  - 0.55dB (typical) at 6GHz
  - 0.85dB (typical) at 10GHz
- Off isolation:
  - 26dB (typical) at 6GHz
  - 23dB (typical) at 10GHz
- Return loss:
  - 28dB (typical) at 6GHz
  - 25dB (typical) at 10GHz
- High input IIP3: 70dBm (typical)
- High RF power handling: 33dBm (maximum)
- On resistance: 1.9Ω (typical)
- High DC current handling: 200mA (maximum)
- High switch cycle count: 100 million cycles (minimum at +85°C)
- Fast switching time: 200µs T_{ON} (maximum)
- Integrated 3.3V driver for simple control with parallel interface and SPI
- Space saving integrated passive shunt resistors
- Small 24-lead, 3mm × 3mm × 1.5mm land grid array package
- Temperature range: −40°C to +85°C

APPLICATIONS

- ATE load and probe boards
- DC with high speed loopback testing
- Supports digital standards: high speed serialization/deserialization, PCIe Gen4/Gen5/Gen6, USB 4, and PAM 4
- Relay replacements
- Reconfigurable filters and attenuators
- Military and microwave radios
- Cellular infrastructure: 5G mmWave

FUNCTIONAL BLOCK DIAGRAM

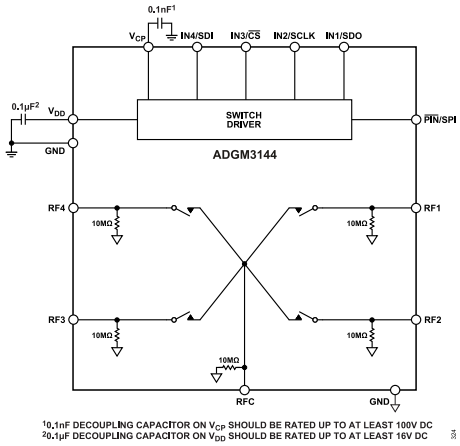

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADGM3144 is a wideband, single-pole, four-throw (SP4T) switch, fabricated using Analog Devices, Inc., microelectromechanical system (MEMS) switch technology. This technology enables a small form factor, wide RF bandwidth, highly linear, low insertion loss switch that is operational down to 0Hz/DC, making it an ideal solution for a wide range of RF and precision equipment switching needs.

An integrated driver chip generates a high voltage to electrostatically actuate switch that can be controlled by a parallel interface or a serial peripheral interface (SPI). All switches are independently controllable.

The device is packaged in a 24-lead, 3mm × 3mm × 1.5mm land grid array package. To ensure optimum operation of the ADGM3144 refer to the Critical Operational Requirements section.

The on-resistance (R_{ON}) performance of the ADGM3144 is affected by part-to-part variation, channel-to-channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

COMPANION PRODUCTS

- Quad PMU : AD5522
- SP4T MEMS switch: ADGM1144, ADGM1304, ADGM1004
- Low noise, LDO regulators: ADP7142, LT1962, LT3045-1

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

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REVISION HISTORY

12/2025—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0V to 3.6V, GND = 0V, and all specifications at 25°C, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
ON-RESISTANCE PROPERTIES						
Initial On-Resistance Properties						
On Resistance	R_{ON}		1.9	3	Ω	Drain source current (I_{DS}) = 50 mA, 0V input bias, at 1ms after first actuation, maximum specification from −40°C to 85°C
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			0.8	Ω	Maximum value tested from −40°C to 85°C
On-Resistance Drift						
Over Time	$\Delta R_{ON\ TIME}$			−0.32	Ω	R_{ON} changed from 1ms to 100ms after first actuation, maximum value tested from −40°C to 85°C
Over Actuations	ΔR_{ON}		0.2	0.32	Ω	Absolute change after 10^6 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C
			±0.7		Ω	Absolute change after 100 × 10^6 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C
				2	Ω	Absolute change after 100 × 10^6 actuations, switch is actuated at 85°C and R_{ON} is measured at 25°C, actuation frequency = 289Hz
RELIABILITY PROPERTIES						
Continuously On Lifetime			10		Years	Time before failure[3] at 85°C
Actuation Lifetime						
Cold Switched		100 × 10^6	500 × 10^6		Actuations	Load between toggling is 150mA, tested at 85°C
RF Hot Switched						RF power = continuous wave (CW), terminated into 50Ω, 50% of test population failure point (T50)
7dBm			500 × 10^6		Actuations	
10dBm			150 × 10^6		Actuations	
13dBm			30 × 10^6		Actuations	
20dBm			20 × 10^3		Actuations	
DC Hot Switched						Terminated into 50Ω, RFx load capacitance = 10µF, 50% of test population failure point (T50)
0.5V or 9mA			500 × 10^6		Actuations	
1V or 18mA			500 × 10^6		Actuations	
2.5V or 46mA			35 × 10^6		Actuations	
3.5V or 65mA			6.5 × 10^3		Actuations	
5V or 93mA			2 × 10^3			
DYNAMIC CHARACTERISTICS						
Operational Frequency Range						
−3dB Bandwidth			19		GHz	RF1, RF4
			17		GHz	RF2, RF3
−6dB Bandwidth			29		GHz	RF1, RF4
			22		GHz	RF2, RF3

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
Insertion Loss	IL					RFx to RFC
			0.31		dB	DC to 2.5GHz
			0.55		dB	2.5GHz to 6GHz
			0.85		dB	6GHz to 10GHz
			2.3		dB	10GHz to 16GHz
			6.1		dB	16GHz to 24GHz
Isolation	ISO					RFx to RFC, with at least one switch on
			30		dB	DC to 2.5GHz
			26		dB	2.5GHz to 6GHz
			23		dB	6GHz to 10GHz
			18		dB	10GHz to 16GHz
			14		dB	16GHz to 24GHz
	ISO					RFx to RFC, all switches are off
			26		dB	DC to 2.5GHz
			19		dB	2.5GHz to 6GHz
			16		dB	6GHz to 10GHz
			13		dB	10GHz to 16GHz
			11		dB	16GHz to 24GHz
Crosstalk	CTK					RF1 to RFx, with RF1 to RFC on
			31		dB	DC to 2.5GHz
			25		dB	2.5GHz to 6GHz
			20		dB	6GHz to 10GHz
			16		dB	10GHz to 16GHz
			12		dB	16GHz to 24GHz
Return Loss	RL					Measured at RFx
			30		dB	DC to 2.5GHz
			28		dB	2.5GHz to 6GHz
			25		dB	6GHz to 10GHz
			19		dB	10GHz to 16GHz
			10		dB	16GHz to 24GHz
Third-Order Intermodulation Intercept	IIP3		70		dBm	Input: 2110MHz and 2170MHz, 3510MHz and 3570MHz; input power = 30dBm
Second Harmonic	HD2		−107		dBc	Input: 5.4MHz; input power = 0dBm
	HD2		−88		dBc	Input: 150MHz, 800MHz; input power = 33dBm
Third Harmonic	HD3		−88		dBc	Input: 150MHz, 800MHz; input power = 33dBm
Total Harmonic Distortion	THD		−103		dBc	R_L = 300Ω, f = 1kHz, RFx = 2.5V p-p
Total Harmonic Distortion Plus Noise	THD + N		−99		dBc	R_L = 300Ω, f = 1kHz, RFx = 2.5V p-p
Maximum RF Power				33	dBm	RF power = CW, terminated into 50 Ω termination; −40°C to +85°C
DC Signal Range		−6		+6	V	On switch DC input bias voltage signal range; −40°C to +85°C
Stand Off voltage		−6		+6	V	−40°C to +85°C, this specification is applied when the switch is in the off position with no RF signal applied
Maximum DC Current				200	mA	−40°C to +85°C
On Switching Time[4]	t_{ON}			200	µs	50% INx to 90% (0.05dB of final IL value) RFx, 50 Ω termination, −40°C to 85°C See Figure 5 for details.

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
Off Switching Time[4, 5]	t_{OFF}			200	µs	50% INx to 10% (0.05dB of final IL value) RFx, 50 Ω termination, −40°C to 85°C See Figure 5 for details.
Power-Up Time			4	5	ms	V_{CP} cap = 100pF, −40°C to +85°C
Video Feedthrough			10		mV peak	1 MΩ termination at RFx and 50Ω termination at RFC
Actuation Frequency			5		kHz	Both switches toggled simultaneously
Internal Oscillator Frequency		8.6	10	11	MHz	
Internal Oscillator Feedthrough			−92.5		dBm	See note[6] for measurement setup details
			−115.5		dBm/Hz	This value comes from calculations
Signal Timing Parameters						Simulated digitally using measured s-parameter models
Phase Delta Between Channels			2.75		degree	
Propagation Delay			49.5		ps	RF1 to RFC, see Figure 49
			48.5		ps	RF2 to RFC, see Figure 49
			48.6		ps	RF3 to RFC, see Figure 49
			50		ps	RF4 to RFC, see Figure 49
Channel-to-Channel Skew			0.5		ps	RF1 to RFC, RF4 to RFC, see Figure 50
			0.2		ps	RF2 to RFC, RF3 to RFC, see Figure 50
			1.2		ps	RF1/4 to RFC, RF2/3 to RFC, see Figure 50
CAPACITANCE PROPERTIES						At 1MHz, includes LGA package capacitance
Input to Output Off Capacitance	$C_{DS(OFF)}$		30		fF	Capacitance from input to output derived from off isolation measurements, see Deriving CDS(OFF) from Off Isolation section
On Switch Channel Capacitance	C_{ON}		3.4		pF	Capacitance measured on RFx with respect to ground when RFx to RFC is on
Off Switch Channel Capacitance	C_{OFF}		1.9		pF	Capacitance measured on RFx with respect to ground when all switches are off
LEAKAGE PROPERTIES						
On Leakage[7]		0.7	1.1	1.39	µA	RFx (off channels) = +6V; RFC/RFx (on channel) = −6V; maximum value tested from −40°C to +85°C
Off Leakage[7]		0.34	0.6	0.77	µA	RFx = +6V; RFC = −6V; maximum value tested from −40°C to +85°C
Internal Shunt Resistor		8.7	11.5	15.2	MΩ	Typical temperature coefficient = 27.5kΩ/°C, maximum and minimum value tested at 25°C
DIGITAL INPUTS						Minimum and maximum over −40°C to 85°C
Input High Voltage	V_{INH}	2			V	
Input Low Voltage	V_{INL}			0.8	V	
Input Current	I_{INL}/I_{INH}		0.025	1	µA	V_{IN} = V_{INL} or V_{INH}
Capacitance			5		pF	
DIGITAL OUTPUTS						Minimum and maximum over −40°C to 85°C
Output Low Voltage	V_{OL}			0.4	V_{MAX}	I_{SINK} = 1mA
Output High Voltage	V_{OH}	V_{DD} − 0.4V			V_{MIN}	I_{SOURCE} = 1mA
Capacitance			5		pF	
POWER REQUIREMENTS						Minimum and maximum over −40°C to 85°C.
Supply Voltage	V_{DD}	3.0		3.6	V	
Supply Current	I_{DD}			2.5	mA	Digital inputs = 0V or V_{DD}, SDO floating in SPI mode

SPECIFICATIONS

[1] Typical specifications tested at 25°C with V_{DD} = 3.3V.

[2] RFx is RF1, RF2, RF3, and RF4. INx is IN1, IN2, IN3, and IN4.

[3] This value shows the time it takes for 1% of a sample lot to fail.

[4] Switch is settled after 200µs. Do not apply RF power between 0µs to 200µs.

[5] RF power should be removed or less than 5dBm, 50µs before turning the switch off.

[6] Spectrum analyzer setup: resolution bandwidth (RBW) = 200Hz, video bandwidth (VBW) = 2Hz, span = 100kHz, input attenuator = 0dB, detector type = peak, maximum hold = off. Measurements taken with one switch on and off switch port terminated into 50Ω. The fundamental feedthrough noise or harmonic thereof is tested (whichever is the highest).

[7] The on leakage and off leakage specifications depend on the DC voltage level applied to the switch node. For example, if 1V is applied at RFx to RFC, the on leakage specification is 0.2µA and off leakage specification is 0.1µA. The leakage specification of the switch is mainly driven by the internal 10MΩ resistors to ground connected on all the RF nodes to avoid floating nodes.

TIMING CHARACTERISTICS

V_{DD} = 3.0V to 3.6V, GND = 0V and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Limit at T_{MIN}	Limit at T_{MAX}	Unit	Conditions
t_1	100		ns	SCLK period
t_2	45		ns	SCLK high pulse width
t_3	45		ns	SCLK low pulse width
t_4	25		ns	$\overline{CS}$ falling edge to SCLK active edge
t_5	20		ns	Data setup time
t_6	20		ns	Data hold time
t_7	25		ns	SCLK active edge to $\overline{CS}$ rising edge
t_8		20	ns	$\overline{CS}$ falling edge to SDO data available
t_9[1]		40	ns	SCLK falling edge to SDO data available
t_{10}		25	ns	$\overline{CS}$ rising edge to SDO data available
t_{11}	100		ns	$\overline{CS}$ high time between SPI commands
t_{12}	25		ns	SCLK edge rejection to $\overline{CS}$ falling edge
t_{13}	25		ns	$\overline{CS}$ rising edge to SCLK edge rejection

[1] Measured with a 20pF load. t_9 determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

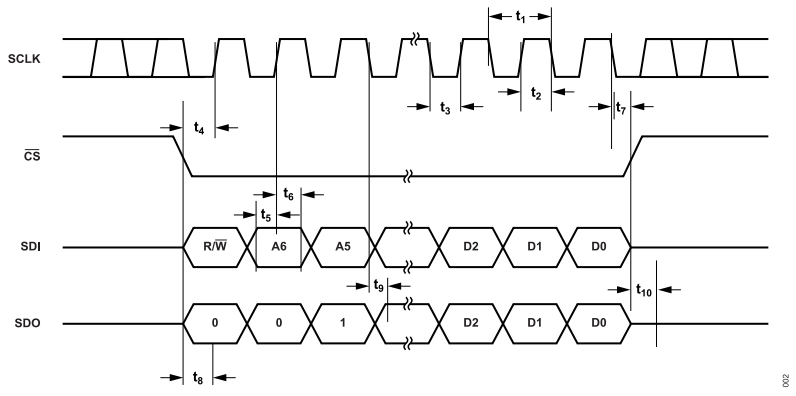


Figure 2. Addressable Mode Timing

SPECIFICATIONS

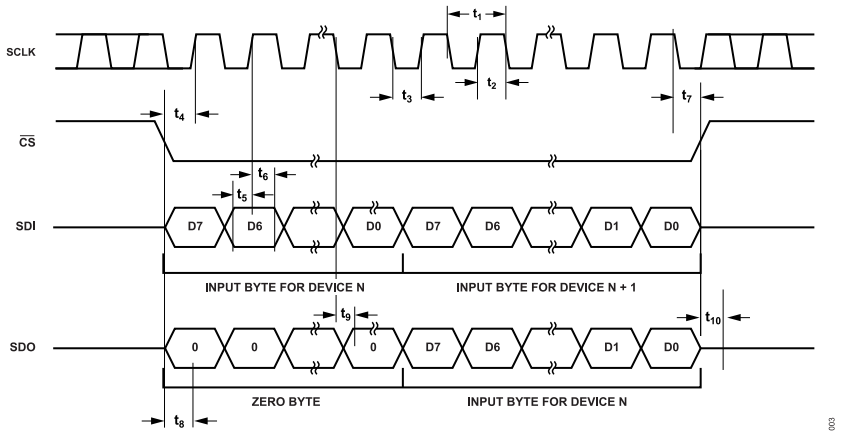


Figure 3. Daisy Chain Timing

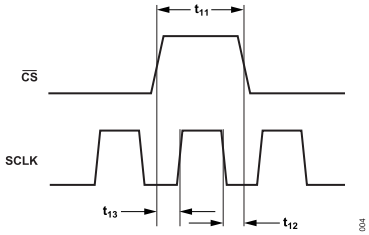


Figure 4. SCLK and $\overline{CS}$ Timing Relationship

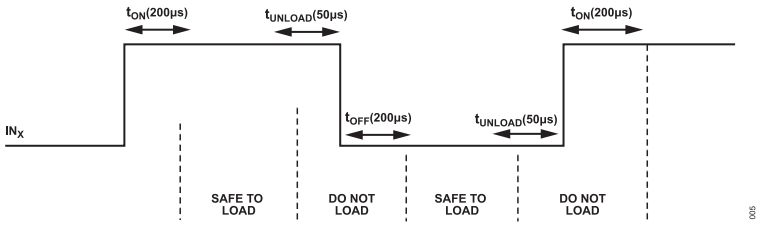


Figure 5. Switch Loading Profile

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to AGND	−0.3V to +6V
Digital Inputs[1]	−0.3V to V_{DD} + 0.3V or 30mA (whichever occurs first).
Switch DC Rating[2]	
Voltage	±7V
Current	220mA
V_{CP}	82V
Stand Off Voltage[3]	±10V
RF Power Rating[4]	34dBm
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10sec to 30sec
Group D	
Mechanical Shock[5]	1500*g* with 0.5ms pulse
Vibration	20Hz to 2000Hz acceleration at 50*g*
Constant Acceleration	30,000*g*

1 Limit the current to the maximum ratings shown.

2 This rating is with respect to the switch in the on position with no RF signal applied.

3 This rating is with respect to the switch in the off position with no RF signal applied.

4 This rating is with respect to the switch in the on position and terminated into 50Ω.

5 If a device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JCT} is the junction to the top of the case thermal resistance.

θ_{JCB} is the junction to the bottom of the case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JCT}	θ_{JCB}	Unit
CC-24-23	68.1	161.7	93.7	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for the handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) as per ANSI/ESDA/JEDEC JS-001. Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 5. ADGM3144, 24-Lead LGA

ESD Model	Withstand Threshold	Class
HBM[1]	150V for RFx and RFC[2] pins 3kV for all other pins	0B
FICDM[3]	1kV	C3

1 Take proper precautions during handling, as outlined in the Handling Precautions section.

2 RFx is RF1, RF2, RF3, and RF4.

3 A safe automated handling and assembly process is achieved at this rating level by implementing industry standard ESD controls.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

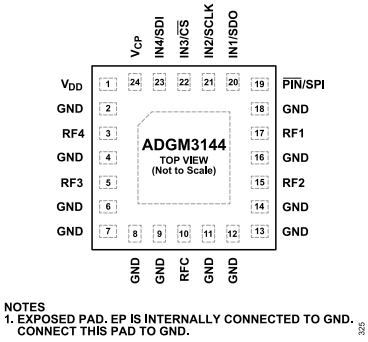


Figure 6. ADGM3144 Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply Input. For the recommended input voltage see Table 1. Place a 0.1µF decoupling capacitor to GND as close to this pin as possible. The decoupling capacitor should be rated to at least 16V DC.
2, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16, 18	GND	Ground Return.
3	RF4	RF4 Port. This pin can be an input or an output. If the pin is unused, it is recommended to either terminate it with a 50Ω resistor to GND (to prevent resonances in high-speed and RF applications) or tie it directly to GND (for DC-only applications).
5	RF3	RF3 Port. This pin can be an input or an output. If the pin is unused, it is recommended to either terminate it with a 50Ω resistor to GND (to prevent resonances in high-speed and RF applications) or tie it directly to GND (for DC-only applications).
10	RFC	Common RFC Port. This pin can be an input or an output.
15	RF2	RF2 Port. This pin can be an input or an output. If the pin is unused, it is recommended to either terminate it with a 50Ω resistor to GND (to prevent resonances in high-speed and RF applications) or tie it directly to GND (for DC-only applications).
17	RF1	RF1 Port. This pin can be an input or an output. If the pin is unused, it is recommended to either terminate it with a 50Ω resistor to GND (to prevent resonances in high-speed and RF applications) or tie it directly to GND (for DC-only applications).
19	$\overline{PIN}$/SPI	Parallel Mode Enable/SPI Mode Enable. The SPI interface is enabled when this pin is high, and the parallel interface (IN1, IN2, IN3, IN4) is enabled when this pin is low.
20	IN1/SDO	Parallel Logic Digital Control Input 1 (IN1). The voltage applied to this pin controls the gate of the RF1 to RFC MEMS switch. In SPI mode, this pin is the serial data output (SDO) pin.
21	IN2/SCLK	Parallel Logic Digital Control Input 2 (IN2). The voltage applied to this pin controls the gate of the RF2 to RFC MEMS switch. In SPI mode, this pin is the serial clock (SCLK) that synchronizes the target device(s) to the controller device.
22	IN3/$\overline{CS}$	Parallel Logic Digital Control Input 3 (IN3). The voltage applied to this pin controls the gate of the RF3 to RFCB MEMS switch. In SPI mode, this pin is the chip select ($\overline{CS}$). $\overline{CS}$ is an active low signal that selects the target device with which the controller device intends to communicate.
23	IN4/SDI	Parallel Logic Digital Control Input 4 (IN4). The voltage applied to this pin controls the gate of the RF4 to RFCB MEMS switch. In SPI mode, this pin is the serial data input (SDI).
24	V_{CP}	Driver IC output. This pin outputs 80V DC. Place a 0.1nF decoupling capacitor to GND as close to this pin as possible. The decoupling capacitor should be rated to at least 100V DC.
	EP	Exposed Pad. EP is internally connected to GND. Connect this pad to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

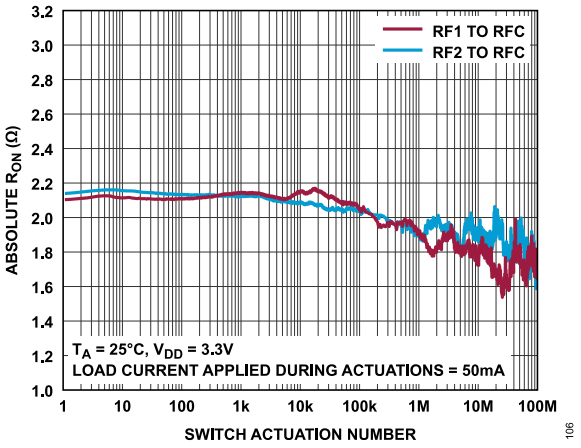


Figure 7. Absolute R_{ON} vs. Switch Actuation Number

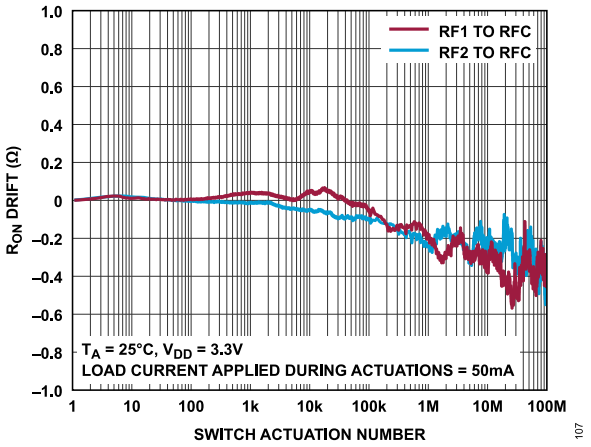


Figure 8. R_{ON} Drift vs. Switch Actuation Number, Normalized at Zero

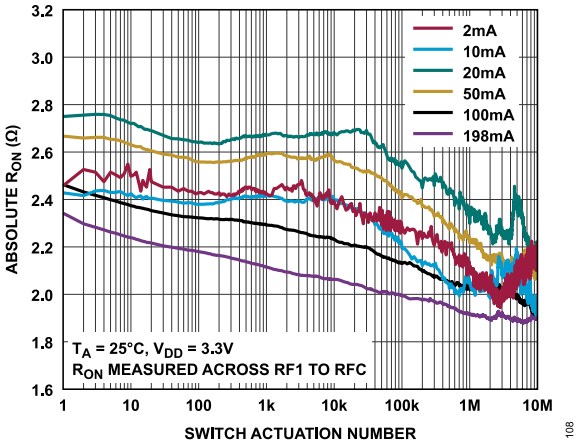


Figure 9. Absolute R_{ON} vs. Switch Actuation Number over Different Currents Applied During Actuations

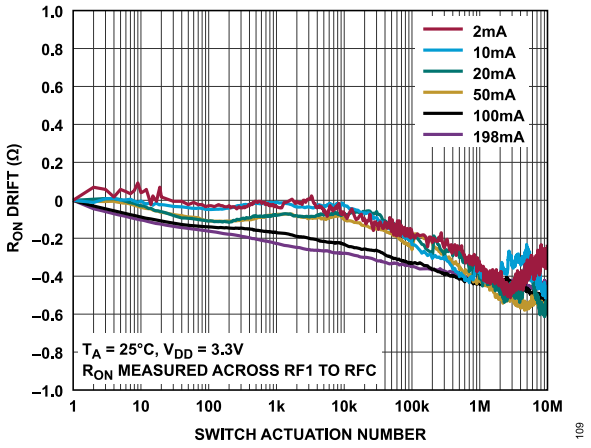


Figure 10. R_{ON} Drift vs. Switch Actuation Number over Different Currents Applied During Actuations, Normalized at Zero

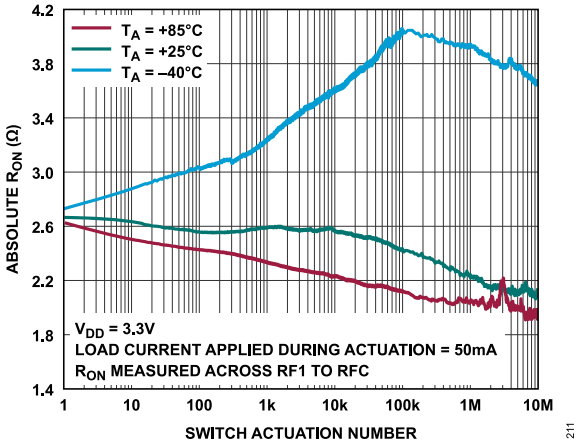


Figure 11. Absolute R_{ON} vs. Switch Actuation Number over Temperature

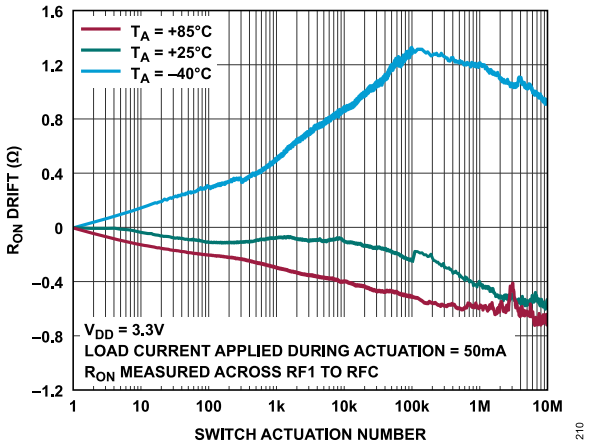


Figure 12. R_{ON} Drift vs. Switch Actuation Number over Temperature, Normalized at Zero

TYPICAL PERFORMANCE CHARACTERISTICS

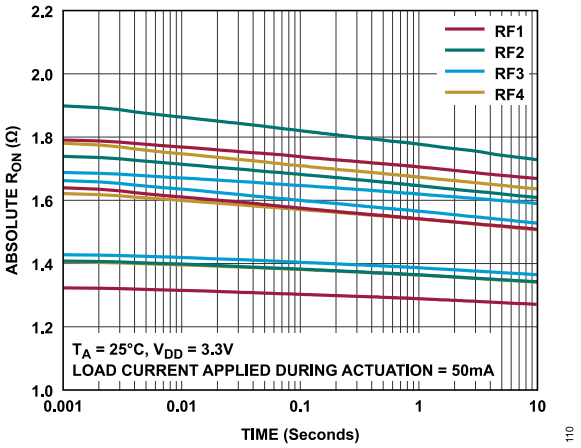


Figure 13. Absolute R_{ON} vs. Time (1ms to 10sec) over Different Channels, Multiple Devices

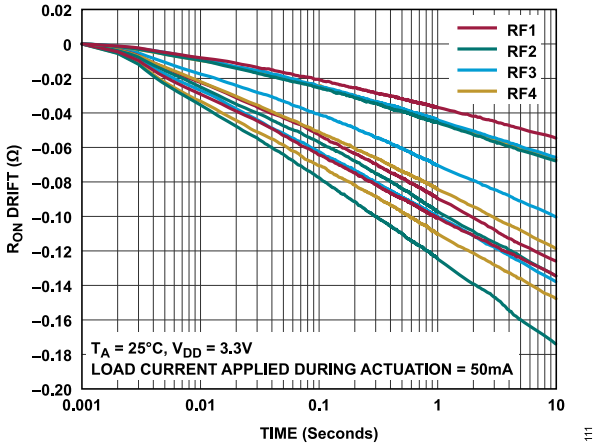


Figure 14. R_{ON} Drift vs. Time (1ms to 10sec) over Different Channels, Multiple Devices, Normalized at Zero

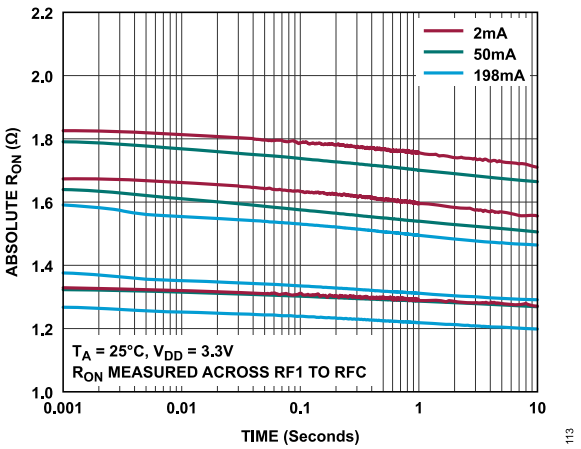


Figure 15. Absolute R_{ON} vs. Time (1ms to 10sec) over Different Current Levels, Multiple Devices

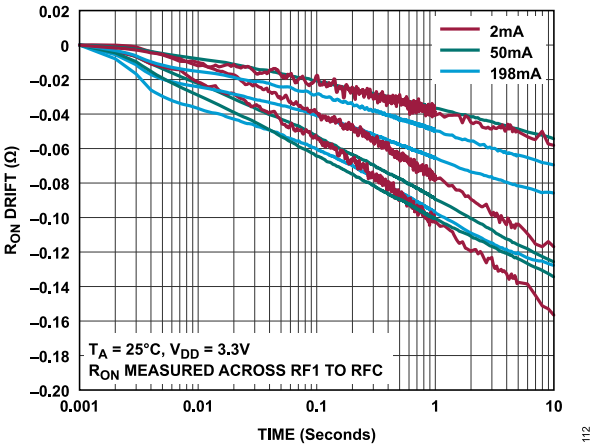


Figure 16. R_{ON} Drift vs. Time (1ms to 10sec) over Different Current Levels, Multiple Devices, Normalized at Zero

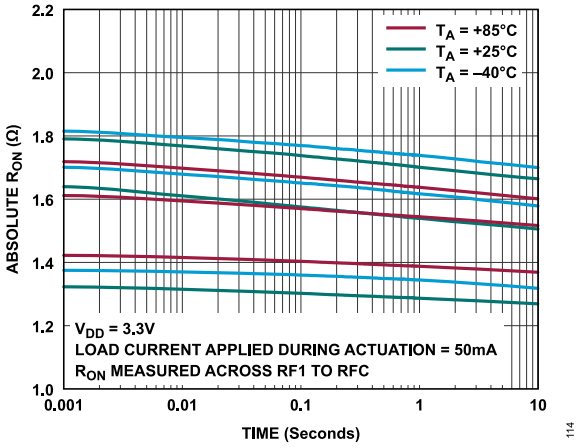


Figure 17. Absolute R_{ON} vs. Time (1ms to 10sec) over Temperature, Multiple Devices

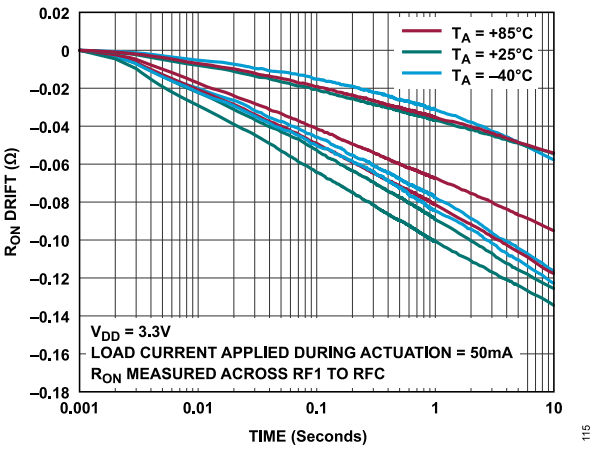


Figure 18. R_{ON} Drift vs. Time (1ms to 10sec) over Temperature, Multiple Devices, Normalized at Zero

TYPICAL PERFORMANCE CHARACTERISTICS

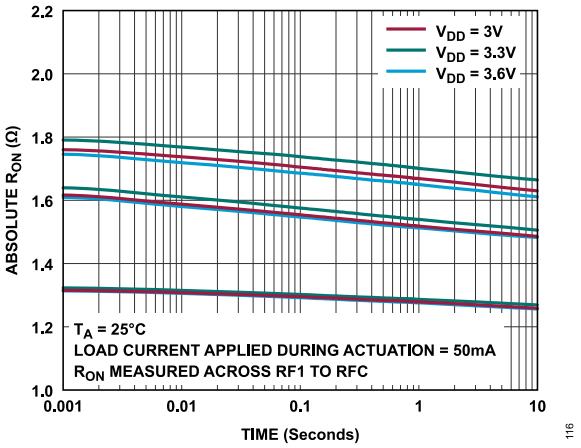


Figure 19. Absolute R_{ON} vs. Time (1ms to 10sec) over Supplies, Multiple Devices

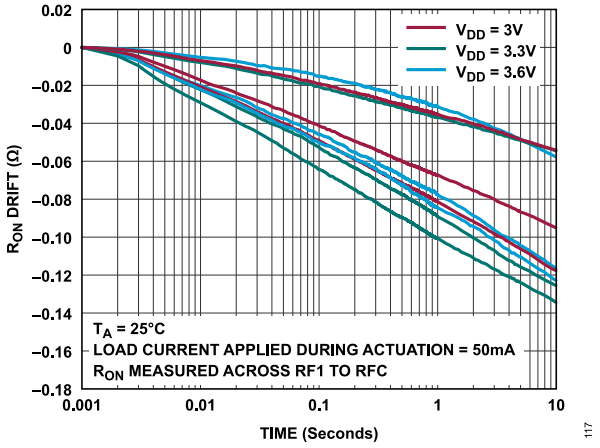


Figure 20. R_{ON} Drift vs. Time (1ms to 10sec) over Supplies, Multiple Devices, Normalized at Zero

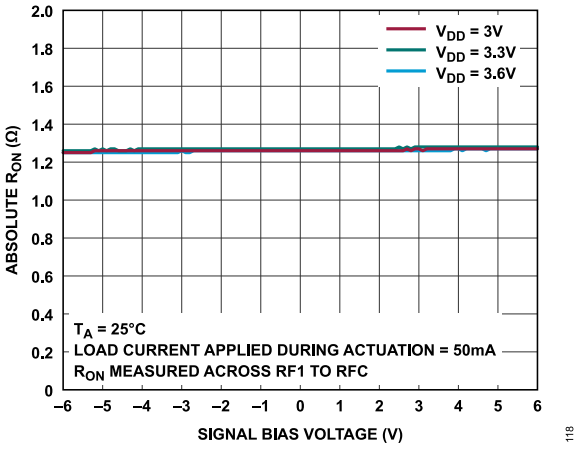


Figure 21. Absolute R_{ON} vs. Signal Bias Voltage over Supply Voltages

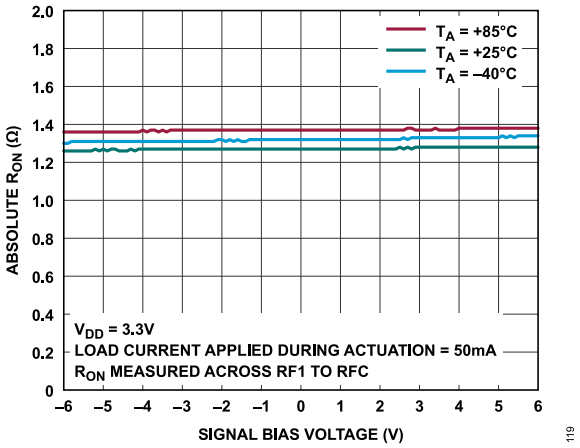


Figure 22. Absolute R_{ON} vs. Signal Bias Voltage over Temperature

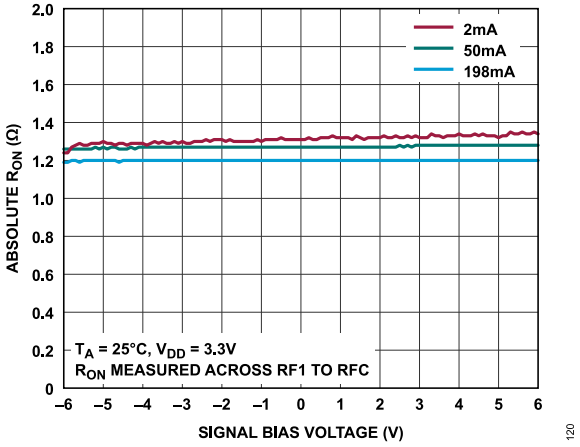


Figure 23. Absolute R_{ON} vs. Signal Bias Voltage over Different Current Levels

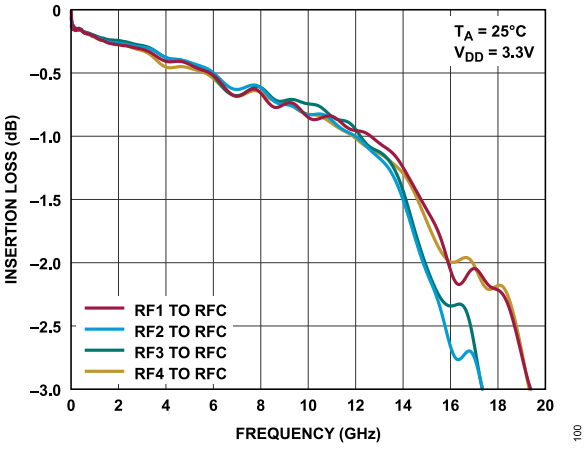


Figure 24. Insertion Loss vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

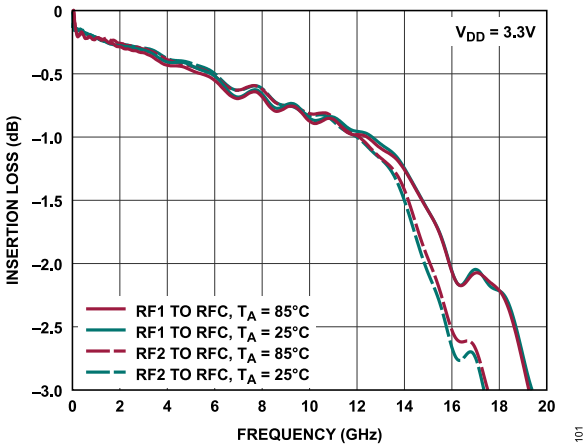


Figure 25. Insertion Loss vs. Frequency over Temperature (RF1 to RFC, RF2 to RFC)

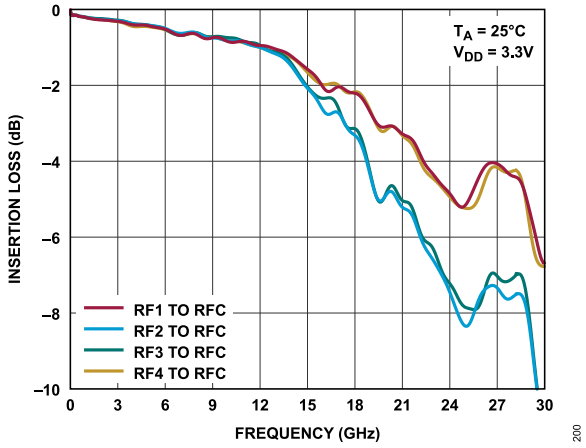


Figure 26. Insertion Loss vs. Frequency

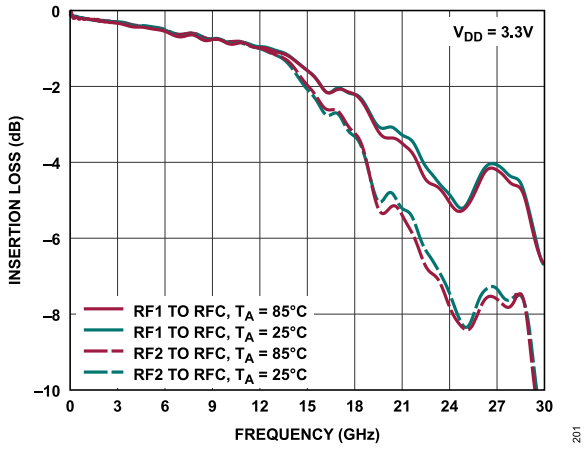


Figure 27. Insertion Loss vs. Frequency over Temperature (RF1 to RFC, RF2 to RFC)

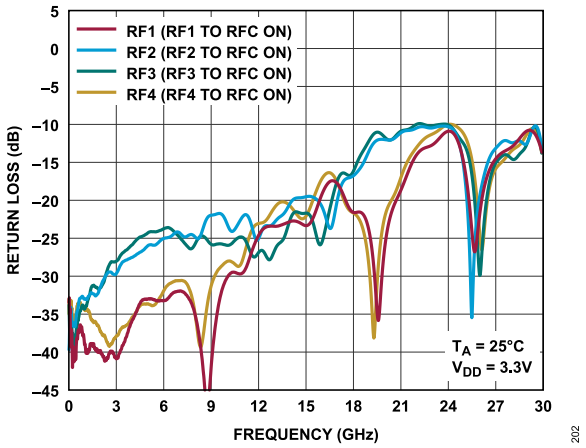


Figure 28. Return Loss vs. Frequency (Measuring from RF1, RF2, RF3, and RF4)

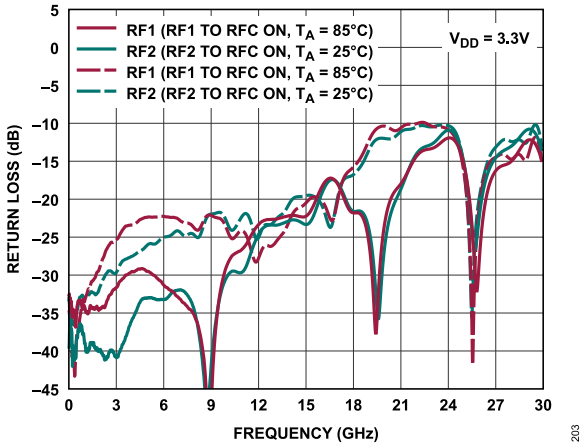


Figure 29. Return Loss vs. Frequency over Temperature (Measuring from RF1, RF2, RF3, and RF4)

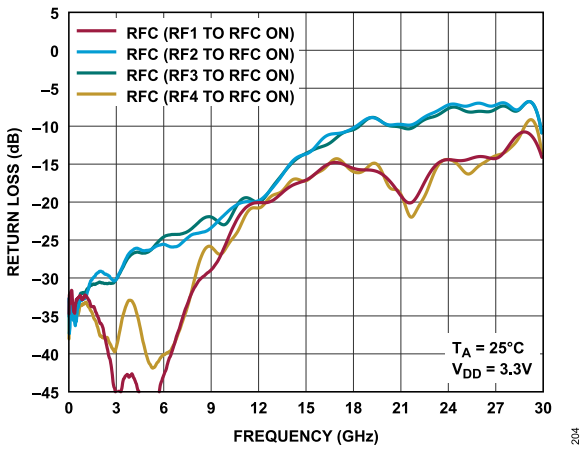


Figure 30. Return Loss vs. Frequency (Measuring from RFC)

TYPICAL PERFORMANCE CHARACTERISTICS

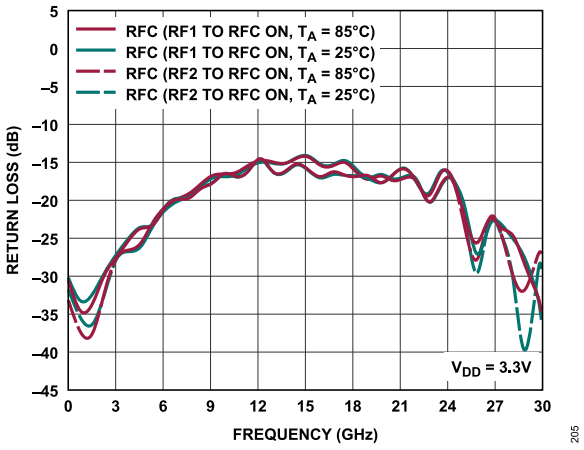


Figure 31. Return Loss vs. Frequency over Temperature (Measuring from RFC)

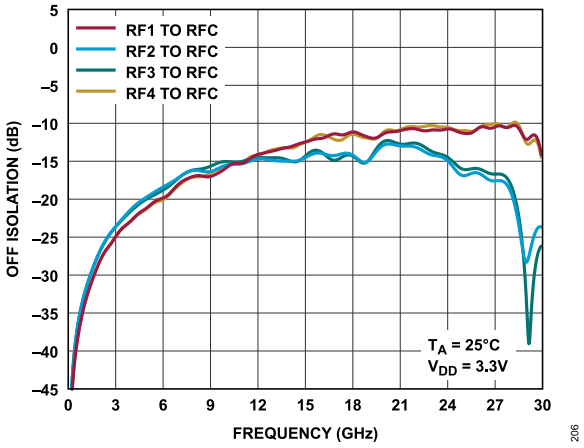


Figure 32. Off Isolation vs. Frequency (All Channels Off)

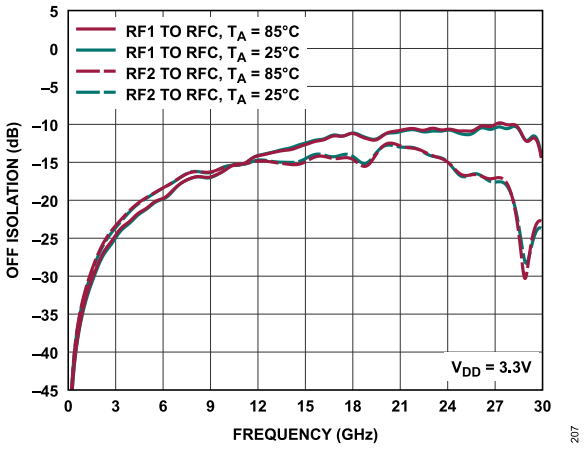


Figure 33. Off Isolation vs. Frequency over Temperature (All Channels Off)

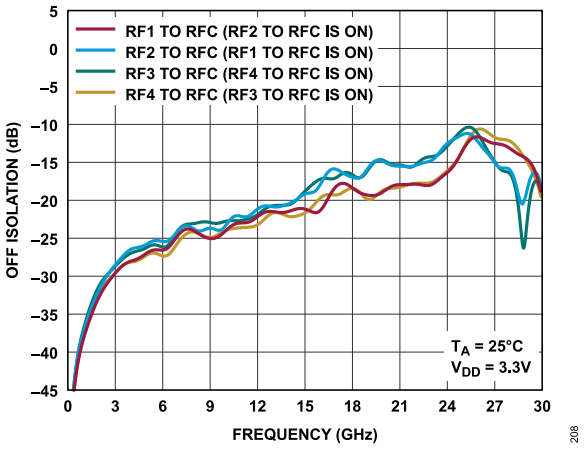


Figure 34. Off Isolation vs. Frequency (One Channel On)

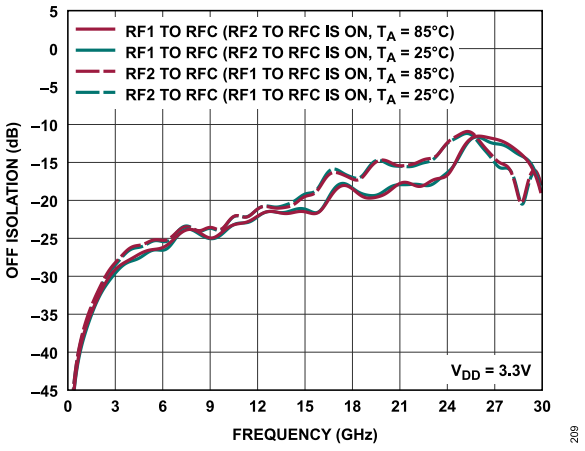


Figure 35. Off Isolation vs. Frequency over Temperature (One Channel On)

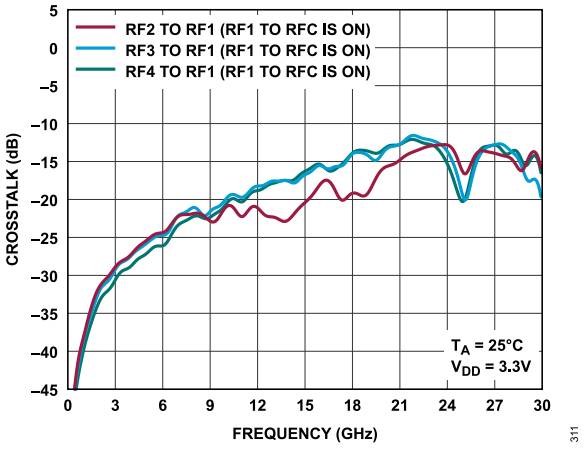


Figure 36. Crosstalk vs. Frequency (RF1 to RFC Is On)

TYPICAL PERFORMANCE CHARACTERISTICS

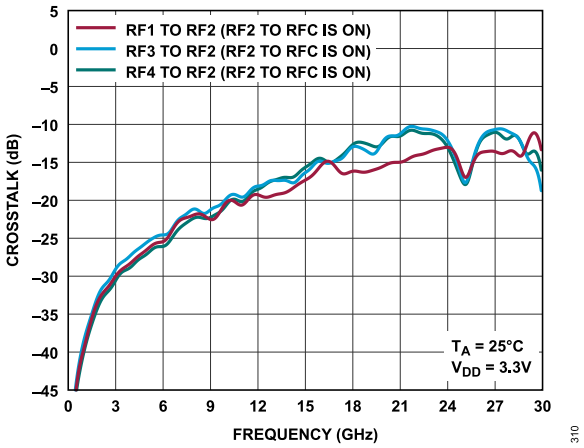


Figure 37. Crosstalk vs. Frequency (RF2 to RFC Is On)

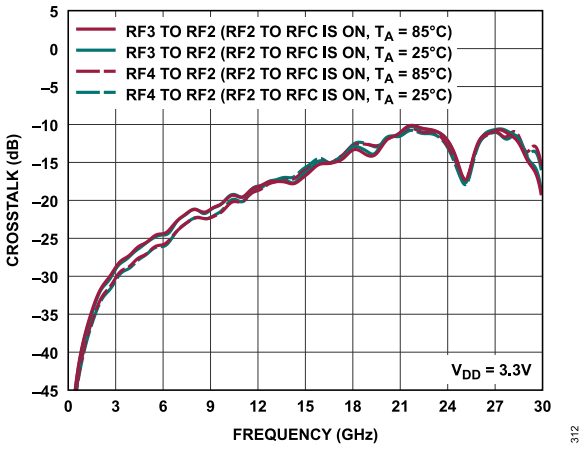
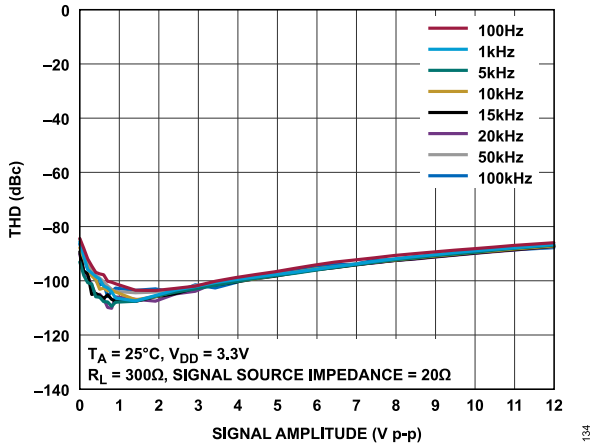


Figure 38. Crosstalk vs. Frequency over Temperature (RF2 to RFC Is On)



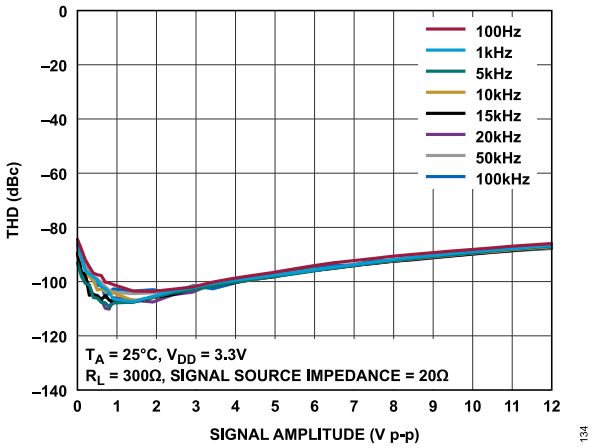


Figure 39. THD vs. Signal Amplitude

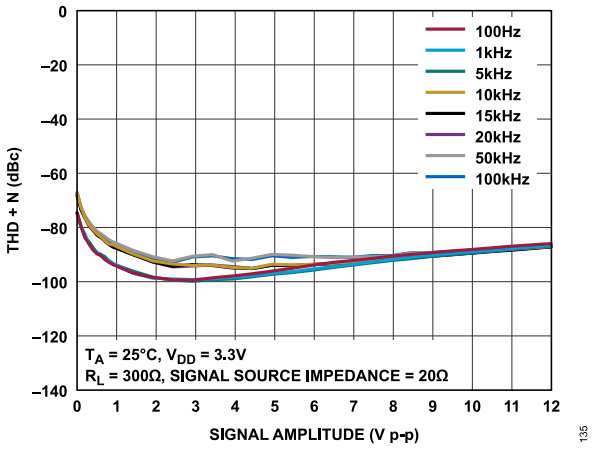


Figure 40. THD + N vs. Signal Amplitude

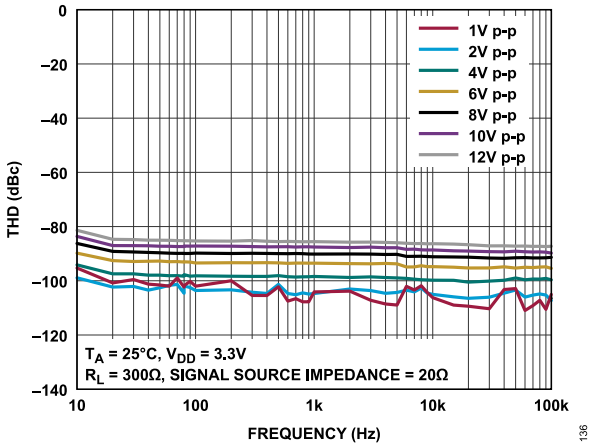


Figure 41. THD vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

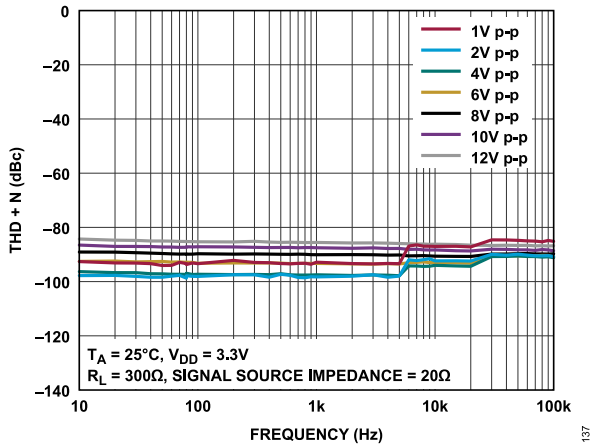


Figure 42. THD + N vs. Frequency

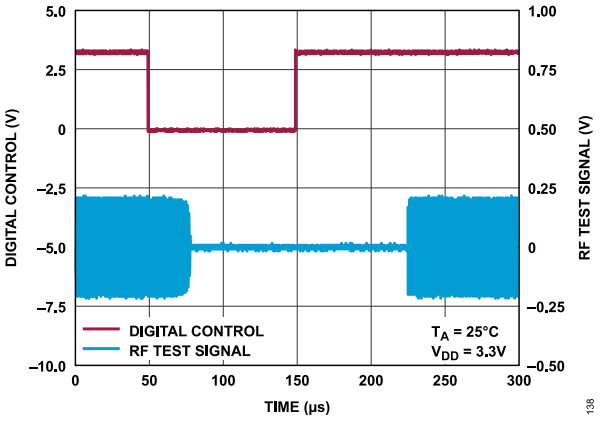


Figure 43. Digital Control and RF Test Signal vs. Time

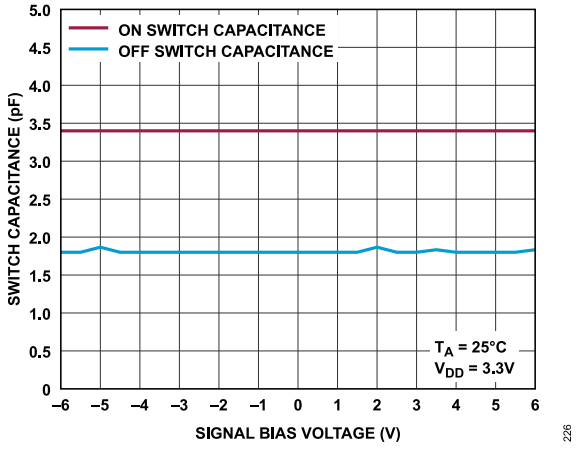


Figure 44. Switch Capacitance vs. Signal Bias Voltage

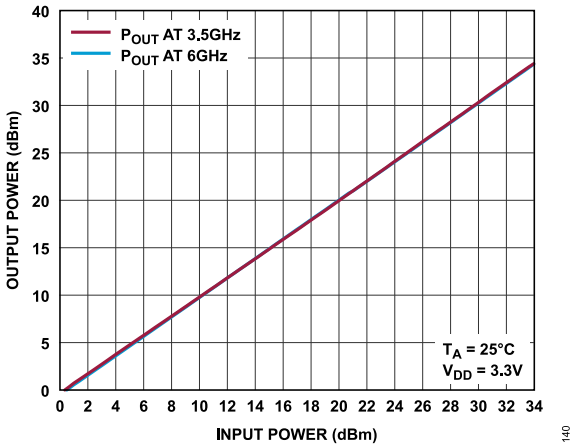


Figure 45. Output Power (P_{OUT}) vs. Input Power (P_{IN})

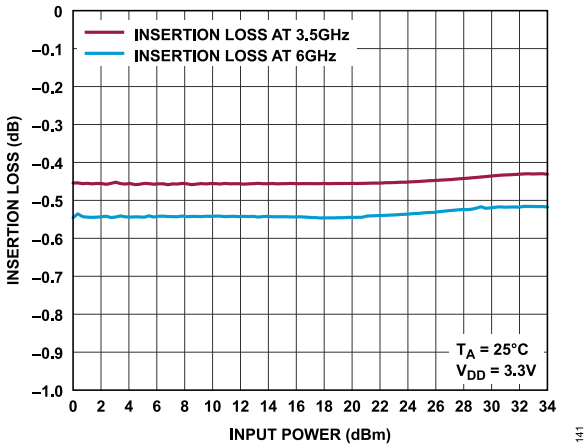


Figure 46. Insertion Loss vs. P_{IN}

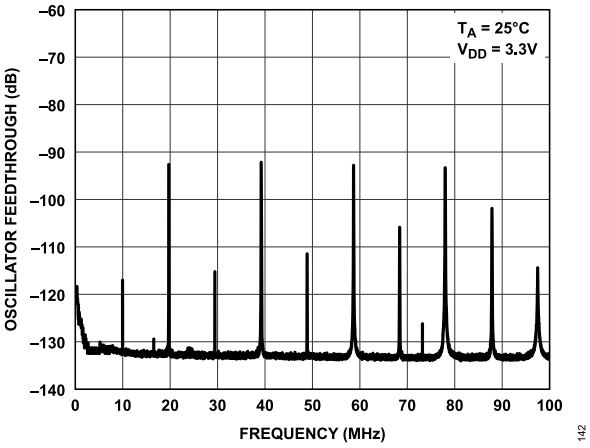


Figure 47. Oscillator Feedthrough vs. Frequency, Wide Bandwidth

TYPICAL PERFORMANCE CHARACTERISTICS

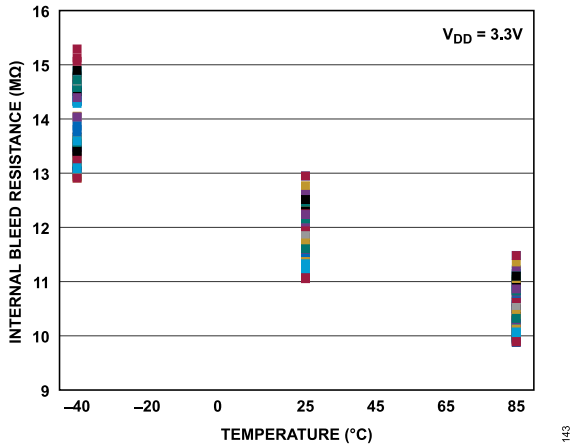


Figure 48. Internal Bleed Resistor Distribution over Temperature

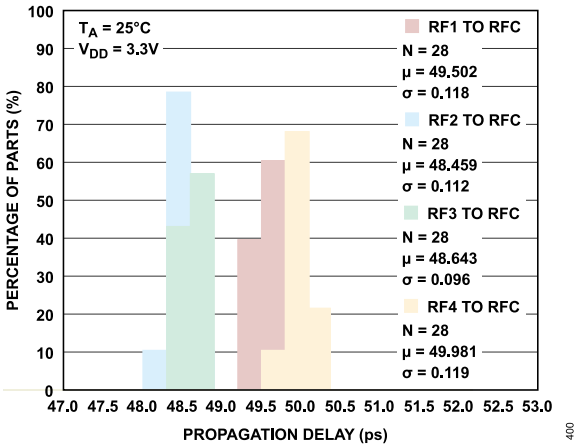


Figure 49. Propagation Delay Histogram

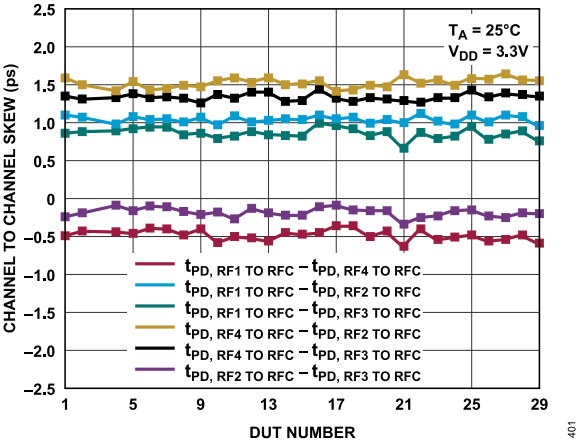


Figure 50. Channel-to-Channel Propagation Delay Skew Across Multiple Devices

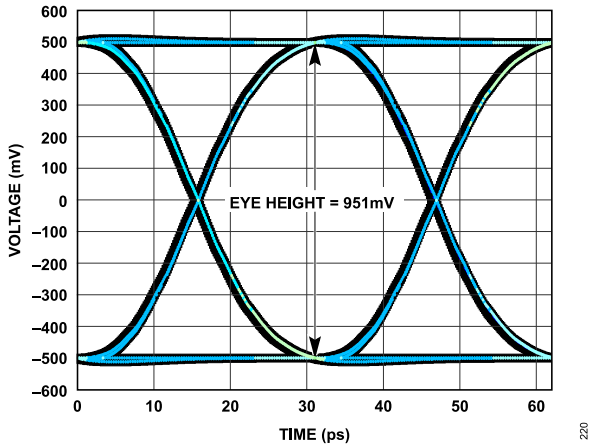


Figure 51. Reference Eye Diagram at 32Gbps (Non-Return-to-Zero (NRZ), T_{RISE}/T_{FALL} = 12ps)

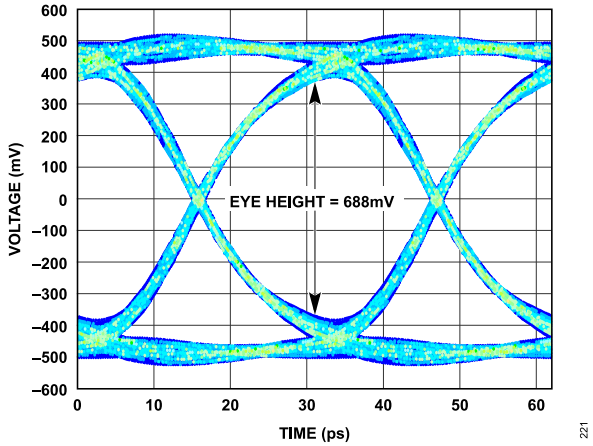


Figure 52. Eye Diagram at 32Gbps (NRZ, T_{RISE}/T_{FALL} = 12 ps, Signal Thru 1 ×ADGM3144)

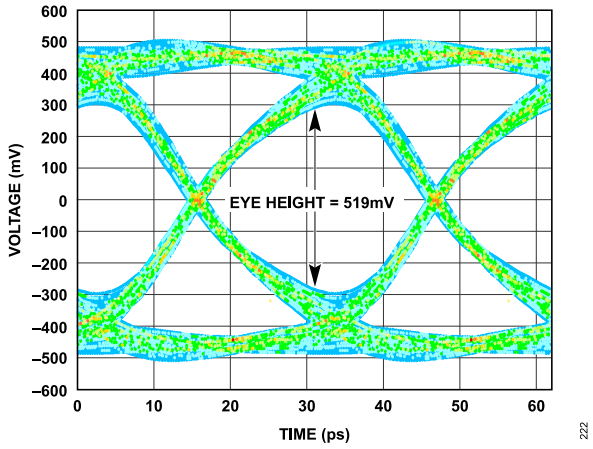


Figure 53. Eye Diagram at 32Gbps (NRZ, T_{RISE}/T_{FALL} = 12ps, Signal Thru 2 × ADGM3144 in Loopback Configuration)

TYPICAL PERFORMANCE CHARACTERISTICS

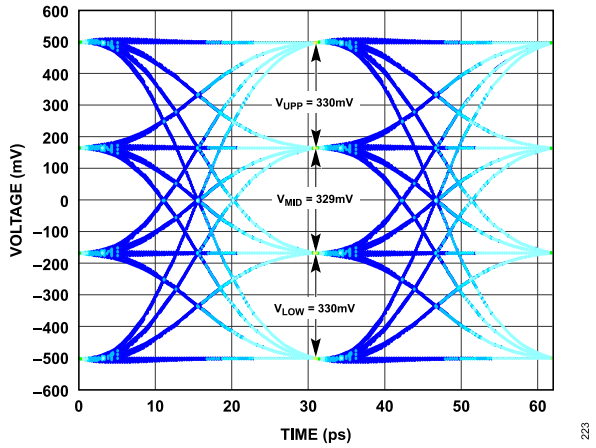


Figure 54. Reference Eye Diagram at 64Gbps (Pattern Used Pulse Amplitude Modulation 4-Level (PAM4), T_{RISE}/T_{FALL} = 12ps)

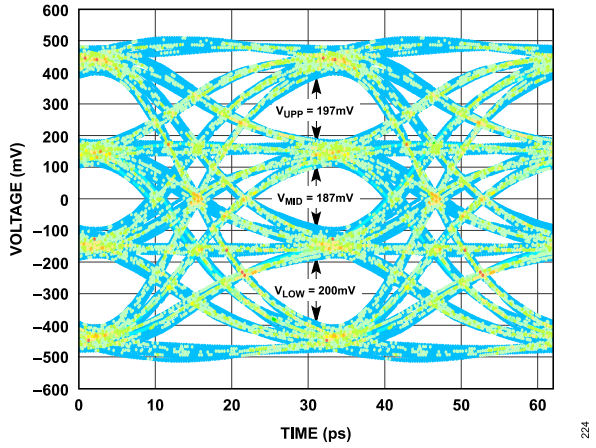


Figure 55. Eye Diagram at 64Gbps (PAM4, T_{RISE}/T_{FALL} = 12ps, Signal Thru 1 × ADGM3144)

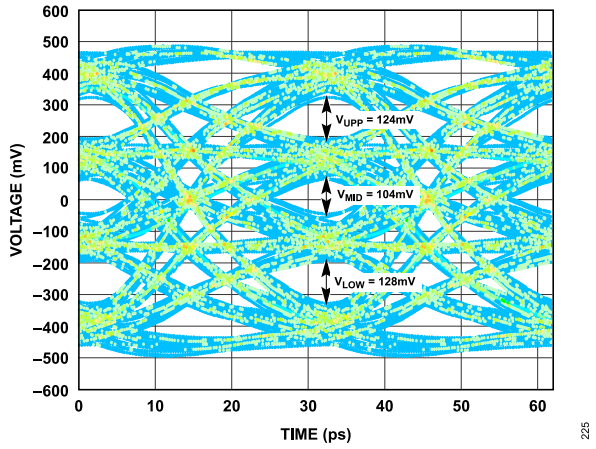


Figure 56. Eye Diagram at 64Gbps (PAM4, T_{RISE}/T_{FALL} = 12ps, Signal Thru 2 × ADGM3144 in Loopback Configuration)

TEST CIRCUITS

DERIVING $C_{DS(OFF)}$ FROM OFF ISOLATION

The following equations is used to derive $C_{DS(OFF)}$ from off isolation measurements taken using the test circuit in Figure 57.

$$OFF\ ISOLATION = 20\log\frac{V_{OUT}}{V_S} \quad (1)$$

$$C_{DS(OFF)} = \frac{1}{2\pi f R_L \left(\frac{2}{10^{OFFISO/20}} - 1\right)} \quad (2)$$

where:

$C_{DS(OFF)}$ is the switch capacitance seen through the switch when all switches are off.

f is the signal frequency.

R_L is the 50 Ω load resistance.

$OFFISO$ is the measured off isolation.

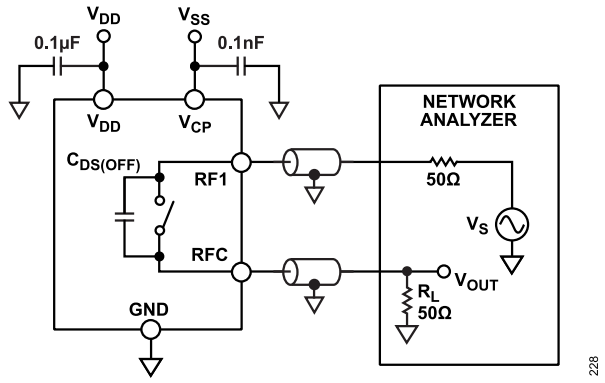


Figure 57. Off Isolation Measurement Test Circuit and $C_{DS(OFF)}$ Derivation

THEORY OF OPERATION

SWITCH DESIGN

The ADGM3144 is a wideband SP4T switch fabricated using Analog Devices' MEMS switch technology. This technology enables high power, low loss, low distortion gigahertz switches to be realized for demanding RF applications.

A key strength of the MEMS switch is that it simultaneously brings together best-in-class high frequency RF performance and 0Hz/DC precision performance. This combination coupled with superior reliability and a tiny surface mountable form factor make the MEMS switch the ideal switching solution for all RF and precision signal instrumentation needs.

The switches are electrostatically actuated MEMS structures. An on board charge pump internally generates the bias voltage (80V) used for actuation of the switch.

PARALLEL DIGITAL INTERFACE

The ADGM3144 can be controlled through a parallel interface. Standard complementary metal-oxide semiconductor (CMOS) or low voltage transistor-transistor logic (LVTTL) signals applied through this interface control the independent actuation or release of all the switch channels of the ADGM3144.

Setting Pin 19 ($\overline{\text{PIN}}$/SPI) low enables the parallel control interface. Pin 20, Pin 21, Pin 22, and Pin 23 (IN1, IN2, IN3, and IN4) control the switching functions of the ADGM3144. When a Logic 1 is applied to one of these pins, the corresponding switch turns on. Conversely, when a Logic 0 is applied, the switch turns off. See Table 7 for the truth table.

When no supply voltage is applied to Pin 1 (V_{DD}), all switches are in an indeterminate state.

Table 7. Truth Table in Parallel Digital Interface Mode

IN1	IN2	IN3	IN4	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
0	0	0	0	Off	Off	Off	Off
0	0	0	1	Off	Off	Off	On
0	0	1	0	Off	Off	On	Off
0	0	1	1	Off	Off	On	On
0	1	0	0	Off	On	Off	Off
0	1	0	1	Off	On	Off	On
0	1	1	0	Off	On	On	Off
0	1	1	1	Off	On	On	On
1	0	0	0	On	Off	Off	Off
1	0	0	1	On	Off	Off	On
1	0	1	0	On	Off	On	Off
1	0	1	1	On	Off	On	On
1	1	0	0	On	On	Off	Off
1	1	0	1	On	On	Off	On
1	1	1	0	On	On	On	Off
1	1	1	1	On	On	On	On

THEORY OF OPERATION

SPI DIGITAL INTERFACE

The ADGM3144 can be controlled through an SPI digital interface when Pin 19 ($\overline{PIN}$/SPI) is high. SPI Mode 0 or Mode 3 can be used with the device, and it operates with SCLK frequencies up to 10MHz. The default mode when the SPI is active is the addressable mode, in which the devices registers are accessed by a 16-bit SPI command bounded by the state of $\overline{CS}$. The ADGM3144 can also operate in the daisy-chain mode.

The SPI pins of the ADGM3144 are $\overline{CS}$, SCLK, SDI, and SDO. Hold $\overline{CS}$ low when using the SPI. Data is captured on SDI on the rising edge of SCLK and data is propagated out on SDO on the falling edge of SCLK. SDO has a push-pull output driver architecture. So, it does not require pull-up resistors. When not pulled low by the ADGM3144, SDO is in a high-impedance state.

Addressable Mode

The addressable mode is the default mode for the ADGM3144 upon power up. A single SPI frame in the addressable mode is bound by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. It comprises 16 SCLK cycles. Figure 58 shows the timing diagram for addressable mode for SPI Mode 0.

The first SDI bit indicates if the SPI command is a read or write command. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command as during these clock cycles SDO propagates out the data contained in the addressed register.

In Mode 0, during any SPI command, SDO sends out eight alignment bits on the $\overline{CS}$ falling edge and the first seven SCLK falling edges (in Mode 3, the first SCLK falling edge is ignored, as shown in Figure 59). The alignment bits observed at SDO are 0x25.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the eighth to the fifteenth SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

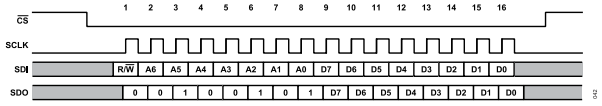


Figure 58. Addressable Mode Timing Diagram (Mode 0)

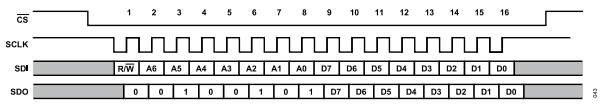


Figure 59. Addressable Mode Timing Diagram (Mode 3)

Daisy-Chain Mode

The connection of several ADGM3144 devices in a daisy-chain configuration is possible. All devices share the same $\overline{CS}$ and SCLK line while the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In the daisy-chain mode, SDO is an 8-cycle delayed version of SDI.

The ADGM3144 may only enter the daisy-chain mode from the addressable mode by sending the 16-bit SPI command, 0x2500. See Figure 60 for an example of this. When the ADGM3144 receives this command, the SDO of devices sends out the same command. This is because the alignment bits at SDO are 0x25. This allows multiple daisy-connected devices to enter the daisy-chain mode in a single SPI frame. A hardware reset is required to exit the daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 61. When $\overline{CS}$ goes high, Device1 writes Command0 [7:0] to its switch data register, Device 2 writes Command1 [7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering the daisy-chain mode, the first eight bits sent out by SDO are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset to zero.

An SCLK rising edge reads in data on SDI while data is propagated out SDO on an SCLK falling edge. The expected number of SCLK cycles should be a multiple of eight before $\overline{CS}$ goes high. When this is not the case, the SPI sends the last eight bits received to the switch data register.

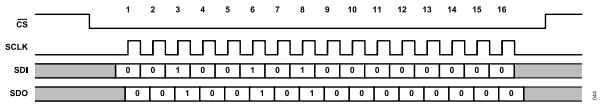


Figure 60. SPI Command to Enter the Daisy-Chain Mode

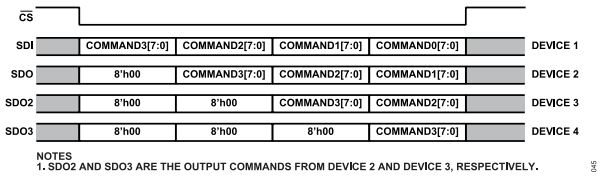


Figure 61. Example of an SPI Frame When Three ADGM3144 are Connected in the Daisy-Chain Mode

Hardware Reset

The digital section of the ADGM3144 goes through an initialization phase during V_{DD} power up. To hardware reset the part, power cycle the V_{DD} input. After power-up or a hardware reset, ensure there is a minimum of 10µs from the time of power-up or reset before any SPI command is issued. Ensure that V_{DD} does not drop out during the 10µs initialization phase because it may result in incorrect operation of the ADGM3144.

THEORY OF OPERATION

Internal Error Status

Where an internal error is detected in the part, it is flagged in the internal error status bits [7:6] of the SWITCH_DATA register. An internal error results from an error in the configuration of the part at power-up.

INTERNAL OSCILLATOR FEEDTHROUGH

The ADGM3144 has an internal oscillator running at a nominal 10MHz. This oscillator drives the charge pump circuitry that provides the actuation voltage for each of the switch gate electrodes. Although this oscillator is very low power, the 10MHz signal is coupled to the switch and can be considered a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −92.5dBm when one switch is on. The V_{DD} level and temperature changes affect the frequency of the noise spur. For the maximum and minimum frequency ranges over temperature and voltage supply range, see Table 1.

TYPICAL OPERATING CIRCUIT

Figure 62 shows the typical operating circuit for the ADGM3144. V_{DD} is connected to 3.3V. EP connects to GND internally. It is recommended to connect GND using one large pad on the PCB to short together GND with EP. Figure 62 shows the ADGM3144 configured to use the internal oscillator as the reference clock to the driver IC control circuit. Decoupling capacitors are required on V_{CP} and V_{DD}. Place a 0.1nF capacitor rated to at least 100V DC as close as possible to V_{CP}. Place a 0.1µF capacitor rated to at least 16V DC as close as possible to V_{DD}.

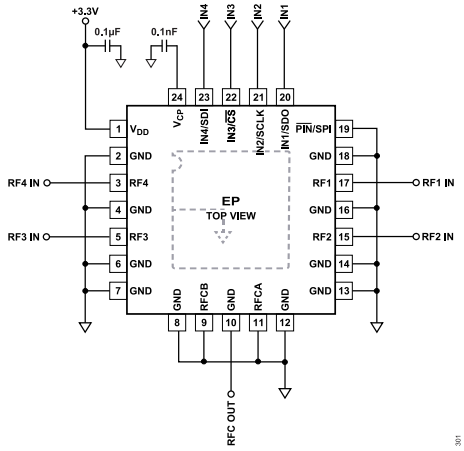


Figure 62. Typical Operating Circuit in the Parallel Digital Interface Mode

APPLICATIONS INFORMATION

POWER SUPPLY RAILS

The ADGM3144 can operate with unipolar supplies between 3.0V and 3.6V. The device is fully specified at a 3.3V analog supply voltage.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

Figure 63 shows an example of a unipolar solution for the ADGM3144. The ADP7142 is a low dropout linear regulator that operates from 2.7V to 40V and is ideal for the regulation of high performance analog and mixed-signal circuits operating from 39V down to 1.2V rails. The ADP7142 has 11µV rms output noise independent of the output voltage. The ADP7142 can be used to power the supply rail for the ADGM3144, a microcontroller, and/or other devices in the signal chain.

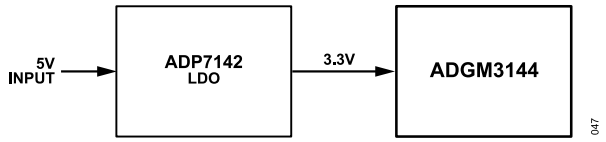


Figure 63. Unipolar Power Solution

If low noise performance at the power supply is required, the ADP7142 can be replaced by the LT1962 or LT3045-1.

Table 8. Recommended Power Management Devices

Product	Description
ADP7142	40V, 200mA, low noise, CMOS low dropout (LDO) linear regulator
LT1962	300mA, low noise, micropower, LDO regulator
LT3045-1	20V, 500mA, ultra-low noise, ultra-high power supply rejection ratio (PSRR) linear regulator with voltage for input to output control (VIOC)

HIGH-SPEED DIGITAL LOOPBACK

Testing high-speed input and output (HSIO) interfaces, such as peripheral component interconnect express (PCIe) Gen 4.0 and PCIe Gen 5.0, in a high volume manufacturing environment is a challenge. A common approach to validate an HSIO interface is the implementation of a high-speed loopback test method. This incorporates both high-speed and DC test paths in one configuration.

To perform high-speed loopback testing, generally a pseudorandom bit sequence (PRBS) is transmitted at high speed from the transmitter and received at the receiver end after being looped back on the load board or test board. At the receiver end, the sequence is analyzed to calculate the bit error rate (BER).

DC parametric tests are performed on the input and output pins, such as a continuity test and a leakage test, to ensure device functionality. To perform these tests, the input/output pins of the DUT must be connected directly to a DC instrument where the DC measurement of the input/output pin is executed.

The ADGM3144 offers both high speed digital and DC testing capability with superior density in a small 3mm × 3mm × 1.5mm LGA package, as shown in Figure 64. The MEMS switch also enables communication from the tester to the device under test (DUT). The ADGM3144 provides excellent performance from DC to 16GHz, which allows the switch to handle both high-speed signals up to 64Gbps and precision DC signals.

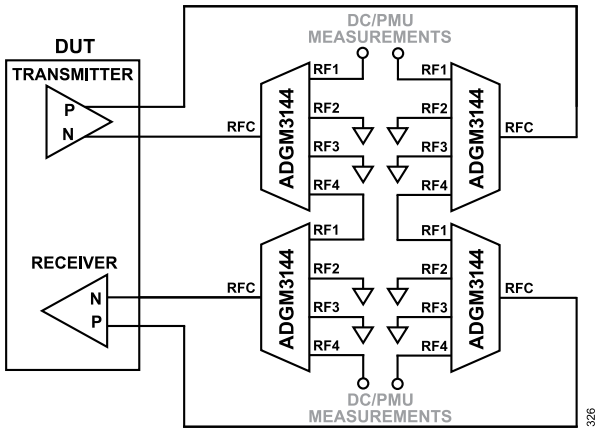


Figure 64. ADGM3144 Enabling Both High-Speed Digital and DC Testing

SWITCHABLE RF ATTENUATOR

It is common to see RF attenuator networks used in RF instrumentation equipment, such as vector network analyzers, spectrum analyzers, and signal generators. Routing RF signals through an attenuator enables the equipment to accept higher power signals and increase the dynamic range of the instrument. In RF attenuation applications, such as vector network analyzers, spectrum analyzers, and signal generators, maintaining the bandwidth of the signal after it passes through the network is critical. Any degradation of the signal reduces the performance of the equipment. Therefore, the RF characteristics of the switches used for routing are integral to the quality of an attenuator network.

The ADGM3144 MEMS switch is suited for use as a switchable RF attenuator due to its low flat insertion loss, wide RF bandwidth, and high reliability. The ADGM3144, as an SP4T switch, also provides added flexibility. Figure 65 shows an example of an attenuation network configuration using two ADGM3144 switches and three different attenuators. The fourth channel of the switches is used as a nonattenuated route.

APPLICATIONS INFORMATION

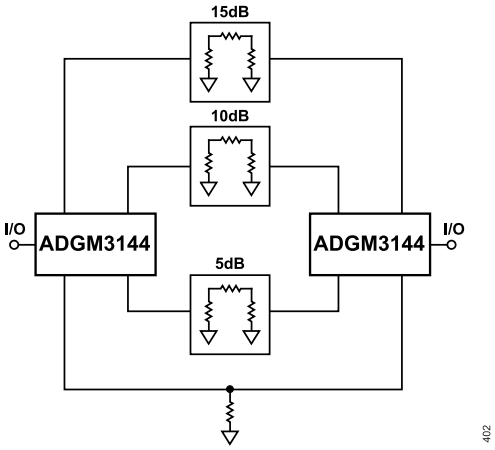


Figure 65. Switching RF Attenuators Using ADGM3144 MEMS Switches

CRITICAL OPERATIONAL REQUIREMENTS

SYSTEM ERROR CONSIDERATIONS DUE TO ON-RESISTANCE DRIFT

The on-resistance (R_{ON}) performance of the ADGM3144 is affected by part-to-part variation, channel-to-channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

In a 50Ω system, the on-resistance drift over switch actuations (ΔR_{ON}) can introduce system inaccuracy. Figure 66 shows the ADGM3144 connected with the load in a 50Ω system, where R_S is the source impedance. To calculate the system error caused by the ADGM3144 ΔR_{ON}, use the following equation:

$$System\ Error\ (\%) = \Delta R / R_{LOAD}$$

where:
ΔR is the ADGM3144 ΔR_{ON}.
R_{LOAD} is the load impedance.

The ADGM3144 ΔR_{ON} also affects insertion loss, which must be considered when using the device. To calculate the on-resistance impact on insertion loss, use the following equation:

$$Insertion\ Loss = 10log\ (1 + (\Delta R / R_{LOAD}))$$

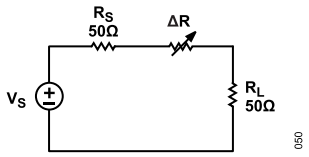


Figure 66. 50Ω System Representation Where the ADGM3144 Is Connected with the Load

Table 9. System Error and Insertion Loss Error Due to ADGM3144 R_{ON} Drift

On-Resistance Drift	System Error (%)	Insertion Loss Error (dB)
0.7	1.4	0.06
2	4	0.17

The ΔR_{ON} over time specification is −0.32Ω (maximum) measured after 100ms, as shown in Figure 13 to Figure 20. According to the plots, the R_{ON} drifts over time is −0.06Ω (typical) after 100ms. The R_{ON} of the ADGM3144 typically drifts by −0.04Ω per decade. For example, after 100ms, the R_{ON} drifts −0.06Ω. After 1s, the R_{ON} drifts −0.1Ω. And after 10s, it drifts −0.14Ω. Therefore, after 1000s, the R_{ON} is expected to drift by −0.22Ω.

ON-RESISTANCE SHIFT DUE TO TEMPERATURE SHOCK POST ACTUATIONS

When the switch is actuated multiple times at one temperature, if there is a sudden shift from this temperature, a large shift is shown in the switch R_{ON}. Figure 67 shows the absolute R_{ON} performance of the population of devices over different number of actuations. During this measurement, the switch is actuated at 85°C and the switch R_{ON} is measured at 25°C. Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for the ADGM3144 ΔR_{ON} over actuations.

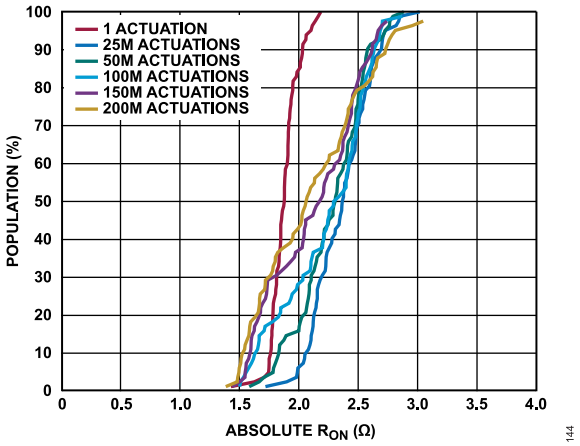


Figure 67. Population vs. Absolute R_{ON}, Switch Actuated at 85°C and R_{ON} Measured at 25°C, Actuation Frequency = 289Hz, V_{DD} = 3.3V

HOT SWITCHING

Hot switching occurs by cycling the switch on or off with an excessive voltage or current applied to the switch. The presence of the applied signal during the switching cycle damages the switch contacts. Hot switching damage is dependent on the current or the voltage levels. Hot switching causes a significant reduction in the cycle lifetime of the switch, as shown in Figure 71 and Figure 73. Figure 68 shows the hot switching condition when the switch is turned on with 1V present at the switch terminal during switching. With a voltage across an off switch, damage can occur as the contact or switch closes.

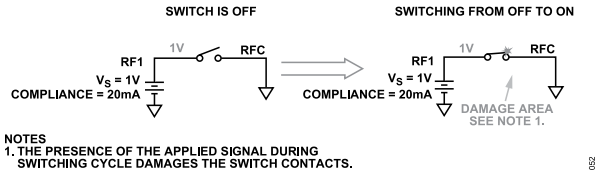


Figure 68. Hot Switching Condition When Turning the Switch from Off to On

Figure 69 shows the hot switching condition when the switch is turned off with 10mA passing through the switch during switching. With current passing through an on switch, damage can occur as the contact or switch opens.

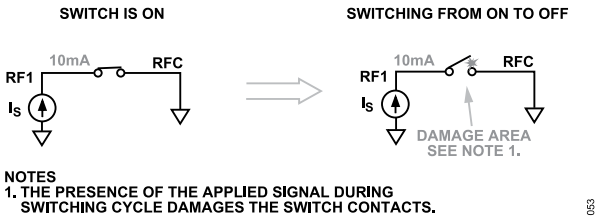


Figure 69. Hot Switching Condition When Turning the Switch from On to Off

CRITICAL OPERATIONAL REQUIREMENTS

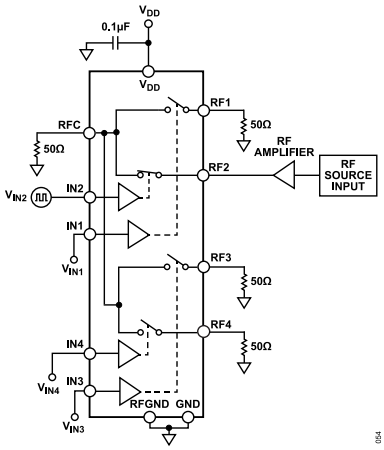


Figure 70. RF Hot Switching Setup

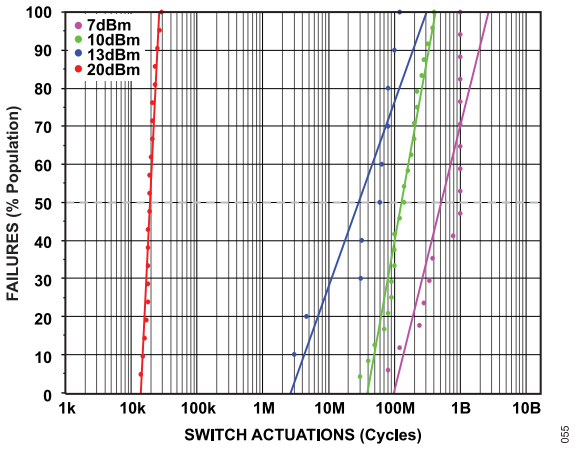


Figure 71. RF Hot Switching Probability Distribution on Log Normal (RF Power = Continuous Wave, Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V)

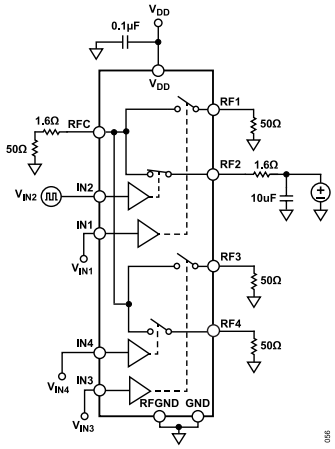


Figure 72. DC Hot Switching Setup

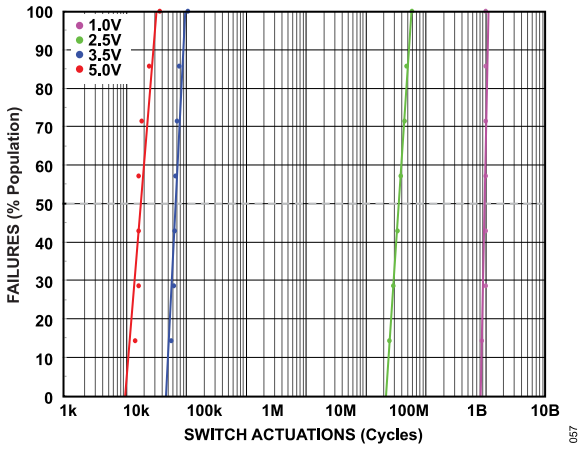


Figure 73. DC Hot Switching Probability Distribution on Log Normal (Terminated into 50Ω, T_A = 25°C, V_{DD} = 3.3 V)

HANDLING PRECAUTIONS

ESD Precautions

All RFx and RFC pins of the ADGM3144 pass the following ESD limits:

- 150V, Class 0B HBM, ANSI/ESDA/JEDEC JS-001-2010
- 1kV Class C3 FICDM ANSI/ESDA/JEDEC JS-002

All RFx and RFC[1] pins are rated to 1kV FICDM, making the device safe for automated handling and assembly process. Standard ESD precautions should be taken during manufacturing.

150V HBM rating of ADGM3144 is susceptible to ESD surge due to human body contact. ESD protection should be added if human body contact is expected.

[1] RFx is RF1, RF2, RF3, and RF4.

CRITICAL OPERATIONAL REQUIREMENTS

Electrical Overstress (EOS) Precautions

ADGM3144 is susceptible to EOS. Therefore, observe the following precautions:

- The ADGM3144 is an ESD-sensitive device. Observe all normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- Avoid running measurement instruments, such as digital multimeters (DMMs), in autorange modes. Some instruments can generate large transient compliance voltages when switching between ranges.
- Use the highest practical DMM range setting (the lowest resolution) for resistance measurements to minimize compliance voltages, particularly during switching.
- Coaxial cables can store charge and lead to EOS when directly connected to the switch. Discharge cables before connecting directly to the switch.
- Avoid connecting capacitive terminations directly to the switch, as shown in Figure 74. A shunt capacitor can store a charge that can potentially lead to hot switching events when the switch opens or closes, affecting the lifetime of the switch.

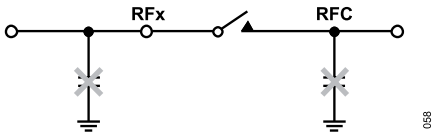


Figure 74. Avoid Large Capacitor Directly Connected to the Switch

Mechanical Shock Precautions

The ADGM3144 passes Group D mechanical shocks tests, as detailed in Absolute Maximum Ratings. These tests validate the robustness of the device to normal mechanical shocks.

The device should not be used if dropped. To reduce excessive mechanical shock and ESD events, avoid handling of loose devices, as outlined in Figure 75.

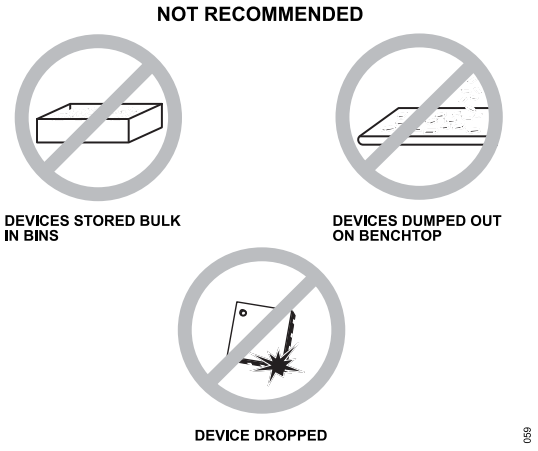


Figure 75. Situations to Avoid During Handling

REGISTER SUMMARY

Table 10. Register Summary

Register (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
0x20	SWITCH_DATA	INTERNAL_ERROR		RESERVED		SWITCH_DATA				0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x20, Reset: 0x00, Name: SWITCH_DATA

The switch data register controls the status of the four switches of the ADGM3144.

Table 11. Bit Descriptions for SWITCH_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	INTERNAL_ERROR		These bits determine if an internal error has occurred.	0x0	R
		00	No error detected.		
		01	Error detected.		
		10	Error detected.		
		11	Error detected.		
[5:4]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
3	SW1_EN		Enable bit for Switch 1.	0x0	R/W
		0	Switch RF1 open.		
		1	Switch RF1 closed.		
2	SW2_EN		Enable bit for Switch 2.	0x0	R/W
		0	Switch RF2 open.		
		1	Switch RF2 closed.		
1	SW3_EN		Enable bit for Switch 3.	0x0	R/W
		0	Switch RF3 open.		
		1	Switch RF3 closed.		
0	SW4_EN		Enable bit for Switch 4.	0x0	R/W
		0	Switch RF4 open.		
		1	Switch RF4 closed.		

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-24-23	LGA	24-Lead Land Grid Array Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADGM3144BCCZ	−40°C to +85°C	24-Terminal Land Grid Array [LGA]	Tray, 490	CC-24-23
ADGM3144BCCZ-R2	−40°C to +85°C	24-Terminal Land Grid Array [LGA]	Reel, 250	CC-24-23
ADGM3144BCCZ-RL7	−40°C to +85°C	24-Terminal Land Grid Array [LGA]	Reel, 1500	CC-24-23

[1] Z = RoHS Compliant Part.