Picoamp Ultra-Low Leakage, Low Voltage, Quad SPST Switch

FEATURES

- ±1.08V to ±2.75V dual supply
- +1.08V to +5.5V single supply
- Ultra-low leakage
  - ±0.3pA typical at 25°C
  - ±8pA typical at 85°C
  - ±56pA typical at 125°C
- 16-lead, 2mm × 2mm LGA Package
- 1.8V and 3V JEDEC compliant logic
- Fully specified at +5V, +3.3V, +1.8V and ±2.5V
- Rail-to-rail signal range

APPLICATIONS

- Instrumentation
- Biosensor measurement
- Electrochemical measurement
- Data acquisition
- Automatic test equipment

GENERAL DESCRIPTION

The ADG2712 is an ultra-low leakage, quad-channel single-pole/single-throw (SPST) switch. The ADG2712 is designed with a unique architecture that provides four individually controlled switch channels each with a typical on leakage current of 8pA at 85°C and 56pA at 125°C. This ultra-low leakage, coupled with low on resistance of just 9.1Ω, provides a compact switching solution for applications that demand the highest precision.

The ADG2712 has a rail-to-rail input signal range. Each switch conducts equally well in both directions when on. The switches are turned on with a Logic 1 input on the corresponding digital control line and the digital control inputs are 1.8V JEDEC compliant for ease of use with microcontrollers and field programmable gate arrays (FPGAs).

The ADG2712 is well suited as a solid-state replacement for mechanical relays in precision measurement and instrumentation applications. It offers significant advantages in reliability, size, and switching speed, while maintaining the low leakage performance traditionally associated with relay-based solutions. The device enables accurate routing of low-level signals without disturbing high-impedance nodes.

With its low leakage characteristics and precision switching performance, the ADG2712 is ideal for use in instrumentation, data acquisition systems, and sensor interfaces—including biosensor and electrochemical measurement applications.

FUNCTIONAL BLOCK DIAGRAM

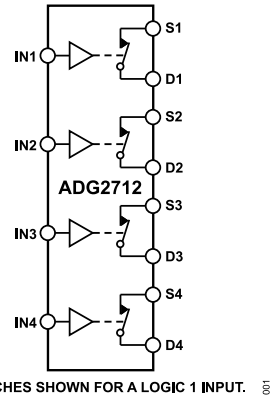

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. Low off-leakage
   a. ±20pA maximum off-leakage at 25°C
   b. ±50pA maximum off-leakage at 85°C
   c. ±160pA maximum off-leakage at 125°C
2. Low on-leakage
   a. ±20pA maximum on-leakage at 25°C
   b. ±55pA maximum on-leakage at 85°C
   c. ±235pA maximum on-leakage at 125°C
3. +1.08V to +5.5V single supply or ±1.08V to ±2.75V dual supply
4. Low on-resistance, 9.1Ω typical
5. JEDEC standard compliant for both 1.8V and 3V logic levels
6. 16-lead, 2mm × 2mm land grid array (LGA)

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REVISION HISTORY

6/2026—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Operating Voltage Range

Supply Voltage	Min	Max	Unit
Dual Supply	±1.08	±2.75	V
Single Supply	+1.08	+5.5	V

+5V SINGLE SUPPLY

V_{DD} = +5V ± 10%, V_{SS} = 0 V, GND = 0V, V_L = 1.65V to 3.6V. All specifications −40°C to +125°C, unless otherwise noted.

Table 2. +5V Single Supply

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +4.5V, V_{SS} = 0V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance (R_{ON})	9.1			Ω typ	Source voltage (V_S) = 0V to V_{DD}, I_S = −10mA
	13	15.5	18	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.07			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	0.3	0.3	0.3	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	2.4			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	3.6	4.3	4.8	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5V
Source Off Leakage, I_S (Off)	±0.1	±2.6	±15	pA typ	V_S = 5V/0.5V, V_D = 0.5V/5V
	±20	±50	±160	pA typ	
Drain Off Leakage, I_D (Off)	±0.1	±2.6	±15	pA typ	V_S = 5V/0.5V, V_D = 0.5V/5V
	±20	±50	±160	pA max	
Channel On Leakage, I_D, I_S (On)	±0.3	±8	±56	pA typ	V_S = V_D = 0.5V, or 5V
	±20	±55	±235	pA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input Current					
I_{INL} or I_{INH}	0.02			μA typ	V_{IN} = V_{INL} or V_{INH}
			0.8	μA max	
Digital-Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
t_{ON}	30			ns typ	Load resistance (R_L) = 300Ω, C_L = 35pF, V_S = 3V
	35	37	38	ns max	
t_{OFF}	214			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 3V
	295	400	490	ns max	
Charge Injection	0.23			pC typ	V_S = 2.5V; R_S = 0Ω, C_L = 1nF
Off Isolation	−60			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 49
	−87			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz see Figure 49
Channel-to-Channel Crosstalk	−104			dB typ	R_L =50Ω, C_L = 5pF, f = 10MHz, see Figure 48
	−119			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz
Total Harmonic Distortion, THD	−80			dB typ	R_L = 10kΩ, 3 V p-p, f = 20kHz
	−77			dB typ	R_L = 10kΩ, 3 V p-p, f = 100kHz
Total Harmonic Distortion + Noise, THD + N	0.01			% typ	R_L = 10kΩ, 3 V p-p, f = 20Hz to 20kHz
Bandwidth −3 dB	473			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 52
Insertion Loss	−0.28			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 52
Source Capacitance, C_S	6			pF typ	V_S = 2.5V, f = 1MHz

SPECIFICATIONS

Table 2. +5V Single Supply (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain Capacitance, C_D	6			pF typ	V_S = 2.5V, f = 1MHz
C_D, C_S (On)	25			pF typ	V_S = 2.5V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = +5.5V
Positive Supply Current, I_{DD}	154			µA typ	Digital inputs = 0V or V_L
	300		300	µA max	
Negative Supply Current, I_{SS}	117			µA typ	Digital inputs = 0V or V_L
	300		300	µA max	
Digital Supply Current, I_L	0.07			µA typ	Digital inputs = 0V or V_L
	1		1	µA max	

+3V SINGLE SUPPLY

V_{DD} = +2.7V to 3.6V, V_{SS} = 0V, GND = 0V, V_L = 1.65V to 3.6V. All specifications −40°C to +125°C, unless otherwise noted.

Table 3. 3V Single Supply

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +2.7V, V_{SS} = 0V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance (R_{ON})	16			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	27	30	33	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	0.4	0.4	0.4	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	4.4			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	8.1	8.8	8.8	Ω max	
LEAKAGE CURRENTS					V_{DD} = +3.6V
Source Off Leakage I_S (Off)	±0.2	±0.8	±10	pA typ	V_S = 3.1V/0.5V, V_D = 0.5V/3.1V
	±20	±35	±100	pA max	
Drain Off Leakage I_D (Off)	±0.2	±0.8	±10	pA typ	V_S = 3.1V/0.5V, V_D = 0.5V/3.1V
	±20	±35	±100	pA max	
Channel On Leakage I_D, I_S (On)	±0.2	±3	±42	pA typ	V_S = V_D = 0.5V, or 3.1V
	±20	±40	±160	pA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input Current					
I_{INL} or I_{INH}	0.02			µA typ	V_{IN} = V_{INL} or V_{INH}
			0.8	µA max	
Digital-Input Capacitance C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
t_{ON}	37			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V
	43	47	49	ns max	
t_{OFF}	175			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V
	249	377	537	ns max	
Charge Injection	0.87			pC typ	V_S = 1.5V; R_S = 0Ω, C_L = 1nF
Off Isolation	−59			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 49
	−86			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 49

SPECIFICATIONS

Table 3. 3V Single Supply (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Channel-to-Channel Crosstalk	−104			dB typ	V_S = 1.5V, R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 48
	−119			dB typ	V_S = 1.5V, R_L = 50Ω, C_L = 5pF, f = 1MHz
THD	−75			dB typ	R_L = 10kΩ, 1.5V p-p, f = 20kHz
	−71			dB typ	R_L = 10kΩ, 1.5V p-p, f = 100kHz
THD + N	0.018			% typ	R_L = 10kΩ, 3V p-p, f = 20Hz to 20kHz
Bandwidth −3 dB	531			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 52
Insertion Loss	−1.1			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 52
C_S	6			pF typ	V_S = 1.5V, f = 1MHz
C_D	6			pF typ	V_S = 1.5V, f = 1MHz
C_D, C_S (On)	24			pF typ	V_S = 1.5V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = +3.6V
I_{DD}	135			µA typ	Digital inputs = 0V or V_L
	300		300	µA max	
I_{SS}	74			µA typ	Digital inputs = 0V or V_L
	300		300	µA max	
I_L	0.08			µA typ	Digital inputs = 0V or V_L
	1		1	µA max	

+1.8V SINGLE SUPPLY

V_{DD} = +1.8V ± 5%, V_{SS} = 0V, GND = 0V. V_L = 1.8V All specifications −40°C to +125°C, unless otherwise noted.

Table 4. +1.8V Single Supply

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +1.71V, V_{SS} = 0V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance (R_{ON})	49			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	88.1	98	98	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.2			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	1.4	1.8	1.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	31			Ω typ	V_S = 0V to V_{DD}, I_S = −10mA
	66.5	78	78	Ω max	
LEAKAGE CURRENTS					V_{DD} = +1.95V
Source Off Leakage I_S (Off)	±0.2	±0.8	±10	pA typ	V_S = 0.5V/1.45V, V_D = 1.45 V/0.5V
	±20	±35	±100	pA max	
Drain Off Leakage I_D (Off)	±0.2	±0.8	±10	pA typ	V_S = 0.5V/1.45V, V_D = 1.45 V/0.5V
	±20	±35	±100	pA max	
Channel On Leakage I_D, I_S (On)	±0.2	±3	±42	pA typ	V_S = V_D = 0.5V, or 1.45V
	±20	±40	±160	pA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input Current					
I_{INL} or I_{INH}	0.02			µA typ	V_{IN} = V_{INL} or V_{INH}
			0.8	µA max	
Digital-Input Capacitance C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					

SPECIFICATIONS

Table 4. +1.8V Single Supply (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
t_{ON}	92			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V
	114	119	120	ns max	
t_{OFF}	145			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V
	377	271	416	ns max	
Charge Injection	0.47			pC typ	V_S = 0.9V; R_S = 0Ω, C_L = 1nF
Off Isolation	−59			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 49
	−85			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 49
Channel-to-Channel Crosstalk	−105			dB typ	V_S = 0.9V, R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 48
	−119			dB typ	V_S = 0.9V, R_L = 50Ω, C_L = 5pF, f = 1MHz
THD	−53			dB typ	R_L = 10kΩ, 1.5V p-p, f =20kHz
	−51			dB typ	R_L = 10kΩ, 1.5V p-p, f = 100kHz
THD + N	0.23			% typ	R_L = 10kΩ, 3 V p-p, f = 20Hz to 20kHz
Bandwidth −3 dB	661			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 52
Insertion Loss	−4.06			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 52
C_S	5			pF typ	V_S = 0.9V, f = 1MHz
C_D	5			pF typ	V_S = 0.9V, f = 1MHz
C_D, C_S (On)	20			pF typ	V_S = 0.9V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = +1.95V
I_{DD}	125			µA typ	Digital inputs = 0 V or V_L
	300		300	µA max	
I_{SS}	84			µA typ	Digital inputs = 0 V or V_L
	300		300	µA max	
I_L	0.07			µA typ	Digital inputs = 0 V or V_L
	1		1	µA max	

±2.5V DUAL SUPPLY

V_{DD} = +2.5V ± 10%, V_{SS} = −2.5V ± 10%, V_L = 1.8V, GND = 0V. All specifications −40°C to +125°C, unless otherwise noted.

Table 5. ±2.5V Dual Supply

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +2.25V, V_{SS} = −2.25V
Analog Signal Range	V_{SS} to V_{DD}			V	
On Resistance (R_{ON})	9.1			Ω typ	V_S = V_{SS} to V_{DD}, I_S = −10mA
	13	15.5	18	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.07			Ω typ	V_S = V_{SS} to V_{DD}, I_S = −10mA
	0.3	0.3	0.3	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	2.4			Ω typ	V_S = V_{SS} to V_{DD}, I_S = −10mA
	3.6	4.3	4.8	Ω max	
LEAKAGE CURRENTS					V_{DD} = +2.75V, V_{SS} = −2.75V
Source Off Leakage I_S (Off)	±0.1	±2.6	±15	pA typ	V_S = +2.25V/−2.25V, V_D = −2.25V/+2.25V
	±20	±50	±160	pA max	
Drain Off Leakage I_D (Off)	±0.1	±2.6	±15	pA typ	V_S = +2.25V/−2.25V, V_D = −2.25V/+2.25V
	±20	±50	±160	pA max	
Channel On Leakage I_D, I_S (On)	±0.3	±8	±56	pA typ	V_S = V_D = −2.25V or +2.25V
	±20	±55	±235	pA max	

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Table 5. ±2.5V Dual Supply (Continued)

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 × V_L	V min	
Input Low Voltage, V_{INL}			0.35 × V_L	V max	
Input Current					
I_{INL} or I_{INH}	0.02			μA typ	V_{IN} = V_{INL} or V_{INH}
			0.8	μA max	
Digital-Input Capacitance C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS					
t_{ON}	32			ns typ	R_L = 300Ω, C_L = 35pF, V_S = 1.5V
	38	40	41	ns max	
t_{OFF}	60			ns typ	R_L = 300Ω, C_L = 35pF, V_S =1.5 V
	70	92	205	ns max	
Charge Injection	0.19			pC typ	V_S = 0V; R_S = 0Ω, C_L = 1nF
Off Isolation	−57			dB typ	R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 49
	−86			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 49
Channel-to-Channel Crosstalk	−104			dB typ	V_S = 0V, R_L = 50Ω, C_L = 5pF, f = 10MHz, see Figure 48
	−118			dB typ	V_S = 0V, R_L = 50Ω, C_L = 5pF, f = 1MHz
THD	−87			dB typ	R_L = 10kΩ, 3V p-p, f = 20kHz
	−76			dB typ	R_L = 10kΩ, 3V p-p, f = 100kHz
THD + N	0.004			% typ	R_L = 10kΩ, 3V p-p, f = 20Hz to 20kHz
Bandwidth −3 dB	509			MHz typ	R_L = 50Ω, C_L = 5pF, see Figure 52
Insertion Loss	−0.52			dB typ	R_L = 50Ω, C_L = 5pF, f = 1MHz, see Figure 52
C_S	6			pF typ	V_S = 0V, f = 1MHz
C_D	6			pF typ	V_S = 0V, f = 1MHz
C_D, C_S (On)	24			pF typ	V_S = 0V, f = 1MHz
POWER REQUIREMENTS					V_{DD} = +2.75V
I_{DD}	138			μA typ	Digital inputs = 0V or V_L
	300		300	μA max	
I_{SS}	77			μA typ	Digital inputs = 0V or V_L
	300		300	μA max	
I_L	0.06			μA typ	Digital inputs = 0V or V_L
	1		1	μA max	

CONTINUOUS CURRENT PER CHANNEL, SX OR DX

Table 6. One Channel On, Per Channel

Parameter	25°C	85°C	125°C	Unit	Test Conditions/ Comments
CONTINUOUS CURRENT, Sx OR Dx[1] (θ_{JA} = 150 °C/W)					
V_{DD} = +5V, V_{SS} = 0V	132	56	22	mA maximum	V_S = V_{SS} to V_{DD}
V_{DD} = +3V, V_{SS} = 0V	100	49	21	mA maximum	V_S = V_{SS} to V_{DD}
V_{DD} = +1.8V, V_{SS} = 0V	70	40	20	mA maximum	V_S = V_{SS} to V_{DD}
V_{DD} = +2.5V, V_{SS} = −2.5V	124	55	22	mA maximum	V_S = V_{SS} to V_{DD}

[1] Sx refers to S1 to S4 pins, and Dx refers to the D1 to D4 pins

SPECIFICATIONS

Table 7. Four Channels On, Per Channel

Parameter	25°C	85°C	125°C	Unit	Test Conditions/ Comments
CONTINUOUS CURRENT, Sx OR Dx [1] (θ_{JA} = 150°C/W)					
V_{DD} = +5V, V_{SS} = 0V	76	42	21	mA maximum	V_S = V_{SS} to V_{DD}
V_{DD} = +3V, V_{SS} = 0V	57	34	19	mA maximum	V_S = V_{SS} to V_{DD}
V_{DD} = +1.8V, V_{SS} = 0V	39	26	16	mA maximum	V_S = V_{SS} to V_{DD}
V_{DD} = +2.5V, V_{SS} = −2.5V	71	40	20	mA maximum	V_S = V_{SS} to V_{DD}

[1] Sx refers to S1 to S4 pins, and Dx refers to the D1 to D4 pins

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8. Absolute Maximum Ratings

Parameter	Rating
V_{DD} to V_{SS}	6V
V_{DD} to GND	−0.3V to +6V
V_{SS} to GND	+0.3V to −6V
V_L to GND	−0.3V to +6V
V_L to V_{SS}	−0.3V to +6V
Analog Inputs[1]	V_{SS} − 0.3V to V_{DD} + 0.3V or 30mA, whichever occurs first
Digital Inputs[1]	GND − 0.3V to +6V or V_{SS} − 0.3V to +6V or 30mA, whichever occurs first
Peak Current, Sx or Dx Pins[2]	354mA (pulsed at 1ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data[3] + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−40°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020

1 Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

2 Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

3 See Table 6 and Table 7.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JCB}[1]	Unit
CC-16-10[2]	150	74.8	°C/W

1 θ_{JCB} is the junction to the bottom of the case value.

2 Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADG2712

Table 10. ADG2712, 16-Lead LGA

Package Type	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

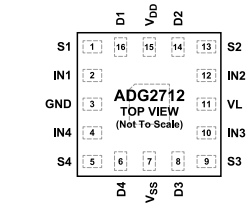

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin	Mnemonic	Description
1	S1	Source Terminal 1. This pin can be an input or output.
2	IN1	Digital Control Input. Logic state controls the status of the switch S1 to D1.
3	GND	Ground (0V) Reference.
4	IN4	Digital Control Input. Logic state controls the status of the switch S4 to D4.
5	S4	Source Terminal 4. This pin can be an input or output.
6	D4	Drain Terminal 4. This pin can be an input or output.
7	V_{SS}	Most Negative Power-Supply Potential. Decouple the V_{SS} pin using a 0.1µF capacitor to GND.
8	D3	Drain Terminal 3. This pin can be an input or output.
9	S3	Source Terminal 3. This pin can be an input or output.
10	IN3	Digital Control Input. Logic state controls the status of the switch S3 to D3.
11	V_L	Digital Logic Power Supply.
12	IN2	Digital Control Input. Logic state controls the status of the switch S2 to D2.
13	S2	Source Terminal 2. This pin can be an input or output.
14	D2	Drain Terminal 2. This pin can be an input or output.
15	V_{DD}	Most Positive Power-Supply Potential. Decouple the V_{DD} pin using a 0.1µF capacitor to GND.
16	D1	Drain Terminal 1. This pin can be an input or output.
EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 12. ADG2712 Truth Table

ADG2712 In	Switch Condition
0	Off
1	On

TYPICAL PERFORMANCE CHARACTERISTICS

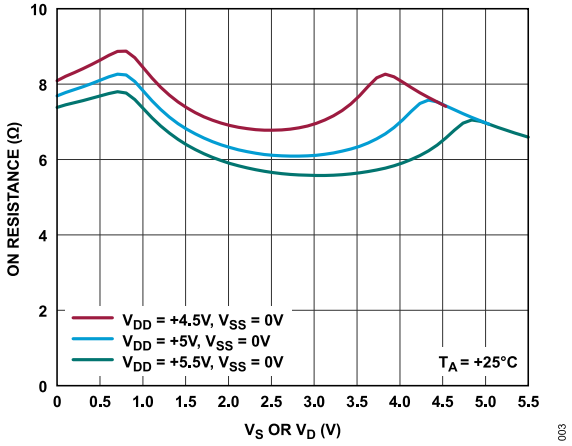

Figure 3. On Resistance vs. V_S or V_D, 5V Single Supply

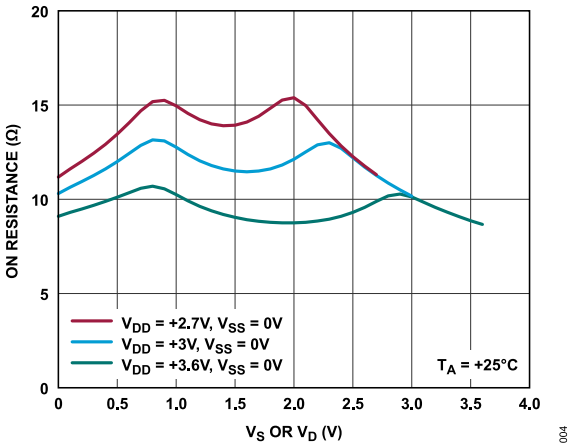

Figure 4. On Resistance vs. V_S or V_D, 3V Single Supply

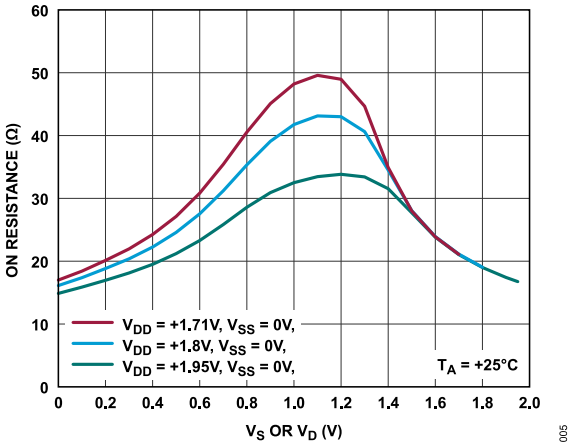

Figure 5. On Resistance vs. V_S or V_D, 1.8V Single Supply

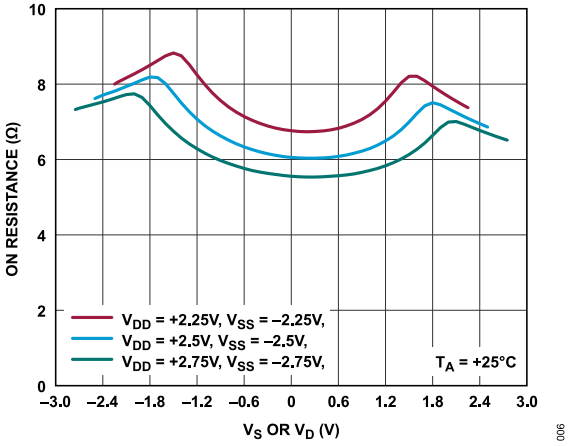

Figure 6. On Resistance vs. V_S or V_D, 2.5V Dual Supply

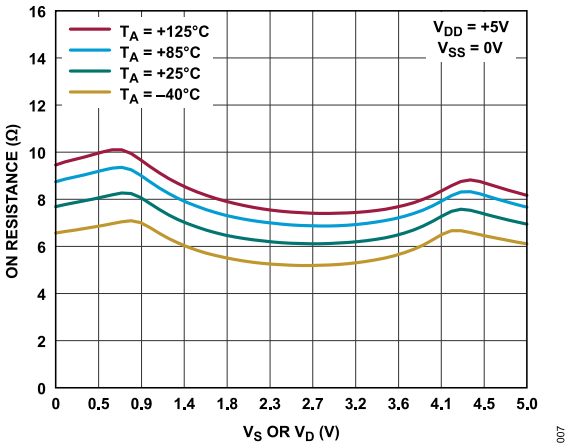

Figure 7. On Resistance vs. V_S or V_D for Different Temperatures, +5V Single Supply

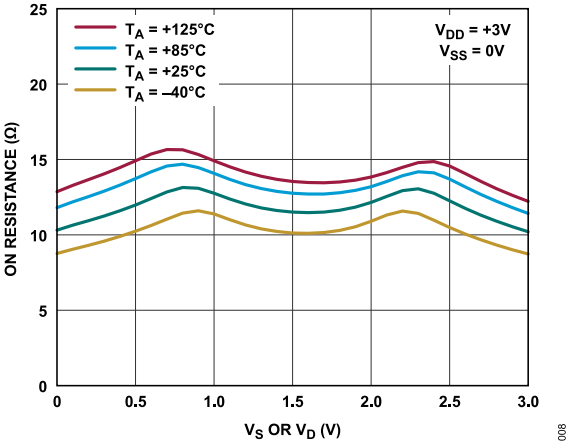

Figure 8. On Resistance vs. V_S or V_D for Different Temperatures, +3V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

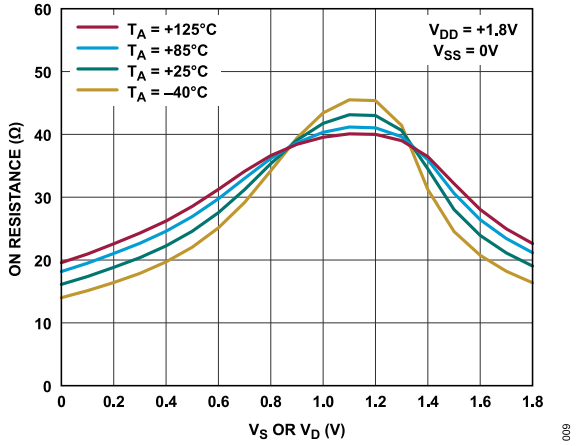

Figure 9. On Resistance vs. V_S or V_D for Different Temperatures, +1.8V Single Supply

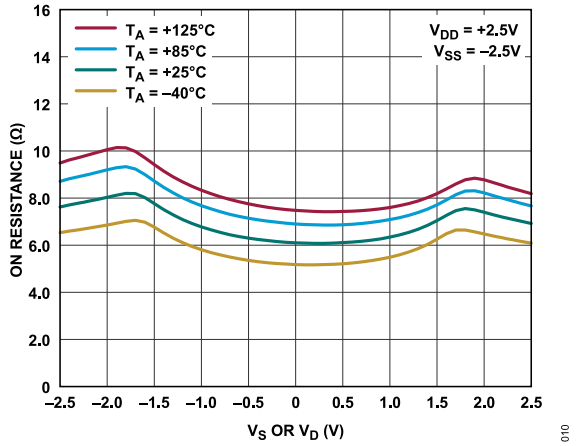

Figure 10. On Resistance vs. V_S or V_D for Different Temperatures, +2.5V Single Supply

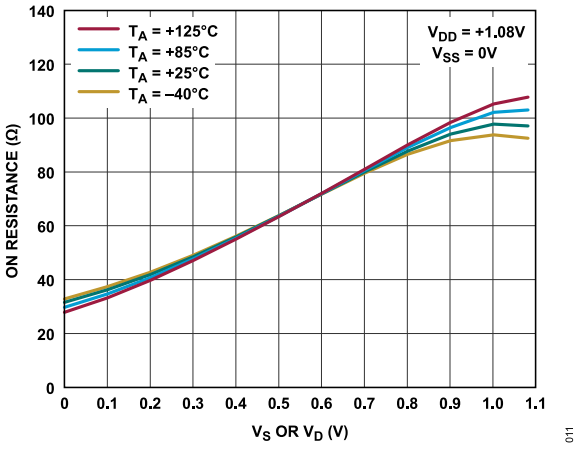

Figure 11. On Resistance vs. V_S or V_D for Different Temperatures, +1.08V Single Supply

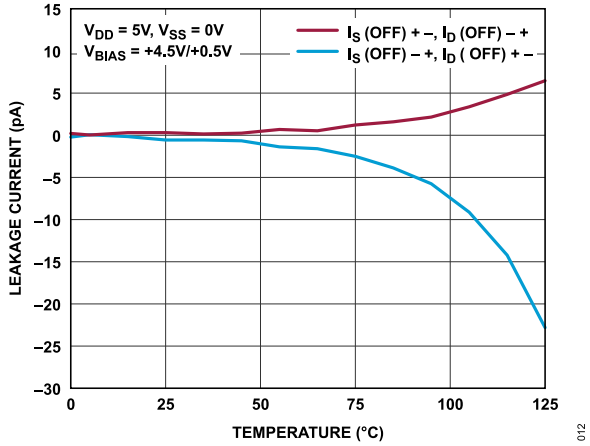

Figure 12. Off-Leakage Currents vs. Temperature, +5V Single Supply

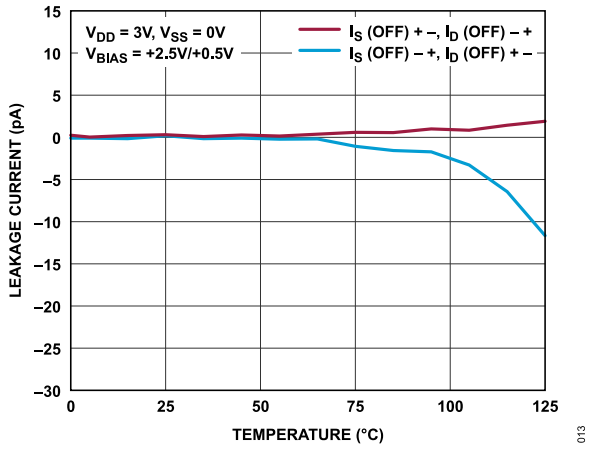

Figure 13. Off-Leakage Currents vs. Temperature, +3V Single Supply

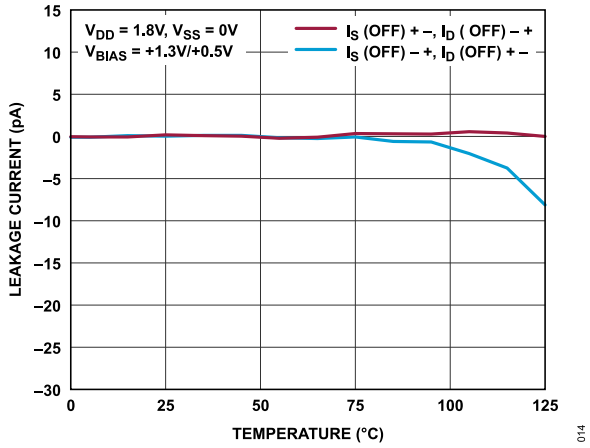

Figure 14. Off-Leakage Currents vs. Temperature, +1.8V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

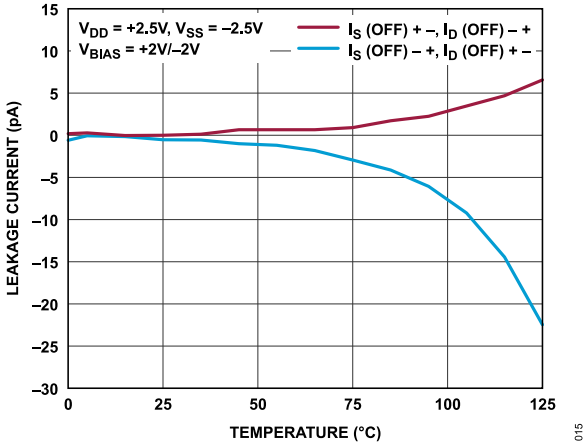

Figure 15. Off-Leakage Currents vs. Temperature, ±2.5V Dual Supply

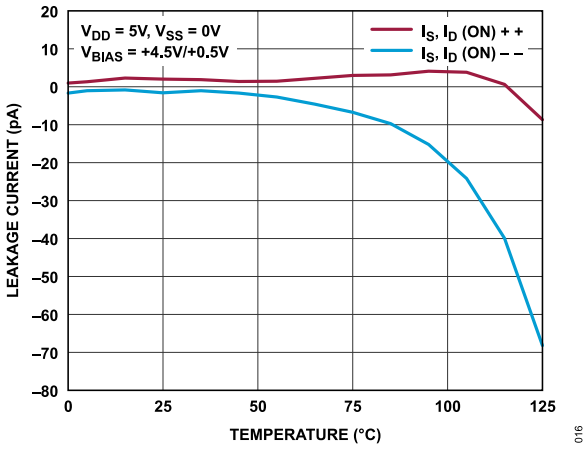

Figure 16. On-Leakage Currents vs. Temperature, +5V Single Supply

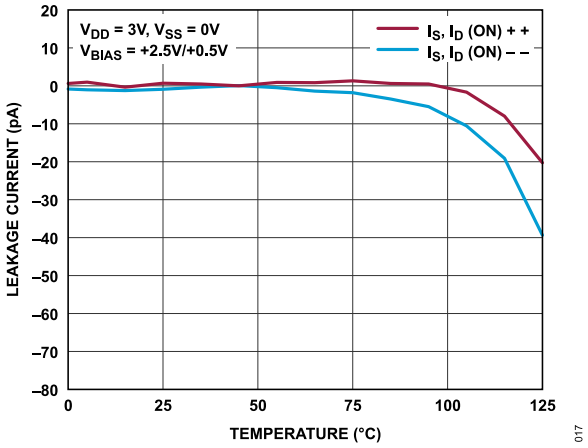

Figure 17. On-Leakage Currents vs. Temperature, +3V Single Supply

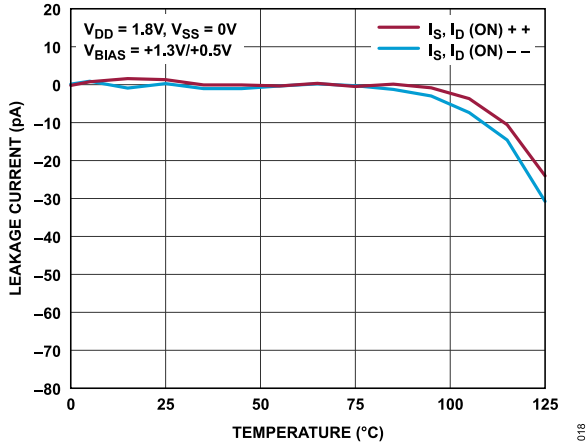

Figure 18. On-Leakage Currents vs. Temperature, +1.8V Single Supply

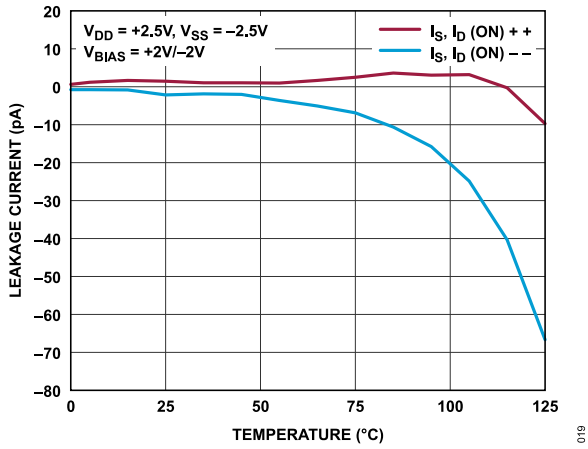

Figure 19. On-Leakage Currents vs. Temperature, +2.5V Dual Supply

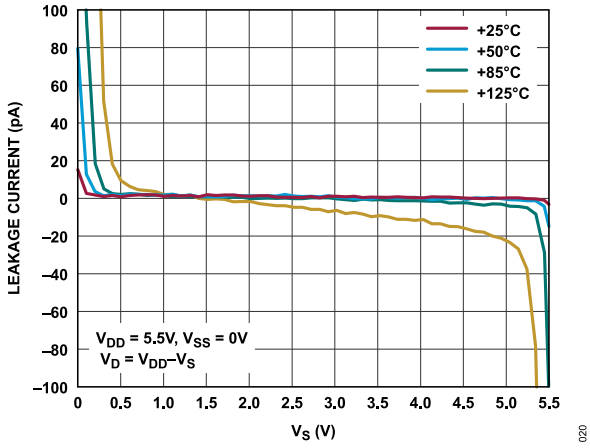

Figure 20. Source Off-Leakage Currents vs. V_S, +5.5V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

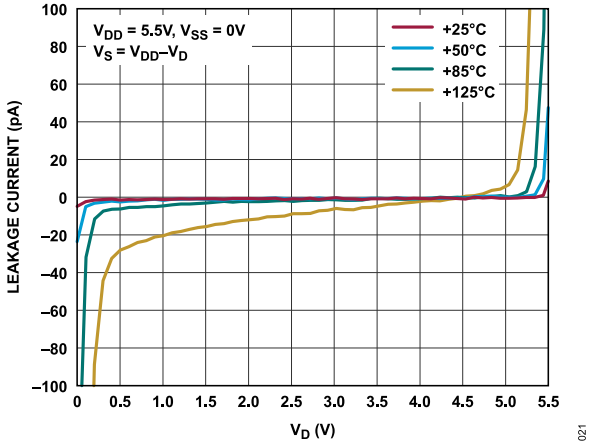

Figure 21. Drain Off-Leakage Currents vs. V_D, +5.5V Single Supply

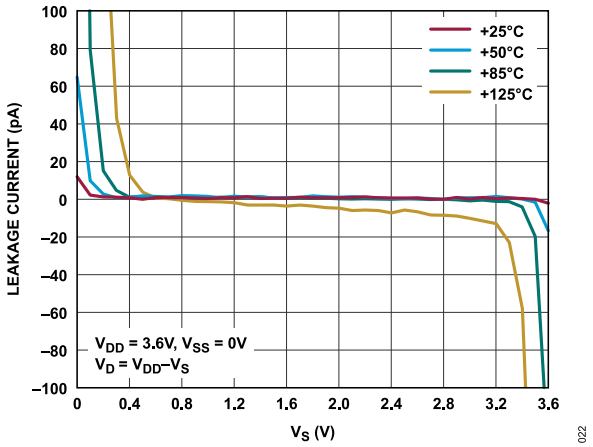

Figure 22. Source Off-Leakage Currents vs. V_S, +3.6V Single Supply

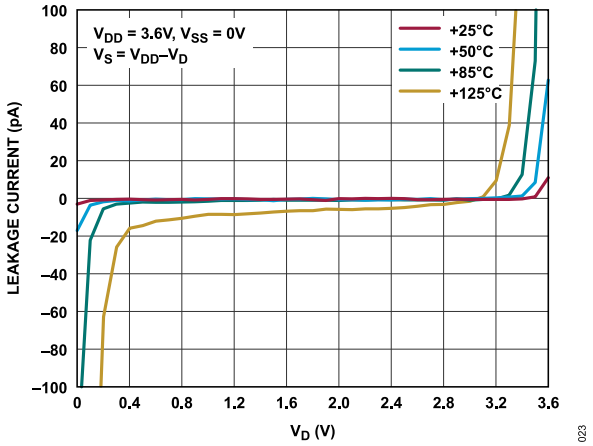

Figure 23. Drain Off-Leakage Currents vs. V_D, +3.6V Single Supply

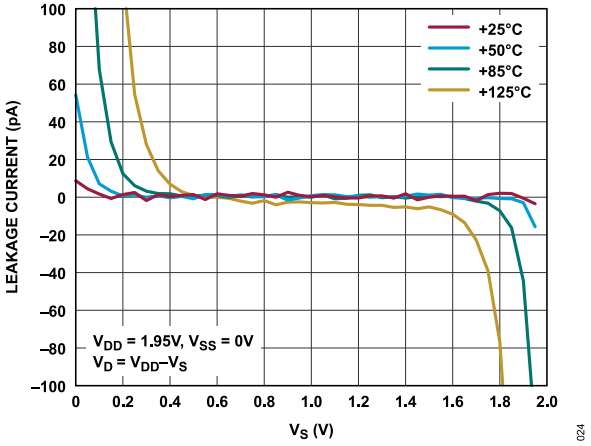

Figure 24. Source Off-Leakage Currents vs. V_S, +1.95V Single Supply

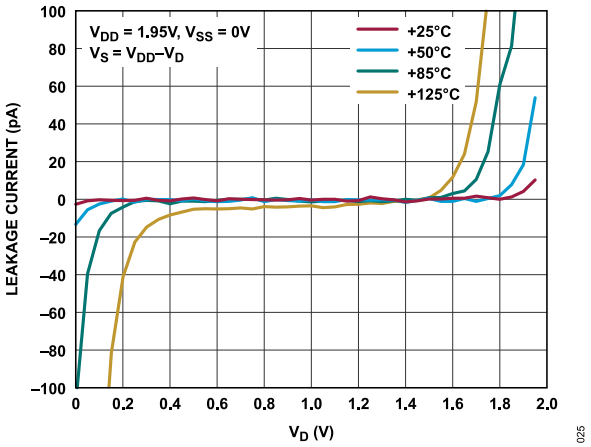

Figure 25. Drain Off-Leakage Currents vs. V_D, +1.95V Single Supply

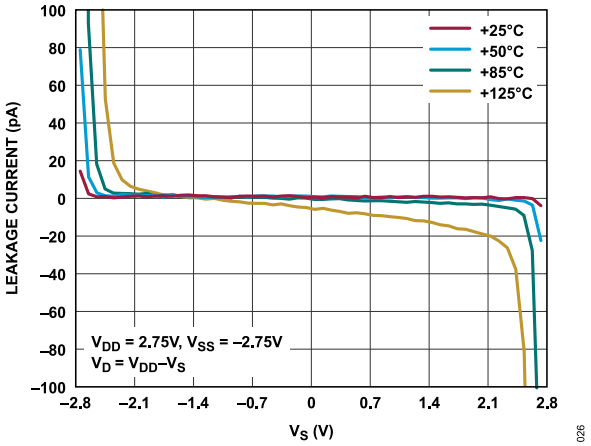

Figure 26. Source Off-Leakage Currents vs. V_S, ±2.75V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

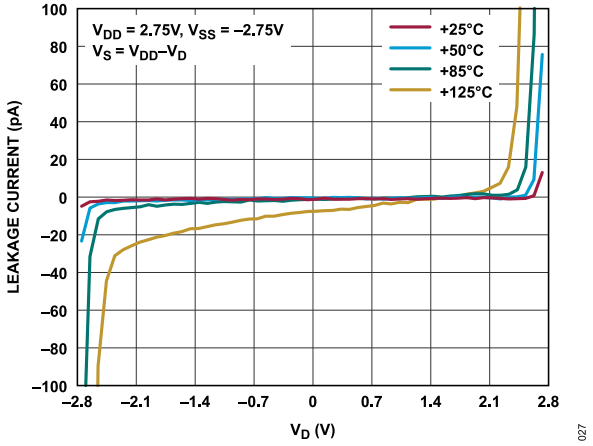

Figure 27. Drain Off-Leakage Currents vs. V_D, ±2.75V Dual Supply

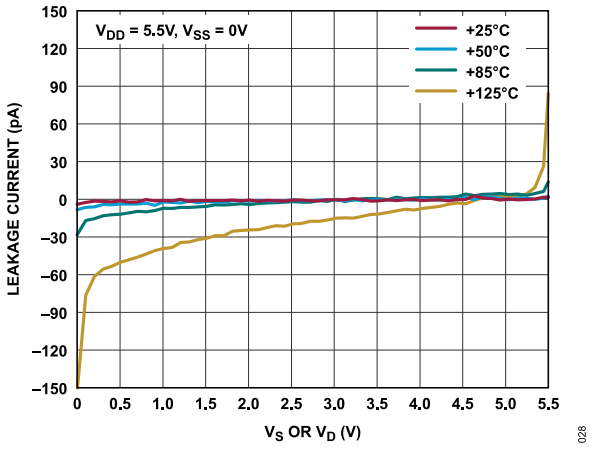

Figure 28. On-Leakage Currents vs. V_S, (V_D), +5.5V Single Supply

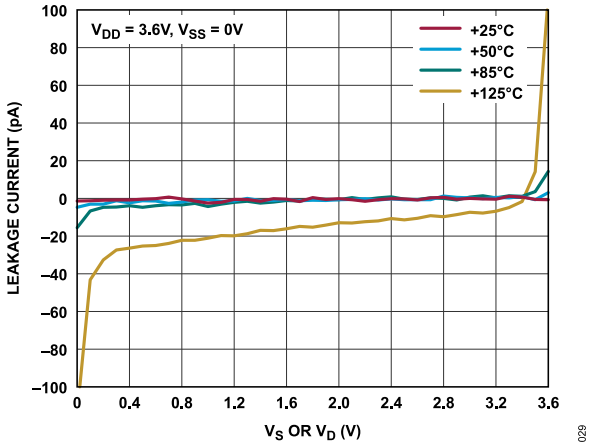

Figure 29. On-Leakage Currents vs. V_S, (V_D), +3.6V Single Supply

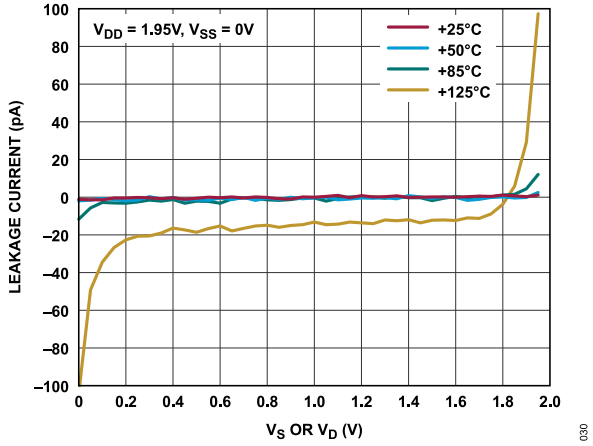

Figure 30. On-Leakage Currents vs. V_S, (V_D), +1.95V Single Supply

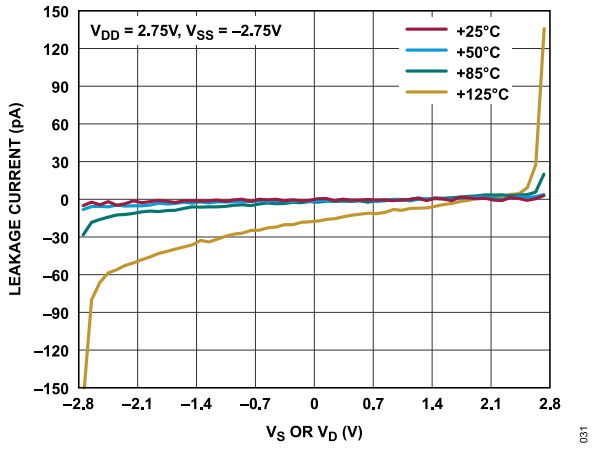

Figure 31. On-Leakage Currents vs. V_S, (V_D), ±2.75V Dual Supply

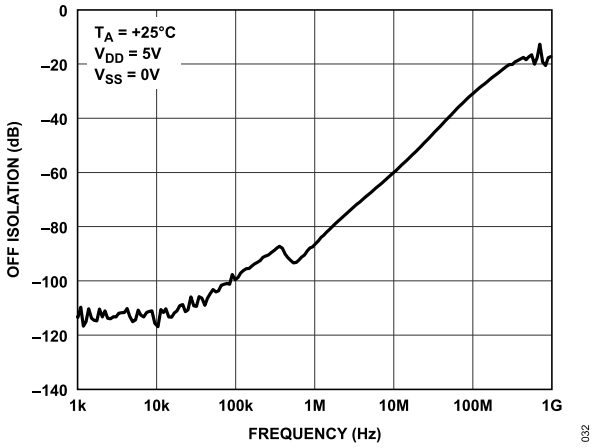

Figure 32. Off-Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

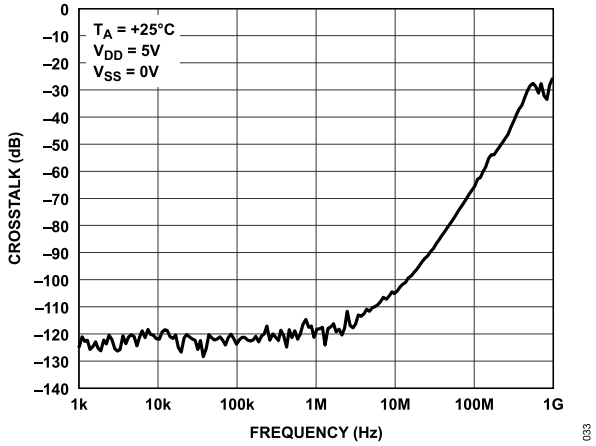

Figure 33. Crosstalk vs. Frequency, 5V Single Supply

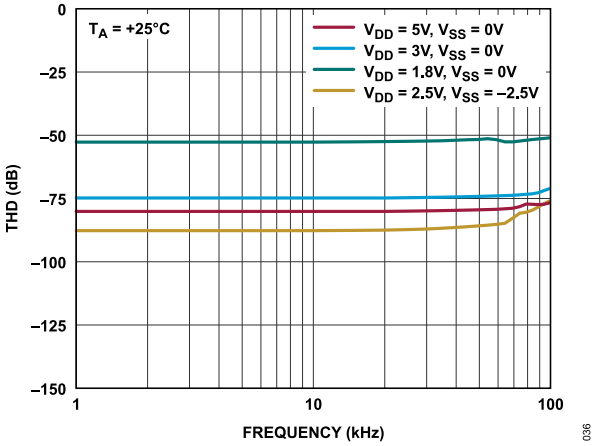

Figure 36. THD vs. Frequency

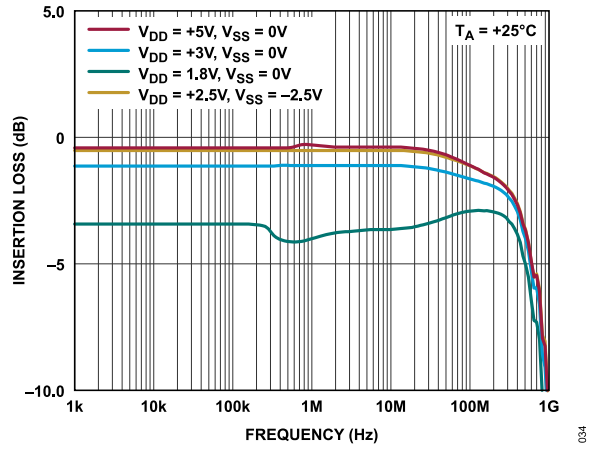

Figure 34. Insertion Loss vs. Frequency

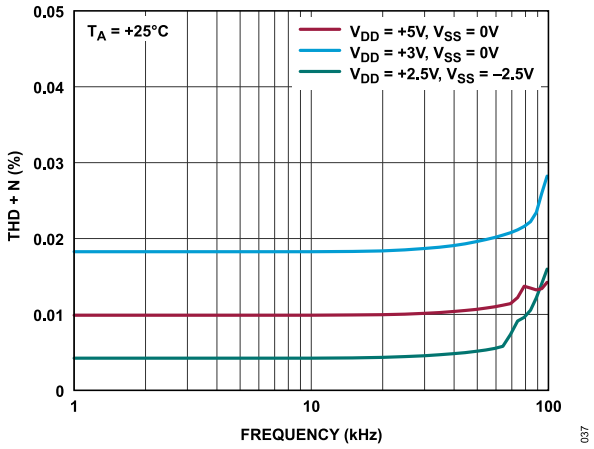

Figure 37. THD + N vs. Frequency

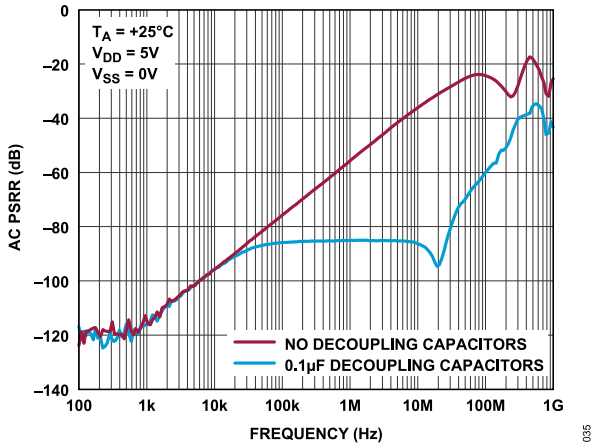

Figure 35. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, 5V Single Supply

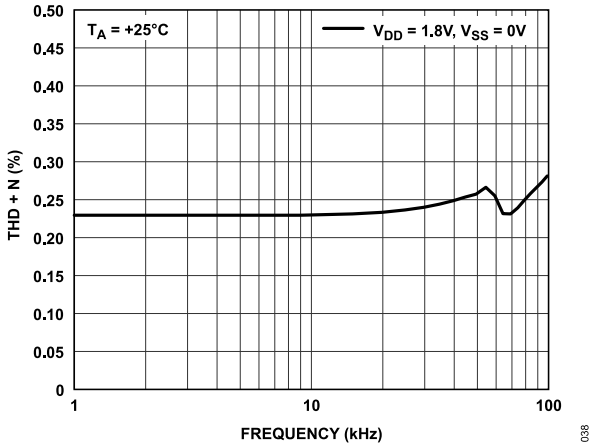

Figure 38. THD + N vs. Frequency, 1.8V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

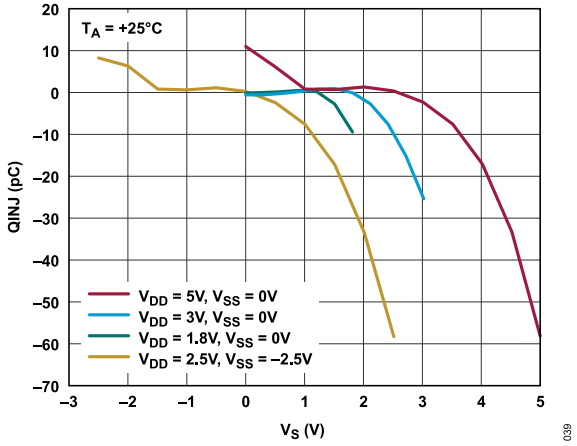

Figure 39. Charge Injection (QINJ) vs. V_S

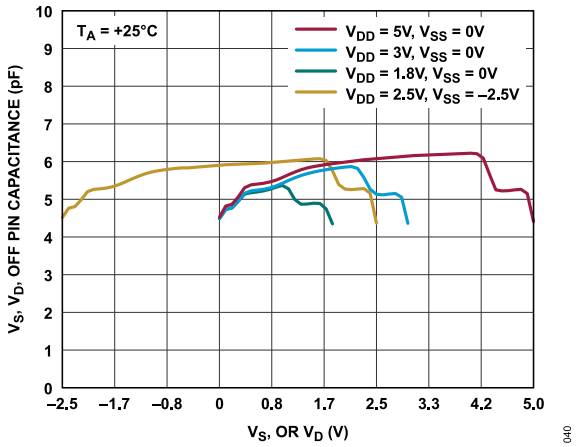

Figure 40. Off Pin Capacitance vs. V_S

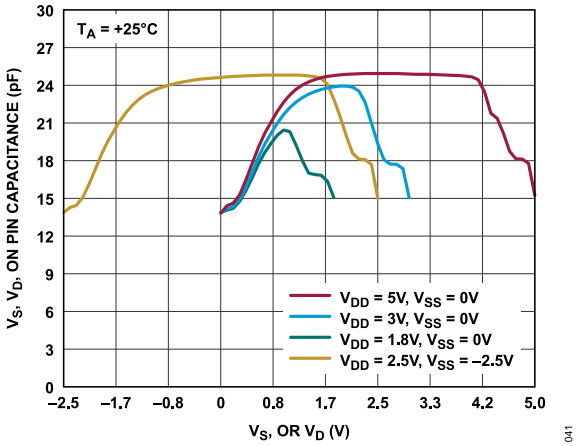

Figure 41. On Pin Capacitance vs. V_S

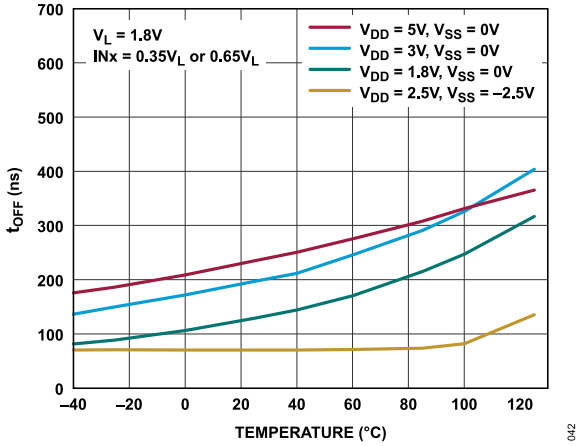

Figure 42. T_{OFF} Times vs. Temperature

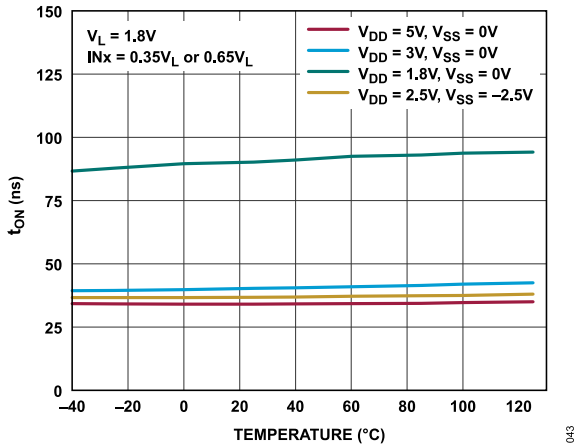

Figure 43. T_{ON} Times vs. Temperature

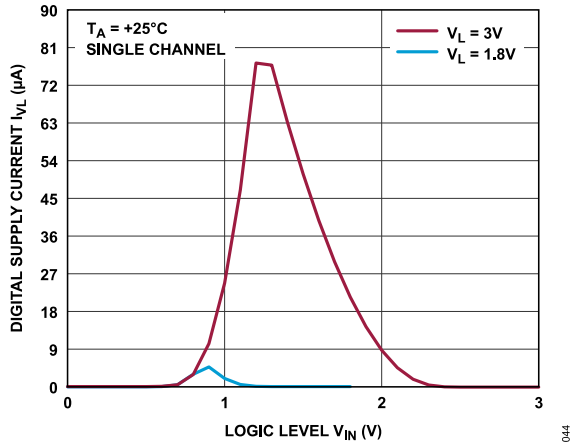

Figure 44. Digital Supply Current vs. Logic Level

TYPICAL PERFORMANCE CHARACTERISTICS

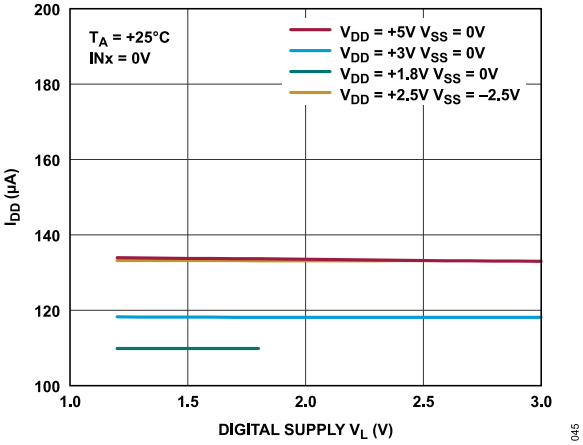

Figure 45. Positive Supply Current (I_{DD}) vs. Digital Supply (V_L)

TEST CIRCUITS

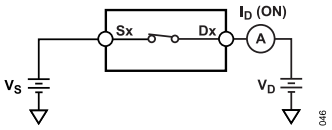

Figure 46. On-Leakage

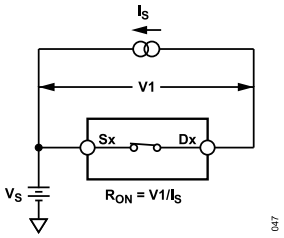

Figure 47. On Resistance

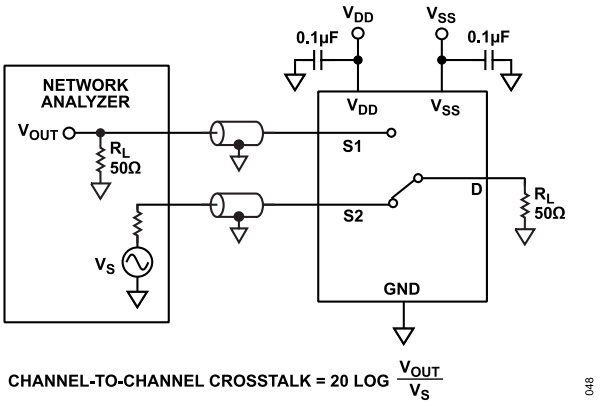

Figure 48. Channel-to-Channel Crosstalk

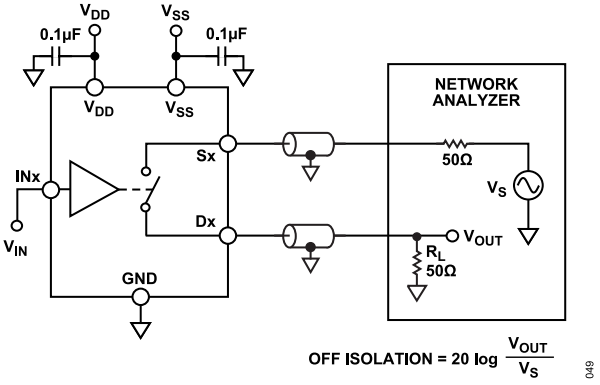

Figure 49. Off-Isolation

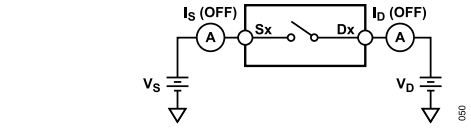

Figure 50. Off-Leakage

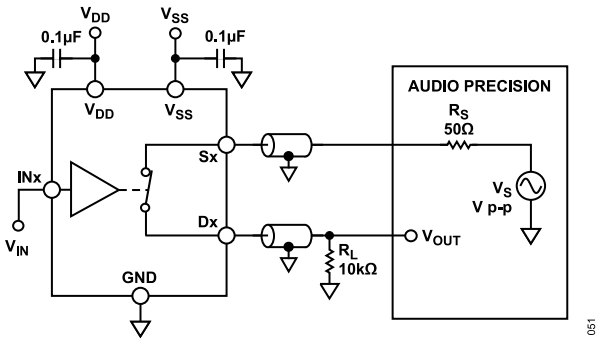

Figure 51. THD + Noise

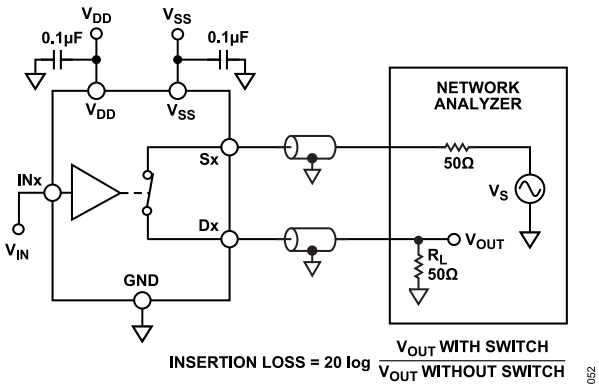

Figure 52. Bandwidth

TEST CIRCUITS

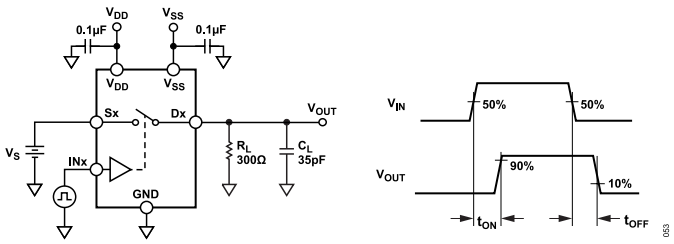

Figure 53. Switching Times

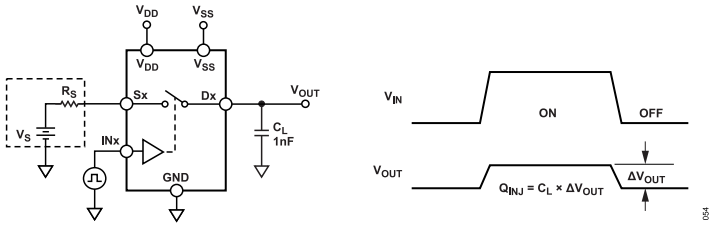

Figure 54. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON}

t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}

t_{OFF} represents the delay between applying the digital control input and the output switching off.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_{BIAS}

V_{BIAS} represents the DC voltage applied to the source or drain of the switch.

THEORY OF OPERATION

SWITCH ARCHITECTURE

The ADG2712 is a set of low voltage CMOS quad SPST switches that are compatible with a wide range of power supply voltages.

The ADG2712 is designed for precision applications where low leakage is a priority. The switch analog inputs are optimized for ultra-low leakage through a patented leakage compensation circuitry that minimizes parasitic currents across voltage and temperature. An internal buffer amplifier actively drives the compensation network to counter residual leakage, enabling accurate performance in high impedance measurement applications.

The ADG2712 gives an optimal balance of low leakage, and low on-resistance (9.1Ω, typical) in a very small 2mm × 2mm LGA package, to suit a very broad range of user applications.

3V AND 1.8V JEDEC COMPLIANCE

An external V_L supply provides flexibility for lower logic levels. The following V_L conditions must be satisfied for the switch to operate in either 3V or 1.8V logic operation:

- V_L = 2.7V to 3.6V for 3V logic
- V_L = 1.65V to 1.95V for 1.8V logic

VL FLEXIBILITY

The absolute maximum voltage rating for the digital control input pins (INx) is −0.3V to +6V. The digital control inputs are not limited to the external V_L supply or V_{DD}. This allows the digital input voltages to be present without the V_L supply and gives the ability to use the V_L pin as an enable pin for all four switch channels in the ADG2712. Regardless of the input voltage on the digital input pins, if V_L = 0V, all of the switch channels will be off. This flexibility also allows V_L voltages higher than V_{DD}. If required, do not violate the 6V maximum voltage rating between V_L and V_{SS}.

LEAKAGE SETTLING TIME

All leakage current measurements require a defined settling period to allow transient effects to decay and the measurement to reach a stable value. For the ADG2712, leakage specifications are measured after a 256ms settling interval to ensure accurate and repeatable results. This interval is illustrated in Figure 55 as t_S.

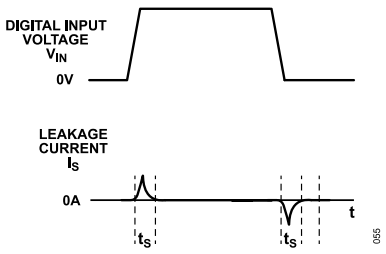

Figure 55. Leakage Settling Time

OUTPUT LOAD RESISTANCE TRANSIENT CURRENT INJECTION

The ADG2712 is optimized for high-impedance applications, where load resistances are typically 20kΩ or greater. The turn-off behavior of the switch channel is influenced by the dynamic response of the internal leakage-compensation amplifier and its associated discharge paths.

During channel turn-off, with lower load resistances, the finite settling time of the internal amplifier can result in a short-duration (~1µs) transient current injection into the load.

APPLICATIONS INFORMATION

POWER-SUPPLY RAILS

To guarantee correct operation of the ADG2712, 0.1µF decoupling capacitors are required on the V_{DD}, V_{SS}, and V_L supply pins.

The ADG2712 can operate with single supplies from +1.08V to +5.5V and dual supplies between ±1.08V to ±2.75V. The supplies on V_{DD} and V_{SS} do not have to be asymmetrical. However, the V_{DD} to V_{SS} range must not exceed 5.5V as stated in Table 1.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a 3V unipolar power solution is shown in Figure 56. The ADP162 ultra-low quiescent current, 150mA, CMOS linear regulator generates a positive supply rail for the ADG2712 along with other components such as amplifiers and/or a precision converter in a typical signal chain.

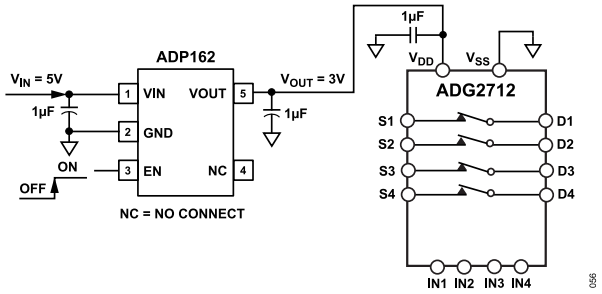

Figure 56. Power Supply Recommendation

POWER UP INITIALIZATION

During power-up, the ADG2712 leakage compensation circuitry requires an initialization period before the specified leakage performance is achieved. Allow a minimum of 120µs after V_{DD} is applied before performing leakage measurements.

PCB LAYOUT

The effective leakage of a switch input in a system can be substantially degraded if the PCB traces are contaminated. Solder flux, body oils, dust, and dirt are all possible sources of contamination. Some of these contaminants form a parallel leakage path across the surface of the existing PCB traces, effectively increasing the insulation resistance. Cleaning and guarding techniques help to suppress these effects.

Cleaning

It is recommended that any contamination is removed by an appropriate cleaning process. The EVAL-ADG2712EBZ evaluation boards for the ADG2712 are cleaned in an electronic PCB washing machine with deionized water on a program shown in Table 13.

Table 13. PCB Cleaning Sequence

Cycle	Time	Temp
Prewash	3 mins	30°C
Wash	15 mins	60°C
Dry	1 hour	90°C

Guarding

Guarding techniques are used to protect against parasitic leakage currents by greatly reducing the voltage gradient seen by the input node. Physically, the concept of guarding is to surround the high-impedance conductor with another conductor (guard) that is driven to the same voltage potential. If there is no voltage across the insulation resistance (between high-impedance conductor and guard), there cannot be any current flowing through it.

The EVAL-ADG2712EBZ evaluation board for the ADG2712 uses guard traces to prevent parasitic leakage currents flowing between conductors on the PCB. The source and drain pin combinations (S1 and D1, S2 and D2, S3 and D3, and S4 and D4) in the pin out of the ADG2712 are purposely placed adjacent to each other so that each source drain pin combination can be guarded together.

The EVAL-ADG2712EBZ evaluation boards are six-layer boards, and the signals were routed on Layer 4. In addition to the adjacent guard traces, guard traces are placed above the signal on Layer 3 and below the signal on Layer 5 to prevent any leakage vertically through the board. An example of the signal guarding in Layer 4 of the evaluation board can be seen in Figure 57. See EVAL-ADG2712EBZ user guide for more details on the PCB layout stackup.

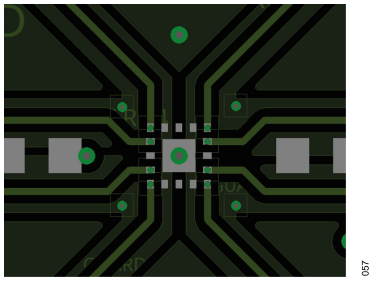

Figure 57. Guarding

Figure 58 and Figure 59 show off-leakage and on-leakage measurements taken from the EVAL-ADG2712EBZ evaluation board. Both graphs illustrate off- and on-leakage measurements within ±1pA.

APPLICATIONS INFORMATION

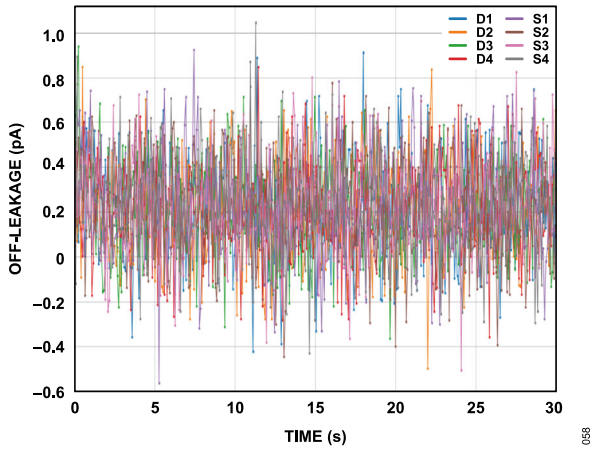

Figure 58. Off-Leakage

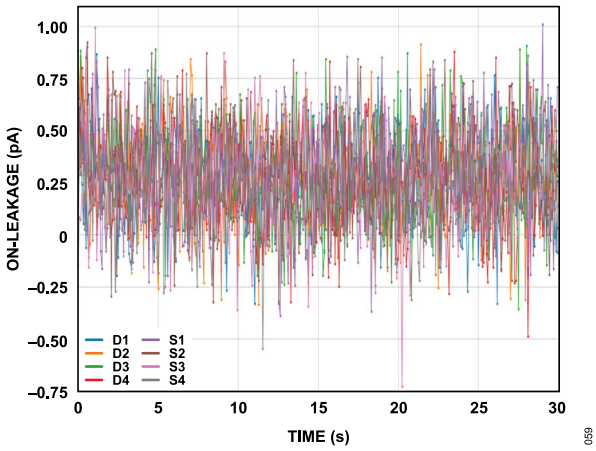

Figure 59. On-Leakage

HIGH-IMPEDANCE SENSOR INPUT

The ADG2712 can be deployed across a wide variety of precision signal-switching applications, particularly where low-voltage signals and high-impedance nodes demand exceptionally low leakage. By minimizing unwanted leakage currents, the device helps maintain measurement accuracy in sensitive systems such as biosensor interfaces, test and measurement equipment, and precision analog front ends.

Figure 60 shows a single channel of a biosensor measurement system, illustrating the role of the ADG2712 in preserving signal integrity in a high-impedance signal chain. The biosensor output is buffered by a low input bias current amplifier before being digitized by an analog-to-digital converter (ADC). In such systems, leakage current at the switching stage can introduce significant measurement errors due to the high source impedance of the sensor. The ADG2712, with its ultra-low off-leakage specification, minimizes unwanted current flow into or out of the measurement node, ensuring accurate acquisition of low-level signals.

The ADG2712 also enables flexible system operation by selectively connecting a digital-to-analog converter (DAC) to the sensor node. When enabled, the switch allows the DAC to apply an excitation voltage or to force a defined potential, such as ground, to one of the sensor terminals while other nodes are measured. This functionality is essential in applications such as electrochemical sensing and impedance measurement, where both stimulus and response must be accurately controlled. The combination of low leakage, precision switching, and high-impedance compatibility makes the ADG2712 well suited for biosensor and other sensitive measurement applications.

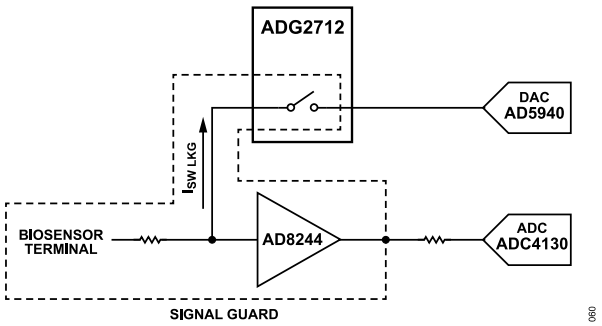

Figure 60. Typical Application

OUTLINE DIMENSIONS

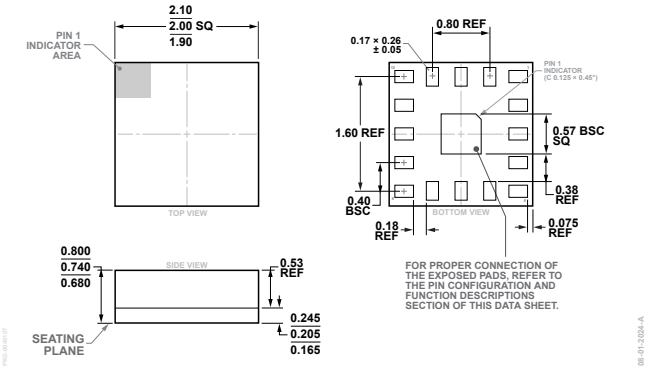

Figure 61. 16-Terminal Land Grid Array [LGA]
2mm × 2mm and 0.74 Package Height
(CC-16-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Packing Quantity
ADG2712BCCZ-RL7	−40°C to +125°C	16-Terminal Land Grid Array [LGA]	CC-16-10	Reel, 3000

[1] Z = RoHS Compliant Part.