Data Sheet

ADEMA124/ADEMA127

Simultaneously Sampling 4- and 7-Channel ΣΔ ADC with SPI

FEATURES

- 4- or 7-channel high performance, simultaneous sampling Σ-Δ ADCs
  - SNR up to 105dB
  - Programmable sample rate of up to 64kSPS
  - Wide input-voltage range: $\pm 1.2V_{PK}$, $848mV_{RMS}$ full-scale
  - High impedance, differential inputs
- Internal voltage reference temperature coefficient: 5ppm/°C typical
- Integrated digital integrator and high-pass filter for use with Rogowski coils
- Fast start-up with first samples in 0.5ms after valid supply
- Tamper detect mode, low power for battery back-up
- 4-wire SPI with bidirectional CRC and daisy-chain functionality
- Simple synchronization of multiple ADC devices
- Gain, phase, and offset compensation for each channel
- Unique SPI readable part ID registers
- Only 18mW power consumption with 7-channel ADC
- Wide temperature range: −40°C to +125°C
- Compact 32-lead, 5mm x 5mm LFCSP

APPLICATIONS

- Polyphase energy meters
- Split-phase energy meters
- Branch circuit monitoring
- Power distribution units
- Power quality monitoring
- Circuit breakers
- Protection relays
- Electric vehicle supply equipment

GENERAL DESCRIPTION

The ADEMA124/ADEMA127 are 4- and 7-channel simultaneously sampling 24-bit sigma delta analog-to-digital converters (ADC), ideal for use in polyphase or split-phase energy metering applications. The ADEMA124/ADEMA127 are compatible with voltage dividers, shunts, and isolated current sensors such as current transformers and Rogowski coils.

The ADEMA124/ADEMA127 include independent hardware and DSP filters enabling gain, phase and offset compensation on each ADC channel. The ADEMA124/ADEMA127 also have bespoke compensation and DSP features, which include an integrator and second-order high-pass filter to allow streamlined Rogowski sensor implementations. DSP filter coefficients for typical use cases are automatically loaded and are accessible for customization of filter characteristics.

The sinc compensation, LPF, and DSP decimate-by-2 feature extend the usable analog bandwidth by up to 70% for a given output sample rate. The high bandwidth makes ADEMA124/ADEMA127 suitable for IEC 61000-4-30 Power Quality Class A and Class S meters. The ADEMA124/ADEMA127 can be used in systems compliant to active energy standards IEC 62053-21, IEC 62053-22, OIML R46ANSI, and C12.20 and reactive energy standards IEC 62053-23, IEC 62053-24, and EN 50470-3. The ADEMA124/ADEMA127 can be used in circuit breakers and protection relays, particularly with a Rogowski sensor due to a 0.5ms fast start-up time.

The ADEMA124/ADEMA127 have a flexible SPI interface for configuration and data retrieval. The daisy-chain SPI interface allows multiple compatible ADCs to be serviced simultaneously by a single SPI port, which saves many pins on the host microcontroller. Additionally, the SPI port is daisy-chain compatible with the 2- and 3-channel isolated ADC, ADE9112/ADE9113. To maintain integrity of ADC waveform data, independent cyclic redundancy checks (CRC) are available to detect errors in inbound and outbound SPI packets, and incidental changes of configuration registers.

Table 1. Product Comparison

Model	24-Bit ADC Channels
ADEMA124	4
ADEMA127	7

Rev. 0

TABLE OF CONTENTS

REVISION HISTORY

7/2025—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

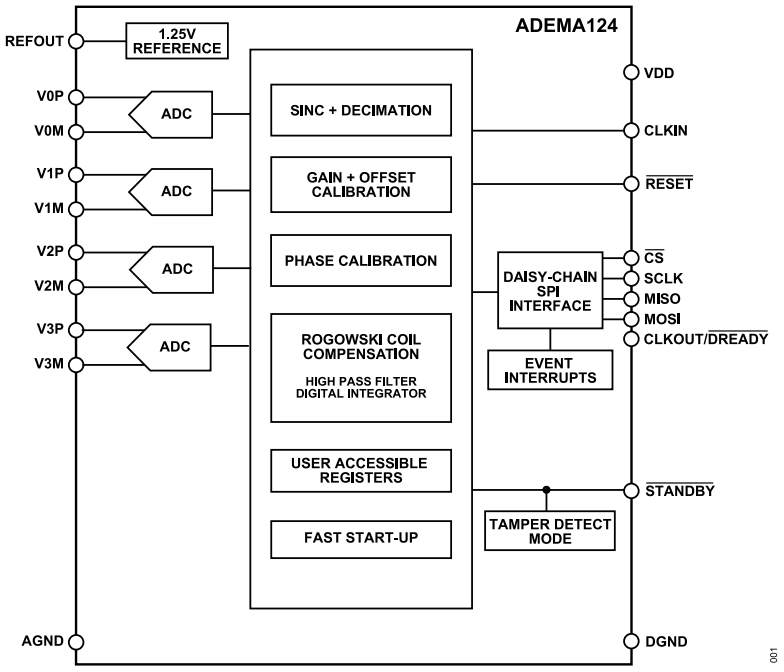


Figure 1. ADEMA124 Functional Block Diagram

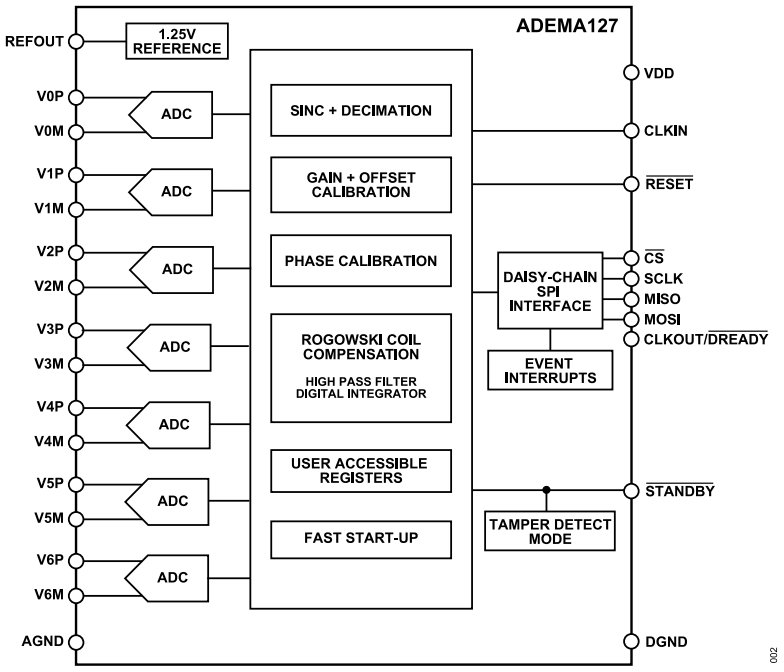


Figure 2. ADEMA127 Functional Block Diagram

SPECIFICATIONS

V_{DD} = 3.3V ± 10%, GND = 0V, on-chip reference, f_{XTALIN} = 16.384MHz, T_{MIN} to T_{MAX} = −40°C to +125°C , T_A = 25°C (typical). Output rate 4kHz. Values are based off full performance mode, ADC_POWER_MODE = 11, unless otherwise specified.

Table 2. Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Start-Up Inrush[1]		55		mA	Includes required decoupling capacitors
ADEMA124					
High Resolution		9.9	11.2	mA	All DSP filters enabled, f_{XTALIN} = 16.384MHz, f_{MOD} = 2.048MHz, f_s = 64kSPS
Default Configuration		4.2	4.9	mA	No DSP filters enabled, f_{XTALN} = 16.384MHz, f_{MOD} = 2.048MHz, f_s = 32kSPS
Low Power		1.8	2.3	mA	f_{XTALIN} = 2.048MHz, f_{MOD} = 256kHz, DSP off, f_s = 1kSPS, ADC_POWER_MODE = 0x0
Standby/Reset Mode		4		µW	
Tamper Detect Mode		11.25		mW	2 ADC channels active
ADEMA127					
High Resolution		11.5	13.1	mA	All DSP filters enabled, f_{XTALIN} = 16.384MHz, f_{MOD} = 2.048MHz, f_s = 64kSPS
Default Configuration		5.4	6.3	mA	DSP off, f_{XTALIN} = 16.384MHz, f_{MOD} = 2.048MHz, f_s = 32kSPS
Low Power		2.2	2.8	mA	f_{XTALIN} = 2.048MHz, f_{MOD} = 256kHz, DSP off, f_s = 1kSPS, ADC_POWER_MODE = 0x0
Standby/Reset Mode		4		µW	
Tamper Detect Mode		12.5		mW	4 ADC channels active
INTERNAL VOLTAGE REFERENCE[2]					
Voltage Reference		1.25		V	V_{REF}
Temperature Coefficient		5	15	ppm/°C	
EXTERNAL VOLTAGE REFERENCE					
Input Voltage (REFOUT)		1.25		V	V_{REF}
Input Impedance (REFOUT)		20		kΩ	
TEMPERATURE RANGE					
Operating Range	−40		+125	°C	
ANALOG INPUTS					
Differential Voltage Range					VxP − VxN
1x Gain	−1.2		+1.2	V	ADC_GAIN_CHx = 0
2x Gain	−0.6		+0.6	V	ADC_GAIN_CHx = 1
Common-Mode Range					(VxP + VxN)/2
ADC_CMI_CHx = 0	−0.1		+0.1	V	Input from CT or voltage divider
ADC_CMI_CHx = 1	0.9		1.2	V	Input from preamplifier with DC offset
Single-Ended Voltage Range					Pseudodifferential connection, voltage on the pin with respect to AGND (AGND = DGND)
1x Gain	−0.6		+0.6	V	Full-scale without clipping, ADC_CMI_CHx = 0, ADC_GAIN_CHx = 0
2x Gain	−0.3		+0.3	V	Full-scale without clipping, ADC_CMI_CHx = 0, ADC_GAIN_CHx = 1
Crosstalk					Aggressor channels at full-scale
1x Gain		−120		dB	
2x Gain		−120		dB	

SPECIFICATIONS

Table 2. Electrical Characteristics (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Differential Input Impedance					
1x Gain		150		kΩ	
2x Gain		75		kΩ	
ADC Offset Error					
1x Gain	−150	±20	150	µV	
2x Gain	−150	±45	150	µV	
ADC Offset Drift over Temperature			150	nV/°C	
ADC Gain Error	−2.0	±0.1	+2.0	%	Not including anti-aliasing filter
ADC Gain Drift over Temperature		5		ppm/°C	Without internal reference
ADC Gain Drift over Temperature		2	10	ppm/°C	With internal reference
ADC Transfer Function					1.25V internal reference
1x Gain		4,772,275		codes/V	
2x Gain		9,543,472		codes/V	
Tamper Detect Mode					
Total Unadjusted Error (TUE)	−2		+2	%FSR	
POWER-SUPPLY REJECTION RATIO (PSRR)/ COMMON-MODE REJECTION RATIO (CMRR)					
PSRR		120		dB	120mV$_{RMS}$ 50Hz contaminated VDD
CMRR					
1x Gain		110		dB	ADC_CMI_CHx = 0
1x Gain		95		dB	ADC_CMI_CHx = 1
2x Gain		110		dB	ADC_CMI_CHx = 0
ADC PERFORMANCE					f_{MOD} = 2.048MHz
32kSPS					
Signal-to-Noise Ratio (SNR)					
1x Gain		97		dBFS	Figure 25, Figure 27
2x Gain		97		dBFS	
Signal-to-Noise and Distortion Ratio (SINAD)					
1x Gain		95		dBFS	
2x Gain		87		dBFS	
Total Harmonic Distortion (THD)					
1x Gain		−98		dBFS	Figure 26, Figure 28
2x Gain		−88		dBFS	
Spurious-Free Dynamic Range (SFDR)					
1x Gain		100		dBFS	
2x Gain		89		dBFS	
4kSPS					
SNR					
1x Gain		102		dBFS	
2x Gain		101		dBFS	
SINAD					
1x Gain		98		dBFS	
2x Gain		90		dBFS	
THD					
1x Gain		-101		dBFS	
2x Gain		-90		dBFS	
SFDR					
1x Gain		104		dBFS	
2x Gain		92		dBFS	

SPECIFICATIONS

Table 2. Electrical Characteristics (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL OSCILLATOR					
Nominal Crystal Frequency	12.288		16.384	MHz	
Internal Capacitance on CLKIN, CLKOUT		3.5		pF	
Internal Feedback Resistance between CLKIN and CLKOUT		2.5		MΩ	
Transconductance (g_m)	6	8		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency	0.3	16.384	16.547	MHz	
XTALIN Duty Cycle	45		55	%	
With XTALOUT Routed to Other Devices	47.5		52.5	%	
XTALIN Pulse Width	28			ns	
CLOCK OUTPUT					
XTALIN to CLKOUT Propagation Delay		6		ns	CLKOUT_EN = 1
OUTPUT SAMPLE RATE					ADC_POWER_MODE = 0b11
ΣΔ Modulator Frequency (f_{MOD})			2.048	MHz	
DSP Frequency (f_{DSP})			64	kSPS	
LOGIC INPUTS - XTALIN Pin					
Input High Voltage, V_{INH}	1.2			V	
Input Low Voltage, V_{INL}			0.5	V	
LOGIC INPUTS - MOSI, SCLK, $\overline{CS}$, $\overline{STDBY}$, and $\overline{RESET}$ Pins					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN} (MOSI, SCLK, $\overline{CS}$)			8	µA	Integrated pull-up
Input Current, I_{IN} ($\overline{STDBY}$, and $\overline{RESET}$)			200	nA	
LOGIC OUTPUTS - CLKOUT/$\overline{DREADY}$, and MISO Pins					
Output High Voltage, V_{OH}	2.4				Source current (I_{SOURCE}) = 3.5mA
Output Low Voltage, V_{OL}			0.4		Sink current (I_{SINK}) = 3.5mA
LOW DROPOUT REGULATORS (LDOs)					
ALDOOUT		1.9		V	
VLDOOUT		1.9		V	
UNDERVOLTAGE LOCKOUT[1]					UVLO
Positive VDD Threshold			2.8	V	Rising supply voltage enable threshold, V_{UVLO+}
Negative VDD Threshold	2.2			V	Falling supply voltage lockout threshold, V_{UVLO-}
VDD Hysteresis		14		mV	UVLO hysteresis, V_{UVLO_HYS}

[1] Guaranteed by design. Not subject to production test.

[2] The reference temperature coefficient is trimmed in production test to optimize channel gain.

SPECIFICATIONS

BANDWIDTH AND PASS-BAND FLATNESS

All specifications typical figures for f_{XTALIN} = 16.384MHz and default DSP filter coefficients.

Table 3. Bandwidth and Pass-Band Flatness Characteristics

Parameter	Sinc Decimation Only	Sinc Compensation	Sinc Compensation and LPF	Sinc Compensation, LPF, and DSP Decimate-by-2	Comment
Output Bandwidth (−3dB)					ADC Output Bandwidth
64kSPS	17,000	21,000	14,500	N/A[1]	Figure 7
32kSPS	8,400	9,300	7,150	14,500	Figure 10
16kSPS	4,200	5,300	3,650	7,200	Figure 8
8kSPS	2,100	3,400	1,850	3,650	Figure 11
4kSPS	1,050	1,600	920	1,850	Figure 9
2kSPS	740	>f_S/2	465	920	Figure 12
1kSPS	420	410	250	465	Figure 13
500SPS	225	>f_S/2	125	230	Figure 15
250SPS	120	>f_S/2	58	115	Figure 14
Pass-Band Flatness (−0.1dB)					ADC Pass-Band Flatness
64kSPS	3,100	10,000	11,000	N/A[1]	Figure 7
32kSPS	1,600	4,800	4,600	11,000	Figure 10
16kSPS	800	2,900	2,950	4,600	Figure 8
8kSPS	400	1,800	1,700	3,300	Figure 11
4kSPS	200	850	850	1,650	Figure 9
2kSPS	150	700	385	760	Figure 12
1kSPS	94	180	180	420	Figure 13
500SPS	70	185	104	115	Figure 15
250SPS	55	80	31[2]	95	Figure 14

[1] N/A means not applicable. This is not a valid configuration.

[2] Referenced to 10Hz.

SPECIFICATIONS

TIMING CHARACTERISTICS

V_{DD} = 3.3V ± 10%, AGND = 0V, DGND = 0V, on-chip reference, f_{XTALIN} = 16.384MHz, and T_{MIN} to T_{MAX} = −40°C to +125°C, unless otherwise noted.

Table 4. SPI Interface Timing Parameters

Parameter[1]	Symbol	Min	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}	10		ns
SCLK Frequency[2]	f_{SCLK}	250	22,000	kHz
SCLK Duty Cycle		40	60	%
SCLK Low Pulse Width	t_{SL}	20		ns
SCLK High Pulse Width	t_{SH}	20		ns
Data Output Valid After $\overline{CS}$ Edge	t_{DAVFB}		20	ns
Subsequent Data Output Valid after SCLK Edge	t_{DAVSB}		20	ns
Data Input Setup Time before SCLK Edge	t_{DSU}	10		ns
Data Input Hold Time after SCLK Edge	t_{DHD}	10		ns
Data Output Fall Time	t_{DF}		10	ns
Data Output Rise Time	t_{DR}		10	ns
SCLK Rise Time	t_{SR}		5	ns
SCLK Fall Time	t_{SF}		5	ns
MISO Disable after $\overline{CS}$ Rising Edge	t_{DIS}		20	ns
$\overline{CS}$ High after SCLK Edge	t_{SFS}		10	ns
$\overline{CS}$ High Time between SPI Transactions[3]	t_{CH}	400		ns

1 Specifications guaranteed by design and characterization and not subject to production test.

2 f_{SCLK} must be <1.4 × f_{XTALIN}.

3 For f_{XTALIN} < 16.384MHz, t_{CH} must be >6/f_{XTALIN}. For more details, see the SPI Compatible Communication section.

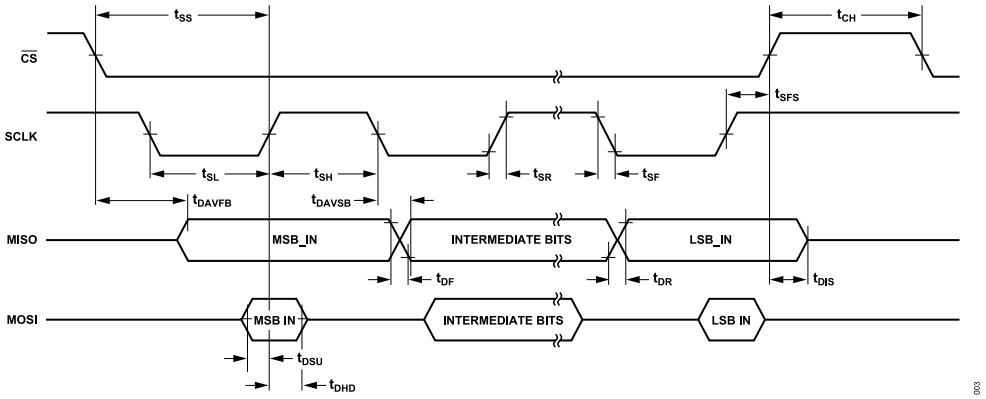


Figure 3. SPI Timing, SPI mode 3 (CPOL = 1 and CHPA = 1)

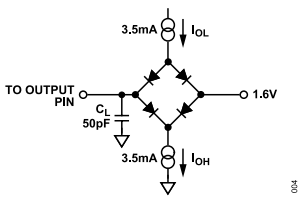


Figure 4. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 5. ADEMA124/ADEMA127 Absolute Maximum Ratings

Parameter	Rating
V_{DD} to DGND	−0.3V to +3.7V
Analog Input Voltage	
V_{0P} and V_{0M} to DGND	−1.7V to +2V
V_{1P} and V_{1M} to DGND	−1.7V to +2V
V_{2P} and V_{2M} to DGND	−1.7V to +2V
V_{3P} and V_{3M} to DGND	−1.7V to +2V
V_{4P} and V_{4M} to DGND	−1.7V to +2V
V_{5P} and V_{5M} to DGND	−1.7V to +2V
V_{6P} and V_{6M} to DGND	−1.7V to +2V
Digital Input Voltage	
MOSI, SCLK, $\overline{CS}$, XTALIN, $\overline{STDBY}$, $\overline{RESET}$ to DGND	−0.3V to V_{DD} + 0.3V
Digital Output Voltage	
CLKOUT/$\overline{DREADY}$, MISO, XTALOUT to DGND	−0.3V to V_{DD} + 0.3V
Reference Voltage	
REFOUT to DGND	−0.3V to +2.2V
Temperature	
Operating	−40°C to +125°C
Storage Range	−65°C to +150°C
Lead (Soldering, 10sec)[1]	260°C
Moisture Sensitivity Level	MSL 3

[1] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. For the latest revision of this standard, refer to the JEDEC.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure and θ_{JC} is the junction-to-case thermal resistance.

Table 6. Thermal Resistance

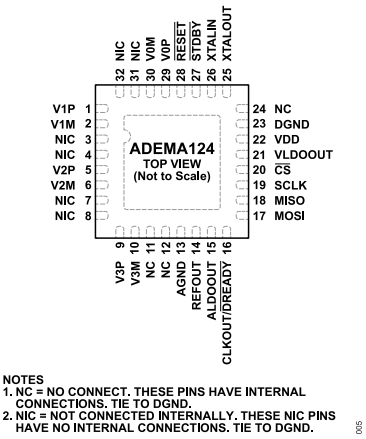
Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-32-20	31.73	25.60	°C/W

[1] Test condition 1: Thermal impedance simulated values are based upon use of 2S2P JEDEC PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

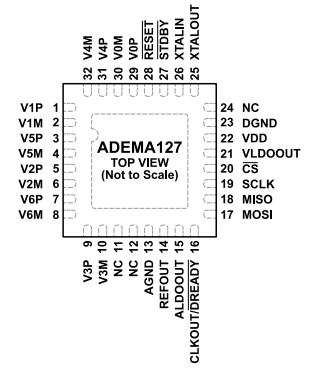
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THESE PINS HAVE INTERNAL CONNECTIONS. TIE TO DGND.
2. NIC = NOT CONNECTED INTERNALLY. THESE NIC PINS HAVE NO INTERNAL CONNECTIONS. TIE TO DGND.

005

Figure 5. ADEMA124 Pin Configuration



NOTES
1. NC = NO CONNECT. THESE PINS HAVE INTERNAL CONNECTIONS. TIE TO DGND.

006

Figure 6. ADEMA127 Pin Configuration

Table 7. Pin Function Descriptions

Pin Number			
ADEMA124	**ADEMA127**	**Name**	**Description**
1, 2	1, 2	V1P, V1M	Analog Inputs for ADC Channel 1.
3, 4, 7, 8, 31, 32		NIC	Not Connected Internally. These NIC pins have no internal connections. Connect to DGND.
	3, 4	V5P, V5M	Analog Inputs for ADC Channel 5.
5, 6	5, 6	V2P, V2M	Analog Inputs for ADC Channel 2.
	7, 8	V6P, V6M	Analog Inputs for ADC Channel 6.
9, 10	9, 10	V3P, V3M	Analog Inputs for ADC Channel 3.
11, 12	11, 12	NC	No Connect. These pins have internal connections. Connect to DGND.
13	13	AGND	Analog Ground Reference. Connect to DGND.
14	14	REFOUT	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25V. Decouple the REFOUT pin to DGND with a 0.1µF capacitor and 2.2µF capacitor. Place capacitors as close as possible. To use the internal voltage reference with external circuits, a buffer is required. An external voltage reference may be connected to this pin. For more details, see the Voltage Reference section.
15	15	ALDOOUT	1.9V Output of Analog Low Dropout (LDO) Regulator. Decouple this pin with a 0.22µF capacitor to DGND. Do not connect the external load circuitry to the ALDOOUT pin.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions (Continued)

Pin Number			
ADEMA124	ADEMA127	Name	Description
16	16	CLKOUT/$\overline{\text{DREADY}}$	Data Ready, Active Low ($\overline{\text{DREADY}}$). The $\overline{\text{DREADY}}$ pin generates an active-low signal to indicate the availability of new ADC samples and is synchronous to the ADC output frequency. Use this signal to synchronize the reading of ADC outputs. $\overline{\text{DREADY}}$ is the default functionality of the pin. The first rising edge after reset indicates that SPI port is ready for commands. A falling edge indicates ADC sample availability in CCM. See Figure 38. $\overline{\text{DREADY}}$ may be set as an interrupt pin when ADEMA124/ADEMA127 operates in TDM. For more details, see the Tamper Detect Mode section. Clock Output (CLKOUT). Pin function set by CLKOUT_EN bit. When CLKOUT functionality is selected, the ADEMA124/ADEMA127 generates a digital signal synchronous to the controller clock at the XTALIN pin. Use CLKOUT to provide a clock to other devices.
17	17	MOSI	Data Input for SPI Port.
18	18	MISO	Data Output for SPI Port.
19	19	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock.
20	20	$\overline{\text{CS}}$	Chip Select for SPI Port.
21	21	VLDOOUT	1.9V Output of Digital Low Dropout (LDO) Regulator. Decouple this pin with a 0.22µF capacitor to DGND. Do not connect the external load circuitry to the VLDOOUT pin.
22	22	VDD	Supply Voltage, 3.3V +/- 10%. Decouple this pin with a 0.1µF and 2.2µF capacitor to DGND.
23	23	DGND	Digital Ground Reference.
24	24	NC	No Connect. This pin has an internal connection. Connect to DGND.
25	25	XTALOUT	Crystal Output. Choose a crystal based on the transconductance (g_m) shown in Table 2. Connect a crystal across XTALIN and XTALOUT to provide a clock source for the ADEMA124/ADEMA127. The XTALOUT pin must float when unused.
26	26	XTALIN	Controller Clock Input. An external clock can be provided at this logic input, such as the CLKOUT signal provided by another device. Alternatively, a crystal can be connected across XTALIN and XTALOUT.
27	27	$\overline{\text{STDBY}}$	Active Low Standby Input. This pin requires an external pull-up and should be tied to VDD if unused. For more details, see the Standby Mode section.
28	28	$\overline{\text{RESET}}$	Active Low Reset Input. This pin requires an external pull-up and must be connected to VDD if unused.
29, 30	29, 30	V0P, V0M	Analog Inputs for ADC Channel 0.
	31, 32	V4P, V4M	Analog Inputs for ADC Channel 4.
		EPAD	Exposed Pad. The exposed pad must be connected to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

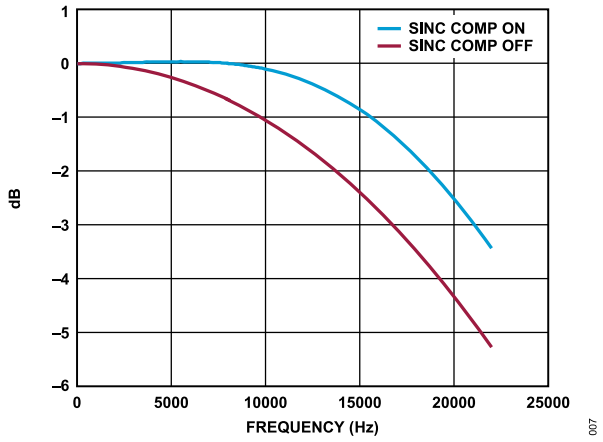


Figure 7. Bandwidth at 64kSPS

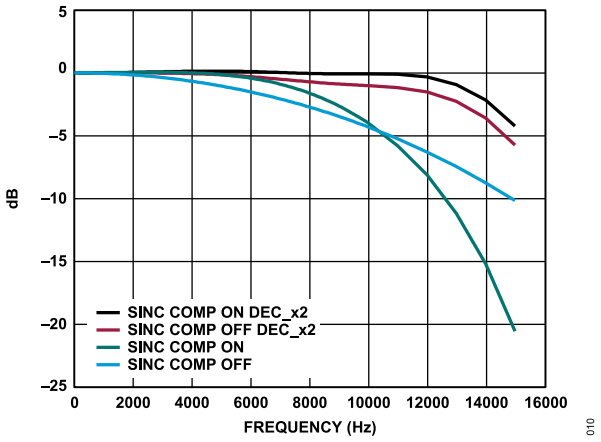


Figure 10. Bandwidth at 32kSPS

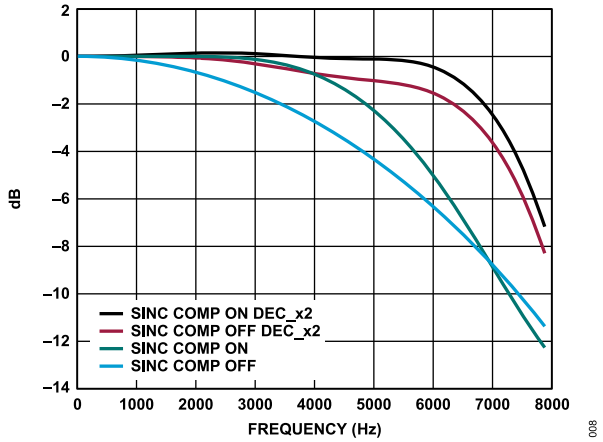


Figure 8. Bandwidth at 16kSPS

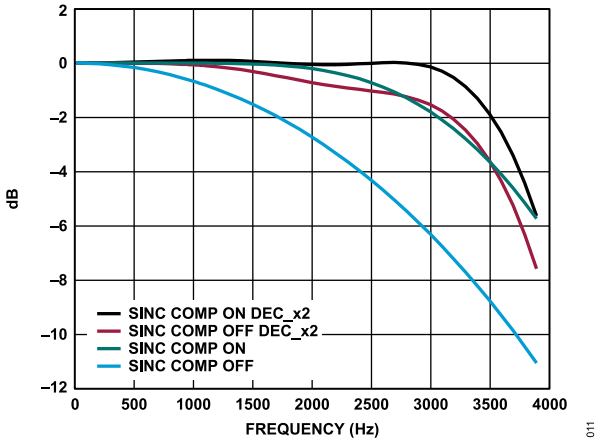


Figure 11. Bandwidth at 8kSPS

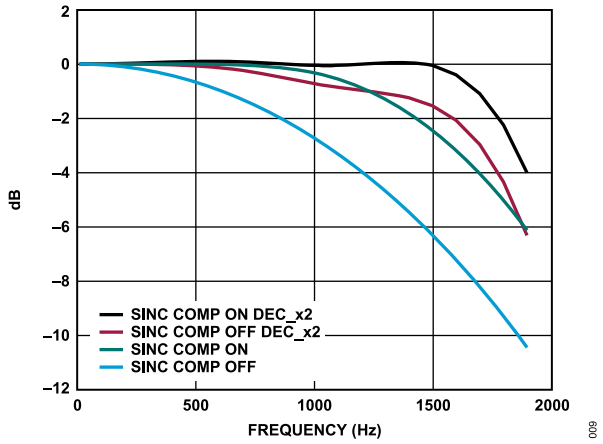


Figure 9. Bandwidth at 4kSPS

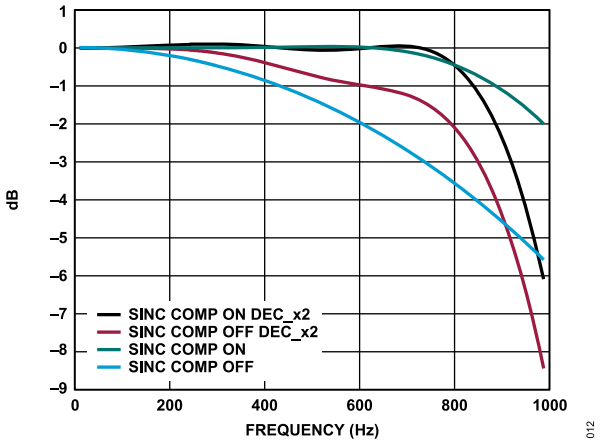


Figure 12. Bandwidth at 2kSPS

TYPICAL PERFORMANCE CHARACTERISTICS

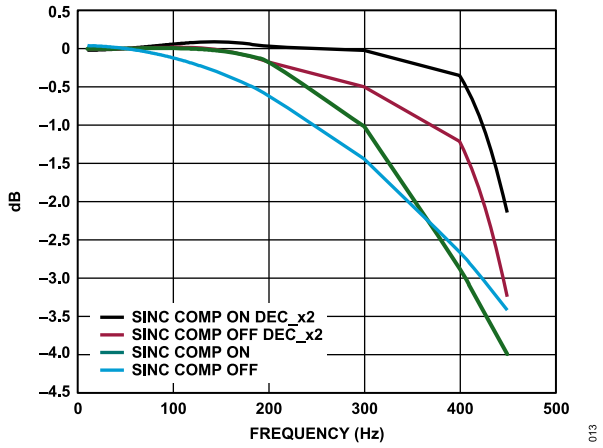


Figure 13. Bandwidth at 1kSPS

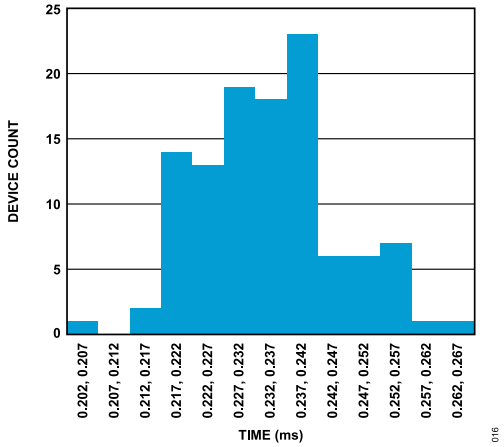


Figure 16. Fast Start-up Time Histogram

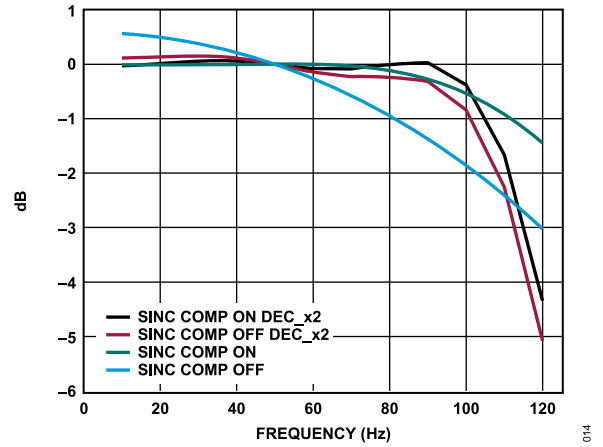


Figure 14. Bandwidth at 250kSPS

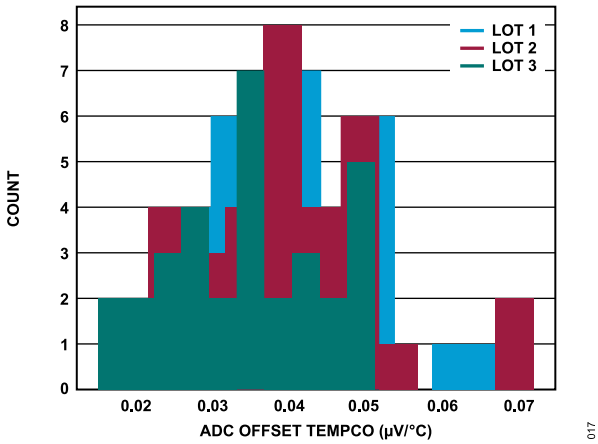


Figure 17. Input Offset Voltage vs. Temperature Histogram

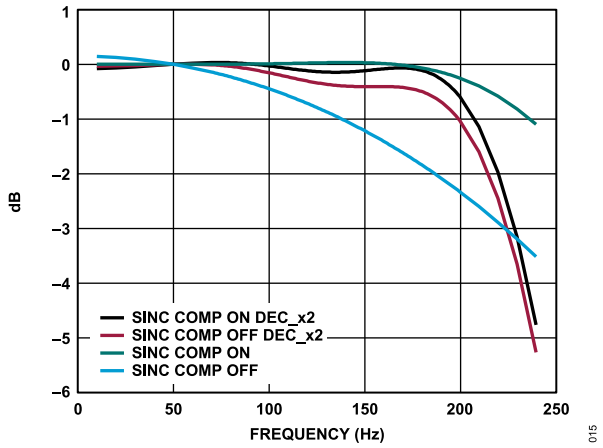


Figure 15. Bandwidth at 500kSPS

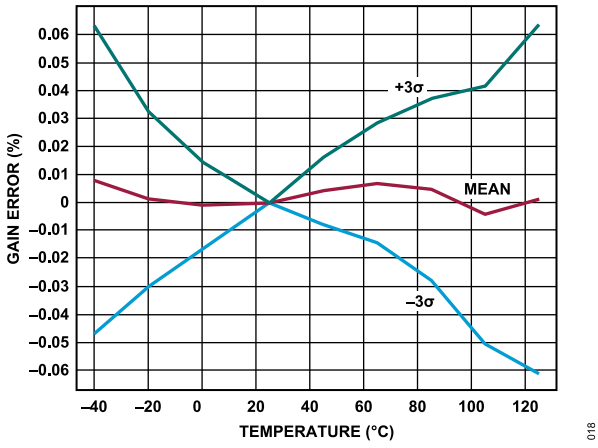


Figure 18. Gain Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

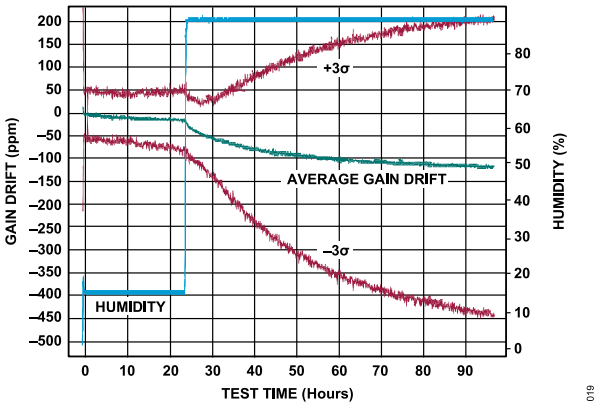


Figure 19. Gain Drift vs. Humidity, Mean and ±3σ

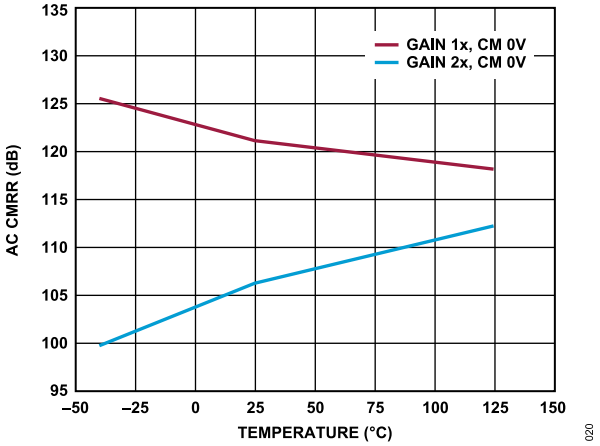


Figure 20. AC CMRR vs. VDD 50Hz, V_{DD} = 3.3V, Full Power Mode

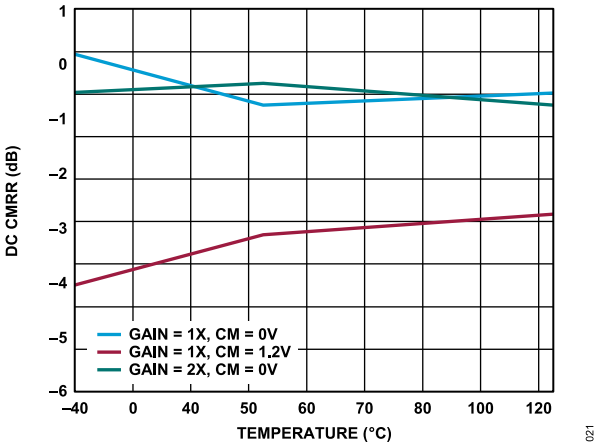


Figure 21. DC CMRR vs. Temperature, Full Power Mode

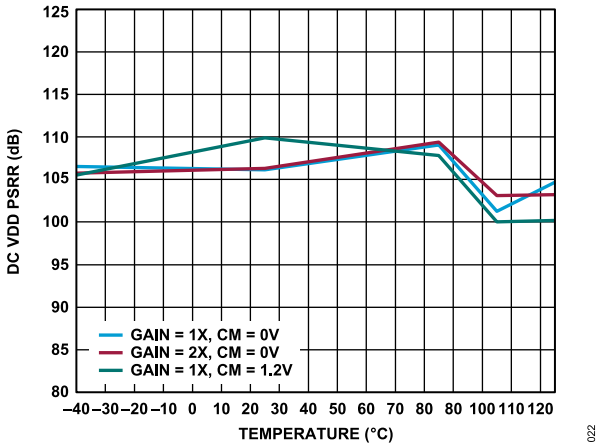


Figure 22. DC VDD PSRR vs. Temperature, Full Power Mode

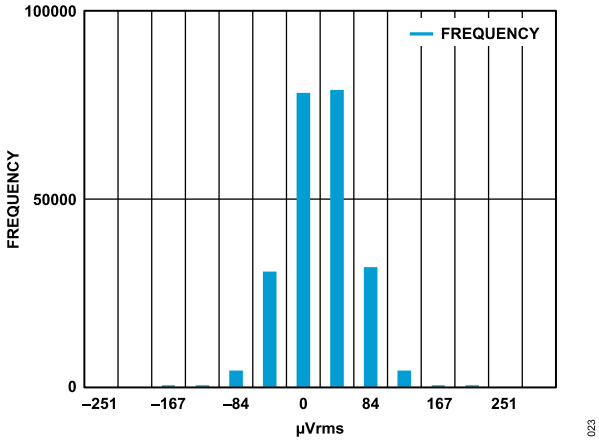


Figure 23. Single Device Noise Histogram at 32kSPS, Inputs Shorted, Gain = 1

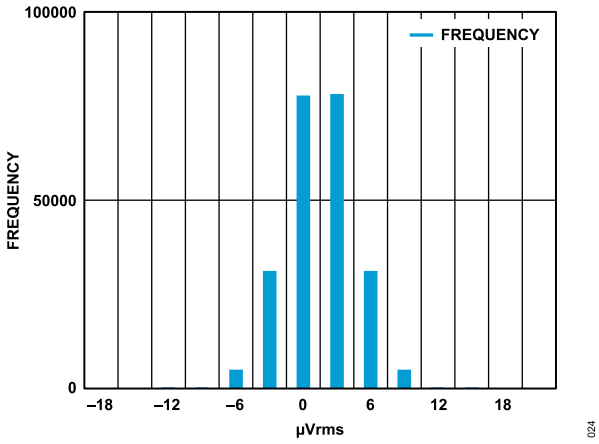


Figure 24. Single Device Noise Histogram at 4kSPS, ADC Inputs Shorted, Gain = 1

TYPICAL PERFORMANCE CHARACTERISTICS

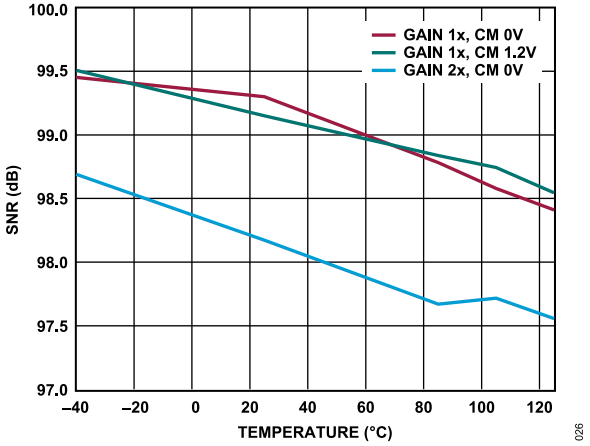


Figure 25. SNR vs. Temperature 32kSPS

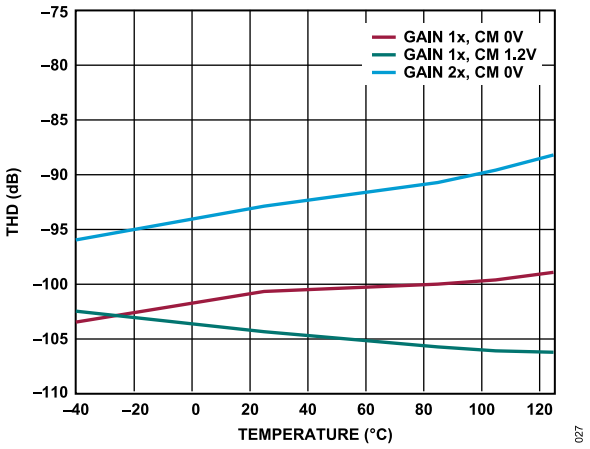


Figure 26. THD vs. Temperature 32kSPS

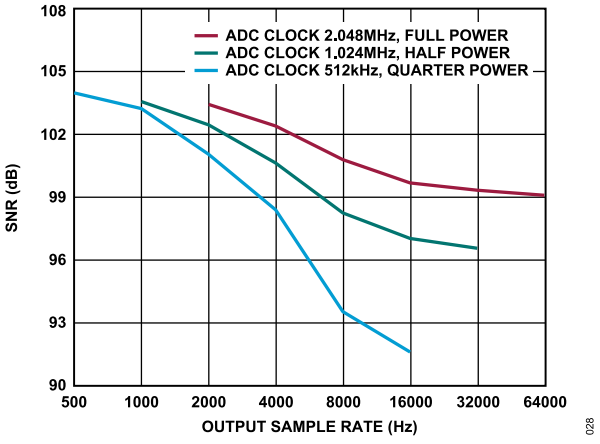


Figure 27. SNR vs. OSR Gain = 1

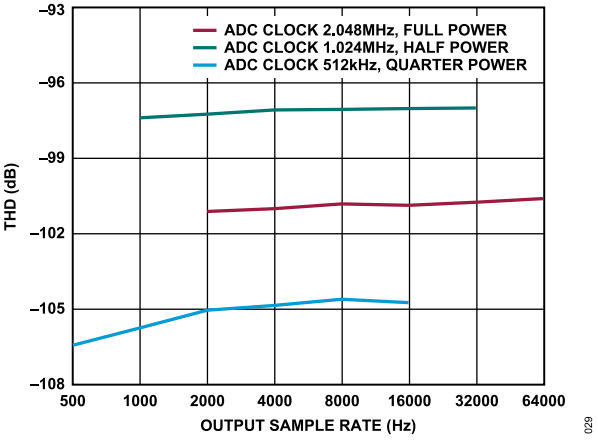


Figure 28. THD vs. OSR Gain = 1

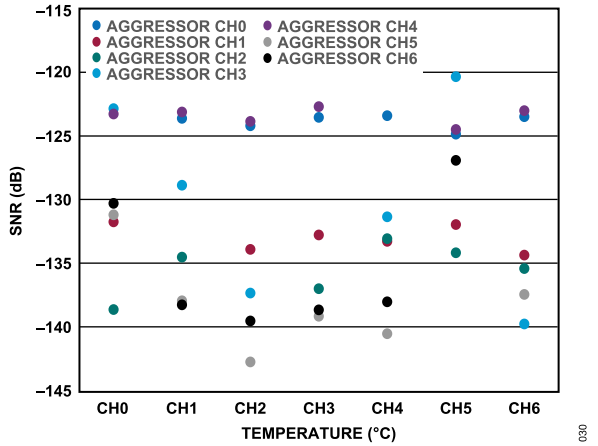


Figure 29. Crosstalk vs. Channel, Gain = 1x, Common-Mode = 0V

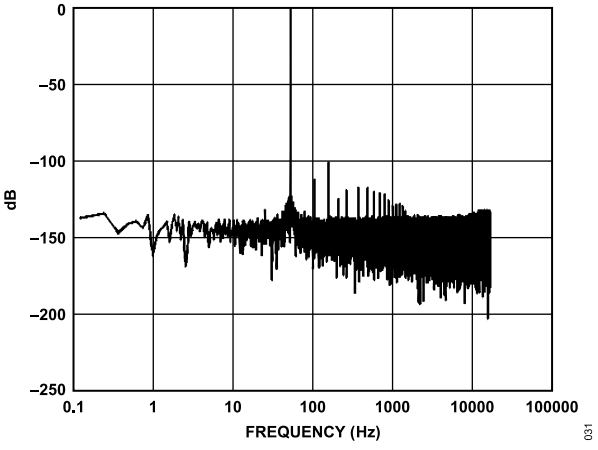


Figure 30. 50Hz Input, Fast Fourier Transform (FFT), 32kSPS Sinc3 Only

TYPICAL PERFORMANCE CHARACTERISTICS

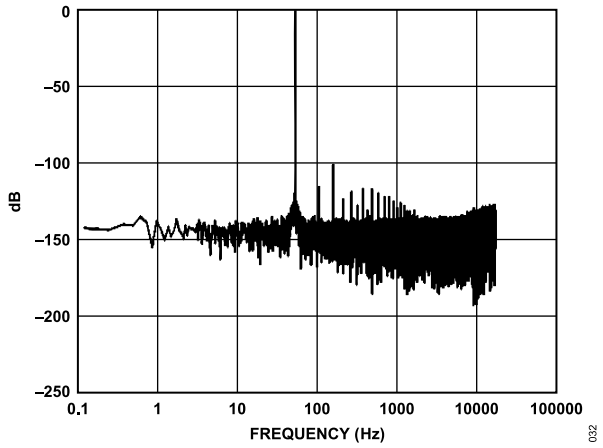


Figure 31. 50Hz Input, FFT, 32kSPS with DSP Sinc Compensation, Digital LPF and Decimate by 2 Enabled

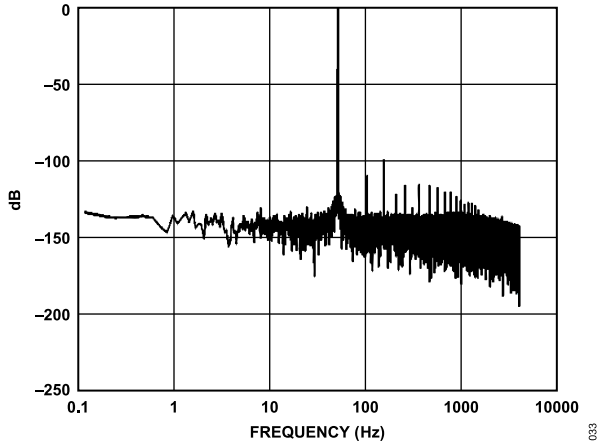


Figure 32. 50Hz Input, FFT, 8kSPS Sinc3 Only

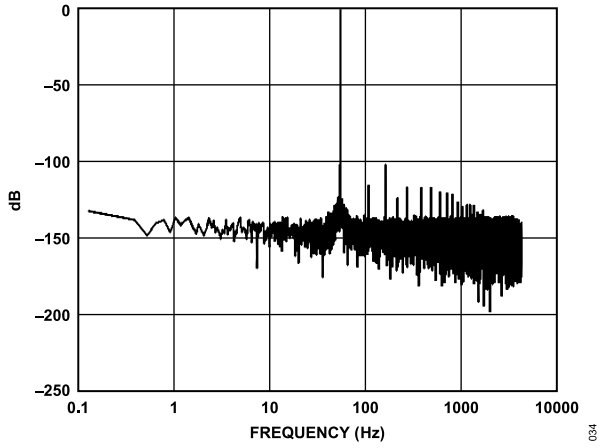


Figure 33. 50Hz Input, FFT, 8kSPS with DSP Sinc Compensation, Digital LPF and Decimate by 2 Enabled

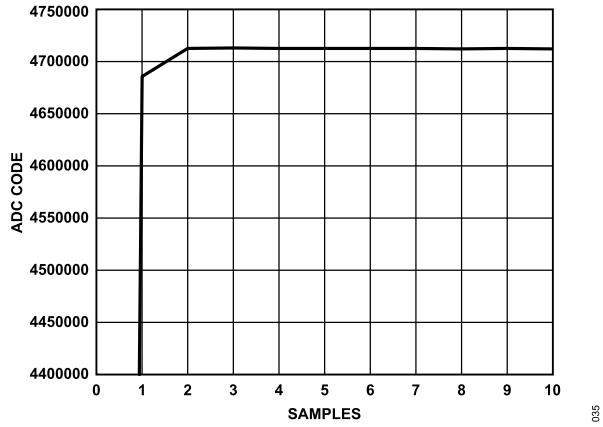


Figure 34. Sample Count Convergence to Specified Gain Error, Reset to CCM, f_{XTALIN} = 16.384MHz, Gain=1x, 1VDC input

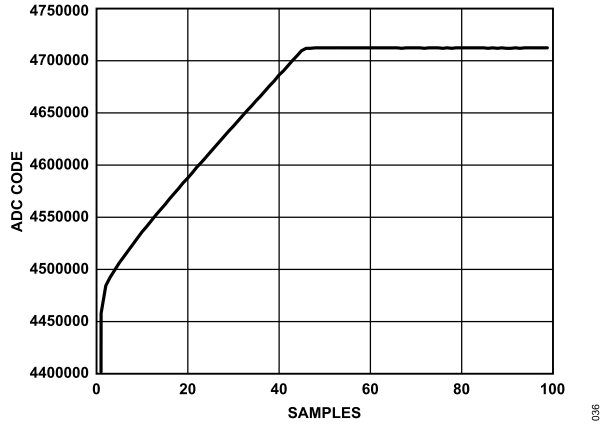


Figure 35. Sample Count Convergence to Specified Gain Error, TDM to CCM, f_{XTALIN} = 16.384MHz, Gain=1x, 1VDC input

TEST CIRCUIT

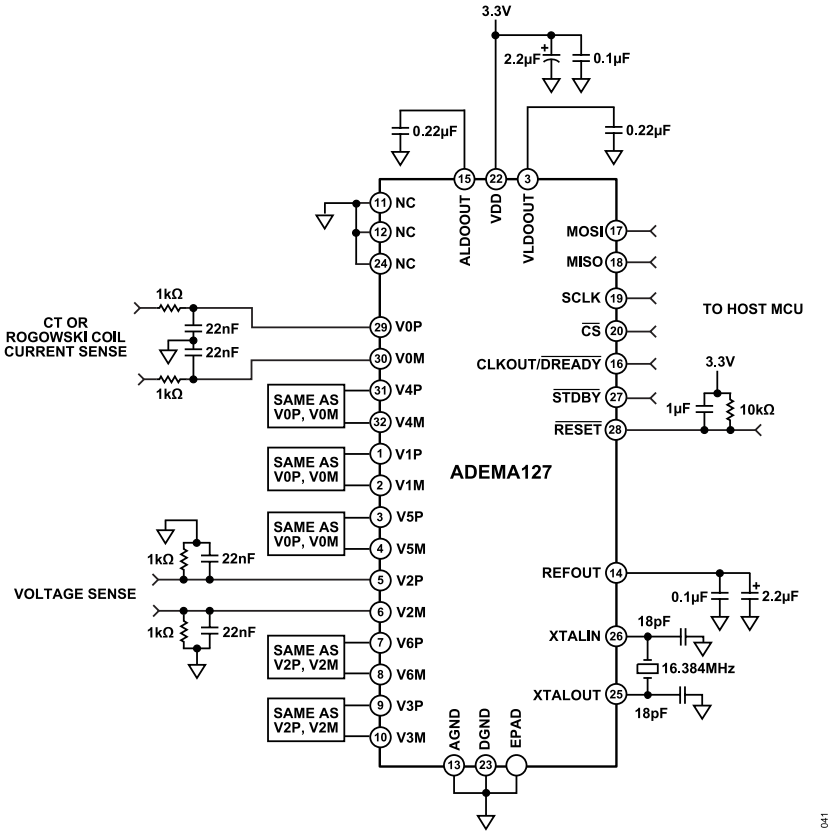


Figure 36. ADEMA127 Test Circuit, 3PH Voltage and Current

TERMINOLOGY

Crosstalk

Crosstalk is measured by grounding 1-channel and applying a full-scale 50Hz or 60Hz signal on all the other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 100sec. Crosstalk is expressed in decibels.

Differential Input Impedance (DC)

The differential input impedance represents the impedance between the pair VxP and VxM. It varies with the ADC_GAIN_CHx gain selection, as shown in Differential Input Impedance specification in Table 2.

ADC Offset Error

ADC offset error is the difference between the average measured ADC output code with both inputs connected to AGND and the ideal ADC output code of zero. ADC offset is expressed in µV.

ADC Offset Drift Over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +125°C. Calculate the offset drift over temperature as follows:

$$Drift = max\left(\left|\frac{Offset(-40°C) - Offset(+25°C)}{(-40°C - +25°C)}\right|, \left|\frac{Offset(+125°C) - Offset(+25°C)}{(+125°C - +25°C)}\right|\right) \quad (1)$$

Offset drift is expressed in nV/°C.

ADC Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.25V is used. The difference is expressed as a percentage of the ideal code. It represents the overall gain error of 1-channel.

ADC Gain Drift Over Temperature

This temperature coefficient includes the temperature variation of the ADC gain while using an external voltage reference of 1.25V. It represents the overall temperature coefficient of one current or voltage channel. With an external voltage reference of 1.25V in use, the ADC gain is measured at −40°C, +25°C, and +125°C. Then the temperature coefficient is computed as follows:

$$Drift = max\left(\left|\frac{Gain(-40°C) - Gain(+25°C)}{Gain(+25°C) \times (-40°C - +25°C)}\right|, \left|\frac{Gain(+125°C) - Gain(+25°C)}{Gain(+25°C) \times (+125°C - +25°C)}\right|\right) \quad (2)$$

Gain drift is measured in ppm/°C.

AC Power-Supply Rejection Ratio (PSRR)

AC PSRR quantifies the measurement error as a percentage of reading when the DC power supply is nominal (V_{NOM}) and modulated with AC, and the inputs are grounded. For the AC PSRR measurement, 20sec samples are captured with nominal supplies (3.3V, which is V_1) and a second set (V_2) is captured with an additional AC signal (120mV_{rms} at 50Hz) introduced onto the supplies. Then, the PSRR is expressed as PSRR = $20\log_{10}(V_2/V_1)$.

Signal-to-Noise Ratio (SNR)

SNR is calculated by inputting a 50Hz signal, and samples are acquired for 8sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3dB) are calculated. To determine the SNR, the signal at 50Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

Signal-to-Noise and Distortion Ratio (SINAD)

SINAD is calculated by inputting a 50Hz signal, and samples are acquired for 8sec. To determine the SINAD, the signal at 50Hz is compared to the sum of the power from all the other frequencies. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)

THD is calculated by inputting a 50Hz signal, and samples are acquired for over 8sec. To determine the THD, the amplitudes of the 50Hz harmonics up to the bandwidth are root sum squared. The value for THD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is calculated by inputting a 50Hz signal, and samples are acquired for over 8sec. To determine the SFDR, the amplitude of the largest signal that is not a harmonic of 50Hz is recorded. The value for SFDR is expressed in decibels.

ADC Pass-Band Flatness

The bandwidth to which the ADC output is within 0.1dB of a 50Hz reference signal input.

ADC Output Bandwidth

The ADC output bandwidth is the bandwidth within −3dB, resulting from the digital filtering in the sinc3 and enabled DSP features.

THEORY OF OPERATION

Accurate measurement, real-time monitoring, and comprehensive management of energy flow is required across the electrical power distribution networks. The ADEMA124 and ADEMA127 are 4- and 7-channel simultaneously sampling ADCs designed with features specifically for energy metering. All ADC channels have fully-differential inputs, identical dynamic range, programmable gain, and an independent 24-bit sigma delta ADC. Each ADC channel of the ADEMA124/ADEMA127 can directly support shunts, current transformers (CTs), and with the on-board digital integrators and HPFs, Rogowski sensors.

The ADEMA124/ADEMA127 ADCs are flexible and scalable components in energy metrology systems. The daisy-chain communication interface simplifies system architecture and allows a microcontroller to service a series of ADEMA124/ADEMA127 as though they are a single device. Synchronization of the multiple ADCs is simplified to a SPI write to the SYNC_SNAP register of each ADC followed by a simultaneous assertion of the $\overline{CS}$ pins. The integrated gain, phase, and offset compensation along with other DSP features reduce processing resources of the host microcontroller and make processed ADC waveform samples immediately available to the system.

The DSP decimate-by-2 enables higher bandwidth for reliable measurement of harmonics and, thus, superior power quality analysis for renewable energy resources, more efficient power delivery across the grid, and improved longevity of devices.

GAIN AND OFFSET CORRECTION

Gain and offset correction is commonly required in metrology systems. The ADEMA124/ADEMA127 provide gain and offset calibration bit fields for each ADC channel, which reduces the required processing burden of the host microcontroller.

QUICK START GUIDE

Upon providing the ADEMA124/ADEMA127 a 3.3V power supply and clock, the ADC immediately begins to produce samples per default configurations as shown in Figure 38. All communication with the ADEMA124/ADEMA127 is via SPI port. For more details, see the Fast Start-Up section.

The typical use case provides a valid supply and clock, configures the datapath, write locks the configuration, and then harvests ADC waveform data in response to $\overline{DREADY}$ pin low transitions. It is most efficient to retrieve ADC waveform samples with long format SPI operations. The CRC checksums, STATUS0 and STATUS1 registers are returned alongside ADC waveform data from all channels with long format SPI responses. The recommended repeated command is a long format SPI read of the STATUS2 register so all ADEMA124/ADEMA127 status information is continually returned to the microcontroller.

The DATAPATH_CONFIG_LOCK and DSP_MEM_ACCESS_REQ have multiple functions but both bits are SPI write locks that protect their spaces by default. The functions of these bits is fully described in Configuration Lock and Access Bits section. The ADEMA124/ADEMA127 has an 8-bit register called SCRATCH that is not write protected and can be used for test SPI writes and reads. There are debug features to verify the 24-bit ADC waveform samples are being reliably retrieved by the system discussed in Communication Debug Features section.

All values in DSP RAM are overwritten when any configuration of the MMR occurs. Configuration of the ADEMA124/ADEMA127 requires MMR addresses to be configured before DSP RAM addresses. All default DSP filter coefficients loaded into DSP RAM are based on the typical 16.384MHz f_{XTALIN}. The DSP coefficients can be modified.

Writing the Lock Key to the WR_LOCK prevents unintended SPI writes to the ADEMA124/ADEMA127 configuration registers. The CRC_CHG bits in STATUS0 is set high if a change in configurations has occurred and can be monitored by the microcontroller.

APPLICATIONS INFORMATION

START-UP SEQUENCE AND TIMING

Fast Start-Up

The ADEMA124/ADEMA127 immediately start sampling and producing waveform data once a valid power supply is present. The ADC must be provided with a valid clock input signal or have an external crystal present and neither the $\overline{\text{RESET}}$ pin nor $\overline{\text{STDBY}}$ pin asserted.

Start-up is shown in Figure 37. Fast start-up time is defined as the time between VDD supply reaching the minimum valid supply level and first data samples being available. The first low-to-high transition of the $\overline{\text{DREADY}}$ pin indicates the SPI port is available for communication. The first high-to-low transition of the $\overline{\text{DREADY}}$ pin indicates the first ADC sample set is available. The first SPI read returns 0x00 for all ADC waveform data. If the first ADC sample set is required, read the SPI port on the first $\overline{\text{DREADY}}$ pin rising edge. The first set of ADC samples is then available to be read on the first $\overline{\text{DREADY}}$ pin high-to-low transition. The first two ADC wavefrom data sets pass through the lower latency sinc1 filter with a decimation factor of 64.

The ADEMA124/ADEMA127 provide valid ADC samples in less than 0.5ms when provided an external clock from the time that VDD is at 90% ($t_{START-UP}$). Valid ADC samples are generated with 15ms when the ADEMA124/ADEMA127 must first start the crystal oscillator circuit to generate a clock from an external crystal.

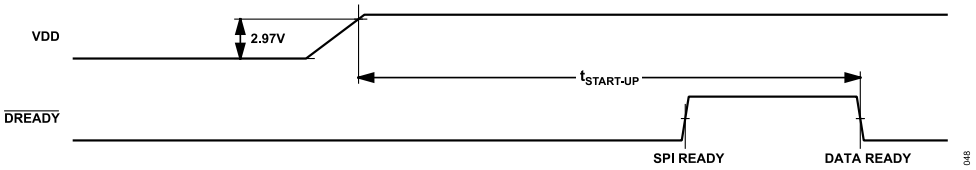


Figure 37. Fast Start-Up Timing

APPLICATIONS INFORMATION

MODES OF OPERATION

The ADEMA124/ADEMA127 have three modes of operation; continuous conversion mode (CCM), standby mode, and tamper detect mode (TDM). CCM is the default mode that the ADEMA124/ADEMA127 enter after power-up or reset. SPI communication is active and ADC samples are available at the configured sampling rate in CCM. For more details on the CCM, see the Continuous Conversion Mode section.

Standby mode can be entered from CCM by setting the $\overline{\text{STDBY}}$ pin low. In this mode, SPI communication is not accessible and the power consumption of the ADEMA124/ADEMA127 is greatly reduced. For more details on the standby mode, see the Standby Mode section.

TDM can be entered only from standby mode. It provides a mechanism to check for the presence of a signal above a configurable threshold without requiring full power-up into CCM. For more details on the TDM, see the Tamper Detect Mode section.

$\overline{\text{DREADY}}$ pin modes of operation are shown in Figure 38 and Figure 39, respectively. If a resistor is required on the $\overline{\text{DREADY}}$ pin trace for EMC in noisy environments, install a pull-down resistor. Do not install a pull-up resistor on the $\overline{\text{DREADY}}$ pin.

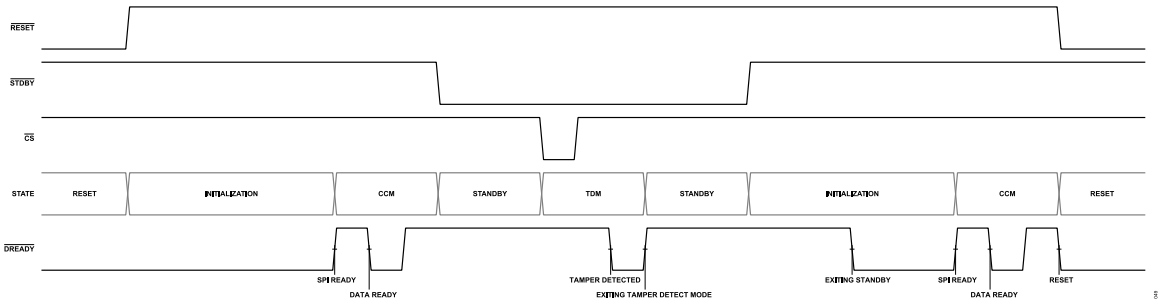


Figure 38. Default $\overline{\text{DREADY}}$ Pin Behavior (TDM_DREADYB_EN = 1)

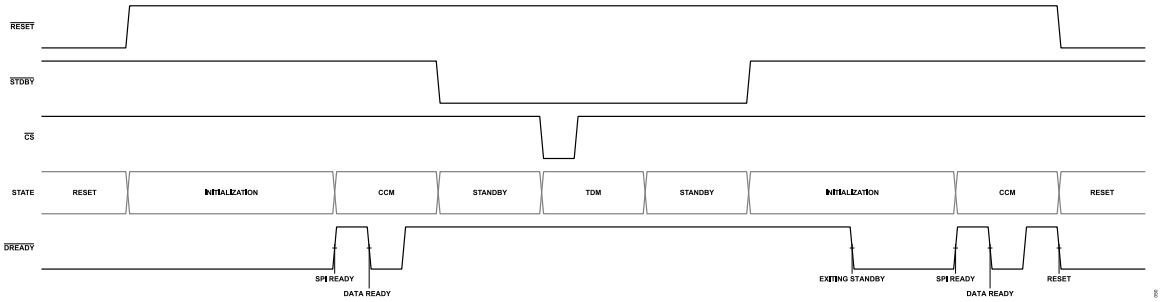


Figure 39. $\overline{\text{DREADY}}$ Pin Behavior (TDM_DREADYB_EN = 0)

APPLICATIONS INFORMATION

Continuous Conversion Mode

CCM is the default operational mode of the ADEMA124/ADEMA127 when the VDD supply is valid, and neither $\overline{\text{RESET}}$ nor $\overline{\text{STDBY}}$ pins are asserted.

The SPI port is only active in CCM. The ADEMA124/ADEMA127 indicate entry into CCM and availability of the SPI port with the first rising edge on the $\overline{\text{DREADY}}$ pin, as shown in Figure 38 and Figure 39.

Standby Mode

Standby mode is a low-power idle state. The ADEMA124/ADEMA127 enter standby mode from CCM by setting the $\overline{\text{STDBY}}$ pin low. Set the $\overline{\text{STDBY}}$ pin high to exit standby mode.

While the ADEMA124/ADEMA127 are in standby mode, the SPI port is not accessible. All settings in the registers shown in Table 27 are retained when the ADEMA124/ADEMA127 enter and exit standby mode. The registers shown in Table 28 are reset to default values and require reconfiguration upon exit of standby mode.

Tamper Detect Mode

TDM enables detection of load current while a system operates under a significantly reduced power budget. The ADC channels set active in the ADC_PD register operate as configurable digital inputs while the ADEMA124/ADEMA127 are in TDM. When the configured conditions are met, the TAMPER_DETECTED bit field is set and, optionally, an interrupt can be sent to the system by the $\overline{\text{DREADY}}$ pin.

The duration of the TDM cycle is set by the TDM_LEN bit field. The ADEMA124/ADEMA127 sample at a fixed 7.227kS/s rate in TDM. The sample clock is generated internally during a TDM cycle. Any crystal or external clock signal are ignored. Do not use an external voltage reference in TDM.

The input threshold is set with the 12-bit TDM_THRSH bit field. The TDM_THRSH value is left shifted 11 bits and compared with the absolute value of the 24-bit ADC data value. The TDM_THRSH setting is shared by all channels and sets an absolute detection level. Samples above the input threshold are counted and continuously compared to the TDM_NUM setting. Each channel maintains a unique count of samples above the input threshold and sets an internal flag if the TDM_NUM setting is met. These flags are routed to either a logical AND or OR gate as set by the TDM_ALLCH bit to trigger a tamper detection.

A tamper detection is always written to the TAMPER_DETECTED bit. This setting persists until the bit is cleared by SPI write or the ADEMA124/ADEMA127 is reset. The TDM_DREADYB_EN bit sets the ADEMA124/ADEMA127 to simultaneously notify the system by setting the $\overline{\text{DREADY}}$ pin low, as shown in Figure 40. The $\overline{\text{DREADY}}$ pin remains low for a minimum of 6µs if tamper detection is triggered on the last sample and transitions high at end of the TDM cycle.

The ADEMA124/ADEMA127 only enter a TDM cycle from standby mode. Configuration of TDM must be completed before the ADEMA124/ADEMA127 enter standby mode. With the $\overline{\text{STDBY}}$ pin held low, assert the $\overline{\text{CS}}$ pin for a minimum of 10µs to trigger entry into a TDM cycle.

If both $\overline{\text{CS}}$ and $\overline{\text{STDBY}}$ pin remain low when the ADEMA124/ADEMA127 exit a TDM cycle, a new TDM cycle begins. New TDM cycles can also be started with a new $\overline{\text{CS}}$ assertion while in standby mode. A full TDM cycle runs to completion regardless of the $\overline{\text{STDBY}}$ pin state, the $\overline{\text{CS}}$ pin state, or if a tamper is detected.

Settings for ADC_PD, TDM_LEN, TDM_THRSH, TDM_NUM, and TDM_ALLCH bit fields are shown in Table 29.

The external REFOUT capacitor is discharged in TDM. Figure 35 shows the effects of the charging REFOUT capacitor and convergence to specified gain accuracy when the ADEMA124/ADEMA127 enter CCM immediately after exiting a TDM cycle.

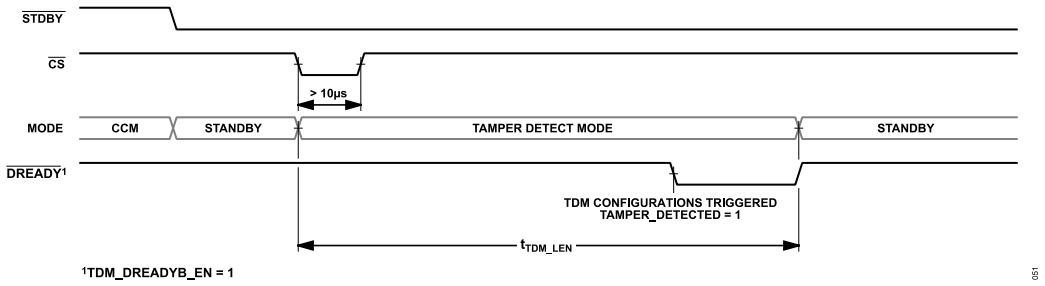


Figure 40. TDM Entry and Event Detection

APPLICATIONS INFORMATION

Software Reset

The SWRST register manages the software reset functionality. If this register is set to software reset command value of 0xD6, the ADEMA124/ADEMA127 enter the software reset state. In this state, all registers are reset to default values. When the software reset ends, the SWRST register clears automatically, and RESET_DONE bit in the STATUS0 register is set. The SWRST register is protected from writes when the lock key is set in the WR_LOCK register; First unlock the registers before initiating a software reset. For more details on WR_LOCK, see the Full Configuration Lock section.

Do not write SPI commands before the SPI port is indicated as ready by the $\overline{\text{DREADY}}$ pin, SPI ready is shown in Figure 38. Any attempt to initiate a subsequent SPI command during software reset processing results in a failed SPI transaction. The ADEMA124/ADEMA127 have internal control blocks, regulators, and references not affected by software reset.

After software reset, one of the procedures shown in the Start-Up Sequence and Timing section must be followed to initialize the ADEMA124/ADEMA127. On reset, the default retained MMR and MMR values are restored. The values in DSP RAM are reinitialized to default values when a DSP filter is enabled and DATAPATH_CONFIG_LOCK bit cycled.

Hardware Reset

The ADEMA124/ADEMA127 enter the reset state when the $\overline{\text{RESET}}$ pin is low. All retained MMR and MMR registers are initialized to the default values when the device exits the reset state. DSP RAM values are initialized when a DSP filter is enabled.

APPLICATIONS INFORMATION

SPI COMPATIBLE COMMUNICATION

The SPI port consists of the following pins; SCLK, MOSI, MISO, $\overline{CS}$ and typically $\overline{DREADY}$ to call for ADC waveform data retrieval. All configuration and ADC waveform data retrieval operations are performed via SPI port.

The ADEMA124/ADEMA127 operate only in SPI mode 3, where CPOL = 1 and CPHA = 1. All data transfer operations synchronize to the serial clock signal routed to the SCLK pin. The maximum and minimum serial clock frequencies supported by the SPI port are specified by the SCLK frequency, f_{SCLK}, parameter shown in Table 4.

The integrity of data transmission to and from the SPI port of the ADEMA124/ADEMA127 is protected by bidirectional CRC. Commands sent to the ADEMA124/ADEMA127 are always 32 bits and contain an 8-bit CRC. Commands do not execute unless the received SPI command CRC matches the computed value for the command. The command response, which is returned the next SPI frame, ends with a 16-bit CRC computed from the response. It also contains an alert if the 8-bit CRC does not match. The communication error detection scheme is enabled by default but can be disabled and ignored. For more details on the CRC calculation and usage, see the CRC Protection section.

The flexible interface allows devices to connect to the microcontroller as shown in the Individually Addressed section or in daisy-chain, as shown in the Daisy-Chain section. The daisy-chain configuration allows multiple devices to be serviced as a single device by the microcontroller. There is no configuration required to indicate whether each ADEMA124/ADEMA127 device is being addressed individually or as a member of a daisy-chain.

The $\overline{DREADY}$ pin enables efficient SPI communications between the ADEMA124/ADEMA127 and microcontroller. At power-up, the first rising edge of the $\overline{DREADY}$ pin indicates that SPI port is ready to receive SPI commands. Thereafter, the $\overline{DREADY}$ falling edge marks the availability of a new ADC sample set to be retrieved by the microcontroller. $\overline{DREADY}$ stays low for 15ns when operating from the typical 16.384MHz clock frequency. Default $\overline{DREADY}$ pin operation is shown in Figure 39.

When the $\overline{CS}$ pin transitions high-to-low, the SPI response packet including ADC waveform data is latched into a buffer to be shifted out with SCLK. ADC waveform data without a transfer initiated before the next $\overline{DREADY}$ pin high-to-low transition is overwritten.

Command and Response

The ADEMA124/ADEMA127 communication scheme enables full-duplex communication. As shown in Figure 41, a new command is shifted into the ADEMA124/ADEMA127 device while a response to the previous command is being shifted out. The most significant bit of the SPI frame is received first by the ADEMA124/ADEMA127 MOSI pin.

SPI commands are executed once the $\overline{CS}$ pin transitions from low-to-high. The SPI command bit field is interpreted as the last 32 bits received before the $\overline{CS}$ pin transition. The component bit fields of the SPI command are shown in Figure 42 and detailed in Table 8.

The SPI command response is delivered in the directly subsequent SPI frame. The SPI command echo bit field makes up the first byte of every response. This 8-bit command echo can be used to confirm that the previous command is interpreted correctly. The component bit fields of the SPI command echo are shown in Figure 43 and detailed in Table 9.

The remainder of the command response varies based on the specific command issued to the ADEMA124/ADEMA127. Command responses are summarized in Table 10. All response frames end with a 16-bit CRC computed from the response frame.

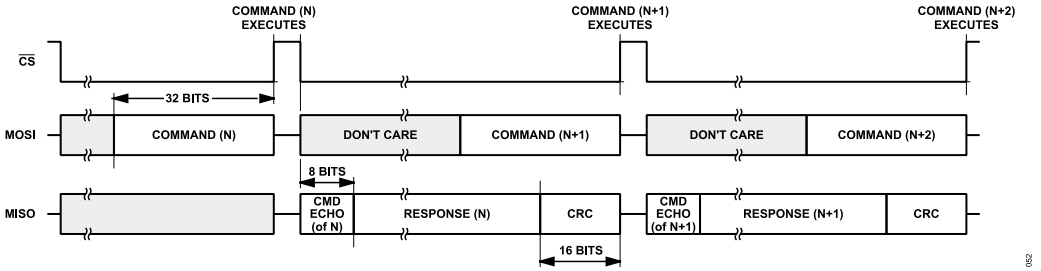


Figure 41. Full-Duplex Communication with a Single Device

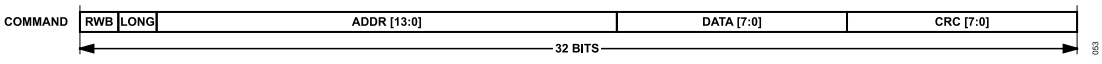


Figure 42. SPI Command Bit Field

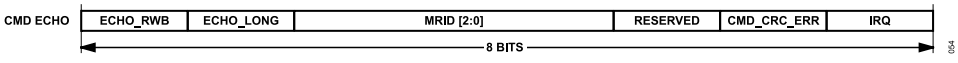


Figure 43. SPI Command Echo Bit Field

APPLICATIONS INFORMATION

Table 8. SPI Command Bit Fields

Bit Field Location	Bit Field Name	Description
31	RWB	Set this bit to 1 if an SPI read operation is to be executed. Clear this bit to 0 if an SPI write operation is to be executed.
30	LONG	Set this bit to 1 for a long frame structure. Clear this bit to 0 for a short frame structure. Short frames are not supported for daisy-chain connected devices.
[29:16]	ADDR[13:0]	14-bit address of the register to be read or written.
[15:8]	DATA[7:0]	Data payload if a write operation is executed.
[7:0]	CRC[7:0]	Command frame contents protect with 8-bit CRC. For more details, see the SPI Command CRC section.

Table 9. SPI Command Echo Bit Fields

Bit Field Location	Bit Field Name	Description
7	ECHO_RWB	Echo of last issued command. 1 for SPI read operation. 0 for SPI write operation.
6	ECHO_LONG	Echo of requested command format. 1 for a long format. 0 for short format.
[5:3]	MRID[2:0]	Indicates which memory region the requested address belongs to: 000 for Register Map (0x0000 to 0x00FF). 001 for DSP RAM (0x0400 to 0x07FF). 010 Reserved. 011 Reserved. 100 Reserved. 101 Reserved. 111 Reserved.
2	RSRVD	Reserved. This bit is set to 0.
1	CMD_CRC_ERR	CRC check on the corresponding Command Frame. 0 indicates the Command Frame CRC check passed. 1 indicates the Command Frame CRC check failed. For more details, see the SPI Command Response CRC section.
0	IRQ	Command response interrupt bit. 0 indicates that no interrupt is raised. 1 indicates that an unmaskable or configured interrupt has been raised. For more details, see the Status Registers and IRQ section.

Table 10. Response Frame Types

Response Type	Description
Default Response	Transmitted between PoR release and MCLK on.
Long Read Response	The 24-bit waveform sample for all ADC channels on the device plus a readback value for registers at address and address+1. For more details, see the Long Format Operation section.
Long Write Response	The 24-bit waveform sample for all ADC channels on the device plus an echo of the write address and a readback value for the register at that address. For more details, see the Long Format Operation section.
Short Read Response	A readback value for registers at address and address+1. For more details, see the Short Format Operation section.
Short Read of Channel Data	A 24-bit waveform sample from the selected channel. For more details, see the Short Format Operation section.
Short Write Response	Echo of the write address and a readback value for that register. For more details, see the Short Format Operation section.
Command Error Response	Transmitted if the command frame was found to be invalid. For more details, see the SPI Command Error Response Frame section.

APPLICATIONS INFORMATION

Long Format Operation

All long format responses include the 24-bit waveform data registers from all ADC channels and the contents of the STATUS0 and STATUS1 registers. ADC waveform data is in 24-bit two's complement representation. Bytes from the ADC waveform registers are transmitted Vx_WAV_LO, Vx_WAV_MD, Vx_WAV_HI in little-endian format. The long format read of STATUS2 is the recommended SPI transaction for typical CCM operation since all ADC data and status information is returned.

The ADEMA127 has a 256 bits long format response. The ADEMA124 long format response is 160 bits. The ADEMA124/ADEMA127 devices connected in daisy-chain must communicate only with long format operations.

The structure of the ADEMA127 long read response frame is shown in Figure 45 below. The structure of the ADEMA127 long write response frame is shown in Figure 46.

The ADEMA124 long format command and response is shown in Figure 47. The structure of the ADEMA124 long read response frame is shown in Figure 48. The structure of the ADEMA124 long write response frame is shown in Figure 49.

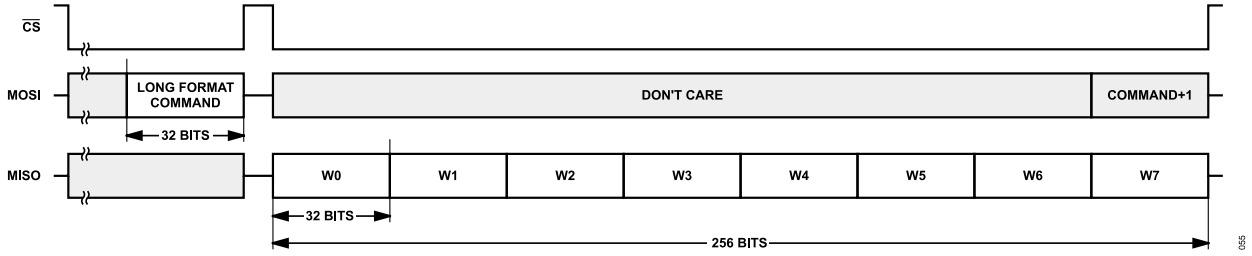


Figure 44. ADEMA127 Long Format

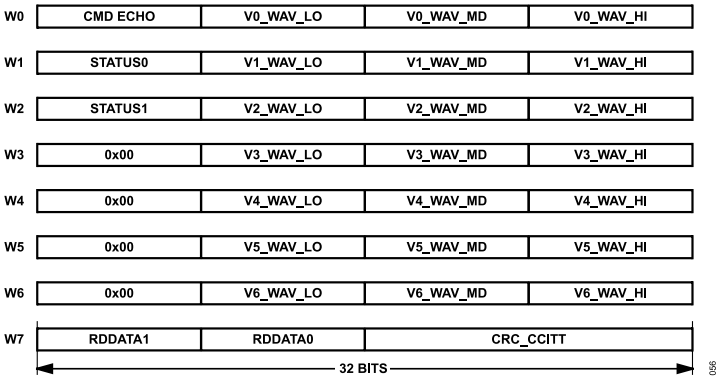


Figure 45. ADEMA127 Long Format Read Response Packet

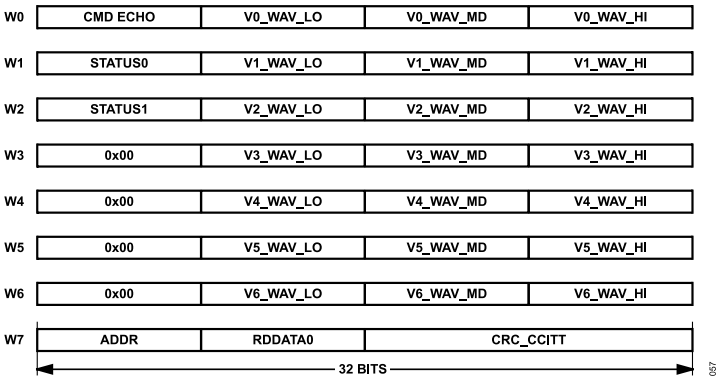


Figure 46. ADEMA127 Long Format Write Response Packet

APPLICATIONS INFORMATION

Table 11. ADEMA127 Long Format Response Bit Fields

Bit Field Location	Long Read Bit Field Name	Long Write Bit Field Name	Description
[255:248]	CMD ECHO [7:0]	CMD ECHO [7:0]	For more details, see Figure 43 and Table 9.
[247:224]	ADC V0 Waveform Data [23:0]	ADC V0 Waveform Data [23:0]	
[223:216]	STATUS0 [7:0]	STATUS0 [7:0]	For more details, see Table 30.
[215:192]	ADC V1 Waveform Data [23:0]	ADC V1 Waveform Data [23:0]	
[191:184]	STATUS1 [7:0]	STATUS1 [7:0]	For more details, see Table 30.
[183:160]	ADC V2 Waveform Data [23:0]	ADC V2 Waveform Data [23:0]	
[159:152]	RESERVED [7:0]	RESERVED [7:0]	0x00 is transmitted.
[151:128]	ADC V3 Waveform Data [23:0]	ADC V3 Waveform Data [23:0]	
[127:120]	RESERVED [7:0]	RESERVED [7:0]	0x00 is transmitted.
[119:96]	ADC V4 Waveform Data [23:0]	ADC V4 Waveform Data [23:0]	
[95:88]	RESERVED [7:0]	RESERVED [7:0]	0x00 is transmitted.
[87:64]	ADC V5 Waveform Data [23:0]	ADC V5 Waveform Data [23:0]	
[63:56]	RESERVED [7:0]	RESERVED [7:0]	0x00 is transmitted.
[55:32]	ADC V6 Waveform Data [23:0]	ADC V6 Waveform Data [23:0]	
[31:24]	RDDATA1 [7:0]	-	Readback value at the requested address+1.
	-	ADDR [7:0]	LSB of requested write address echoed back.
[23:16]	RDDATA0 [7:0]	RDDATA0 [7:0]	Readback value at the requested address.
[15:0]	CRC_CCITT [15:0]	CRC_CCITT [15:0]	For more details, see the SPI Command Response CRC section.

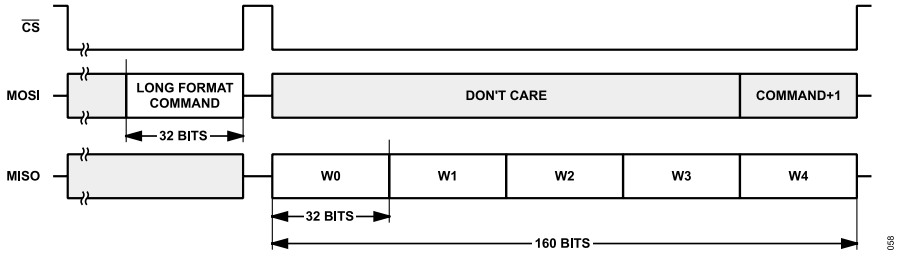


Figure 47. ADEMA124 Long Format

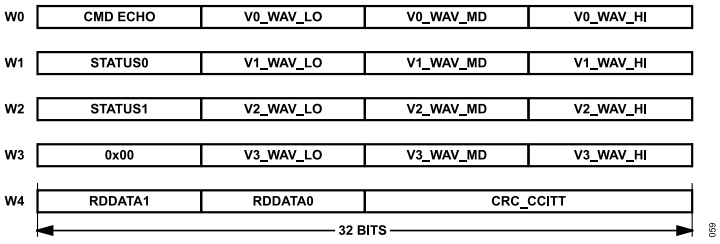


Figure 48. ADEMA124 Long Format Read Response Packet

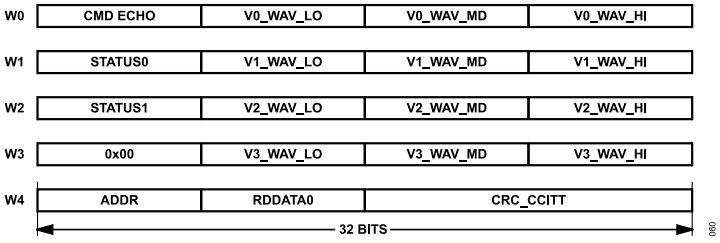


Figure 49. ADEMA124 Long Format Write Response Packet

APPLICATIONS INFORMATION

Table 12. ADEMA124 Long Format Response Bit Fields

Bit Field Location	Long Read Bit Field Name	Long Write Bit Field Name	Description
[159:152]	CMD ECHO [7:0]	CMD ECHO [7:0]	For more details, see Figure 43 and Table 9.
[151:128]	ADC V0 Waveform Data [23:0]	ADC V0 Waveform Data [23:0]	
[127:120]	STATUS0 [7:0]	STATUS0 [7:0]	For more details, see Table 30.
[119:96]	ADC V1 Waveform Data [23:0]	ADC V1 Waveform Data [23:0]	
[95:88]	STATUS1 [7:0]	STATUS1 [7:0]	For more details, see Table 30.
[87:64]	ADC V2 Waveform Data [23:0]	ADC V2 Waveform Data [23:0]	
[63:56]	RESERVED [7:0]	RESERVED [7:0]	0x00 is transmitted.
[55:32]	ADC V3 Waveform Data [23:0]	ADC V3 Waveform Data [23:0]	
[31:24]	RDDATA1 [7:0]	-	
	-	ADDR [7:0]	LSB of requested write address echoed back.
[23:16]	RDDATA0 [7:0]	RDDATA0 [7:0]	
[15:0]	CRC_CCIT [15:0]	CRC_CCIT [15:0]	For more details, see the SPI Command Response CRC section.

APPLICATIONS INFORMATION

Short Format Operation

Short response frames are 48 bits for both ADEMA124 and ADEMA127 devices. Short frame responses to not carry the ADC waveform data from all ADC channels and may be used for quicker device configuration and status querying of a single device. Short format operations are available only for uniquely addressed devices, as shown in the Individually Addressed section, and are not supported for daisy-chain connected devices.

CRC_CCITT for a short write response packet is calculated over bits [47:16].

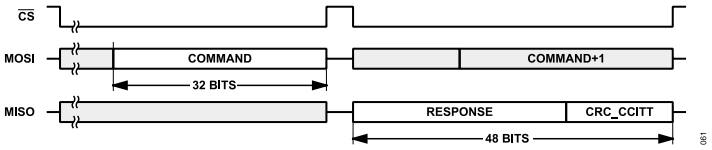


Figure 50. Short Format

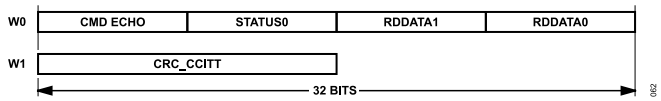


Figure 51. Short Read Response Packet

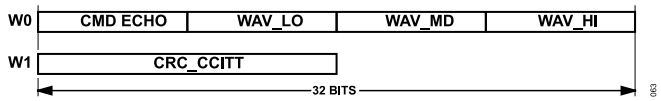


Figure 52. Short Read Response Packet of ADC Waveform Register

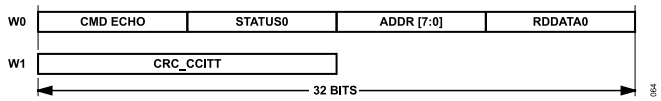


Figure 53. Short Write Response Packet

SPI Command Error Response Frame

When the ADEMA124/ADEMA127 detect a CRC mismatch in the SPI command, the command error response frame is transmitted in the directly subsequent frame. The command error response is a long format frame. The CRC interrupt bit, as shown in Figure 43 and Table 9, is set in the command response.

Note that if the next requested SPI frame is a short format frame, then the microcontroller may reduce the error response to a 48-bit fragment in anticipation of receiving a short format response. The first 8-bits of both short and long format responses is the command echo, which contains the CMD_CRC_ERR bit. When the CMD_CRC_ERR bit is set, the host must discard the rest of the packet.

APPLICATIONS INFORMATION

Communication Debug Features

The ADEMA124/ADEMA127 have a dedicated SCRATCH register that allows test write and read operations. The contents of the registers are not changed by the ADEMA124/ADEMA127 unless reset to default values with a hardware reset, software reset, or entry into standby mode.

The ADEMA124/ADEMA127 also have two modes to aid in debugging retrieval of ADC data: static and count mode. Static and count modes can be enabled by writing to the STREAM_DBG bits in the CONFIG0 register. The modes are available for both SPI long format and SPI short format operation.

When static mode is enabled, the ADC waveform registers are prevented from being updated by the ADEMA124/ADEMA127 DSP channels. The ADC waveform registers hold the last ADC sample until the value is overwritten by SPI command. The mode is used to verify correct extraction of ADC samples from the data stream by the host firmware.

To write and hold a value to the ADC waveform registers, do the following steps:

1. Set STREAM_DBG = Static Mode.
2. Wait for $\overline{\text{DREADY}}$ pin to go low.
3. Write to required values to ADC waveform data registers.
4. $\overline{\text{DREADY}}$ is asserted according to the set sample rate.

Count mode starts incrementing the ADC waveform registers from the last value in the registers. Count mode is used to verify directly subsequent ADC samples are captured by the by the host firmware and not missed or duplicated. Note that if writing a continuous waveform to ADC waveform registers, take care to synchronize to the $\overline{\text{DREADY}}$ signal to avoid an unexpected increment.

To write and start incrementation of the ADC waveform registers, do the following steps:

1. Set STREAM_DBG = Static Mode.
2. Wait for $\overline{\text{DREADY}}$ pin low.
3. Write to required values to ADC waveform data registers.
4. Set STREAM_DBG = Count Mode.
5. $\overline{\text{DREADY}}$ is asserted according to the set sample rate. On each $\overline{\text{DREADY}}$ assertion, all ADC waveform registers increment by one.

Set STREAM_DBG = Normal Mode or reset the ADEMA124/ADEMA127 to exit either debug mode.

Table 13. STREAM_DBG Bit Configuration

STREAM_DBG	Data Mode
0b00	Normal Mode
0b01	Static Mode
0b10	Count Mode

APPLICATIONS INFORMATION

Daisy-Chain

The bidirectional, serial port interface (SPI) supports a daisy-chain connection, which allows access to all registers while reducing the required microcontroller pin count. In the case of the SPI daisy-chain configuration, the $\overline{CS}$ signals from all connected devices are shared.

Daisy-chain devices function as successive shift registers. In the example configuration of Figure 54, data is shifted out of the microcontroller to the ADEMA127, then to the ADEMA124, and finally the ADE9113. The instant $\overline{CS}$ transitions from low-to-high, the portion of the SPI frame contained in the shift register of each device is interpreted. The example communications bit stream shown in Figure 55 corresponds with the example circuit in Figure 54.

The ADEMA124/ADEMA127 register configuration is not required for daisy-chain connected devices, however, SPI long frame format shown in Long Format Operation must be used for communication. The full SPI frame for daisy-chain connected devices must be the sum of all long format packets for all devices connected in daisy-chain.

Daisy-chain connected devices must operate from the same clock source. The clock source may be external, or it may be generated by the ADEMA124/ADEMA127 and shared via CLKOUT pin. Only a single $\overline{DREADY}$ pin is required for the daisy-chain to call for service. For more details on synchronization of sampling, see the Synchronization of Multiple Devices section.

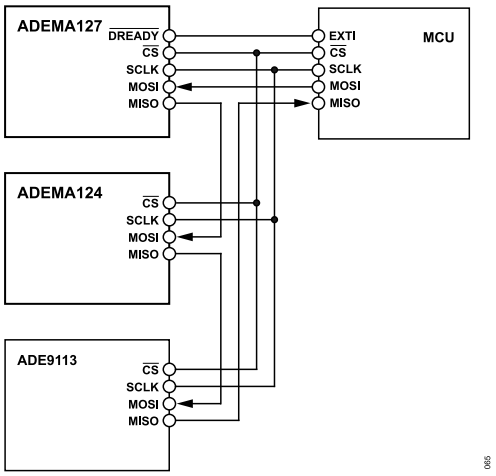


Figure 54. Daisy-Chain Connected Devices Example

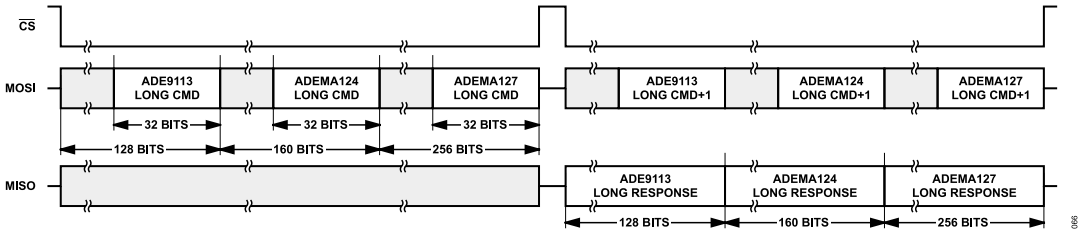


Figure 55. Daisy-Chain Communication Example

Individually Addressed

Individually addressed devices may be issued both short and long format commands.

APPLICATIONS INFORMATION

DATAPATH CONFIGURATION

All ADC channels of the ADEMA124 and ADEMA127 have identical electrical characteristics and configuration options. The input clock source, clock prescaler, and decimation rate settings are shared by all ADC channels. Each ADC channel has individual hardware filters and DSP filters, which can be configured independently. All filters are available at any configured output sample rate.

The ADEMA124/ADEMA127 immediately begin sampling and producing ADC waveform data at 32kSPS upon power-up provided the typical 16.384MHz clock input is available. The first two ADC waveform data sets are produced by the low latency sinc1 filter, as shown in Figure 56. For more details on start-up, see the Fast Start-Up section.

Datapath configuration of the ADEMA124/ADEMA127 is done via the SPI port. Configuration bit fields reside in MMR and if a DSP filter is enabled, DSP RAM also. Configuration bit fields are write locked by default, for more details, see the Configuration Lock and Access Bits and Full Configuration Lock sections.

Configuration of the DSP RAM must occur subsequent to any datapath configuration register writes. The step by step process for writing to the SPI accessible register and DSP RAM address are shown in Configuration Procedure section. For further register details, see the Register Details section. For more details on DSP RAM, see the DSP RAM Details section.

Synchronization of multiple devices is shown in the Synchronization of Multiple Devices section.

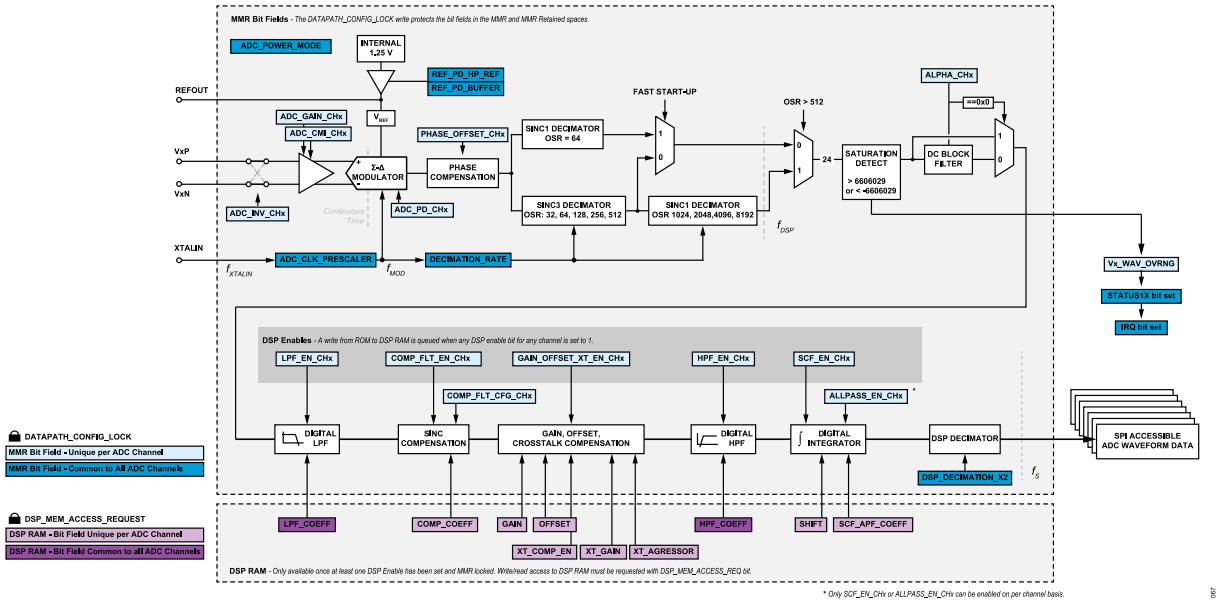


Figure 56. ADEMA124/ADEMA127 Datapath

APPLICATIONS INFORMATION

Analog Input

Each ADEMA124/ADEMA127 channel has an independent, second-order, simultaneously sampling Σ-Δ converter. Each ADC channel supports fully differential and pseudodifferential input configurations, each of which can go above and below AGND.

General guidance on sensor connection and external circuitry are shown in the Sensor to ADC Interface section.

Selectable Gain

Each ADC has an independent selectable gain of 1 or 2 set by the corresponding ADC_GAIN_CHx bit in the ADC_GAIN register. The differential voltage range and single-ended voltage range is simultaneously adjusted based on the selected gain setting. For specifications, see differential voltage range and single-ended voltage range in Table 2.

Overranging of the ADC input results in saturation of the full-scale codes. There are no overwraps or sign changes. Overranging sets the Vx_WAV_OVRNG bit corresponding to the ADC channel the event occurred on. For more details on overrange indication, see Figure 56 and Figure 59.

Common-Mode

Each ADC channel has an independent common-mode range setting bit, ADC_CMI_CHx, in the ADC_CMI register. The typical CT and voltage divider sensors of AC measurement systems oscillate around AGND/DGND and do not require a common-mode offset. This is the default configuration.

This feature enables the use of external amplifiers with a common-mode offset of 1.2V to better interface with Rogowski coil sensors requiring a preamplifier. The feature is only available when the channel gain is 1. Setting both ADC_GAIN_CHx = 1 and ADC_CMI_CHx = 1 on a given channel is an invalid configuration.

Invert

Inversion of the ADC inputs allows for easy correction of inadvertent assembly miswires or can be used as a design choice for more convenient PCB layout. Inversion of individual ADC channels is possible either by setting a negative gain value in the gain compensation or by setting corresponding bits in the ADC_INV register. Setting ADC_INV_CHx bits allows the ADC channels to be inverted without the increased power consumption associated with an enabled DSP filter. It is recommend to use the ADC_INV_CHx bit for an ADC channel rather than setting the associated GAIN[23:0] bit field to −1.

Details on the gain compensation is shown in the Gain, Offset, and Crosstalk Compensation section. Bit field settings for the ADC_INV register is shown in Table 29.

Voltage Reference

The ADEMA124/ADEMA127 include a low noise, low drift, internal band gap reference. The internal reference voltage of the ADEMA124/ADEMA127 is production trimmed to 1.25V. The ADEMA124/ADEMA127 have a 1.25V internal voltage reference enabled by default as the voltage reference (V_{REF}) for all ADC channels.

An external voltage reference may be routed to the REFOUT pin. To disable the internal reference and prevent contention between the internal and external voltage references, both the REF_PD_HP_REF bit and the REF_PD_BUFFER bit in the CONFIG0 register must be set to 0.

The REFOUT pin input impedance is shown in Table 2.

APPLICATIONS INFORMATION

Configuration Lock and Access Bits

Bit fields are partitioned into three distinct memory regions: Retained MMR, MMR, and DSP RAM. The DATAPATH_CONFIG_LOCK bit is a SPI write protect for the configuration bit fields in the Retained MMR and MMR spaces. The DSP_MEM_ACCESS_REQ is a SPI write protect for the configuration bit fields in DSP RAM. Both bits prevent SPI writes to their spaces by default. The specific memory location of individual bit fields is shown in Figure 56.

Both the DATAPATH_CONFIG_LOCK and DSP_MEM_ACCESS_REQ have additional functionality, as shown in Table 14 and Table 15.

Table 14. DATAPATH_CONFIG_LOCK Functions

DATAPATH_CONFIG_LOCK State	Action
1	SPI write protect for the datapath configuration bit fields in Retained MMR and MMR active.
	SPI read operations in Retained MMR and MMR always allowed.
1->0	ADC conversion process halted.
0	SPI writes to configuration bit fields in Retained MMR and MMR allowed.
0->1	1. If any LPF_EN_CHx, COMP_FLT_EN_CHx, GAIN_OFFSET_XT_EN_CHx, HPF_EN_CHx, or SCF_EN_CHx bit is high, DSP RAM is activated. a. Once DSP RAM activated, a ROM to DSP RAM write of all DSP RAM bit fields is initiated. The specific values written to DSP RAM are determined by the DATARATE bit field and the individual channel configurations of the ALLPASS_EN_CHx, SCF_EN_CHx and COMP_FLT_CFG_CHx bits[1]. 2. ADC conversion process begins.

[1] All default DSP filter coefficients loaded into DSP RAM are based on a 16.384MHz f_{XTALIN}.

Table 15. DSP_MEM_ACCESS_REQ Functions

DSP_MEM_ACCESS_REQ State	Action
0	SPI write protect for the datapath configuration bit fields in DSP RAM active.
	SPI read operations in DSP RAM not allowed. Read attempts return 0x00 regardless of bit field content.
0->1	-
1	SPI writes to configuration bit fields in DSP RAM allowed.
	SPI read operations in DSP RAM allowed.
1->0	-

For a detailed step-by-step instruction for the configuration process, see the Configuration Procedure section.

After configuration is complete, a larger group of bit fields may optionally be locked with the WR_LOCK bit. For more details, see the Full Configuration Lock section.

ADC Transfer Function

Precision measurements require calibration. ADC gain error, offset error, gain drift, and offset drift influence the measurement. The output code can be approximated with the ADC transfer function in Equation 3 for gain setting of 1 and Equation 4 for a gain setting of 2. Setting ADC_INV_CHx inverts the channel inputs. The ADC transfer function assumes DC input to remove the effects of datapath filters.

$$Typical\ Output\ Code, Gain\ of\ 1 = \frac{7}{8} \times \frac{VxP - VxM}{V_{REF}} \times 2^{23} \quad (3)$$

$$Typical\ Output\ Code, Gain\ of\ 2 = \frac{7}{4} \times \frac{VxP - VxM}{V_{REF}} \times 2^{23} \quad (4)$$

The saturation detect, as shown in Figure 56, latches the Vx_WAV_OVRNG bit if code is greater than 6606029 or less than −6606029. A Vx_WAV_OVRNG bit remains latched until the STATUS1 register bit is cleared.

Output Sample Rate

The output sample rate (f_s) is set by the external clock source and the bit field settings of the DATARATE register. A valid f_s configuration satisfies Equation 5 and the timing constraints of Equation 6 and Equation 7. Setting ADC_POWER_MODE to non default settings reduces the maximum valid f_{MOD} frequency.

$$5 + ADC\_CLK\_PRESCALER + DECIMATION\_RATE + DSP\_DECIMATION\_X2 \leq 16 \quad (5)$$

APPLICATIONS INFORMATION

The bit field values from ADC_CLK_PRESCALER, DECIMATION_RATE, and DSP_DECIMATION_X2 are taken directly for the Equation 5 calculation.

$$f_{MOD} \leq 2.048MHz \quad (6)$$

$$f_{DSP} \leq 64MHz \quad (7)$$

The f_s of ADEMA124/ADEMA127 is Equation 8.

$$f_s = \frac{f_{XTALIN}}{2^x} \quad (8)$$

where:

x = 5 + ADC_CLK_PRESCALER + DECIMATION_RATE + DSP_DECIMATION_X2.

Example calculation: With the default DATARATE register settings, ADC clock prescaler of 8 (ADC_CLK_PRESCALER = 0x3), decimation rate of 64 (DECIMATION_RATE = 0x1), and DSP decimation turned off (DSP_DECIMATION_X2 = 0x0), set the output sample rate to 32kSPS.

$$f_s = \frac{16.384MHz}{2^{5+0x3+0x1+0x0}} = 32kSPS \quad (9)$$

The default 16.384MHz input clock frequency can generate an output sample rate of 64kSPS, 32kSPS, 16kSPS, 8kSPS, 4kSPS, 2kSPS, 1kSPS, 500SPS, or 250SPS with recommend settings, as shown in Table 16. For intermediary or lower output sample rates, a lower input clock frequency must be provided. For available settings and details, see the DATARATE register in Table 30 .

Use of the Decimate-by-2 feature, DSP_DECIMATION_X2=1, requires that the LPF_EN_CHx bits for all active ADC channels be set to 1 to prevent foldback from above the Nyquist frequency.

Table 16. Recommended DATARATE Settings for Full Performance Mode

f_s, when f_{XTALIN} = 16.384MHz	DATARATE Setting	DSP Decimate-by-2	Over Sample Rate
64kSPS	0x30	-	32
32kSPS	0x31 (default)	-	64
16kSPS	0x32	-	128
8kSPS	0x33	-	256
4kSPS	0x34	-	512
2kSPS	0x35	-	1,024
1kSPS	0x36	-	2,048
500SPS	0x37	-	4,096
250SPS	0x38	-	8,192
32kSPS	0xB0	Enabled	64
16kSPS	0xB1	Enabled	128
8kSPS	0xB2	Enabled	256
4kSPS	0xB3	Enabled	512
2kSPS	0xB4	Enabled	1,024
1kSPS	0xB5	Enabled	2,048
500SPS	0xB6	Enabled	4,096
250SPS	0xB7	Enabled	8,192

Table 16. Recommended DATARATE Settings for Full Performance Mode (Continued)

Phase Compensation

The ADEMA124/ADEMA127 datapath can compensate for unequal phase error and datapath latencies between channels.

The ADEMA124/ADEMA127 compensate for phase delay and latency differences between channels by adjusting the start of the ADC sample set used to generate the ADC waveform data. Phase delay differences of integer multiples of the ADC sample period ($1/f_s$) are easily sorted by the microcontroller servicing the ADEMA124/ADEMA127. All channels are adjusted to either match the channel with the greatest phase delay exactly or be an integer multiple of the sample period different ($1/f_s$).

The target phase delay is set with the PHASE_OFFSET_CHx according to Equation 10.

$$Fine\ Phase\ Offset = \frac{PHASE\_OFFSET\_CHx[12:0]}{f_S \times 8192} \quad (10)$$

The resolution of the phase offset is determined by f_{MOD} and phase interpolator. All active ADC channels ADEMA124/ADEMA127 sample simultaneously under all operating conditions. The phase interpolator produces virtual samples in ¼ steps between the actual sigma delta modulator samples.

$$PHASE\_OFFSET\ Resolution = \frac{1}{f_{MOD} \times 4} \quad (11)$$

If the target phase delay setting is not evenly divisible by the resolution, the phase delay of the channel is rounded down to an integer multiple of the resolution.

Phase delay can be converted to degrees at a given frequency with Equation 12.

$$phase\ \ delay(^\circ) = 360^\circ \times \frac{PHASE\_OFFSET\_CHx[12:0]}{f_{MOD} \times 8192} \times decimation\_rate \times f_{LINE} \quad (12)$$

Sinc Decimation Filter

The 3-bit samples from the ΣΔ modulator are downsampled to 24-bit waveform data in the sinc decimation filter. The filter is third-order cascaded integrator comb (CIC) filter followed by a first order CIC filter for over sample rates of 1024 and above.

The ADEMA124/ADEMA127 start sampling immediately upon power up with an over sample rate of 64. To decrease output settling time, the first two samples are produced by a sinc1 filter. The third sample and all samples after are produced by the sinc3 filter.

APPLICATIONS INFORMATION

Table 17. Recommended DATARATE Settings for Full Performance Mode and f_{XTALIN} = 16.384MHz

DECIMATION_RATE Setting	Sinc3 OSR	Sinc1 OSR	Over Sample Rate	Latency	Latency[1] (µs)
0000	32	-	32	48.5/f_{MOD}	23.7
0001	64	-	64	96.5/f_{MOD}	47.1
0010	128	-	128	192.5/f_{MOD}	94.0
0011	256	-	256	384.5/f_{MOD}	188
0100	512	-	512	768.5/f_{MOD}	375
0101	512	2	1,024	1,024.5/f_{MOD}	500
0110	512	4	2,048	1,536.5/f_{MOD}	750
0111	512	8	4,096	2,560.5/f_{MOD}	1,250
1000	512	16	8,192	4,608.5/f_{MOD}	2,250

[1] f_{XTALIN} = 16.384MHz, f_{MOD} = 2.048MHz.

DC Block Filter

The DC blocking filter implements the block diagram, as shown in Figure 57. The alpha value in the transfer function is set by the ALPHA_CHx register where alpha = 2 − (2 × ALPHA_CHx). The DC block filter is bypassed by default and when the ALPHA_CHx bit field is set to 0x0.

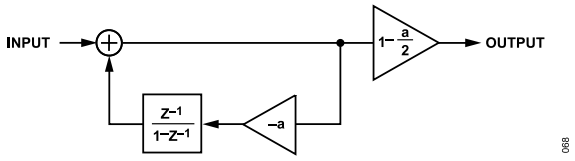


Figure 57. DC Block Filter Transfer Function

Table 18. DC Block Characteristics

f_s	ALPHA_CHx	Pass-Band Attenuation (50Hz)	Pass-Band Attenuation (60Hz)	−3dB Corner
32kSPS	1/4	29.28	27.70	1,453.90
	1/16	16.45	14.91	328.29
	1/64	5.52	4.45	80.32
	1/128	2.14	1.59	39.99
	1/512	0.16	0.11	9.97
	1/4,096	0.00	0.00	1.25
	1/32,768	−0.01	−0.01	0.19
16kSPS	1/4	23.27	21.70	719.61
	1/16	10.71	9.29	162.76
	1/64	2.15	1.60	40.15
	1/128	0.64	0.45	23.16
	1/512	0.04	0.02	4.98
	1/4,096	0.00	0.00	0.62
	1/32,768	−0.01	−0.01	0.14
4kSPS	1/4	11.52	10.07	184.34
	1/16	2.23	1.66	41.00
	1/64	0.17	0.11	9.57
	1/128	0.04	0.02	4.98
	1/512	0.00	0.00	1.25
	1/4,096	−0.01	−0.01	0.16
	1/32,768	−0.01	−0.01	0.15

APPLICATIONS INFORMATION

Digital Low-Pass Filter (LPF)

Each ADC channel has an independent enable bit LPF_EN_CHx in the DATAPATH_CONFIG_CHx register. The digital low-pass filter can be used independently. However, using the digital LPF in conjunction with the DSP decimate-by-2 feature produces greater signal bandwidth for a given f_S.

The digital low-pass filter can be tuned by setting the LPF_COEFF_B1 through LPF_COEFF_B17 bit fields.

$$H[Z] = B0 \cdot Z^{-0} + B1 \cdot Z^{-1} + B2 \cdot Z^{-2} + B3 \cdot Z^{-3} \ldots + B17 \cdot Z^{-17} \quad (13)$$

Sinc Compensation Filter

Sinc compensation corrects for roll off at higher frequencies by applying gain to flatten the frequency response. Pass-band flatness with and without the sinc compensation filters turned on is shown in Bandwidth and Pass-Band Flatness.

The compensation filter of each channel is enabled by setting the corresponding COMP_FLT_EN_CHx bit to 1. Based on the configuration bit and decimation rate, a set of DSP filter coefficients are loaded from ROM to the COMP_COEFF_B0 through COMP_COEFF_B6 RAM addresses when the DATAPATH_CONFIG_LOCK is set to 1.

The configuration bit COMP_FLT_CFG_CHx sets the filter characteristics. Setting COMP_FLT_CFG_CHx = 0 compensates for sinc droop only, while setting COMP_FLT_CFG_CHx = 1 compensates for sinc droop and distortion introduced by an external 8kHz band limiting filter.

$$H[Z] = B0 \cdot Z^{-0} + B1 \cdot Z^{-1} + B2 \cdot Z^{-2} + B3 \cdot Z^{-3} + B4 \cdot Z^{-4} \quad (14)$$

Gain, Offset, and Crosstalk Compensation

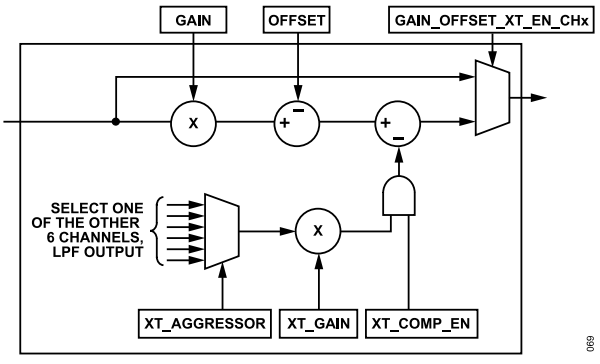


Figure 58. Gain, Offset, and Crosstalk Compensation

Gain, offset, and crosstalk compensation are enabled on a channel-by-channel basis by setting the GAIN_OFFSET_XT_CHx bit in the DATAPATH_CONFIG_CHx register.

Gain settings are written to the individual GAIN[23:0] bit field for each ADC channel in DSP RAM. The incoming data stream is multiplied by the value in this register. Entering a negative gain compensation value inverts the waveform data. Negative gain compensation values can be used for correction of assembly miswires or as a design choice.

The range of GAIN is ±2. The gain value is entered in signed 2.22 format. The 2.22 is interpreted as a 24-bit two's complement that is right shifted by 22 bits as shown in Equation 15.

$$ADC\ Channel\ Gain = \frac{GAIN[23:0]}{2^{22}} \quad (15)$$

Table 19. 2.22 Format Examples

GAIN_HI	GAIN_MD	GAIN_LO	Decimal Gain Value Equivalent
00.11 1110	1000 0000	0000 0000	0.9765625
01.00 0000	0000 0000	0000 0000	1
11.00 0000	0000 0000	0000 0000	−1
10.11 0001	0000 0000	0000 0000	−1.234375

Offset settings are written to the individual OFFSET[23:0] bit field for each ADC channel in DSP RAM. These values are a two's complement representation of ADC codes and are the same format as ADC waveform registers. The functional offset range is ±1.5V. Negative offset values generates a positive offset and accordingly, positive offset value generates a negative offset. Note that as per Figure 58, gain compensation is applied before offset compensation.

The DSP RAM address for GAIN[23:0] and OFFSET[23:0] of individual ADC channels are given in Table 33.

Crosstalk Compensation

The crosstalk compensation can be used to subtract samples from one ADC channel from the samples of another. The tap for aggressor channels are taken from the LPF output of the respective channel. LPF may be either enabled or disabled.

Gain settings are written to the individual XT_GAIN[23:0] bit field for each ADC channel in DSP RAM. The gain value for the aggressor channel is entered in signed 2.22 format.

Digital High-Pass Filter (HPF)

A high-pass filter is provided to remove DC offsets for accurate RMS and energy measurements. The digital HPF is disabled by default. The digital HPF are enabled independently for each ADC channel by setting the HPF_EN_CHx bit field in the DATAPATH_CONFIG_CHx register. The corner frequency of the digital HPF is set to 10Hz with fXTALIN = 16.384MHz.

The HPF coefficient values loaded to HPF_COEFF_B0, HPF_COEFF_B1, HPF_COEFF_B2, HPF_COEFF_A1, HPF_COEFF_A2 when the HPF filter is enabled is based on DECIMATION_RATE

APPLICATIONS INFORMATION

settings. Filter characteristics are adjustable. For more details, see Equation 16 HPF filter transfer function and the Configuration Procedure section.

$$H(z) = \frac{B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}}{1 + A1 \cdot z^{-1} + A2 \cdot z^{-2}} \quad (16)$$

Table 20. Digital High-Pass Filter Phase Response

Output Sample Rate (SPS)	Phase Response at 50Hz (°)	Amplitude Response at 50Hz (dB)
64,000	16.407043	−0.005443
32,000	16.408815	−0.005181
16,000	16.408806	−0.004744
8,000	16.411425	−0.002658
4,000	16.405784	−0.002284
2,000	16.381072	−0.002178
1,000	16.281255	−0.002187
500	15.879128	−0.002052
250	14.226326	−0.001711

Digital Integrator and All Pass Filter

The user programmable integrator in the ADEMA124/ADEMA127 is specifically designed for Rogowski coil sensor compensation. The leaky integrator filter is first order IIR filter enables seamless compatibility with di/dt current sensors. Rogowski coil sensor output increases by 20dB/decade over the frequency range. To compensate for this increase, the digital integrator applies −20dB/decade gain with a phase shift of approximately −90°.

Each ADC channel has independent enable bits SCF_EN_CHx for the digital integrator and ALLPASS_EN_CHx for the all pass filter in the DATAPATH_CONFIG_CHx register. The choice of filters on each channel is mutually exclusive, which enables both digital integrator and the all pass filter on the same channel simultaneously is invalid.

Default DSP coefficients are loaded to the SCF_APF_COEFF_B0[23:0], SCF_APF_COEFF_B1[23:0], SCF_APF_COEFF_A1[23:0] address in DSP RAM based on the DECIMATION_RATE register setting, and SCF_EN_CHx and ALLPASS_EN_CHx settings on a per ADC channel basis when the DATAPATH_CONFIG_LOCK is set to 1.

Equation 17 is the transfer function of the SCF.

$$H(z) = \frac{B0 + B1 \cdot z^{-1}}{1 + A1 \cdot z^{-1}} \quad (17)$$

The SHIFT function enables a left shift of small input signals before the integrator to reduce quantization noise that otherwise occurs with small signals.

The all pass filter is available to tune the latency of a channel. This filter is to help a non-Rogowski signal path meet a higher meter accuracy class by correcting for predictable phase and amplitude errors from the sinc and band-limiting filter.

For more details on latency of the ADEMA124/ADEMA127 with various datapath options enabled, see the Conversion Latency section.

The ALLPASS_EN_CHx enable bits do not enable the DSP and require at least one LPF_EN_CHx, COMP_FLT_EN_CHx, GAIN_OFFSET_XT_EN_CHx, HPF_EN_CHx or SCF_EN_CHx bit in any DATAPATH_CONFIG_CHx register to be set high for the all pass filter to be activated.

Full Configuration Lock

The configuration lock feature prevents changes to the ADEMA124/ADEMA127 configuration. When enabled, the configuration lock feature does not allow changes to writable configuration registers. To enable this feature, write the Lock Key to the WR_LOCK register. To disable the feature, write the Unlock Key. For more details, see the WR_LOCK row of Table 30.

CONFIGURATION PROCEDURE

The analog-to-digital conversion process must be paused while any datapath configuration registers are being written. The DATAPATH_CONFIG_LOCK bit is the mechanism to safely pause and restart data conversion with the new register settings applied. Configuring register values only requires the following steps:

1. Unlock the datapath. Set DATAPATH_CONFIG_LOCK = 0.
2. Make all changes to datapath configuration registers.
3. Lock the datapath. Set DATAPATH_CONFIG_LOCK = 1.
4. Wait for $\overline{\text{DREADY}}$ pin to be set low. The $\overline{\text{DREADY}}$ pin low transition indicates ADC operation has restarted and all internal ROM to DSP RAM writes have completed. The process requires approximately 40µs. Do not perform SPI transaction before the process is completed.

Writing any DSP RAM address requires additional steps and must be the final step of ADEMA124/ADEMA127 configuration. When any DSP filter is enabled in any DATAPATH_CONFIG_CHx register, setting DATAPATH_CONFIG_LOCK = 1 causes DSP coefficients to be loaded from ROM to all the SPI accessible DSP RAM addresses. Note this operation overwrites all values stored in DSP RAM. Writes to the DSP RAM require a memory access request using the DSP_MEM_ACCESS_REQ bit.

To write both register values and DSP RAM values, do the following steps exactly for the changes to DSP RAM changes to take effect:

1. Unlock the datapath. Set DATAPATH_CONFIG_LOCK = 0.
2. Make all changes to datapath configuration registers.
3. Lock the datapath. Set DATAPATH_CONFIG_LOCK = 1.
4. Wait for $\overline{\text{DREADY}}$ pin to be set low. The $\overline{\text{DREADY}}$ pin low transition indicates ADC operation has restarted and all internal ROM to DSP RAM writes have completed. The process requires approximately 40µs. Do not perform SPI transaction before the process is completed.

APPLICATIONS INFORMATION

5. Request DSP memory access. Set DSP_MEM_ACCESS_REQ = 1.
6. Wait for DSP actions to halt. Read from STATUS2 register until DSP_MEM_ACCESS_READY = 1.
7. Make all changes to the DSP coefficients in Table 33 and Table 34.
8. Set DSP_MEM_ACCESS_REQ = 0.
9. ADC waveform samples are immediately valid, however, filters have a settling time based on the datapath configuration.

STATUS REGISTERS AND IRQ

The IRQ bit is a configurable interrupt for system events. The events which trigger a IRQ bit are configured by setting corresponding bits in the MASK0, MASK1, and MASK2 registers to 1.

The IRQ bit is returned with every SPI response frame as part of the command echo bit field, as shown in the Figure 43 and Table 9. SPI operations return different levels of status register detail, as shown in Table 21.

Table 21. Status Registers and IRQ by SPI Operation

SPI Response	IRQ	STATUS0	STATUS1	STATUS2
Error	✓			
Short Read	✓	✓		
Short Read, ADC Waveform	✓			
Short Write	✓	✓		
Long Read	✓	✓	✓	
Long Write	✓	✓	✓	

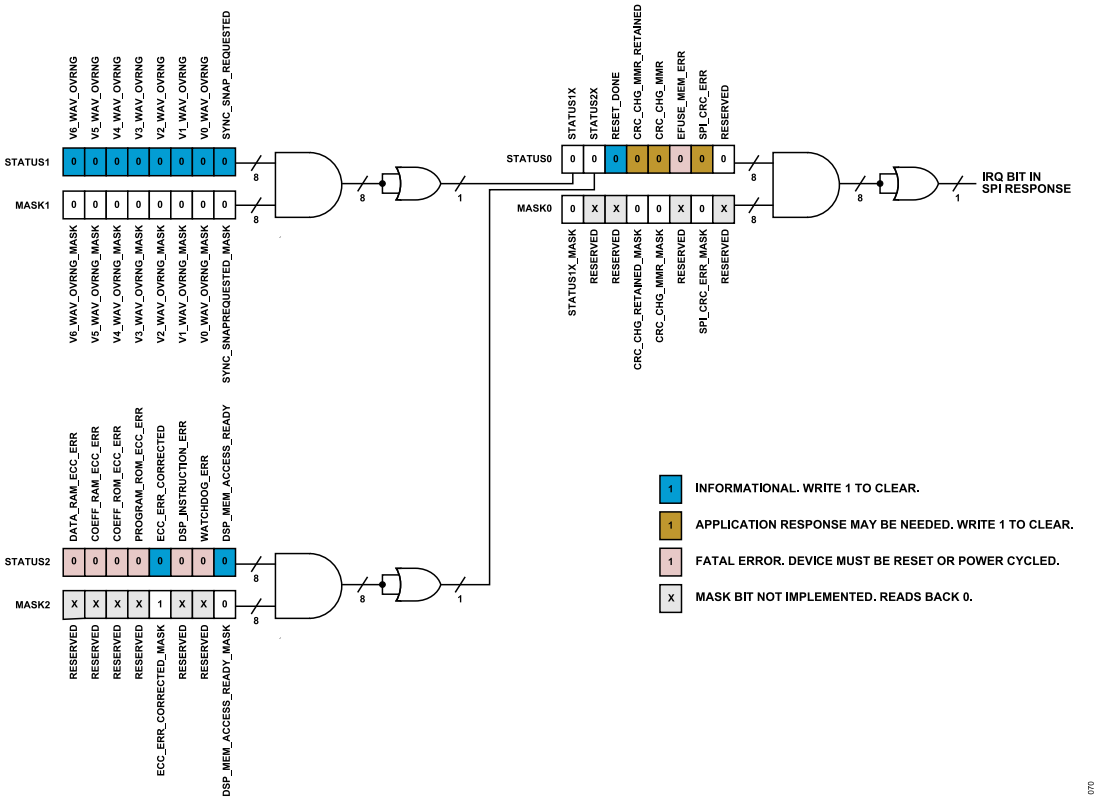


Figure 59. IRQ Generation

The bits in the STATUS0, STATUS1, and STATUS2 registers of the ADEMA124/ADEMA127 characterize the state of the device. The STATUS0 and STATUS1 registers are readback as part of all long SPI transactions, and STATUS0 is readback as part of most short SPI transaction. The STATUS0 is not returned in the special case of short format waveform register reads.

At power-up, the ADEMA124/ADEMA127 signal the end of the reset period by setting RESET_DONE = 1 in the STATUS0 register, indicating that the IC is ready for configuration. SPI_CRC_ERR is set to 1 if a CRC error is detected on the previous SPI command received by the ADEMA124/ADEMA127.

STATUS1 contains the overrange status of all of the ADC channels. These bits are W1C. Continuous writes to the STATUS1 register while retrieving ADC data indicates if samples are persistently out of range.

The DATA_RAM_ECC_ERR, COEFF_RAM_ECC_ERR, COEFF_ROM_ECC_ERR, PROGRAM_ROM_ECC_ERR, DSP_INSTRUCTION_ERR, and WATCHDOG_ERR int the STATUS2 register indicate fatal faults. These errors are unmaskable and set both the STATUS2X bit in STATUS0 register and the IRQ bit in the SPI command response. These errors require a reset of the ADEMA124/ADEMA127. Reading the STATUS2 register before reset

APPLICATIONS INFORMATION

provides insight to the cause of error within the ADEMA124/ADEMA127.

The WATCHDOG_ERR bit may be set after a fatal fault condition. This bit may indicate the DSP is under-clocked for the set ADC sample rate when triggered during hardware development.

The DSP_MEM_ACCESS_READY bit in the STATUS2 register is a handshake response to the DSP_MEM_ACCESS_REQ bit in the ACCESS_EXTENDED_MMAP register. Operations requiring use of these bits are shown in Configuration Procedure section.

CRC PROTECTION

Ensuring the integrity of ADC waveform data is critical in energy metering applications. The ADEMA124/ADEMA127 has four unique CRC to protect bidirectional SPI communication and the configurations affecting ADC waveform data in MMR. All of the DSP RAM space is protected by ECC.

SPI Command CRC

The ADEMA124/ADEMA127 SPI commands have an 8-bit CRC error detection scheme. The CRC is enabled by default and computed for each received SPI command frame. SPI commands are executed only when the received CRC matches the computed value. If the CRC does not match, the SPI command is ignored, the SPI_CRC_ERR bit is set, and the SPI command error response frame is transmitted by the ADEMA124/ADEMA127 in response. The SPI_CRC_ERR bit is W1C.

The 8-bit CRC required in the command packet is calculated over SPI command bits[31:8] in Table 8. The polynomial in Table 22 is used.

Table 22. SPI Command CRC

Description	Characteristic
Polynomial	$x^8 + x^2 + x + 1$
Seed	0x00
XOR	0x55

The CRC of the SPI command can be disabled by clearing the CRC_EN_SPI_WRITE bit in the CONFIG0 register. The short format command to disable the CRC in hexadecimal is 00 02 C0 31. The long format disable is 40 02 C0 B7.

APPLICATIONS INFORMATION

SPI Command Response CRC

Each response from the ADEMA124/ADEMA127 is protected by a 16-bit CRC, as shown in Table 23. The initial value of 0xFFFF ensures a nonzero output with zero input.

Table 23. SPI Command Response CRC

Description	Characteristic
Polynomial	$x^{16} + x^{12} + x^5 + 1$
Seed	0xFFFF
XOR	None

The CRC_CCITT for the ADEMA124 long read response, long write response, and command error response packet is calculated over bits [159:16]. The CRC_CCITT for the ADEMA127 long read response, long write response, and command error response packet is calculated over bits [255:16]. The CRC_CCITT for a short format response packet is calculated over bits [47:16] for both ADEMA124 and ADEMA127.

The 16-bit CRC_CCITT generated by the ADEMA124/ADEMA127 can be ignored or not retrieved by the microcontroller. Note the position of the SPI command bit field is denoted by the $\overline{CS}$ pin low-to-high transition, as shown in Figure 60. The length of the SPI packet on must be adjusted to compensate for the shorted packet.

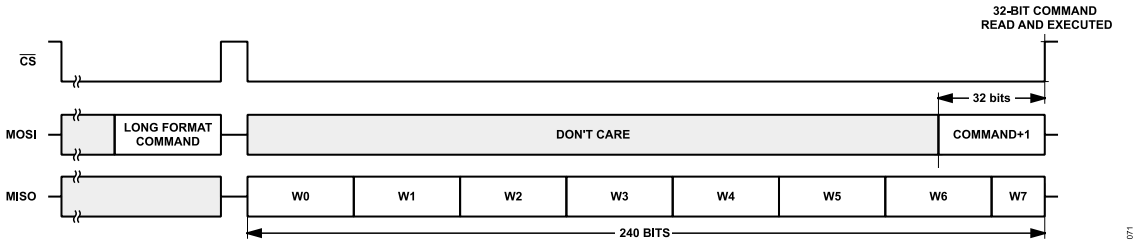


Figure 60. ADEMA127 Long Format, 16-Bit CRC_CCITT not Retrieved

APPLICATIONS INFORMATION

Configuration Register Background CRC

Two independent 16-bit CRC are calculated over the configuration bit fields in retained MMR and MMR approximately every 8ms. The result from Retained MMR is stored in the CRC_RESULT_MMR_RETAINED bit field and MMR result in CRC_RESULT_MMR bit field. The default value in the CRC_RESULT_MMR_RETAINED and CRC_RESULT_MMR bits is the CRC result of the default configuration. If there is a change in the CRC result, the CRC_CHG_MMR_RETAINED or CRC_CHG_MMR bit inside of STATUS0 is set.

The CRC calculation of the configuration registers can also be performed on command, bypassing the scheduled calculation every 8ms by writing to the CRC_FORCE_MMR_RETAINED bit or the CRC_FORCE_MMR bit. The CRC_FORCE bits automatically clear once the calculation is complete and the respective CRC_DONE_MMR_RETAINED or CRC_DONE_MMR bit is set once the calculation is complete.

DSP RAM ECC

ECC protects against individual bit errors due to environmental corruption.

An ECC is computed across every 3 adjacent bytes in DSP RAM. The ECC vales are internal and cannot be read. Errors in DSP RAM are reported in the STATUS2 register.

SENSOR TO ADC INTERFACE

The impedance of the ADEMA124/ADEMA127 depends on the programmable gain selected. There is no internal buffering of the input signal. For more details, see the differential input impedance specification in Table 2.

For more details on ADC input configuration options, see the Analog Input section.

Anti-Aliasing Filters

Aliasing is an artifact of all sampled systems, regardless of the architecture. Aliasing refers to the frequency components of the input signal that are higher than half the output sampling rate, f_s, which appear in the sampled signal at a frequency less than half the sampling rate. Frequency components more than half the sampling frequency, $f_{Nyquist}$, are imaged or folded back, as shown in Figure 61.

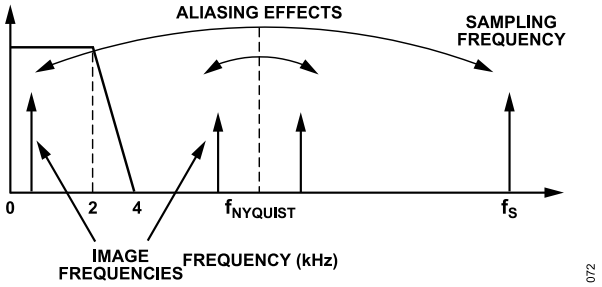


Figure 61. Aliasing Effects

Choose the anti-aliasing filter cutoff frequency (f_c) based on the Nyquist frequency of the output sample rate to provide sufficient attenuation of out of band signals. The same cutoff frequency is used for all the VxP and VxM pins of both current and voltage sensors to avoid introducing phase errors between the signals. Filter caps must be NP0 or C0G variety for low temperature coefficient. R_{th} in Equation 18 is the Thevenin's equivalent resistance at the node shared by the ADC input pin and anti-aliasing filter cap.

$$f_c = \frac{1}{2\pi \times R_{th} \times C} \quad (18)$$

Interfacing to Current and Voltage Sensors

Figure 62 shows an interface circuit to measure the mains voltage that produces a pseudodifferential input signal to the ADC channel. A current transformer (CT) with center tapped burden resistor, as shown in Figure 63 generates differential, antiphase signals at the ADC inputs. Figure 64 shows the recommended circuit to connect to Rogowski coil current sensors.

Metering applications must scale voltage and current sensor output to meter accurately in all system states without clipping. A voltage sensor is typically scaled for approximately 2/3 of the ADC full-scale range (FSR) with nominal system voltage applied. A current sensor output is typically scaled for only 1/2 of FSR at nominal levels to allow for accurate inrush current measurements. The differential voltage range and common-mode range of each channel depend on gain settings. The ADC analog input voltage ranges are shown in Table 2.

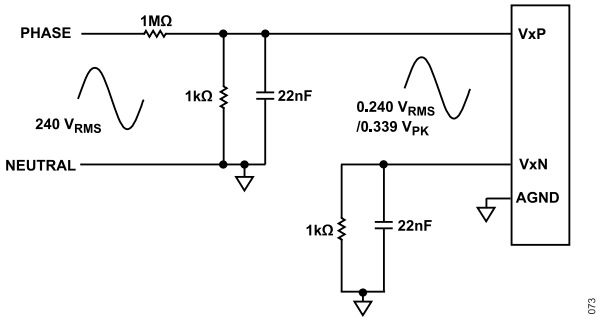


Figure 62. Phase Voltage Sensed Through Resistor Divider, 1x Gain, Pseudodifferential Input

APPLICATIONS INFORMATION

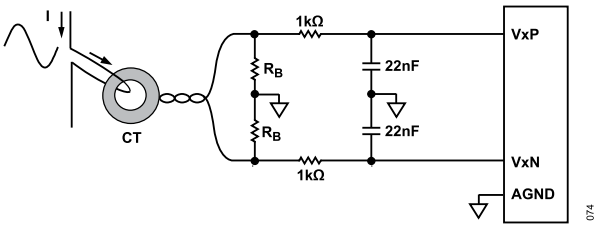


Figure 63. Current Transformer Current Sensor Interface Circuit

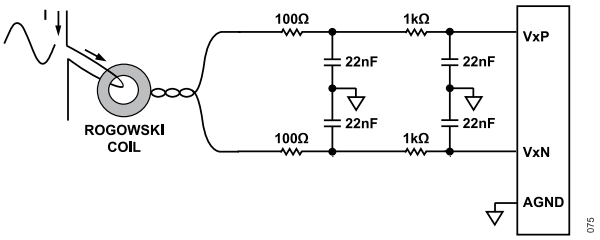


Figure 64. Rogowski Coil Current Sensor Interface Circuit

Note that the Rogowski coil input network has a second-order anti-alias filter to further reduce out of band noise because the Rogowski sensor has a 1/f response.

Unused ADC channels are left floating or tied to AGND. Disable the channel by setting the corresponding ADC_PD_CHx bit in the ADC_PD register.

Fully Differential Inputs

Figure 65 and Figure 66 show two common types of input signals for an energy monitoring application. Figure 65 shows the maximum input allowed with differential antiphase signals. A current transformer with center tapped burden resistor generates differential, antiphase signals. Figure 66 shows the maximum input signal with pseudodifferential signals, similar to those obtained when sensing the mains voltage signal through a resistive divider.

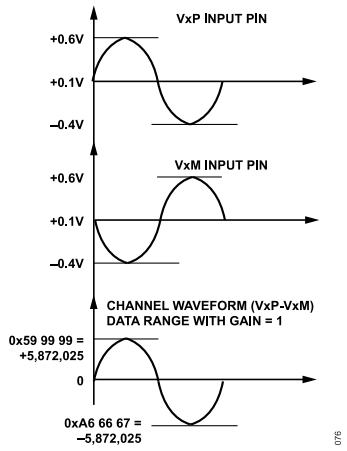


Figure 65. Maximum Input Signal with Differential Antiphase Input with Common-Mode Voltage = 0.1V, Gain = 1

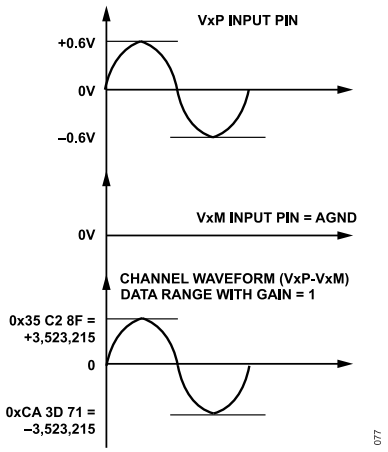


Figure 66. Maximum Input Signal with Pseudodifferential Input with Common-Mode Voltage = 0V, Gain = 1

CRYSTAL OSCILLATOR/EXTERNAL CLOCK

The ADEMA124/ADEMA127 require either an external digital clock signal or crystal for operation.

A digital clock signal is routed to the XTALIN pin to clock the ADEMA124/ADEMA127. Leave the XTALOUT pin floating when XTALIN is provided an external digital clock source. The requirements for external digital clock source frequency, duty cycle and voltage levels are shown in Table 2.

When a crystal is used as the clock source for the ADEMA124/ADEMA127, attach the crystal and the ceramic capacitors, with capacitance of C_1 and C_2, as shown in Figure 67. It is not recommended to attach an external feedback resistor in parallel to the crystal.

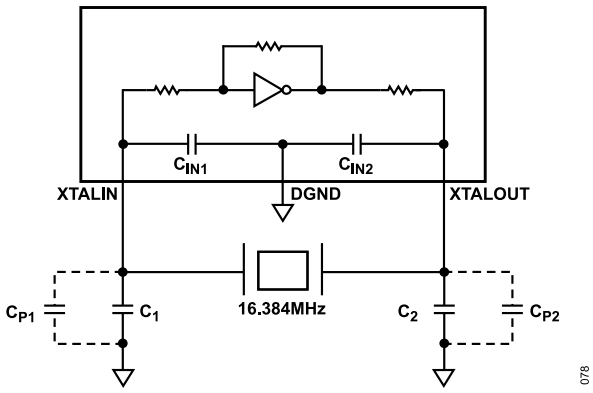


Figure 67. Crystal Application Circuit

Crystal Selection

The ADEMA124/ADEMA127 are compatible with crystals from 12.288MHz to 16.384MHz. The typical application uses a 16.384MHz crystal because it divides by powers of 2 to the specified sample rates.

APPLICATIONS INFORMATION

A 16.384MHz crystal with a critical transconductance, $gm_{CRITICAL}$, five times smaller than the minimum transconductance specification, g_m, in Table 2 can be connected across the XTALIN and XTALOUT pins to provide a clock source for the ADEMA124/ADEMA127. The term $gm_{CRITICAL}$ is defined as the minimum gain required to start the crystal oscillator circuit, expressed in mA/V, and found with Equation 19.

$$gm_{CRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2\pi \times f_{CLK})^2 \times (C_0 + C_L)^2 \quad (19)$$

where:

- ESR_{MAX} is the maximum ESR, expressed in ohms.
- f_{CLK} is 16.384MHz expressed in Hz as 16.384×10^6.
- C_0 is the maximum shunt capacitance, expressed in farads.
- C_L is the load capacitance, expressed in farads.

The figures ESR_{MAX}, C_0, and C_L are provided by the manufacturer of the crystal in the associated component data sheet. Crystals with low ESR and smaller load capacitance have a lower $gm_{CRITICAL}$ and are easier to drive.

Load Capacitor Calculation

Crystal manufacturers specify the combined load capacitance across the crystal, C_L. The elements contributing to the capacitance across the crystal are shown in Figure 67 can be described as follows:

- C_{P1} and C_{P2}: Parasitic capacitance on the clock pins formed due to printed circuit board (PCB) traces.
- C_{IN1} and C_{IN2}: Internal capacitance of the XTALIN and XTALOUT pins respectively, and shown in Table 2.
- C_1 and C_2: Selected load capacitors to get the correct combined C_L for the crystal.

The combined load capacitance, C_L, at the XTALIN and XTALOUT pins is:

$$C_L = \frac{(C_1 + C_{P1} + C_{IN1}) \times (C_2 + C_{P2} + C_{IN2})}{C_1 + C_{P1} + C_{IN1} + C_2 + C_{P2} + C_{IN2}} \quad (20)$$

Keep the total capacitance on both the XTALIN pin and XTALOUT pin equal. Layout the crystal circuitry such that $C_{P1} = C_{P2}$. Select load capacitors such that $C_1 = C_2$.

$$C_1 + C_{P1} + C_{IN1} = C_2 + C_{P2} + C_{IN2} \quad (21)$$

Using Equation 20 and Equation 21, the values of C_1 and C_2 can be calculated.

SYNCHRONIZATION OF MULTIPLE DEVICES

Metrology applications require simultaneous ADC sampling for power calculations. The prerequisite to simultaneous ADC samples from multiple devices is shared f_{XTALIN} and f_s frequencies. Configure all ADEMA124/ADEMA127 devices with the same DATARATE register settings and provide each with a shared input clock source. The ADC sampling must also occur at the same points in time and devices must be ready for waveform data retrieval simultaneously.

The ADEMA124/ADEMA127 coordinate all operation from an internal 14-bit counter. The SNAPSHOT bit provides the mechanism to verify synchronization of the 14-bit counters between multiple devices. The ALIGN bit synchronizes the counters and also reports the 14-bit counter value immediately before the synchronization command is executed. Either operation may be performed at any time the ADEMA124/ADEMA127 are in CCM.

The verification and synchronization operations are both two step procedures. The device is first primed by setting either SNAPSHOT = 1 for verification or ALIGN = 1 for synchronization and then triggered by the next transition of the $\overline{CS}$ pin from high-to-low, as shown in Figure 68 and Figure 69.

Asserting the $\overline{CS}$ pin causes the ADEMA124/ADEMA127 to drive the MISO as the device prepares to shift data out. Setting PREP_BROADCAST = 1 along with either ALIGN or SNAPSHOT sets the MISO output pin to a high-impedance state for the duration of the next $\overline{CS}$ pin assertion. This prevents contention between MISO pin output drivers when individually addressed devices share a MISO signal trace on the PCB. Daisy-chain connected devices do not have shared signal traces and do not use the PREP_BROADCAST bit.

The 14-bit counter value is written to SNAPSHOT_COUNT[13:0] in the SHAPSHOT_COUNT_HI and SHAPSHOT_COUNT_LO registers within one period of f_{XTALIN}. The 14-bit counter decrements from the initial value C_0 , shown in Table 24, to 0 and repeats. The contents of SNAPSHOT_COUNT_HI and SNAPSHOT_COUNT_LO are shown in Figure 70. These values can then be read out and compared by the host microcontroller. Counter values ±1 count can be attributed to the difference between microcontroller and ADC clock sources.

Table 24. Counter Initial Values as a Function of DATARATE Register Settings

ADC Output Frequency (kHz)[1]	Counter C0 Initial Value
64	255
32	511
8	2,047
4	4,095
2	8,191
1	16,383

[1] XTALIN = 16.384MHz.

The SYNC_SNAP_REQUESTED bit in the STATUS1 register is set when synchronization is initiated. The ADEMA124/ADEMA127 alignment verification and synchronization mechanisms are compatible with ADE9103/ADE9112/ADE9113 devices.

Setting ALIGN = 1 and SNAPSHOT = 1 with the same SPI write is not a valid operation.

APPLICATIONS INFORMATION

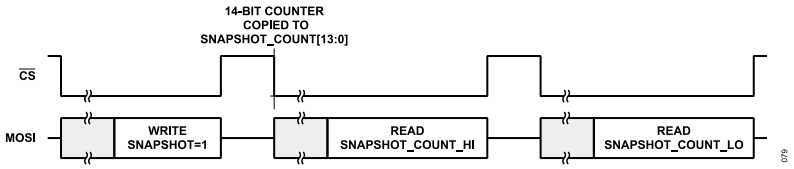


Figure 68. Alignment Verification with SNAPSHOT bit of Daisy-Chain Connected Devices

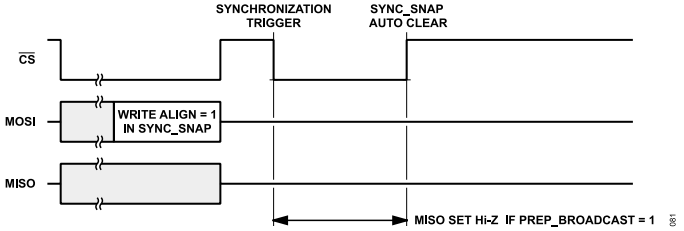


Figure 69. Synchronization with ALIGN Bit

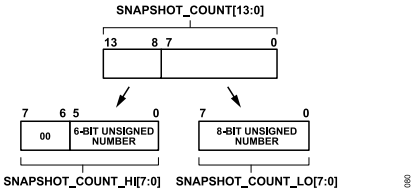


Figure 70. 14-Bit Counter Value

POWER CONSUMPTION

Reduced power consumption can be achieved by reducing the XTALIN frequency, reducing the OSR, and/or operating with the DSP disabled.

APPLICATIONS INFORMATION

POLYPHASE ENERGY METERS

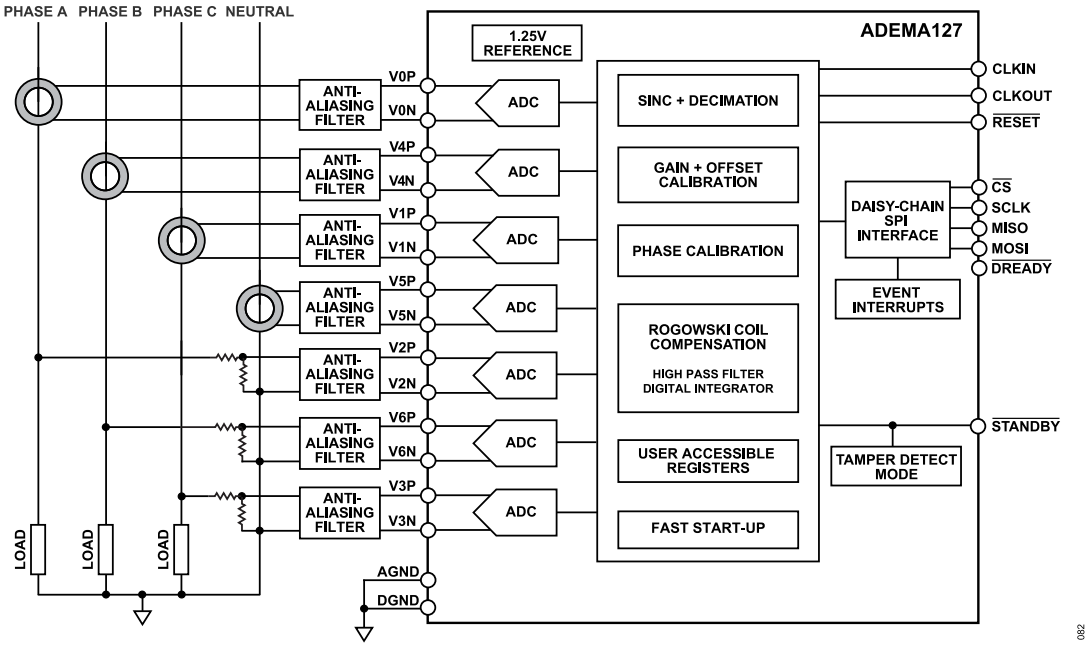


Figure 71. 3-Phase Energy Meter

Figure 72 shows daisy connected devices with shared clock signal.

APPLICATIONS INFORMATION

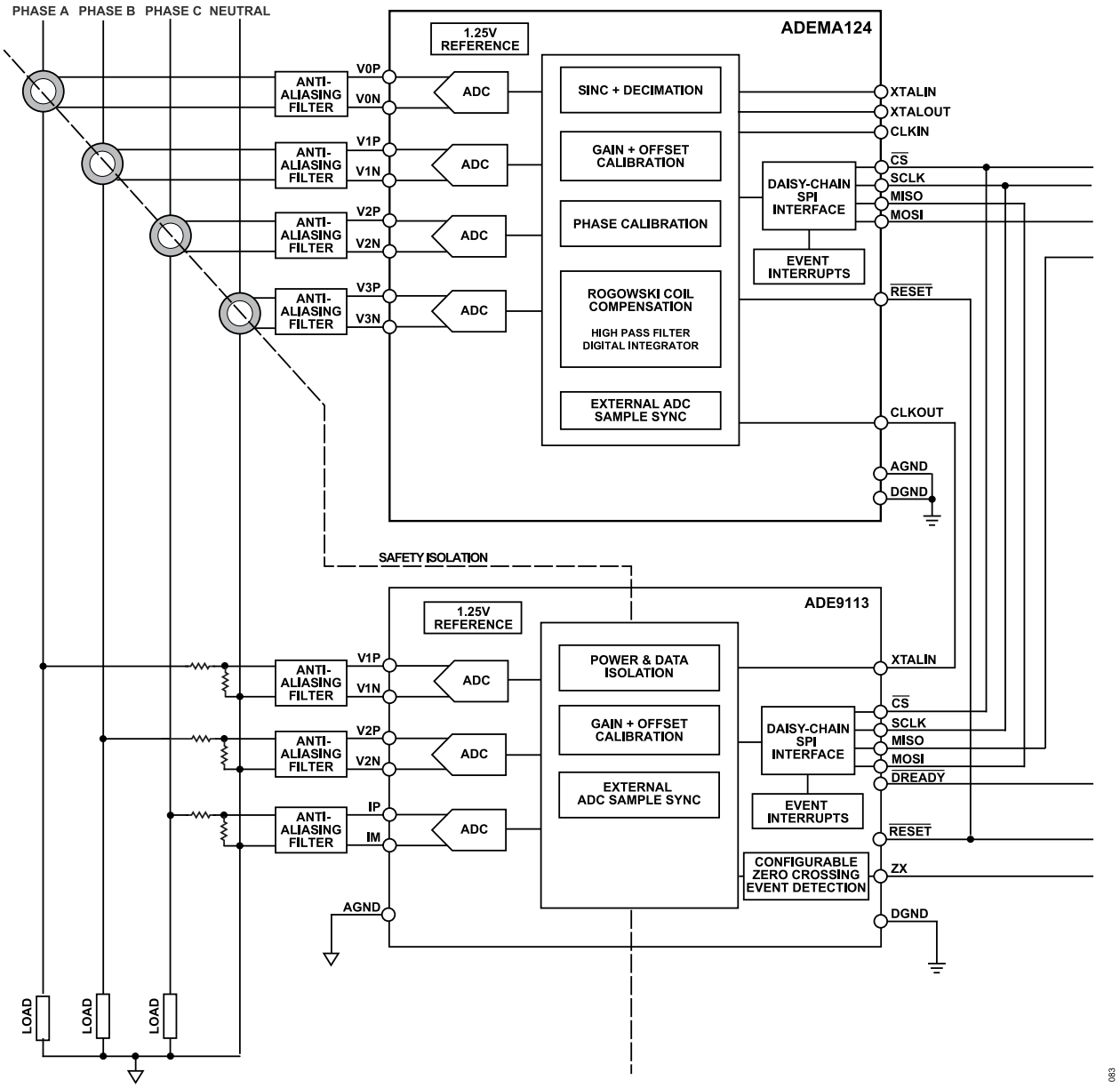


Figure 72. 3-Phase Energy Meter with Isolated Voltage Sense

APPLICATIONS INFORMATION

SPLIT PHASE ENERGY METERS

Figure 73 shows the ADEMA124 as a split phase energy meter.

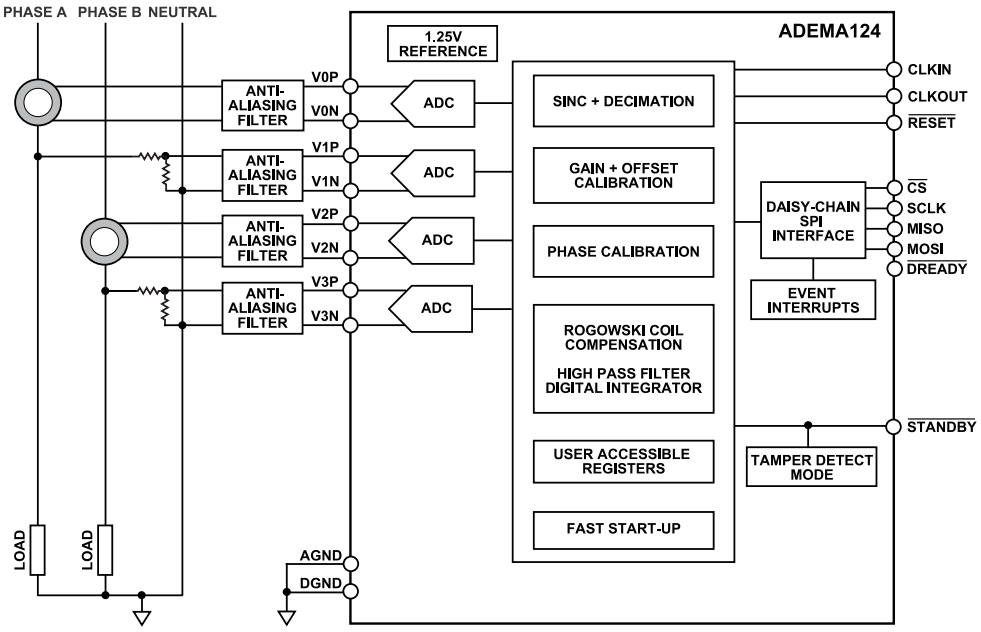


Figure 73. Split Phase Energy Meter

HARDWARE IDENTIFIERS

PRODUCT_ID register identifies the ADEMA124/ADEMA127 device.

The SILICON_REVISION register identifies the version of the ADEMA124/ADEMA127.

The UNIQUE_PART_ID_5 to UNIQUE_PART_ID_0 registers are a 48-bit unique ID number for each device, which enables traceability of all devices even after these devices are deployed.

SPI ACCESSIBLE ADDRESSES

The ADEMA124/ADEMA127 has 8-bit SPI accessible register and RAM addresses.

Table 25. Memory Map - Registers

14-Bit Address Range	Description	Notes
0x001 - 0x00F	Retained Registers. Individual register functions shown in Table 29.	Values in these registers are retained when the ADEMA124/ADEMA127 enter and exit standby mode. ADC configuration registers are write protected by the DATAPATH_CONFIG_LOCK bit. Writable registers in the space subject to the WR_LOCK bit. For more details, see the Configuration Lock and Access Bits.
0x010 - 0x07E	Registers. Individual register functions shown in Table 30.	Values in these registers are reset to the default value when the ADEMA124/ADEMA127 enter standby mode. ADC configuration registers are write protected by the DATAPATH_CONFIG_LOCK bit. Writable registers in the space subject to the WR_LOCK bit. For more details, see the Configuration Lock and Access Bits.

Table 26. Memory Map - DSP RAM

14-Bit Address Range	Description	Notes
0x401 - 0x5BB	DSP RAM. Contains DSP per channel adjustments for gain, offset, and filter coefficients. Individual register functions are shown in Table 33.	Read and write operations are protected by the DSP_MEM_ACCESS_REQ bit. For more details, see the Configuration Lock and Access Bits. Writing values to this space requires a specific order of operations. See the Configuration Procedure section.
0x5C1 - 0x623	DSP RAM. Contains DSP filter coefficients that are common to all enabled ADC channels. Individual register functions are shown in Table 34.	Read and write operations are protected by the DSP_MEM_ACCESS_REQ bit. For more details, see the Configuration Lock and Access Bits. Writing values to this space requires a specific order of operations. See the Configuration Procedure section.

REGISTER SUMMARY

Table 27. Retained MMR Summary

14-Bit Address	Name	Description	Default Value	Access
0x001	SWRST	Software Reset.	0x00	W
0x002	CONFIG0	ADC Configuration.	0xC2	R/W
0x003	TDM_STATUS	Tamper Detect Status.	0x00	R/W
0x004	ADC_PD	ADC Power Down.	0x00	R/W
0x005	ADC_CMI	ADC Input Common-Mode Configuration.	0x00	R/W
0x006	ADC_GAIN	ADC Gain Configuration.	0x00	R/W
0x007	ADC_INV	ADC Input Inversion.	0x00	R/W
0x008	CONFIG_CRC_MMR_RETAINED	Configuration of Background Retained Register Map CRC.	0x00	R/W
0x009	TDM_CONFIG	Tamper Detect Configuration.	0x80	R/W
0x00A	TDM_THRSH_MSB	Tamper Detect Threshold Most Significant Bits.	0x00	R/W
0x00B	TDM_THRSH_LSB	Tamper Detect Threshold Least Significant Bits.	0x00	R/W
0x00E	CRC_RESULT_MMR_RETAINED_HI	Background Retained Register Map CRC Most Significant Byte.	0x22	R
0x00F	CRC_RESULT_MMR_RETAINED_LO	Background Retained Register Map CRC Least Significant Byte.	0xC7	R

Note the registers in Table 28 are reset to the default value when the ADEMA124/ADEMA127 enter standby mode. For more details, see the Standby Mode section.

Table 28. MMR Summary

14-Bit Address	Name	Description	Default Value	Access
0x010	EFUSE_REFRESH	EFuse Refresh.	0x00	R/W
0x012	ACCESS_EXTENDED_MMAP	Extended Memory Map Access Control.	0x00	R/W
0x013	SCRATCH	Software Debug Register.	0x00	R/W
0x014	SYNC_SNAP	ADC Synchronization Control.	0x00	R/W
0x017	SNAPSHOT_COUNT_HI	System Timing Controller Counter.	0x00	R
0x018	SNAPSHOT_COUNT_LO	System Timing Controller Counter.	0x00	R
0x019	MASK0	High Priority Interrupt Mask.	0x00	R/W
0x01A	MASK1	Lower Priority Interrupt Mask.	0x00	R/W
0x01B	MASK2	DSP Interrupt Mask.	0x08	R/W
0x01F	WR_LOCK	Configuration Lock.	0x5E	R/W
0x020	STATUS0	Latched Status of High Priority Interrupts.	0x00	R/W
0x021	STATUS1	Latched Status of Lower Priority Interrupts.	0x00	R/W
0x022	STATUS2	DSP Status.	0x01	R/W
0x025	CONFIG_CRC_MMR	Configuration of Background Register Map CRC.	0x00	R/W
0x026	V0_WAV_HI	ADC Channel 0 Waveform Data Most Significant Byte.	0x00	R/W
0x027	V0_WAV_MD	ADC Channel 0 Waveform Data Middle Byte.	0x00	R/W
0x028	V0_WAV_LO	ADC Channel 0 Waveform Data Least Significant Byte.	0x00	R/W
0x029	V1_WAV_HI	ADC Channel 1 Waveform Data Most Significant Byte.	0x00	R/W
0x02A	V1_WAV_MD	ADC Channel 1 Waveform Data Middle Byte.	0x00	R/W
0x02B	V1_WAV_LO	ADC Channel 1 Waveform Data Least Significant Byte.	0x00	R/W
0x02C	V2_WAV_HI	ADC Channel 2 Waveform Data Most Significant Byte.	0x00	R/W
0x02D	V2_WAV_MD	ADC Channel 2 Waveform Data Middle Byte.	0x00	R/W
0x02E	V2_WAV_LO	ADC Channel 2 Waveform Data Least Significant Byte.	0x00	R/W
0x02F	V3_WAV_HI	ADC Channel 3 Waveform Data Most Significant Byte.	0x00	R/W
0x030	V3_WAV_MD	ADC Channel 3 Waveform Data Middle Byte.	0x00	R/W
0x031	V3_WAV_LO	ADC Channel 3 Waveform Data Least Significant Byte.	0x00	R/W
0x032	V4_WAV_HI	ADC Channel 4 Waveform Data Most Significant Byte.	0x00	R/W
0x033	V4_WAV_MD	ADC Channel 4 Waveform Data Middle Byte.	0x00	R/W

REGISTER SUMMARY

Table 28. MMR Summary (Continued)

14-Bit Address	Name	Description	Default Value	Access
0x034	V4_WAV_LO	ADC Channel 4 Waveform Data Least Significant Byte.	0x00	R/W
0x035	V5_WAV_HI	ADC Channel 5 Waveform Data Most Significant Byte.	0x00	R/W
0x036	V5_WAV_MD	ADC Channel 5 Waveform Data Middle Byte.	0x00	R/W
0x037	V5_WAV_LO	ADC Channel 5 Waveform Data Least Significant Byte.	0x00	R/W
0x038	V6_WAV_HI	ADC Channel 6 Waveform Data Most Significant Byte.	0x00	R/W
0x039	V6_WAV_MD	ADC Channel 6 Waveform Data Middle Byte.	0x00	R/W
0x03A	V6_WAV_LO	ADC Channel 6 Waveform Data Least Significant Byte.	0x00	R/W
0x03B	DATAPATH_CONFIG_LOCK	Datapath Configuration Lock.	0x01	R/W
0x03C	DATARATE	ADC Sample Rate and Output Data Rate Configuration.	0x31	R/W
0x03D	DATAPATH_ALPHA_CH0_1	ADC Channel 0 and 1 DC Block Filter Configuration.	0x00	R/W
0x03E	DATAPATH_ALPHA_CH2_3	ADC Channel 2 and 3 DC Block Filter Configuration.	0x00	R/W
0x03F	DATAPATH_ALPHA_CH4_5	ADC Channel 4 and 5 DC Block Filter Configuration.	0x00	R/W
0x040	DATAPATH_ALPHA_CH6	ADC Channel 6 DC Block Filter Configuration.	0x00	R/W
0x041	DATAPATH_CONFIG_CH0	ADC Channel 0 DSP Data Path Configuration.	0x00	R/W
0x042	DATAPATH_CONFIG_CH1	ADC Channel 1 DSP Data Path Configuration.	0x00	R/W
0x043	DATAPATH_CONFIG_CH2	ADC Channel 2 DSP Data Path Configuration.	0x00	R/W
0x044	DATAPATH_CONFIG_CH3	ADC Channel 3 DSP Data Path Configuration.	0x00	R/W
0x045	DATAPATH_CONFIG_CH4	ADC Channel 4 DSP Data Path Configuration.	0x00	R/W
0x046	DATAPATH_CONFIG_CH5	ADC Channel 5 DSP Data Path Configuration.	0x00	R/W
0x047	DATAPATH_CONFIG_CH6	ADC Channel 6 DSP Data Path Configuration.	0x00	R/W
0x048	PHASE_OFFSET_CH0_HI	ADC Channel 0 Phase Offset Most Significant Byte.	0x00	R/W
0x049	PHASE_OFFSET_CH0_LO	ADC Channel 0 Phase Offset Least Significant Byte.	0x00	R/W
0x04A	PHASE_OFFSET_CH1_HI	ADC Channel 1 Phase Offset Most Significant Byte.	0x00	R/W
0x04B	PHASE_OFFSET_CH1_LO	ADC Channel 1 Phase Offset Least Significant Byte.	0x00	R/W
0x04C	PHASE_OFFSET_CH2_HI	ADC Channel 2 Phase Offset Most Significant Byte.	0x00	R/W
0x04D	PHASE_OFFSET_CH2_LO	ADC Channel 2 Phase Offset Least Significant Byte.	0x00	R/W
0x04E	PHASE_OFFSET_CH3_HI	ADC Channel 3 Phase Offset Most Significant Byte.	0x00	R/W
0x04F	PHASE_OFFSET_CH3_LO	ADC Channel 3 Phase Offset Least Significant Byte.	0x00	R/W
0x050	PHASE_OFFSET_CH4_HI	ADC Channel 4 Phase Offset Most Significant Byte.	0x00	R/W
0x051	PHASE_OFFSET_CH4_LO	ADC Channel 4 Phase Offset Least Significant Byte.	0x00	R/W
0x052	PHASE_OFFSET_CH5_HI	ADC Channel 5 Phase Offset Most Significant Byte.	0x00	R/W
0x053	PHASE_OFFSET_CH5_LO	ADC Channel 5 Phase Offset Least Significant Byte.	0x00	R/W
0x054	PHASE_OFFSET_CH6_HI	ADC Channel 6 Phase Offset Most Significant Byte.	0x00	R/W
0x055	PHASE_OFFSET_CH6_LO	ADC Channel 6 Phase Offset Least Significant Byte.	0x00	R/W
0x05C	CRC_RESULT_MMR_HI	Background Register Map CRC Most Significant Byte.	0x1A	R
0x05D	CRC_RESULT_MMR_LO	Background Register Map CRC Least Significant Byte.	0x4D	R
0x075	UNIQUE_PART_ID_5	Unique Part ID.	0x00[1]	R
0x076	UNIQUE_PART_ID_4	Unique Part ID.	0x00	R
0x077	UNIQUE_PART_ID_3	Unique Part ID.	0x00	R
0x078	UNIQUE_PART_ID_2	Unique Part ID.	0x00	R
0x079	UNIQUE_PART_ID_1	Unique Part ID.	0x00	R
0x07A	UNIQUE_PART_ID_0	Unique Part ID.	0x00	R
0x07D	SILICON_REVISION	Silicon Revision.	0x01[2]	R
0x07E	PRODUCT_ID	Product Id.	0x16[3]	R

[1] The default value is unique to every individual IC.

[2] Subject to change with each silicon revision.

REGISTER SUMMARY

[3] Default value follows product version.

REGISTER DETAILS

Table 29. Retained MMR Details

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x001	SWRST	[7:0]	SWRST		Software Reset.	0x0	W
				0xD6	Software Reset Command. It resets all digital logic apart from the POR qualification counter, which is only initiated upon POR release.		
				0x00	Software Reset Register NOP.		
0x002	CONFIG0	[7:6]	ADC_POWER_MODE		ADC Modulator Power Mode. Set the ADC modulator power mode. Lower power modes result in lower accuracy ADC measurements.	0x3	R/W
				00	Quarter Power Mode. f_{MOD} ADC up to 0.512MHz supported.		
				10	Half Power Mode. f_{MOD} ADC up to 1.024MHz supported.		
				11	Full Performance Mode. f_{MOD} ADC up to 2.048MHz supported.		
		5	REF_PD_HP_REF		Power Down Bit for the Reference Core. Active high control bit. When the reference core is powered down, the buffer loses one of the PTAT bias currents. Therefore, when reference core is powered down, the buffer also needs to be powered down.	0x0	R/W
		4	REF_PD_BUFFER		Power Down Bit for the Reference Buffer. Active high control bit. When the reference core is powered down, the buffer loses one of the PTAT bias currents. Therefore, when the reference core is powered down, the buffer also needs to be powered down.	0x0	R/W
		[3:2]	STREAM_DBG		Stream Debug Mode. Stream debug mode offers the ability to change the behavior of the ADC results for the purpose of developing or verifying the communications link between the ADEMA124/ADEMA127 and the communications host.	0x0	R/W
				00	Normal Mode. x_WAV_x registers contain conversion results.		
				01	WAV Static Mode. x_WAV_x registers become static and hold their value until a register write is performed to the x_WAV_x register with a new value.		
				10	Data Increments at ADC Conversion Rate. x_WAV_x registers increment at the output data rate across the full 24 bit range, starting from the value in each register when this mode is activated.		
				11	Reserved. Same as functional mode.		
		1	CRC_EN_SPI_WRITE		Enables CRC Check on SPI Write.	0x1	R/W
		0	CLKOUT_EN		Enable Clock Output on $\overline{\text{DREADY}}$. Set this bit to 1 to enable CLKOUT when the device is providing the clock to additional ADCs. Clear this bit to 0 if receiving an external clock, in which case this pin is $\overline{\text{DREADY}}$.	0x0	R/W
0x003	TDM_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	TAMPER_DETECTED		Tamper Detect Indicator. Indicates that a tamper has been detected.	0x0	R/W1C
0x004	ADC_PD	7	RESERVED		Reserved.	0x0	R
		6	ADC_PD_CH6		ADC Channel 6 Power Down. This bit must be clear to use ADC Channel 6.	0x0	R/W
		5	ADC_PD_CH5		ADC Channel 5 Power Down. This bit must be clear to use ADC Channel 5.	0x0	R/W
		4	ADC_PD_CH4		ADC Channel 4 Power Down. This bit must be clear to use ADC Channel 4.	0x0	R/W

REGISTER DETAILS

Table 29. Retained MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	ADC_PD_CH3		ADC Channel 3 Power Down. This bit must be clear to use ADC Channel 3.	0x0	R/W
		2	ADC_PD_CH2		ADC Channel 2 Power Down. This bit must be clear to use ADC Channel 2.	0x0	R/W
		1	ADC_PD_CH1		ADC Channel 1 Power Down. This bit must be clear to use ADC Channel 1.	0x0	R/W
		0	ADC_PD_CH0		ADC Channel 0 Power Down. This bit must be clear to use ADC Channel 0.	0x0	R/W
0x005	ADC_CMI	7	RESERVED		Reserved.	0x0	R
		6	ADC_CMI_CH6		ADC Channel 6 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
		5	ADC_CMI_CH5		ADC Channel 5 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
		4	ADC_CMI_CH4		ADC Channel 4 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
		3	ADC_CMI_CH3		ADC Channel 3 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
		2	ADC_CMI_CH2		ADC Channel 2 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
		1	ADC_CMI_CH1		ADC Channel 1 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
		0	ADC_CMI_CH0		ADC Channel 0 Input Common Mode Setting.	0x0	R/W
				0	0.0V.		
				1	1.2V.		
0x006	ADC_GAIN	7	RESERVED		Reserved.	0x0	R
		6	ADC_GAIN_CH6		ADC Channel 6 Gain Setting.	0x0	R/W
				0	1.0x.		
				1	2.0x.		
		5	ADC_GAIN_CH5		ADC Channel 5 Gain Setting.	0x0	R/W
				0	1.0x.		
				1	2.0x.		
		4	ADC_GAIN_CH4		ADC Channel 4 Gain Setting.	0x0	R/W
				0	1.0x.		
				1	2.0x.		
		3	ADC_GAIN_CH3		ADC Channel 3 Gain Setting.	0x0	R/W
				0	1.0x.		
				1	2.0x.		
		2	ADC_GAIN_CH2		ADC Channel 2 Gain Setting.	0x0	R/W
				0	1.0x.		
				1	2.0x.		
		1	ADC_GAIN_CH1		ADC Channel 1 Gain Setting.	0x0	R/W
				0	1.0x.		

REGISTER DETAILS

Table 29. Retained MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1	2.0x.		
		0	ADC_GAIN_CH0		ADC Channel 0 Gain Setting.	0x0	R/W
				0	1.0x.		
				1	2.0x.		
0x007	ADC_INV	7	RESERVED		Reserved.	0x0	R
		6	ADC_INV_CH6		Invert ADC Channel 6 Inputs.	0x0	R/W
		5	ADC_INV_CH5		Invert ADC Channel 5 Inputs.	0x0	R/W
		4	ADC_INV_CH4		Invert ADC Channel 4 Inputs.	0x0	R/W
		3	ADC_INV_CH3		Invert ADC Channel 3 Inputs.	0x0	R/W
		2	ADC_INV_CH2		Invert ADC Channel 2 Inputs.	0x0	R/W
		1	ADC_INV_CH1		Invert ADC Channel 1 Inputs.	0x0	R/W
		0	ADC_INV_CH0		Invert ADC Channel 0 Inputs.	0x0	R/W
0x008	CONFIG_CRC_MMR_RETAINED	[7:2]	RESERVED		Reserved.	0x0	R
		1	CRC_DONE_MMR_RETAINED		Retained Register Map CRC Done Flag. Indicates that CRC recalculation initiated by a CRC_FORCE has completed, or that a scheduled CRC recalculation has yielded an updated CRC.	0x0	R/W1C
		0	CRC_FORCE_MMR_RETAINED		Force Background Retained Register Map CRC Recalculation. Automatically clears when CRC recalculation has completed.	0x0	R/W
0x009	TDM_CONFIG	7	TDM_DREADYB_EN		Tamper Detect $\overline{\text{DREADY}}$ Enable. Enable Tamper Detect Event interrupt via $\overline{\text{DREADY}}$ pin.	0x1	R/W
				0	TDM $\overline{\text{DREADY}}$ Disable.		
				1	TDM $\overline{\text{DREADY}}$ Enable.		
		[6:4]	TDM_LEN		Tamper Detect Duration. Time window after TDM start in which the programmed number samples must exceed the threshold to trigger a Tamper Detect Event.	0x0	R/W
				000	53ms.		
				001	106ms.		
				010	213ms.		
				011	319ms.		
				100	531ms.		
				101	744ms.		
				110	1063ms.		
				111	1488ms.		
		3	TDM_ALLCH		Tamper Detect Indication All vs. Any Channels. If set low, then a tamper indication will be triggered if any channel's tamper detect flag goes high. If set high, then a tamper indication is triggered only if all enabled channels' tamper detect flags go high.	0x0	R/W
		[2:0]	TDM_NUM		Tamper Detect Number of Samples Exceeding Threshold. Number of samples that must exceed the threshold for a Tamper Detect Event to be triggered.	0x0	R/W
				000	1.		
				001	2.		
				010	4.		
				011	8.		
				100	16.		
				101	32.		

REGISTER DETAILS

Table 29. Retained MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				110 111	64. 128.		
0x00A	TDM_THRSH_MSB	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	TDM_THRSH[11:8]		Tamper Detect Threshold. Each ADC sample is compared with threshold value to determine whether a tamper condition exist. This threshold is multiplied by 2048 and compared to the absolute value of the 24 bit ADC data value.	0x0	R/W
0x00B	TDM_THRSH_LSB	[7:0]	TDM_THRSH[7:0]		Tamper Detect Threshold. Each ADC sample is compared with threshold value to determine whether a tamper condition exist. This threshold is multiplied by 2048 and compared to the absolute value of the 24 bit ADC data value.	0x0	R/W
0x00E	CRC_RESULT_MMR_RETAINED_HI	[7:0]	CRC_RESULT_MMR_RETAINED[15:8]		Retained Register Map CRC. For more details, see the CRC Protection section.	0x22	R
0x00F	CRC_RESULT_MMR_RETAINED_LO	[7:0]	CRC_RESULT_MMR_RETAINED[7:0]		Retained Register Map CRC. For more details, see the CRC Protection section.	0xC7	R

The register block shown in Table 30 supports the ADEMA124/ADEMA127 operation in CCM. These include ADC waveform data, datapath configuration, and counters.

Note the registers shown in Table 30 are reset to the default value when the ADEMA124/ADEMA127 enter standby mode. For more details, see the Standby Mode section.

Table 30. MMR Details

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x010	EFUSE_REFRESH	[7:1]	RESERVED		Reserved.	0x0	R
		0	EFUSE_REFRESH		Forces a Refresh of EFuse Memory. This can be used as a recovery method from a EFUSE memory error without having to undertake the penalty of a reset. On completion of EFUSE refresh, this bit auto-clears and the reset_done IRQ is issued.	0x0	R/W
0x012	ACCESS_EXTENDED_MMAP	[7:1]	RESERVED		Reserved.	0x0	R
		0	DSP_MEM_ACCESS_REQ		DSP Memory Access Request from User. Set this bit high to request read and write access to the DSP memory.	0x0	R/W
0x013	SCRATCH	[7:0]	SCRATCH		Software Debug. Allows development of the SPI interface and user software by providing a user accessible register that can be read/written but has no other function.	0x0	R/W
0x014	SYNC_SNAP	[7:3]	RESERVED		Reserved.	0x0	R
		2	PREP_BROADCAST		ADC Prepare Broadcast. In a system where multiple device MISO pins are connected together, set this bit whenever also setting the ALIGN or SNAPSHOT bit during ADC synchronization. If this bit field is set high, the MISO pad drive is disconnected for the duration for the next $\overline{CS}$ low interval. This tristating of the pad allows a ADC synchronization to be performed on several chips simultaneously connected to a single SPI main. The bit clears itself back to 0 after the ADC synchronization SPI transaction to allow the SPI interface to return to normal functionality.	0x0	R/W
		1	ALIGN		ADC Align. Set this bit high via a broadcast SPI write operation, and on the next falling edge of $\overline{CS}$, all devices in the	0x0	R/W

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
					system latch internal counters to SNAPSHOT_COUNT_LO/HI and synchronize. After synchronizing, all devices sample data, simultaneously. This bit clears itself back to 0 after one f_{XTALIN} cycle.		
		0	SNAPSHOT		ADC Snapshot. Set this bit high via a broadcast SPI write operation, and on the next falling edge of $\overline{CS}$, all devices in the system latch internal counters to SNAPSHOT_COUNT_LO/HI. This bit clears itself back to 0 after one f_{XTALIN} cycle.	0x0	R/W
0x017	SNAPSHOT_COUNT_HI	[7:0]	SNAPSHOT_COUNT[15:8]		System Timing Controller Count. Snapshot value of the system timing controller counter used in synchronization operation.	0x0	R
0x018	SNAPSHOT_COUNT_LO	[7:0]	SNAPSHOT_COUNT[7:0]		System Timing Controller Count. Snapshot value of the system timing controller counter used in synchronization operation.	0x0	R
0x019	MASK0	7	STATUS1X_MASK		STATUS1X Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R
		4	CRC_CHG_MMR_RETAINED_MASK		CRC_CHG_MMR_RETAINED Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		3	CRC_CHG_MMR_MASK		CRC_CHG_MMR Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		2	RESERVED		Reserved.	0x0	R
		1	SPI_CRC_ERR_MASK		SPI_CRC_ERR Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R
0x01A	MASK1	7	V6_WAV_OVRNG_MASK		V6_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		6	V5_WAV_OVRNG_MASK		V5_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		5	V4_WAV_OVRNG_MASK		V4_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		4	V3_WAV_OVRNG_MASK		V3_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		3	V2_WAV_OVRNG_MASK		V2_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		2	V1_WAV_OVRNG_MASK		V1_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		1	V0_WAV_OVRNG_MASK		V0_WAV_OVRNG Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
		0	SYNC_SNAP_REQUESTED_MASK		SYNC_SNAP_REQUESTED Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W
0x01B	MASK2	[7:4]	RESERVED		Reserved.	0x0	R
		3	ECC_ERR_CORRECTED_MASK		ECC_ERR_CORRECTED Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x1	R/W
		[2:1]	RESERVED		Reserved.	0x0	R
		0	DSP_MEM_ACCESS_READY_MASK		DSP_MEM_ACCESS_READY Interrupt Mask. Mask high to allow interrupt source to be sent as part of SPI command response.	0x0	R/W

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01F	WR_LOCK	[7:0]	WR_LOCK		Configuration Register Write Lock. When enabled, the lock feature does not allow changes to writable registers of address ranges 0x000 to 0x01E, 0x03B to 0x05B. Also, when enabled, the lock feature does not allow changes to writable registers of address of DSP RAM (0x400 to 0x7FF). The default value is the unlock key 0x5E, write 0xD4 to enable the register write lock feature. The WR_LOCK register reads back as the lock or unlock key depending on the state.	0x5E	R/W
				0xD4	Lock Key.		
				0x5E	Unlock Key.		
0x020	STATUS0	7	STATUS1X		STATUS1 Indicator. Logical OR of the STATUS1 bit fields that have the corresponding MASK1 bit set. When this condition is satisfied STATUS1X asserts. To clear this bit field, the source driving interrupt in STATUS1 must be cleared via a W1C.	0x0	R
		6	STATUS2X		STATUS2 Indicator. Logical OR of the STATUS2 bit fields that have the corresponding MASK2 bit set. When this condition is satisfied STATUS2X asserts. To clear this bit field, the source driving interrupt in STATUS2 must be cleared via a W1C.	0x0	R
		5	RESET_DONE		Reset Done or Efuse Refresh Done. Non-maskable interrupt. The reset_done interrupt indicates that a reset or fuse refresh of the device has completed, and that the device is ready for configuration.	0x0	R/W1C
		4	CRC_CHG_MMR_RETAINED		Retained Register Map Background CRC Change Interrupt. The value of a register included in the background CRC has changed. The new CRC value is located in CRC_RESULT.	0x0	R/W1C
		3	CRC_CHG_MMR		Register Map Background CRC Change Interrupt. The value of a register included in the background CRC has changed. The new CRC value is located in CRC_RESULT.	0x0	R/W1C
		2	EFUSE_MEM_ERR		EFUSE Memory Error. EFUSE Memory Error. Non-maskable interrupt. There has been a uncorrectable error in the EFUSE memory. This bit field is not W1C and user action must be to request a EFUSE memory refresh using the EFUSE_REFRESH field. When a EFUSE_REFRESH is requested, this bit deasserts immediately. Upon completion of the EFUSE refresh sequence, this bit either stays 0 to indicate that EFUSE memory error is no longer present or may assert again to indicate a uncorrectable error in the EFUSE memory. If this condition persists, it is recommended to issue a reset.	0x0	R
		1	SPI_CRC_ERR		SPI Write CRC Error Interrupt. CRC error detected on the previous SPI command received by the device. This error bit is set on the SPI read response.	0x0	R/W1C
		0	RESERVED		Reserved.	0x0	R
0x021	STATUS1	7	V6_WAV_OVRNG		ADC Channel 6 Waveform Overrange. Channel 6 has exceeded the maximum range and the output v6_wav is clamped to +/−6606029.	0x0	R/W1C

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		6	V5_WAV_OVRNG		ADC Channel 5 Waveform Overrange. Channel 5 has exceeded the maximum range and the output v5_wav is clamped to +/−6606029.	0x0	R/W1C
		5	V4_WAV_OVRNG		ADC Channel 4 Waveform Overrange. Channel 4 has exceeded the maximum range and the output v4_wav is clamped to +/−6606029.	0x0	R/W1C
		4	V3_WAV_OVRNG		ADC Channel 3 Waveform Overrange. Channel 3 has exceeded the maximum range and the output v3_wav is clamped to +/−6606029.	0x0	R/W1C
		3	V2_WAV_OVRNG		ADC Channel 2 Waveform Overrange. Channel 2 has exceeded the maximum range and the output v2_wav is clamped to +/−6606029.	0x0	R/W1C
		2	V1_WAV_OVRNG		ADC Channel 1 Waveform Overrange. Channel 1 has exceeded the maximum range and the output v1_wav is clamped to +/−6606029.	0x0	R/W1C
		1	V0_WAV_OVRNG		ADC Channel 0 Waveform Overrange. Channel 0 has exceeded the maximum range and the output v0_wav is clamped to +/−6606029.	0x0	R/W1C
		0	SYNC_SNAP_REQUESTED		Align or Snapshot Initiated. The ALIGN or SNAPSHOT bit is set in the SYNC_SNAP register, causing a new system timing counter value to be latched in SNAPSHOT_COUNT_LO/HI.	0x0	R/W1C
0x022	STATUS2	7	DATA_RAM_ECC_ERR		DSP Data RAM Read Error.	0x0	R
		6	COEFF_RAM_ECC_ERR		DSP Coefficient RAM Read Error.	0x0	R
		5	COEFF_ROM_ECC_ERR		DSP Coefficient ROM Read Error.	0x0	R
		4	PROGRAM_ROM_ECC_ERR		DSP Program ROM Read Error.	0x0	R
		3	ECC_ERR_CORRECTED		DSP Memory Error Corrected.	0x0	R
		2	DSP_INSTRUCTION_ERR		Invalid DSP Instruction or Invalid DSP Memory Pointer.	0x0	R
		1	WATCHDOG_ERR		Watchdog Timeout Error. The DSP has stopped producing data in response to data available from the ADCs.	0x0	R/W1C
		0	DSP_MEM_ACCESS_READY		DSP Memory Access Ready from DSP to User. The DSP asserts this bit to signal that the user can read and write DSP memory.	0x1	R
0x025	CONFIG_CRC_MMR	[7:2]	RESERVED		Reserved.	0x0	R
		1	CRC_DONE_MMR		CRC Done Flag. Indicates that CRC recalculation initiated by a CRC_FORCE has completed, or that a scheduled CRC recalculation has yielded an updated CRC.	0x0	R/W1C
		0	CRC_FORCE_MMR		Force Background Register Map CRC Recalculation. Automatically clears when CRC recalculation has completed.	0x0	R/W
0x026	V0_WAV_HI	[7:0]	V0_WAV[23:16]		ADC Channel 0 Waveform Data.	0x0	R/W
0x027	V0_WAV_MD	[7:0]	V0_WAV[15:8]		ADC Channel 0 Waveform Data.	0x0	R/W
0x028	V0_WAV_LO	[7:0]	V0_WAV[7:0]		ADC Channel 0 Waveform Data.	0x0	R/W
0x029	V1_WAV_HI	[7:0]	V1_WAV[23:16]		ADC Channel 1 Waveform Data.	0x0	R/W
0x02A	V1_WAV_MD	[7:0]	V1_WAV[15:8]		ADC Channel 1 Waveform Data.	0x0	R/W
0x02B	V1_WAV_LO	[7:0]	V1_WAV[7:0]		ADC Channel 1 Waveform Data.	0x0	R/W
0x02C	V2_WAV_HI	[7:0]	V2_WAV[23:16]		ADC Channel 2 Waveform Data.	0x0	R/W
0x02D	V2_WAV_MD	[7:0]	V2_WAV[15:8]		ADC Channel 2 Waveform Data.	0x0	R/W
0x02E	V2_WAV_LO	[7:0]	V2_WAV[7:0]		ADC Channel 2 Waveform Data.	0x0	R/W
0x02F	V3_WAV_HI	[7:0]	V3_WAV[23:16]		ADC Channel 3 Waveform Data.	0x0	R/W
0x030	V3_WAV_MD	[7:0]	V3_WAV[15:8]		ADC Channel 3 Waveform Data.	0x0	R/W

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x031	V3_WAV_LO	[7:0]	V3_WAV[7:0]		ADC Channel 3 Waveform Data.	0x0	R/W
0x032	V4_WAV_HI	[7:0]	V4_WAV[23:16]		ADC Channel 4 Waveform Data.	0x0	R/W
0x033	V4_WAV_MD	[7:0]	V4_WAV[15:8]		ADC Channel 4 Waveform Data.	0x0	R/W
0x034	V4_WAV_LO	[7:0]	V4_WAV[7:0]		ADC Channel 4 Waveform Data.	0x0	R/W
0x035	V5_WAV_HI	[7:0]	V5_WAV[23:16]		ADC Channel 5 Waveform Data.	0x0	R/W
0x036	V5_WAV_MD	[7:0]	V5_WAV[15:8]		ADC Channel 5 Waveform Data.	0x0	R/W
0x037	V5_WAV_LO	[7:0]	V5_WAV[7:0]		ADC Channel 5 Waveform Data.	0x0	R/W
0x038	V6_WAV_HI	[7:0]	V6_WAV[23:16]		ADC Channel 6 Waveform Data.	0x0	R/W
0x039	V6_WAV_MD	[7:0]	V6_WAV[15:8]		ADC Channel 6 Waveform Data.	0x0	R/W
0x03A	V6_WAV_LO	[7:0]	V6_WAV[7:0]		ADC Channel 6 Waveform Data.	0x0	R/W
0x03B	DATAPATH_CONFIG_LOCK	[7:1]	RESERVED		Reserved.	0x0	R
		0	DATAPATH_CONFIG_LOCK		Datapath Configuration Lock. User must deassert this bit before attempting to write to addresses 0x03C to 0x05B inclusive.	0x1	R/W
0x03C	DATARATE	7	DSP_DECIMATION_X2		Add a Decimate by 2 in the Datapath. Halves the output sample rate, but maintains the signal bandwidth. Output Data Rate = (Input Clock Frequency)/(2^ (adc_clk_prescaler + 5 + decimation_rate + dsp_decimation_x2)).	0x0	R/W
		[6:4]	ADC_CLK_PRESCALER		ADC Clock Prescaler. This divider sets the ratio of the input clock to the ADC sampling rate. Data Rate = XTALIN/(2^ (adc_clk_prescaler + 5 + decimation_rate + dsp_decimation_x2)). For more details, see the Datapath Configuration section.	0x3	R/W
				001	Div 2.		
				010	Div 4.		
				011	Div 8.		
				100	Div 16.		
				101	Div 32.		
		[3:0]	DECIMATION_RATE		Decimation Rate. Combined with the dsp_decimation_x2 field, this divider sets the ratio of the ADC sampling rate to the output Data Rate. The divider must be set such that the output Data Rate is within the supported range. Note 1: Data Rate = XTALIN/(2^ (adc_clk_prescaler + 5 + decimation_rate + dsp_decimation_x2)). Note 2: The configuration must satisfy the following constraint: (adc_clk_prescaler + 5 + decimation_rate + dsp_decimation_x2) <=16. That is, for some extremely low output sample rates, a lower input clock frequency must be provided. For more details, see the Datapath Configuration section.	0x1	R/W
				0	Div 32.		
				1	Div 64.		
				2	Div 128.		
				3	Div 256.		
				4	Div 512.		
				5	Div 1024.		
				6	Div 2048.		

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				7	Div 4096.		
				8	Div 8192.		
0x03D	DATAPATH_ALPHA_CH0_1	[7:4]	ALPHA_CH1		DC Blocking Filter Alpha Setting for Channel 1.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
		[3:0]	ALPHA_CH0		DC Blocking Filter Alpha Setting for Channel 0.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
0x03E	DATAPATH_ALPHA_CH2_3	[7:4]	ALPHA_CH3		DC Blocking Filter Alpha Setting for Channel 3.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
		[3:0]	ALPHA_CH2		DC Blocking Filter Alpha Setting for Channel 2.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
0x03F	DATAPATH_ALPHA_CH4_5	[7:4]	ALPHA_CH5		DC Blocking Filter Alpha Setting for Channel 5.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
		[3:0]	ALPHA_CH4		DC Blocking Filter Alpha Setting for Channel 4.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
0x040	DATAPATH_ALPHA_CH6	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	ALPHA_CH6		DC Blocking Filter Alpha Setting for Channel 6.	0x0	R/W
				0000	Filter Bypassed.		
				0001	Alpha = 1/4.		
				0010	Alpha = 1/8.		
				0011	Alpha = 1/16.		
				0100	Alpha = 1/32.		
				0101	Alpha = 1/64.		
				0110	Alpha = 1/128.		
				0111	Alpha = 1/256.		
				1000	Alpha = 1/512.		
				1001	Alpha = 1/1024.		
				1010	Alpha = 1/2048.		
				1011	Alpha = 1/4096.		
				1100	Alpha = 1/8192.		
				1101	Alpha = 1/16384.		
				1110	Alpha = 1/32768.		
				1111	Alpha = 1/65536.		
0x041	DATAPATH_CONFIG_CH0	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH0		Allpass Filter Enable for Channel 0. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W
		5	LPF_EN_CH0		Low-Pass Filter Enable for Channel 0.	0x0	R/W
		4	COMP_FLT_CFG_CH0		Compensation Filter Configuration for Channel 0.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH0		Compensation Filter Enable for Channel 0.	0x0	R/W
		2	HPF_EN_CH0		High-Pass Filter Enable for Channel 0.	0x0	R/W
		1	SCF_EN_CH0		Sensor Compensation Filter Enable for Channel 0.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH0		Gain/Offset/Crosstalk Compensation Enable for Channel 0.	0x0	R/W
0x042	DATAPATH_CONFIG_CH1	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH1		Allpass Filter Enable for Channel 1. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		5	LPF_EN_CH1		Low-Pass Filter Enable for Channel 1.	0x0	R/W
		4	COMP_FLT_CFG_CH1		Compensation Filter Configuration for Channel 1.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH1		Compensation Filter Enable for Channel 1.	0x0	R/W
		2	HPF_EN_CH1		High-Pass Filter Enable for Channel 1.	0x0	R/W
		1	SCF_EN_CH1		Sensor Compensation Filter Enable for Channel 1.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH1		Gain/Offset/Crosstalk Compensation Enable for Channel 1.	0x0	R/W
0x043	DATAPATH_CONFIG_CH2	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH2		Allpass Filter Enable for Channel 2. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W
		5	LPF_EN_CH2		Low-Pass Filter Enable for Channel 2.	0x0	R/W
		4	COMP_FLT_CFG_CH2		Compensation Filter Configuration for Channel 2.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH2		Compensation Filter Enable for Channel 2.	0x0	R/W
		2	HPF_EN_CH2		High-Pass Filter Enable for Channel 2.	0x0	R/W
		1	SCF_EN_CH2		Sensor Compensation Filter Enable for Channel 2.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH2		Gain/Offset/Crosstalk Compensation Enable for Channel 2.	0x0	R/W
0x044	DATAPATH_CONFIG_CH3	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH3		Allpass Filter Enable for Channel 3. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W
		5	LPF_EN_CH3		Low-Pass Filter Enable for Channel 3.	0x0	R/W
		4	COMP_FLT_CFG_CH3		Compensation Filter Configuration for Channel 3.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH3		Compensation Filter Enable for Channel 3.	0x0	R/W
		2	HPF_EN_CH3		High-Pass Filter Enable for Channel 3.	0x0	R/W
		1	SCF_EN_CH3		Sensor Compensation Filter Enable for Channel 3.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH3		Gain/Offset/Crosstalk Compensation Enable for Channel 3.	0x0	R/W
0x045	DATAPATH_CONFIG_CH4	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH4		Allpass Filter Enable for Channel 4. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W
		5	LPF_EN_CH4		Low-Pass Filter Enable for Channel 4.	0x0	R/W
		4	COMP_FLT_CFG_CH4		Compensation Filter Configuration for Channel 4.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH4		Compensation Filter Enable for Channel 4.	0x0	R/W
		2	HPF_EN_CH4		High-Pass Filter Enable for Channel 4.	0x0	R/W

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	SCF_EN_CH4		Sensor Compensation Filter Enable for Channel 4.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH4		Gain/Offset/Crosstalk Compensation Enable for Channel 4.	0x0	R/W
0x046	DATAPATH_CONFIG_CH5	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH5		Allpass Filter Enable for Channel 5. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W
		5	LPF_EN_CH5		Low-Pass Filter Enable for Channel 5.	0x0	R/W
		4	COMP_FLT_CFG_CH5		Compensation Filter Configuration for Channel 5.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH5		Compensation Filter Enable for Channel 5.	0x0	R/W
		2	HPF_EN_CH5		High-Pass Filter Enable for Channel 5.	0x0	R/W
		1	SCF_EN_CH5		Sensor Compensation Filter Enable for Channel 5.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH5		Gain/Offset/Crosstalk Compensation Enable for Channel 5.	0x0	R/W
0x047	DATAPATH_CONFIG_CH6	7	RESERVED		Reserved.	0x0	R/W
		6	ALLPASS_EN_CH6		Allpass Filter Enable for Channel 6. All pass Filter to match the phase response of the SCF. Select either allpass_en_chx or scf_en_chx.	0x0	R/W
		5	LPF_EN_CH6		Low-Pass Filter Enable for Channel 6.	0x0	R/W
		4	COMP_FLT_CFG_CH6		Compensation Filter Configuration for Channel 6.	0x0	R/W
				0	Sinc Droop.		
				1	External BLF and Sinc Droop.		
		3	COMP_FLT_EN_CH6		Compensation Filter Enable for Channel 6.	0x0	R/W
		2	HPF_EN_CH6		High-Pass Filter Enable for Channel 6.	0x0	R/W
		1	SCF_EN_CH6		Sensor Compensation Filter Enable for Channel 6.	0x0	R/W
		0	GAIN_OFFSET_XT_EN_CH6		Gain/Offset/Crosstalk Compensation Enable for Channel 6.	0x0	R/W
0x048	PHASE_OFFSET_CH0_HI	[7:0]	PHASE_OFFSET_CH0[15:8]		Phase Offset for Channel 0. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x049	PHASE_OFFSET_CH0_LO	[7:0]	PHASE_OFFSET_CH0[7:0]		Phase Offset for Channel 0. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x04A	PHASE_OFFSET_CH1_HI	[7:0]	PHASE_OFFSET_CH1[15:8]		Phase Offset for Channel 1. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x04B	PHASE_OFFSET_CH1_LO	[7:0]	PHASE_OFFSET_CH1[7:0]		Phase Offset for Channel 1. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x04C	PHASE_OFFSET_CH2_HI	[7:0]	PHASE_OFFSET_CH2[15:8]		Phase Offset for Channel 2. Phase offset compensation in units of fractional sample period with a maximum of 1 sample	0x0	R/W

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
					period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.		
0x04D	PHASE_OFFSET_CH2_LO	[7:0]	PHASE_OFFSET_CH2[7:0]		Phase Offset for Channel 2. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x04E	PHASE_OFFSET_CH3_HI	[7:0]	PHASE_OFFSET_CH3[15:8]		Phase Offset for Channel 3. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x04F	PHASE_OFFSET_CH3_LO	[7:0]	PHASE_OFFSET_CH3[7:0]		Phase Offset for Channel 3. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x050	PHASE_OFFSET_CH4_HI	[7:0]	PHASE_OFFSET_CH4[15:8]		Phase Offset for Channel 4. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x051	PHASE_OFFSET_CH4_LO	[7:0]	PHASE_OFFSET_CH4[7:0]		Phase Offset for Channel 4. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x052	PHASE_OFFSET_CH5_HI	[7:0]	PHASE_OFFSET_CH5[15:8]		Phase Offset for Channel 5. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x053	PHASE_OFFSET_CH5_LO	[7:0]	PHASE_OFFSET_CH5[7:0]		Phase Offset for Channel 5. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x054	PHASE_OFFSET_CH6_HI	[7:0]	PHASE_OFFSET_CH6[15:8]		Phase Offset for Channel 6. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x055	PHASE_OFFSET_CH6_LO	[7:0]	PHASE_OFFSET_CH6[7:0]		Phase Offset for Channel 6. Phase offset compensation in units of fractional sample period with a maximum of 1 sample period delay. Format is fixed-point with 13 fractional bits and a maximum value of 0x1FFF, the 3MSBs are not used.	0x0	R/W
0x05C	CRC_RESULT_MMR_HI	[7:0]	CRC_RESULT_MMR[15:8]		Register Map CRC. For more details, see the CRC Protection section.	0x1A	R
0x05D	CRC_RESULT_MMR_LO	[7:0]	CRC_RESULT_MMR[7:0]		Register Map CRC. For more details, see the CRC Protection section.	0x4D	R
0x075	UNIQUE_PART_ID_5	[7:0]	UNIQUE_PART_ID[47:40]		Unique Part ID.	0x0	R
0x076	UNIQUE_PART_ID_4	[7:0]	UNIQUE_PART_ID[39:32]		Unique Part ID.	0x0	R
0x077	UNIQUE_PART_ID_3	[7:0]	UNIQUE_PART_ID[31:24]		Unique Part ID.	0x0	R
0x078	UNIQUE_PART_ID_2	[7:0]	UNIQUE_PART_ID[23:16]		Unique Part ID.	0x0	R
0x079	UNIQUE_PART_ID_1	[7:0]	UNIQUE_PART_ID[15:8]		Unique Part ID.	0x0	R
0x07A	UNIQUE_PART_ID_0	[7:0]	UNIQUE_PART_ID[7:0]		Unique Part ID.	0x0	R

REGISTER DETAILS

Table 30. MMR Details (Continued)

14-Bit Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x07D	SILICON_REVISION	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	SILICON_REVISION		Silicon Revision for the Chip.	0x1	R
0x07E	PRODUCT_ID	[7:0]	PRODUCT_ID		Product ID.	0x16	R
				0x16	7-Channel ADEMA127 ADC.		
				0x13	4-Channel ADEMA124 ADC.		

DSP RAM SUMMARY

The DSP RAM bit fields are read and write protected by default by the DSP_MEM_ACCESS_REQ bit. Default values are loaded from ROM to the DSP RAM based on configured DSP options and the DECIMATION_RATE register setting.

For the DSP RAM update procedure, see the Configuration Lock and Access Bits and Configuration Procedure sections.

Table 31. DSP RAM Summary - Independent Per ADC Channel

14-Bit Address										
CH0	CH1	CH2	CH3	CH4	CH5	CH6	Name	Description	Default Value	Access
0x401	0x441	0x481	0x4C1	0x501	0x541	0x581	COMP_COEFF_B0_LO	Compensation Coefficient B0 Least Significant Byte.	0xXX	R/W
0x402	0x442	0x482	0x4C2	0x502	0x542	0x582	COMP_COEFF_B0_MD	Compensation Coefficient B0 Middle Byte.	0xXX	R/W
0x403	0x443	0x483	0x4C3	0x503	0x543	0x583	COMP_COEFF_B0_HI	Compensation Coefficient B0 Most Significant Byte.	0xXX	R/W
0x405	0x445	0x485	0x4C5	0x505	0x545	0x585	COMP_COEFF_B1_LO	Compensation Coefficient B1 Least Significant Byte.	0xXX	R/W
0x406	0x446	0x486	0x4C6	0x506	0x546	0x586	COMP_COEFF_B1_MD	Compensation Coefficient B1 Middle Byte.	0xXX	R/W
0x407	0x447	0x487	0x4C7	0x507	0x547	0x587	COMP_COEFF_B1_HI	Compensation Coefficient B1 Most Significant Byte.	0xXX	R/W
0x409	0x449	0x489	0x4C9	0x509	0x549	0x589	COMP_COEFF_B2_LO	Compensation Coefficient B2 Least Significant Byte.	0xXX	R/W
0x40A	0x44A	0x48A	0x4CA	0x50A	0x54A	0x58A	COMP_COEFF_B2_MD	Compensation Coefficient B2 Middle Byte.	0xXX	R/W
0x40B	0x44B	0x48B	0x4CB	0x50B	0x54B	0x58B	COMP_COEFF_B2_HI	Compensation Coefficient B2 Most Significant Byte.	0xXX	R/W
0x40D	0x44D	0x48D	0x4CD	0x50D	0x54D	0x58D	COMP_COEFF_B3_LO	Compensation Coefficient B3 Least Significant Byte.	0xXX	R/W
0x40E	0x44E	0x48E	0x4CE	0x50E	0x54E	0x58E	COMP_COEFF_B3_MD	Compensation Coefficient B3 Middle Byte.	0xXX	R/W
0x40F	0x44F	0x48F	0x4CF	0x50F	0x54F	0x58F	COMP_COEFF_B3_HI	Compensation Coefficient B3 Most Significant Byte.	0xXX	R/W
0x411	0x451	0x491	0x4D1	0x511	0x551	0x591	COMP_COEFF_B4_LO	Compensation Coefficient B4 Least Significant Byte.	0xXX	R/W
0x412	0x452	0x492	0x4D2	0x512	0x552	0x592	COMP_COEFF_B4_MD	Compensation Coefficient B4 Middle Byte.	0xXX	R/W
0x413	0x453	0x493	0x4D3	0x513	0x553	0x593	COMP_COEFF_B4_HI	Compensation Coefficient B4 Most Significant Byte.	0xXX	R/W
0x41D	0x45D	0x49D	0x4DD	0x51D	0x55D	0x59D	SHIFT	Arithmetic Shift in Datapath.	0xXX	R/W
0x421	0x461	0x4A1	0x4E1	0x521	0x561	0x5A1	GAIN_LO	Channel Gain Least Significant Byte.	0xXX	R/W
0x422	0x462	0x4A2	0x4E2	0x522	0x562	0x5A2	GAIN_MD	Channel Gain Middle Byte.	0xXX	R/W
0x423	0x463	0x4A3	0x4E3	0x523	0x563	0x5A3	GAIN_HI	Channel Gain Most Significant Byte.	0xXX	R/W
0x425	0x465	0x4A5	0x4E5	0x525	0x565	0x5A5	OFFSET_LO	Channel Offset Least Significant Byte.	0xXX	R/W
0x426	0x466	0x4A6	0x4E6	0x526	0x566	0x5A6	OFFSET_MD	Channel Offset Middle Byte.	0xXX	R/W
0x427	0x467	0x4A7	0x4E7	0x527	0x567	0x5A7	OFFSET_HI	Channel Offset Most Significant Byte.	0xXX	R/W
0x429	0x469	0x4A9	0x4E9	0x529	0x569	0x5A9	XT_GAIN_LO	Crosstalk Compensation Gain Least Significant Byte.	0xXX	R/W
0x42A	0x46A	0x4AA	0x4EA	0x52A	0x56A	0x5AA	XT_GAIN_MD	Crosstalk Compensation Gain Middle Byte.	0xXX	R/W
0x42B	0x46B	0x4AB	0x4EB	0x52B	0x56B	0x5AB	XT_GAIN_HI	Crosstalk Compensation Gain Most Significant Byte.	0xXX	R/W
0x42D	0x46D	0x4AD	0x4ED	0x52D	0x56D	0x5AD	XT_AGGRESSOR	Crosstalk Compensation Aggressor.	0xXX	R/W
0x431	0x471	0x4B1	0x4F1	0x531	0x571	0x5B1	SCF_APF_COEFF_B0_LO	Sensor Compensation/All Pass Coefficient B0 Least Significant Byte.	0xXX	R/W
0x432	0x472	0x4B2	0x4F2	0x532	0x572	0x5B2	SCF_APF_COEFF_B0_MD	Sensor Compensation/All Pass Coefficient B0 Middle Byte.	0xXX	R/W
0x433	0x473	0x4B3	0x4F3	0x533	0x573	0x5B3	SCF_APF_COEFF_B0_HI	Sensor Compensation/All Pass Coefficient B0 Most Significant Byte.	0xXX	R/W

DSP RAM SUMMARY

Table 31. DSP RAM Summary - Independent Per ADC Channel (Continued)

14-Bit Address							Name	Description	Default Value	Access
CH0	CH1	CH2	CH3	CH4	CH5	CH6				
0x435	0x475	0x4B5	0x4F5	0x535	0x575	0x5B5	SCF_APF_COEFF_B1_LO	Sensor Compensation/All Pass Coefficient B0 Least Significant Byte.	0xXX	R/W
0x436	0x476	0x4B6	0x4F6	0x536	0x576	0x5B6	SCF_APF_COEFF_B1_MD	Sensor Compensation/All Pass Coefficient B0 Middle Byte.	0xXX	R/W
0x437	0x477	0x4B7	0x4F7	0x537	0x577	0x5B7	SCF_APF_COEFF_B1_HI	Sensor Compensation/All Pass Coefficient B0 Most Significant Byte.	0xXX	R/W
0x439	0x479	0x4B9	0x4F9	0x539	0x579	0x5B9	SCF_APF_COEFF_A1_LO	Sensor Compensation/All Pass Coefficient A1 Least Significant Byte.	0xXX	R/W
0x43A	0x47A	0x4BA	0x4FA	0x53A	0x57A	0x5BA	SCF_APF_COEFF_A1_MD	Sensor Compensation/All Pass Coefficient A1 Middle Byte.	0xXX	R/W
0x43B	0x47B	0x4BB	0x4FB	0x53B	0x57B	0x5BB	SCF_APF_COEFF_A1_HI	Sensor Compensation/All Pass Coefficient A1 Most Significant Byte.	0xXX	R/W

Table 32. DSP RAM Summary - Common for all ADC Channels

14-Bit Address	Name	Description	Default Value	Access
0x5C1	LPF_COEFF_B0_LO	Low-Pass Filter Coefficient B0 Least Significant Byte.	0x00	R/W
0x5C2	LPF_COEFF_B0_MD	Low-Pass Filter Coefficient B0 Middle Byte.	0x00	R/W
0x5C3	LPF_COEFF_B0_HI	Low-Pass Filter Coefficient B0 Most Significant Byte.	0x00	R/W
0x5C5	LPF_COEFF_B1_LO	Low-Pass Filter Coefficient B1 Least Significant Byte.	0x00	R/W
0x5C6	LPF_COEFF_B1_MD	Low-Pass Filter Coefficient B1 Middle Byte.	0x00	R/W
0x5C7	LPF_COEFF_B1_HI	Low-Pass Filter Coefficient B1 Most Significant Byte.	0x00	R/W
0x5C9	LPF_COEFF_B2_LO	Low-Pass Filter Coefficient B2 Least Significant Byte.	0x00	R/W
0x5CA	LPF_COEFF_B2_MD	Low-Pass Filter Coefficient B2 Middle Byte.	0x00	R/W
0x5CB	LPF_COEFF_B2_HI	Low-Pass Filter Coefficient B2 Most Significant Byte.	0x00	R/W
0x5CD	LPF_COEFF_B3_LO	Low-Pass Filter Coefficient B3 Least Significant Byte.	0x00	R/W
0x5CE	LPF_COEFF_B3_MD	Low-Pass Filter Coefficient B3 Middle Byte.	0x00	R/W
0x5CF	LPF_COEFF_B3_HI	Low-Pass Filter Coefficient B3 Most Significant Byte.	0x00	R/W
0x5D1	LPF_COEFF_B4_LO	Low-Pass Filter Coefficient B4 Least Significant Byte.	0x00	R/W
0x5D2	LPF_COEFF_B4_MD	Low-Pass Filter Coefficient B4 Middle Byte.	0x00	R/W
0x5D3	LPF_COEFF_B4_HI	Low-Pass Filter Coefficient B4 Most Significant Byte.	0x00	R/W
0x5D5	LPF_COEFF_B5_LO	Low-Pass Filter Coefficient B5 Least Significant Byte.	0x00	R/W
0x5D6	LPF_COEFF_B5_MD	Low-Pass Filter Coefficient B5 Middle Byte.	0x00	R/W
0x5D7	LPF_COEFF_B5_HI	Low-Pass Filter Coefficient B5 Most Significant Byte.	0x00	R/W
0x5D9	LPF_COEFF_B6_LO	Low-Pass Filter Coefficient B6 Least Significant Byte.	0x00	R/W
0x5DA	LPF_COEFF_B6_MD	Low-Pass Filter Coefficient B6 Middle Byte.	0x00	R/W
0x5DB	LPF_COEFF_B6_HI	Low-Pass Filter Coefficient B6 Most Significant Byte.	0x00	R/W
0x5DD	LPF_COEFF_B7_LO	Low-Pass Filter Coefficient B7 Least Significant Byte.	0x00	R/W
0x5DE	LPF_COEFF_B7_MD	Low-Pass Filter Coefficient B7 Middle Byte.	0x00	R/W
0x5DF	LPF_COEFF_B7_HI	Low-Pass Filter Coefficient B7 Most Significant Byte.	0x00	R/W
0x5E1	LPF_COEFF_B8_LO	Low-Pass Filter Coefficient B8 Least Significant Byte.	0x00	R/W
0x5E2	LPF_COEFF_B8_MD	Low-Pass Filter Coefficient B8 Middle Byte.	0x00	R/W
0x5E3	LPF_COEFF_B8_HI	Low-Pass Filter Coefficient B8 Most Significant Byte.	0x00	R/W
0x5E5	LPF_COEFF_B9_LO	Low-Pass Filter Coefficient B9 Least Significant Byte.	0x00	R/W
0x5E6	LPF_COEFF_B9_MD	Low-Pass Filter Coefficient B9 Middle Byte.	0x00	R/W
0x5E7	LPF_COEFF_B9_HI	Low-Pass Filter Coefficient B9 Most Significant Byte.	0x00	R/W
0x5E9	LPF_COEFF_B10_LO	Low-Pass Filter Coefficient B10 Least Significant Byte.	0x00	R/W
0x5EA	LPF_COEFF_B10_MD	Low-Pass Filter Coefficient B10 Middle Byte.	0x00	R/W

DSP RAM SUMMARY

Table 32. DSP RAM Summary - Common for all ADC Channels (Continued)

14-Bit Address	Name	Description	Default Value	Access
0x5EB	LPF_COEFF_B10_HI	Low-Pass Filter Coefficient B10 Most Significant Byte.	0x00	R/W
0x5ED	LPF_COEFF_B11_LO	Low-Pass Filter Coefficient B11 Least Significant Byte.	0x00	R/W
0x5EE	LPF_COEFF_B11_MD	Low-Pass Filter Coefficient B11 Middle Byte.	0x00	R/W
0x5EF	LPF_COEFF_B11_HI	Low-Pass Filter Coefficient B11 Most Significant Byte.	0x00	R/W
0x5F1	LPF_COEFF_B12_LO	Low-Pass Filter Coefficient B12 Least Significant Byte.	0x00	R/W
0x5F2	LPF_COEFF_B12_MD	Low-Pass Filter Coefficient B12 Middle Byte.	0x00	R/W
0x5F3	LPF_COEFF_B12_HI	Low-Pass Filter Coefficient B12 Most Significant Byte.	0x00	R/W
0x5F5	LPF_COEFF_B13_LO	Low-Pass Filter Coefficient B13 Least Significant Byte.	0x00	R/W
0x5F6	LPF_COEFF_B13_MD	Low-Pass Filter Coefficient B13 Middle Byte.	0x00	R/W
0x5F7	LPF_COEFF_B13_HI	Low-Pass Filter Coefficient B13 Most Significant Byte.	0x00	R/W
0x5F9	LPF_COEFF_B14_LO	Low-Pass Filter Coefficient B14 Least Significant Byte.	0x00	R/W
0x5FA	LPF_COEFF_B14_MD	Low-Pass Filter Coefficient B14 Middle Byte.	0x00	R/W
0x5FB	LPF_COEFF_B14_HI	Low-Pass Filter Coefficient B14 Most Significant Byte.	0x00	R/W
0x5FD	LPF_COEFF_B15_LO	Low-Pass Filter Coefficient B15 Least Significant Byte.	0x00	R/W
0x5FE	LPF_COEFF_B15_MD	Low-Pass Filter Coefficient B15 Middle Byte.	0x00	R/W
0x5FF	LPF_COEFF_B15_HI	Low-Pass Filter Coefficient B15 Most Significant Byte.	0x00	R/W
0x601	LPF_COEFF_B16_LO	Low-Pass Filter Coefficient B16 Least Significant Byte.	0x00	R/W
0x602	LPF_COEFF_B16_MD	Low-Pass Filter Coefficient B16 Middle Byte.	0x00	R/W
0x603	LPF_COEFF_B16_HI	Low-Pass Filter Coefficient B16 Most Significant Byte.	0x00	R/W
0x605	LPF_COEFF_B17_LO	Low-Pass Filter Coefficient B17 Least Significant Byte.	0x00	R/W
0x606	LPF_COEFF_B17_MD	Low-Pass Filter Coefficient B17 Middle Byte.	0x00	R/W
0x607	LPF_COEFF_B17_HI	Low-Pass Filter Coefficient B17 Most Significant Byte.	0x00	R/W
0x609	HPF_COEFF_B0_LO	High-Pass Filter Coefficient B0 Least Significant Byte.	0x00	R/W
0x60A	HPF_COEFF_B0_MD	High-Pass Filter Coefficient B0 Middle Byte.	0x00	R/W
0x60B	HPF_COEFF_B0_HI	High-Pass Filter Coefficient B0 Most Significant Byte.	0x00	R/W
0x60D	HPF_COEFF_B1_LO	High-Pass Filter Coefficient B1 Least Significant Byte.	0x00	R/W
0x60E	HPF_COEFF_B1_MD	High-Pass Filter Coefficient B1 Middle Byte.	0x00	R/W
0x60F	HPF_COEFF_B1_HI	High-Pass Filter Coefficient B1 Most Significant Byte.	0x00	R/W
0x611	HPF_COEFF_B2_LO	High-Pass Filter Coefficient B2 Least Significant Byte.	0x00	R/W
0x612	HPF_COEFF_B2_MD	High-Pass Filter Coefficient B2 Middle Byte.	0x00	R/W
0x613	HPF_COEFF_B2_HI	High-Pass Filter Coefficient B2 Most Significant Byte.	0x00	R/W
0x615	HPF_COEFF_A1_0	High-Pass Filter Coefficient A1 Byte 0.	0x00	R/W
0x616	HPF_COEFF_A1_1	High-Pass Filter Coefficient A1 Byte 1.	0x00	R/W
0x617	HPF_COEFF_A1_2	High-Pass Filter Coefficient A1 Byte 2.	0x00	R/W
0x619	HPF_COEFF_A1_3	High-Pass Filter Coefficient A1 Byte 3.	0x00	R/W
0x61A	HPF_COEFF_A1_4	High-Pass Filter Coefficient A1 Byte 4.	0x00	R/W
0x61B	HPF_COEFF_A1_5	High-Pass Filter Coefficient A1 Byte 5.	0x00	R/W
0x61D	HPF_COEFF_A2_0	High-Pass Filter Coefficient A2 Byte 0.	0x00	R/W
0x61E	HPF_COEFF_A2_1	High-Pass Filter Coefficient A2 Byte 1.	0x00	R/W
0x61F	HPF_COEFF_A2_2	High-Pass Filter Coefficient A2 Byte 2.	0x00	R/W
0x621	HPF_COEFF_A2_3	High-Pass Filter Coefficient A2 Byte 3.	0x00	R/W
0x622	HPF_COEFF_A2_4	High-Pass Filter Coefficient A2 Byte 4.	0x00	R/W
0x623	HPF_COEFF_A2_5	High-Pass Filter Coefficient A2 Byte 5.	0x00	R/W

DSP RAM DETAILS

The DSP RAM bit fields are read and write protected by default by the DSP_MEM_ACCESS_REQ bit. Default values are loaded from ROM to the DSP RAM based on configured DSP options and the DECIMATION_RATE register setting.

For the DSP RAM update procedure, see the Configuration Lock and Access Bits and Configuration Procedure sections.

Table 33. DSP RAM Details - Independent Per ADC Channel

14-Bit Address												
CH0	CH1	CH2	CH3	CH4	CH5	CH6	Name	Bits	Bit Name	Description	Reset[1]	Access
0x401	0x441	0x481	0x4C1	0x501	0x541	0x581	COMP_COEFF_B0_LO	[7:0]	COMP_COEFF_B0[7:0]	Compensation Filter Coefficient B0.	0xX	R/W
0x402	0x442	0x482	0x4C2	0x502	0x542	0x582	COMP_COEFF_B0_MD	[7:0]	COMP_COEFF_B0[15:8]	Compensation Filter Coefficient B0.	0xX	R/W
0x403	0x443	0x483	0x4C3	0x503	0x543	0x583	COMP_COEFF_B0_HI	[7:0]	COMP_COEFF_B0[23:16]	Compensation Filter Coefficient B0.	0xX	R/W
0x405	0x445	0x485	0x4C5	0x505	0x545	0x585	COMP_COEFF_B1_LO	[7:0]	COMP_COEFF_B1[7:0]	Compensation Filter Coefficient B1.	0xX	R/W
0x406	0x446	0x486	0x4C6	0x506	0x546	0x586	COMP_COEFF_B1_MD	[7:0]	COMP_COEFF_B1[15:8]	Compensation Filter Coefficient B1.	0xX	R/W
0x407	0x447	0x487	0x4C7	0x507	0x547	0x587	COMP_COEFF_B1_HI	[7:0]	COMP_COEFF_B1[23:16]	Compensation Filter Coefficient B1.	0xX	R/W
0x409	0x449	0x489	0x4C9	0x509	0x549	0x589	COMP_COEFF_B2_LO	[7:0]	COMP_COEFF_B2[7:0]	Compensation Filter Coefficient B2.	0xX	R/W
0x40A	0x44A	0x48A	0x4CA	0x50A	0x54A	0x58A	COMP_COEFF_B2_MD	[7:0]	COMP_COEFF_B2[15:8]	Compensation Filter Coefficient B2.	0xX	R/W
0x40B	0x44B	0x48B	0x4CB	0x50B	0x54B	0x58B	COMP_COEFF_B2_HI	[7:0]	COMP_COEFF_B2[23:16]	Compensation Filter Coefficient B2.	0xX	R/W
0x40D	0x44D	0x48D	0x4CD	0x50D	0x54D	0x58D	COMP_COEFF_B3_LO	[7:0]	COMP_COEFF_B3[7:0]	Compensation Filter Coefficient B3.	0xX	R/W
0x40E	0x44E	0x48E	0x4CE	0x50E	0x54E	0x58E	COMP_COEFF_B3_MD	[7:0]	COMP_COEFF_B3[15:8]	Compensation Filter Coefficient B3.	0xX	R/W
0x40F	0x44F	0x48F	0x4CF	0x50F	0x54F	0x58F	COMP_COEFF_B3_HI	[7:0]	COMP_COEFF_B3[23:16]	Compensation Filter Coefficient B3.	0xX	R/W
0x411	0x451	0x491	0x4D1	0x511	0x551	0x591	COMP_COEFF_B4_LO	[7:0]	COMP_COEFF_B4[7:0]	Compensation Filter Coefficient B4.	0xX	R/W
0x412	0x452	0x492	0x4D2	0x512	0x552	0x592	COMP_COEFF_B4_MD	[7:0]	COMP_COEFF_B4[15:8]	Compensation Filter Coefficient B4.	0xX	R/W
0x413	0x453	0x493	0x4D3	0x513	0x553	0x593	COMP_COEFF_B4_HI	[7:0]	COMP_COEFF_B4[23:16]	Compensation Filter Coefficient B4.	0xX	R/W
0x41D	0x45D	0x49D	0x4DD	0x51D	0x55D	0x59D	SHIFT	[7:3]	RESERVED	Reserved.	0xX	R
								[2:0]	SHIFT	Arithmetic Shift in Datapath. Arithmetic shift applied to the datapath, at the output of the SCF.	0xX	R/W
0x421	0x461	0x4A1	0x4E1	0x521	0x561	0x5A1	GAIN_LO	[7:0]	GAIN[7:0]	Channel Gain. Signed 2.22 Format.	0xX	R/W
0x422	0x462	0x4A2	0x4E2	0x522	0x562	0x5A2	GAIN_MD	[7:0]	GAIN[15:8]	Channel Gain. Signed 2.22 Format.	0xX	R/W
0x423	0x463	0x4A3	0x4E3	0x523	0x563	0x5A3	GAIN_HI	[7:0]	GAIN[23:16]	Channel Gain. Signed 2.22 Format.	0xX	R/W
0x425	0x465	0x4A5	0x4E5	0x525	0x565	0x5A5	OFFSET_LO	[7:0]	OFFSET[7:0]	Signed static offset subtracted from the channel. Offset format is the same as the	0xX	R/W

DSP RAM DETAILS

Table 33. DSP RAM Details - Independent Per ADC Channel (Continued)

14-Bit Address							Name	Bits	Bit Name	Description	Reset[1]	Access
CH0	CH1	CH2	CH3	CH4	CH5	CH6						
										ADC channel waveform data.		
0x426	0x466	0x4A6	0x4E6	0x526	0x566	0x5A6	OFFSET_MD	[7:0]	OFFSET[15:8]	Signed static offset subtracted from the channel. Offset format is the same as the ADC channel waveform data.	0xX	R/W
0x427	0x467	0x4A7	0x4E7	0x527	0x567	0x5A7	OFFSET_HI	[7:0]	OFFSET[23:16]	Signed static offset subtracted from the channel. Offset format is the same as the ADC channel waveform data.	0xX	R/W
0x429	0x469	0x4A9	0x4E9	0x529	0x569	0x5A9	XT_GAIN_LO	[7:0]	XT_GAIN[7:0]	Crosstalk Compensation Gain. Signed 2.22 Format. Crosstalk Compensation adds channel[xt_aggressor] × xt_gain to the channel. To subtract, the xt_gain should be negative.	0xX	R/W
0x42A	0x46A	0x4AA	0x4EA	0x52A	0x56A	0x5AA	XT_GAIN_MD	[7:0]	XT_GAIN[15:8]	Crosstalk Compensation Gain. Signed 2.22 Format. Crosstalk Compensation adds channel[xt_aggressor] × xt_gain to the channel. To subtract, the xt_gain should be negative.	0xX	R/W
0x42B	0x46B	0x4AB	0x4EB	0x52B	0x56B	0x5AB	XT_GAIN_HI	[7:0]	XT_GAIN[23:16]	Crosstalk Compensation Gain. Signed 2.22 Format. Crosstalk Compensation adds channel[xt_aggressor] × xt_gain to the channel. To subtract, the xt_gain should be negative.	0xX	R/W
0x42D	0x46D	0x4AD	0x4ED	0x52D	0x56D	0x5AD	XT_AGGRESSOR	[7:6]	RESERVED	Reserved.	0xX	R
								5	XT_COMP_EN	Crosstalk Compensation Enable.	0xX	R/W
								[4:3]	RESERVED	Reserved.	0xX	R
								[2:0]	XT_AGGRESSOR	Crosstalk Compensation Aggressor. Select the	0xX	R/W

DSP RAM DETAILS

Table 33. DSP RAM Details - Independent Per ADC Channel (Continued)

14-Bit Address							Name	Bits	Bit Name	Description	Reset[1]	Access
CH0	CH1	CH2	CH3	CH4	CH5	CH6						
										channel number of the aggressor, which is added to the channel for electrostatic compensation.		
0x431	0x471	0x4B1	0x4F1	0x531	0x571	0x5B1	SCF_APF_COEFF_B0_LO	[7:0]	SCF_APF_COEFF_B0[7:0]	Sensor Compensation Filter Coefficient B0.	0xX	R/W
0x432	0x472	0x4B2	0x4F2	0x532	0x572	0x5B2	SCF_APF_COEFF_B0_MD	[7:0]	SCF_APF_COEFF_B0[15:8]	Sensor Compensation Filter Coefficient B0.	0xX	R/W
0x433	0x473	0x4B3	0x4F3	0x533	0x573	0x5B3	SCF_APF_COEFF_B0_HI	[7:0]	SCF_APF_COEFF_B0[23:16]	Sensor Compensation Filter Coefficient B0.	0xX	R/W
0x435	0x475	0x4B5	0x4F5	0x535	0x575	0x5B5	SCF_APF_COEFF_B1_LO	[7:0]	SCF_APF_COEFF_B1[7:0]	Sensor Compensation Filter Coefficient B0.	0xX	R/W
0x436	0x476	0x4B6	0x4F6	0x536	0x576	0x5B6	SCF_APF_COEFF_B1_MD	[7:0]	SCF_APF_COEFF_B1[15:8]	Sensor Compensation Filter Coefficient B0.	0xX	R/W
0x437	0x477	0x4B7	0x4F7	0x537	0x577	0x5B7	SCF_APF_COEFF_B1_HI	[7:0]	SCF_APF_COEFF_B1[23:16]	Sensor Compensation Filter Coefficient B0.	0xX	R/W
0x439	0x479	0x4B9	0x4F9	0x539	0x579	0x5B9	SCF_APF_COEFF_A1_LO	[7:0]	SCF_APF_COEFF_A1[7:0]	Sensor Compensation Filter Coefficient A1.	0xX	R/W
0x43A	0x47A	0x4BA	0x4FA	0x53A	0x57A	0x5BA	SCF_APF_COEFF_A1_MD	[7:0]	SCF_APF_COEFF_A1[15:8]	Sensor Compensation Filter Coefficient A1.	0xX	R/W
0x43B	0x47B	0x4BB	0x4FB	0x53B	0x57B	0x5BB	SCF_APF_COEFF_A1_HI	[7:0]	SCF_APF_COEFF_A1[23:16]	Sensor Compensation Filter Coefficient A1.	0xX	R/W

[1] Register values updated from ROM when corresponding DSP filter is enabled.

Table 34. DSP RAM Details - Common for all ADC Channels

14-Bit Address	Name	Bits	Bit Name	Description	Reset	Access
0x5C1	LPF_COEFF_B0_LO	[7:0]	LPF_COEFF_B0[7:0]	Low-Pass Filter Coefficient B0.	0x0	R/W
0x5C2	LPF_COEFF_B0_MD	[7:0]	LPF_COEFF_B0[15:8]	Low-Pass Filter Coefficient B0.	0x0	R/W
0x5C3	LPF_COEFF_B0_HI	[7:0]	LPF_COEFF_B0[23:16]	Low-Pass Filter Coefficient B0.	0x0	R/W
0x5C5	LPF_COEFF_B1_LO	[7:0]	LPF_COEFF_B1[7:0]	Low-Pass Filter Coefficient B1.	0x0	R/W
0x5C6	LPF_COEFF_B1_MD	[7:0]	LPF_COEFF_B1[15:8]	Low-Pass Filter Coefficient B1.	0x0	R/W
0x5C7	LPF_COEFF_B1_HI	[7:0]	LPF_COEFF_B1[23:16]	Low-Pass Filter Coefficient B1.	0x0	R/W
0x5C9	LPF_COEFF_B2_LO	[7:0]	LPF_COEFF_B2[7:0]	Low-Pass Filter Coefficient B2.	0x0	R/W
0x5CA	LPF_COEFF_B2_MD	[7:0]	LPF_COEFF_B2[15:8]	Low-Pass Filter Coefficient B2.	0x0	R/W
0x5CB	LPF_COEFF_B2_HI	[7:0]	LPF_COEFF_B2[23:16]	Low-Pass Filter Coefficient B2.	0x0	R/W
0x5CD	LPF_COEFF_B3_LO	[7:0]	LPF_COEFF_B3[7:0]	Low-Pass Filter Coefficient B3.	0x0	R/W
0x5CE	LPF_COEFF_B3_MD	[7:0]	LPF_COEFF_B3[15:8]	Low-Pass Filter Coefficient B3.	0x0	R/W
0x5CF	LPF_COEFF_B3_HI	[7:0]	LPF_COEFF_B3[23:16]	Low-Pass Filter Coefficient B3.	0x0	R/W
0x5D1	LPF_COEFF_B4_LO	[7:0]	LPF_COEFF_B4[7:0]	Low-Pass Filter Coefficient B4.	0x0	R/W
0x5D2	LPF_COEFF_B4_MD	[7:0]	LPF_COEFF_B4[15:8]	Low-Pass Filter Coefficient B4.	0x0	R/W
0x5D3	LPF_COEFF_B4_HI	[7:0]	LPF_COEFF_B4[23:16]	Low-Pass Filter Coefficient B4.	0x0	R/W
0x5D5	LPF_COEFF_B5_LO	[7:0]	LPF_COEFF_B5[7:0]	Low-Pass Filter Coefficient B5.	0x0	R/W
0x5D6	LPF_COEFF_B5_MD	[7:0]	LPF_COEFF_B5[15:8]	Low-Pass Filter Coefficient B5.	0x0	R/W
0x5D7	LPF_COEFF_B5_HI	[7:0]	LPF_COEFF_B5[23:16]	Low-Pass Filter Coefficient B5.	0x0	R/W
0x5D9	LPF_COEFF_B6_LO	[7:0]	LPF_COEFF_B6[7:0]	Low-Pass Filter Coefficient B6.	0x0	R/W
0x5DA	LPF_COEFF_B6_MD	[7:0]	LPF_COEFF_B6[15:8]	Low-Pass Filter Coefficient B6.	0x0	R/W
0x5DB	LPF_COEFF_B6_HI	[7:0]	LPF_COEFF_B6[23:16]	Low-Pass Filter Coefficient B6.	0x0	R/W

DSP RAM DETAILS

Table 34. DSP RAM Details - Common for all ADC Channels (Continued)

14-Bit Address	Name	Bits	Bit Name	Description	Reset	Access
0x5DD	LPF_COEFF_B7_LO	[7:0]	LPF_COEFF_B7[7:0]	Low-Pass Filter Coefficient B7.	0x0	R/W
0x5DE	LPF_COEFF_B7_MD	[7:0]	LPF_COEFF_B7[15:8]	Low-Pass Filter Coefficient B7.	0x0	R/W
0x5DF	LPF_COEFF_B7_HI	[7:0]	LPF_COEFF_B7[23:16]	Low-Pass Filter Coefficient B7.	0x0	R/W
0x5E1	LPF_COEFF_B8_LO	[7:0]	LPF_COEFF_B8[7:0]	Low-Pass Filter Coefficient B8.	0x0	R/W
0x5E2	LPF_COEFF_B8_MD	[7:0]	LPF_COEFF_B8[15:8]	Low-Pass Filter Coefficient B8.	0x0	R/W
0x5E3	LPF_COEFF_B8_HI	[7:0]	LPF_COEFF_B8[23:16]	Low-Pass Filter Coefficient B8.	0x0	R/W
0x5E5	LPF_COEFF_B9_LO	[7:0]	LPF_COEFF_B9[7:0]	Low-Pass Filter Coefficient B9.	0x0	R/W
0x5E6	LPF_COEFF_B9_MD	[7:0]	LPF_COEFF_B9[15:8]	Low-Pass Filter Coefficient B9.	0x0	R/W
0x5E7	LPF_COEFF_B9_HI	[7:0]	LPF_COEFF_B9[23:16]	Low-Pass Filter Coefficient B9.	0x0	R/W
0x5E9	LPF_COEFF_B10_LO	[7:0]	LPF_COEFF_B10[7:0]	Low-Pass Filter Coefficient B10.	0x0	R/W
0x5EA	LPF_COEFF_B10_MD	[7:0]	LPF_COEFF_B10[15:8]	Low-Pass Filter Coefficient B10.	0x0	R/W
0x5EB	LPF_COEFF_B10_HI	[7:0]	LPF_COEFF_B10[23:16]	Low-Pass Filter Coefficient B10.	0x0	R/W
0x5ED	LPF_COEFF_B11_LO	[7:0]	LPF_COEFF_B11[7:0]	Low-Pass Filter Coefficient B11.	0x0	R/W
0x5EE	LPF_COEFF_B11_MD	[7:0]	LPF_COEFF_B11[15:8]	Low-Pass Filter Coefficient B11.	0x0	R/W
0x5EF	LPF_COEFF_B11_HI	[7:0]	LPF_COEFF_B11[23:16]	Low-Pass Filter Coefficient B11.	0x0	R/W
0x5F1	LPF_COEFF_B12_LO	[7:0]	LPF_COEFF_B12[7:0]	Low-Pass Filter Coefficient B12.	0x0	R/W
0x5F2	LPF_COEFF_B12_MD	[7:0]	LPF_COEFF_B12[15:8]	Low-Pass Filter Coefficient B12.	0x0	R/W
0x5F3	LPF_COEFF_B12_HI	[7:0]	LPF_COEFF_B12[23:16]	Low-Pass Filter Coefficient B12.	0x0	R/W
0x5F5	LPF_COEFF_B13_LO	[7:0]	LPF_COEFF_B13[7:0]	Low-Pass Filter Coefficient B13.	0x0	R/W
0x5F6	LPF_COEFF_B13_MD	[7:0]	LPF_COEFF_B13[15:8]	Low-Pass Filter Coefficient B13.	0x0	R/W
0x5F7	LPF_COEFF_B13_HI	[7:0]	LPF_COEFF_B13[23:16]	Low-Pass Filter Coefficient B13.	0x0	R/W
0x5F9	LPF_COEFF_B14_LO	[7:0]	LPF_COEFF_B14[7:0]	Low-Pass Filter Coefficient B14.	0x0	R/W
0x5FA	LPF_COEFF_B14_MD	[7:0]	LPF_COEFF_B14[15:8]	Low-Pass Filter Coefficient B14.	0x0	R/W
0x5FB	LPF_COEFF_B14_HI	[7:0]	LPF_COEFF_B14[23:16]	Low-Pass Filter Coefficient B14.	0x0	R/W
0x5FD	LPF_COEFF_B15_LO	[7:0]	LPF_COEFF_B15[7:0]	Low-Pass Filter Coefficient B15.	0x0	R/W
0x5FE	LPF_COEFF_B15_MD	[7:0]	LPF_COEFF_B15[15:8]	Low-Pass Filter Coefficient B15.	0x0	R/W
0x5FF	LPF_COEFF_B15_HI	[7:0]	LPF_COEFF_B15[23:16]	Low-Pass Filter Coefficient B15.	0x0	R/W
0x601	LPF_COEFF_B16_LO	[7:0]	LPF_COEFF_B16[7:0]	Low-Pass Filter Coefficient B16.	0x0	R/W
0x602	LPF_COEFF_B16_MD	[7:0]	LPF_COEFF_B16[15:8]	Low-Pass Filter Coefficient B16.	0x0	R/W
0x603	LPF_COEFF_B16_HI	[7:0]	LPF_COEFF_B16[23:16]	Low-Pass Filter Coefficient B16.	0x0	R/W
0x605	LPF_COEFF_B17_LO	[7:0]	LPF_COEFF_B17[7:0]	Low-Pass Filter Coefficient B17.	0x0	R/W
0x606	LPF_COEFF_B17_MD	[7:0]	LPF_COEFF_B17[15:8]	Low-Pass Filter Coefficient B17.	0x0	R/W
0x607	LPF_COEFF_B17_HI	[7:0]	LPF_COEFF_B17[23:16]	Low-Pass Filter Coefficient B17.	0x0	R/W
0x609	HPF_COEFF_B0_LO	[7:0]	HPF_COEFF_B0[7:0]	High-Pass Filter Coefficient B0.	0x0	R/W
0x60A	HPF_COEFF_B0_MD	[7:0]	HPF_COEFF_B0[15:8]	High-Pass Filter Coefficient B0.	0x0	R/W
0x60B	HPF_COEFF_B0_HI	[7:0]	HPF_COEFF_B0[23:16]	High-Pass Filter Coefficient B0.	0x0	R/W
0x60D	HPF_COEFF_B1_LO	[7:0]	HPF_COEFF_B1[7:0]	High-Pass Filter Coefficient B1.	0x0	R/W
0x60E	HPF_COEFF_B1_MD	[7:0]	HPF_COEFF_B1[15:8]	High-Pass Filter Coefficient B1.	0x0	R/W
0x60F	HPF_COEFF_B1_HI	[7:0]	HPF_COEFF_B1[23:16]	High-Pass Filter Coefficient B1.	0x0	R/W
0x611	HPF_COEFF_B2_LO	[7:0]	HPF_COEFF_B2[7:0]	High-Pass Filter Coefficient B2.	0x0	R/W
0x612	HPF_COEFF_B2_MD	[7:0]	HPF_COEFF_B2[15:8]	High-Pass Filter Coefficient B2.	0x0	R/W
0x613	HPF_COEFF_B2_HI	[7:0]	HPF_COEFF_B2[23:16]	High-Pass Filter Coefficient B2.	0x0	R/W
0x615	HPF_COEFF_A1_0	[7:0]	HPF_COEFF_A1[7:0]	High-Pass Filter Coefficient A1 (Double Precision).	0x0	R/W
0x616	HPF_COEFF_A1_1	[7:0]	HPF_COEFF_A1[15:8]	High-Pass Filter Coefficient A1 (Double Precision).	0x0	R/W

DSP RAM DETAILS

Table 34. DSP RAM Details - Common for all ADC Channels (Continued)

14-Bit Address	Name	Bits	Bit Name	Description	Reset	Access
0x617	HPF_COEFF_A1_2	[7:0]	HPF_COEFF_A1[23:16]	High-Pass Filter Coefficient A1 (Double Precision).	0x0	R/W
0x619	HPF_COEFF_A1_3	[7:0]	HPF_COEFF_A1[31:24]	High-Pass Filter Coefficient A1 (Double Precision).	0x0	R/W
0x61A	HPF_COEFF_A1_4	[7:0]	HPF_COEFF_A1[39:32]	High-Pass Filter Coefficient A1 (Double Precision).	0x0	R/W
0x61B	HPF_COEFF_A1_5	[7:0]	HPF_COEFF_A1[47:40]	High-Pass Filter Coefficient A1 (Double Precision).	0x0	R/W
0x61D	HPF_COEFF_A2_0	[7:0]	HPF_COEFF_A2[7:0]	High-Pass Filter Coefficient A2 (Double Precision).	0x0	R/W
0x61E	HPF_COEFF_A2_1	[7:0]	HPF_COEFF_A2[15:8]	High-Pass Filter Coefficient A2 (Double Precision).	0x0	R/W
0x61F	HPF_COEFF_A2_2	[7:0]	HPF_COEFF_A2[23:16]	High-Pass Filter Coefficient A2 (Double Precision).	0x0	R/W
0x621	HPF_COEFF_A2_3	[7:0]	HPF_COEFF_A2[31:24]	High-Pass Filter Coefficient A2 (Double Precision).	0x0	R/W
0x622	HPF_COEFF_A2_4	[7:0]	HPF_COEFF_A2[39:32]	High-Pass Filter Coefficient A2 (Double Precision).	0x0	R/W
0x623	HPF_COEFF_A2_5	[7:0]	HPF_COEFF_A2[47:40]	High-Pass Filter Coefficient A2 (Double Precision).	0x0	R/W

OUTLINE DIMENSIONS

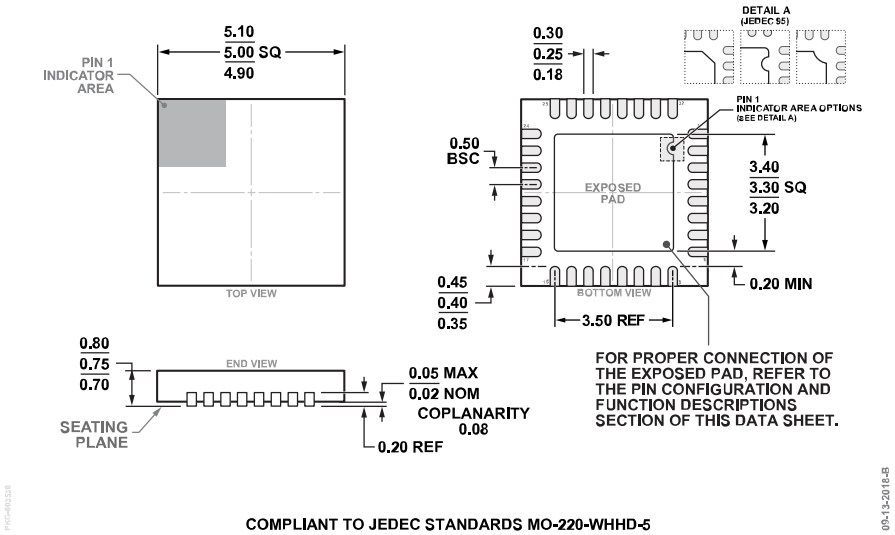


Figure 74. 32-Lead Lead Frame Chip-Scale Package [LFCSP]
5mm × 5mm Body and 0.75mm Package Height
(CP-32-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADEMA124ACPZ	−40°C to +125°C	32-Lead [LFCSP] (5mm × 5mm × 0.75mm)	Tray, 490	CP-32-20
ADEMA124ACPZ-RL	−40°C to +125°C	32-Lead [LFCSP] (5mm × 5mm × 0.75mm)	Reel, 5000	CP-32-20
ADEMA124ACPZ-RL7	−40°C to +125°C	32-Lead [LFCSP] (5mm × 5mm × 0.75mm)	Reel7, 1500	CP-32-20
ADEMA127ACPZ	−40°C to +125°C	32-Lead [LFCSP] (5mm × 5mm × 0.75mm)	Tray, 490	CP-32-20
ADEMA127ACPZ-RL	−40°C to +125°C	32-Lead [LFCSP] (5mm × 5mm × 0.75mm)	Reel, 5000	CP-32-20
ADEMA127ACPZ-RL7	−40°C to +125°C	32-Lead [LFCSP] (5mm × 5mm × 0.75mm)	Reel7, 1500	CP-32-20

[1] Z = RoHS Compliant Part.

Updated: July 25, 2025

EVALUATION BOARDS

Evaluation Board[1]	Description
EVAL-ADEMA127KTZ	Evaluation Board

[1] Z = RoHS Compliant Part.