0.5 GHz to 19 GHz, 1-Channel, Bidirectional True Time Delay Unit

FEATURES

- 0.5 GHz to 19 GHz frequency range
- Programmable 7-bit time delay
- Programmable time delay range (typical)
  - Range 0: 0 ps to 508 ps with 4 ps standard resolution
  - Range 1: 0 ps to 254 ps with 2 ps high resolution
- Programmable 6-bit attenuation
  - 31.5 dB adjustment range
  - 0.5 dB resolution
- Performance at 10 GHz for minimum time delay and attenuation
  - Insertion loss
    - Time Delay Range 0: −20.5 dB
    - Time Delay Range 1: −16.2 dB
  - Input IP3
    - Time Delay Range 0: 15.2 dBm
    - Time Delay Range 1: 14.1 dBm
  - Input P1dB
    - Time Delay Range 0: 5 dBm
    - Time Delay Range 1: 4.1 dBm
  - Noise figure
    - Time Delay Range 0: 21.2 dB
    - Time Delay Range 1: 16.6 dB
- Fully programmable via a 3-wire or 4-wire SPI
- 14-bit shift register for daisy chaining and quick data load
- Power consumption: 1 mW with 1.2 V and 1.0 V dual supplies
- 14-lead, 3 mm × 2 mm, LFCSP

APPLICATIONS

- Electronic steerable antenna arrays
- Multifunction arrays
- Satellite communications (SATCOM)
- Radar
- Data links
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

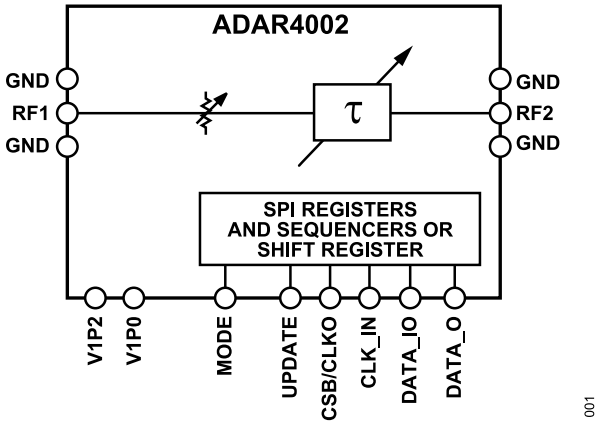

Figure 1. ADAR4002 Block Diagram

GENERAL DESCRIPTION

The ADAR4002 is a low power broadband, bidirectional, single-channel, true time delay unit (TDU) and a digital step attenuator (DSA). The IC has 18.5 GHz of bandwidth over a frequency range of 0.5 GHz to 19 GHz with 50 Ω input impedance at both RF ports. The TDU has two programmable maximum time delays, each with 7-bit control. Range 0 has a maximum delay of 508 ps with a resolution of 4 ps (typical). This range is used at lower frequencies where the ADAR4002 has less insertion loss and where more time delay is required for full 360° phase coverage. Range 1 has a maximum delay of 254 ps and a resolution of 2 ps (typical). This range has less insertion loss compared to Range 0 and is useful at higher frequencies where the ADAR4002 has higher insertion loss, and where less time delay and smaller resolution are required. The DSA has 6-bit resolution with an attenuation range of 0 dB to 31.5 dB and a step size of 0.5 dB.

The ADAR4002 is designed to provide flexible digital control through either a serial port interface (SPI) or a shift register to allow daisy chaining multiple chips together. The ADAR4002 contains register memory for 32 TDU and DSA states. The memory combined with on-chip sequencers, allows a fast bidirectional memory advance via the UPDATE pin.

The ADAR4002 is available in a 14-lead, 2 mm x 3 mm, LFCSP and is specified from −40°C to +85°C.

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REVISION HISTORY

6/2025—Revision A: Initial Version

SPECIFICATIONS

V1P2 = 1.2 V, V1P0 = 1.0 V, T_A = 25°C, frequency = 10 GHz, TDU code = 0, and DSA code = 0, unless otherwise specified. Input second-order intercept (IP2) has 1 GHz tone spacing. Input third-order intercept (IP3) has 10 MHz tone spacing. Low-side tone reported for IP2. Port 1 = RF1 and Port 2 = RF2. Gain is S21, and reverse gain is S12.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Minimum Frequency			500		MHz
Maximum Frequency			19		GHz
Operating Temperature		−40		+85	°C
RF SECTION	RF1 and RF2				
DC Bias Voltage			0[1]		V
Insertion Loss					
Time Delay Range 0	500 MHz		−11.5		dB
	2 GHz		−12.6		dB
	10 GHz		−20.5		dB
	18 GHz		−30.8		dB
Time Delay Range 1	500 MHz		−9.3		dB
	2 GHz		−10.1		dB
	10 GHz		−16.2		dB
	18 GHz		−22.9		dB
Attenuation Range	2 GHz, either time delay range		31.5		dB
Attenuation Resolution			0.5		dB
Gain Flatness vs. Frequency	From 2 GHz to 18 GHz, across any 500 MHz bandwidth				
	Time Delay Range 0		≤1.2		dB
	Time Delay Range 1		≤0.8		dB
Gain Variation vs. Temperature	10 GHz				dB
	Time Delay Range 0		+1.6/−2		dB
	Time Delay Range 1		+1.6/−1.8		dB
RMS Gain Error[2]					
Time Delay Range 0					
500 MHz	DSA Sweep 0 to 15.5 dB		0.25		dB
	DSA Sweep 0 to 31.5 dB		0.2		dB
2 GHz	DSA Sweep 0 to 15.5 dB		0.11		dB
	DSA Sweep 0 to 31.5 dB		0.28		dB
10 GHz	DSA Sweep 0 to 15.5 dB		0.11		dB
	DSA Sweep 0 to 31.5 dB		1.45		dB
18 GHz	DSA Sweep 0 to 15.5 dB		0.77		dB
	DSA Sweep 0 to 31.5 dB		3.16		dB
Time Delay Range 1					
500 MHz	DSA Sweep 0 to 15.5 dB		0.3		dB
	DSA Sweep 0 to 31.5 dB		0.23		dB
2 GHz	DSA Sweep 0 to 15.5 dB		0.16		dB
	DSA Sweep 0 to 31.5 dB		0.24		dB
10 GHz	DSA Sweep 0 to 15.5 dB		0.08		dB
	DSA Sweep 0 to 31.5 dB		1.3		dB
18 GHz	DSA Sweep 0 to 15.5 dB		0.32		dB
	DSA Sweep 0 to 31.5 dB		3.4		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RMS Gain Variation					
Time Delay Range 0					
500 MHz	TDU Sweep 0 to 127		1.45		dB
2 GHz	TDU Sweep 0 to 127		0.72		dB
10 GHz	TDU Sweep 0 to 127		1.43		dB
18 GHz	TDU Sweep 0 to 127		1.52		dB
Time Delay Range 1					
500 MHz	TDU Sweep 0 to 127		0.98		dB
2 GHz	TDU Sweep 0 to 127		0.53		dB
10 GHz	TDU Sweep 0 to 127		0.46		dB
18 GHz	TDU Sweep 0 to 127		1.12		dB
Time Delay Adjustment Range					
Time Delay Range 0					
Time Delay	500 MHz		543.5		ps
	2 GHz		512.5		ps
	10 GHz		531.2		ps
	18 GHz		516.3		ps
Phase[3]	500 MHz		97.83		Degrees
	2 GHz		369		Degrees
	10 GHz		1921.32		Degrees
	18 GHz		3345.6		Degrees
Time Delay Range 1					
Time Delay	500 MHz		276.2		ps
	2 GHz		254.7		ps
	10 GHz		264.8		ps
	18 GHz		260.9		ps
Phase	500 MHz		49.7		Degrees
	2 GHz		183.4		Degrees
	10 GHz		953.3		Degrees
	18 GHz		1690.6		Degrees
Time Delay Resolution					
Time Delay Range 0					
Time Delay	500 MHz		4		ps
	2 GHz		4		ps
	10 GHz		4.15		ps
	18 GHz		4.06		ps
Phase	500 MHz		0.72		Degrees
	2 GHz		2.88		Degrees
	10 GHz		14.4		Degrees
	18 GHz		25.92		Degrees
Time Delay Range 1					
Time Delay	500 MHz		2		ps
	2 GHz		2		ps
	10 GHz		2.1		ps
	18 GHz		2.1		ps
Phase	500 MHz		0.36		Degrees
	2 GHz		1.44		Degrees
	10 GHz		7.2		Degrees
	18 GHz		12.96		Degrees

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RMS Time Delay Error[4]					
Time Delay Range 0					
500 MHz	TDU Sweep 0 to TDU Sweep 127		22.59		ps
2 GHz	TDU Sweep 0 to TDU Sweep 127		2.58		ps
10 GHz	TDU Sweep 0 to TDU Sweep 127		13.68		ps
18 GHz	TDU Sweep 0 to TDU Sweep 127		4.83		ps
Time Delay Range 1					
500 MHz	TDU Sweep 0 to TDU Sweep 127		14.56		ps
2 GHz	TDU Sweep 0 to TDU Sweep 127		1.15		ps
10 GHz	TDU Sweep 0 to TDU Sweep 127		7.1		ps
18 GHz	TDU Sweep 0 to TDU Sweep 127		4.04		ps
RMS Time Delay Variation					
Time Delay Range 0					
500 MHz	DSA sweep, 0 dB to 15.5 dB		2.62		ps
	DSA sweep, 0 dB to 31.5 dB		3.52		ps
2 GHz	DSA sweep, 0 dB to 15.5 dB		0.84		ps
	DSA sweep, 0 dB to 31.5 dB		4.1		ps
10 GHz	DSA sweep, 0 dB to 15.5 dB		0.65		ps
	DSA sweep, 0 dB to 31.5 dB		2.95		ps
18 GHz	DSA sweep, 0 dB to 15.5 dB		0.89		ps
	DSA sweep, 0 dB to 31.5 dB		8.97		ps
Time Delay Range 1					
500 MHz	DSA sweep, 0 dB to 15.5 dB		2.41		ps
	DSA sweep, 0 dB to 31.5 dB		3.34		ps
2 GHz	DSA sweep, 0 dB to 15.5 dB		0.94		ps
	DSA sweep, 0 dB to 31.5 dB		4.28		ps
10 GHz	DSA sweep, 0 dB to 15.5 dB		0.57		ps
	DSA sweep, 0 dB to 31.5 dB		3.4		ps
18 GHz	DSA sweep, 0 dB to 15.5 dB		0.57		ps
	DSA sweep, 0 dB to 31.5 dB		4.46		ps
Noise Figure[5]					
Time Delay Range 0	500 MHz		11.4		dB
	2 GHz		12.77		dB
	10 GHz		21.2		dB
	18 GHz		32		dB
Time Delay Range 1	500 MHz		9.1		dB
	2 GHz		10.4		dB
	10 GHz		16.6		dB
	18 GHz		24.4		dB
Input Return Loss	RF1				
Time Delay Range 0	500 MHz		−13.5		dB
	2 GHz		−20.2		dB
	10 GHz		−10.4		dB
	18 GHz		−14.7		dB
Time Delay Range 1	500 MHz		−13.3		dB
	2 GHz		−20.7		dB
	10 GHz		−10.1		dB
	18 GHz		−14.1		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Return Loss	RF2				
Time Delay Range 0	500 MHz		−10.9		dB
	2 GHz		−12.6		dB
	10 GHz		−13.2		dB
	18 GHz		−25.4		dB
Time Delay Range 1	500 MHz		−11.2		dB
	2 GHz		−12.4		dB
	10 GHz		−13.4		dB
	18 GHz		−25.2		dB
Input Third-Order Intercept (IP3)	RF1				
Time Delay Range 0	500 MHz		8.6		dBm
	2 GHz		10.6		dBm
	10 GHz		15.2		dBm
	18 GHz		16.4		dBm
Time Delay Range 1	500 MHz		7.7		dBm
	2 GHz		9.4		dBm
	10 GHz		14.1		dBm
	18 GHz		16.4		dBm
Input 1 dB Compression (P1dB)	RF1				
Time Delay Range 0	500 MHz		0.05		dBm
	2 GHz		1.7		dBm
	10 GHz		5		dBm
	18 GHz		6.4		dBm
Time Delay Range 1	500 MHz		−0.08		dBm
	2 GHz		0.52		dBm
	10 GHz		4.1		dBm
	18 GHz		6.0		dBm
DSA Settling Time	From 90% of active edge to 10% of RF output, 500 MHz, from DSA Code 0 to DSA Code 63		≤10		ns
TDU Settling Time	From 90% of active edge to 90% of RF output, 500 MHz, from TDU Code 0 to TDU Code 127		≤20		ns
LOGIC INPUTS[6]	CSB/CLKO, CLK_IN, DATA_IO, MODE, and UPDATE pins				
Input Voltage					
High, V_{IH}		0.75[7]			V
	Maximum operating value[8]			1.2	V
Low, V_{IL}				0.18[9]	V
	Minimum operating value [10]	−0.5			V
High and Low Input Currents, I_{INH}, I_{INL}	0 V ≤ input voltage ≤ 1 V, 25°C		±1		µA
Input Capacitance, C_{IN}			1		pF
LOGIC OUTPUTS[11]	DATA_IO, DATA_O, CSB/CLKO				
Output Voltage					
High, V_{OH}	No load		V1P0		V
	Output high current (I_{OH}) = −5 mA	V1P0 − 0.25			V
Low, V_{OL}	No load		0		V
	Output low current (I_{OL}) = 5 mA			0.27	V
POWER SUPPLIES					
V1P2		1.1	1.2	1.3	V
V1P0		0.9	1.0	1.1	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
I_{V1P2}	Quiescent, SPI mode				
DSA = 0, TDU = 0	Time Delay Range 0		0.2		mA
DSA = 63, TDU = 127	Time Delay Range 0		0.5		mA
DSA = 0, TDU = 0	Time Delay Range 1		0.175		mA
DSA = 63, TDU = 127	Time Delay Range 1		0.525		mA
I_{V1P0}	Quiescent, SPI mode				
DSA = 0, TDU = 0	Time Delay Range 0		0.45		mA
DSA = 63, TDU = 127	Time Delay Range 0		0.62		mA
DSA = 0, TDU = 0	Time Delay Range 1		0.45		mA
DSA = 63, TDU = 127	Time Delay Range 1		0.625		mA
DSA = 0, TDU = 0	Quiescent, shift register mode		0.6		mA
DSA = 0, TDU = 0	100 MHz clock, shift register mode		2.38		mA
Power Consumption	Quiescent		1		mW

[1] AC coupling required if the DC bias of the connected devices differs from this value.

[2] The RMS attenuation error is computed with reference to the TDU and DSA in a minimum time delay and attenuation setting.

[3] Phase (f) = f × 360 × TD, where f is the frequency in Hz, and TD is the time delay in seconds. Phase has a unit of degrees.

[4] The RMS time delay error is computed with reference to the TDU and DSA in a minimum time delay and attenuation setting.

[5] Noise Figure = Output Noise Spectral Density (NSD) − Gain − Input NSD, Input NSD = −174 dBm/Hz.

[6] Inputs have at least 140 mV of hysteresis.

[7] All voltages more than this value guaranteed high.

[8] Voltages more than this value sink appreciable current into the pin, which is not recommended for operational use.

[9] All voltages less than this value guaranteed low.

[10] Voltages less than this value can cause damage to the device.

[11] Digital output pins have a 25 Ω series resistor internally in the driver pad that limits the current flow.

SPECIFICATIONS

TIMING SPECIFICATIONS

V1P2 = 1.2 V, V1P0 = 1.0 V, and T_A = 25°C, unless otherwise noted. See Figure 3, Figure 4, Figure 5, and Figure 8 for the supporting timing figures.

Table 2. SPI Timing

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Maximum Clock Rate ($1/t_{CLK\_IN}$)			100	MHz	
Minimum Clock Period (t_{CLK_IN})	10			ns	
Minimum Pulse Width High (t_{PWH})[1]	4			ns	
Minimum Pulse Width Low (t_{PWL})[1]	4			ns	
Minimum Setup Time, DATA_IO to CLK_IN (t_{DS})		2.5		ns	
Minimum Hold Time, DATA_IO to CLK_IN (t_{DH})		1		ns	
Data Valid, CLK_IN to DATA_O (t_{DV})		2		ns	
Setup Time, CSB_CLKO to CLK_IN (t_{DCS})		5		ns	
DATA_IO and DATA_O Rise Time (t_R)		1		ns	Outputs loaded with 80 pF, 10% to 90%
Minimum Clock to Update ($t_{CLK\_IN-UPDATE}$)		10		ns	
Minimum CSB_CLKO to Update ($t_{CSB\_CLKO-UPDATE}$)		10		ns	
Minimum Update to Update ($t_{UPDATE-UPDATE}$)		10		ns	
Minimum Update Pulse width (t_{UPW})		5		ns	
RF Settling Time (t_{RF_SETTLE})		20		ns	TDU settling time between TDU code = 0 to TDU code = 127

[1] Clock Period = Pulse Width High + Pulse Width Low; however, Minimum Clock Period cannot equal Minimum Pulse Width High + Minimum Pulse Width Low, which allows for the SPI signals that are not 50% duty cycle. The extreme example is if the pulse width high = 4 ns, then the pulse width low = 6 ns, or vice versa.

Table 3. Shift Register Mode Timing

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Maximum Clock Rate ($1/t_{CLK\_IN}$)			100	MHz	
Minimum Clock Period (t_{CLK_IN})	10			ns	
Minimum Pulse Width High (t_{PWH})[1]	4			ns	
Minimum Pulse Width Low (t_{PWL})[1]	4			ns	
Minimum Setup Time, DATA_IO to CLK_IN (t_{DS})		2.5		ns	
Minimum Hold Time, DATA_IO to CLK_IN (t_{DH})		1		ns	
Data Valid, CLK_IN to DATA_O (t_{DV})		2		ns	
DATA_IO, DATA_O Rise Time (t_R)		1		ns	Outputs loaded with 80 pF, 10% to 90%
Minimum Clock to Update ($t_{CLK\_IN-UPDATE}$)		10		ns	
RF Settling Time (t_{RF_SETTLE})		20		ns	TDU settling time between TDU code = 0 to TDU code = 127

[1] Clock Period = Pulse Width High + Pulse Width Low; however, Minimum Clock Period cannot equal Minimum Pulse Width High + Minimum Pulse Width Low, which allows for the SPI signals that are not 50% duty cycle. The extreme example is if the pulse width high = 4 ns, then the pulse width low = 6 ns, or vice versa.

TIMING DIAGRAMS

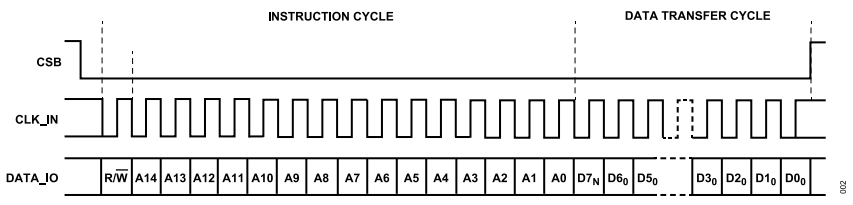

Figure 2. SPI Register Timing (MSB First)

SPECIFICATIONS

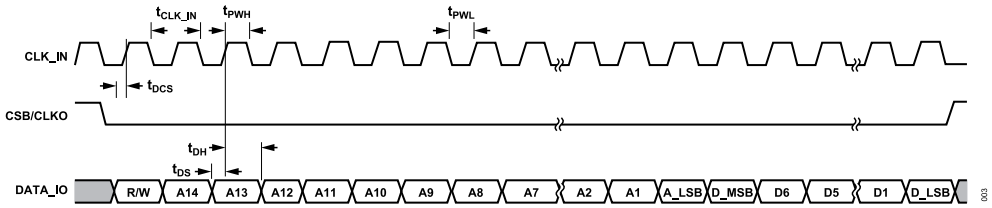

Figure 3. Timing Diagram for the SPI Register Write

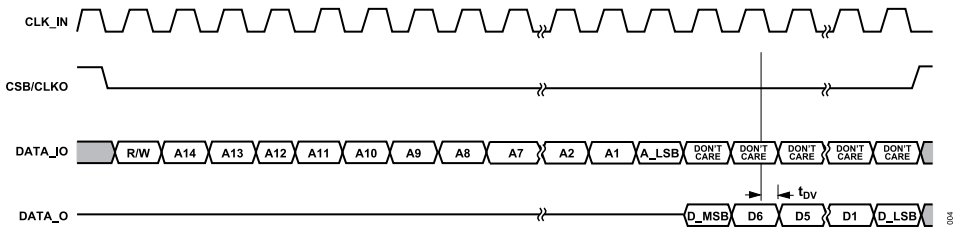

Figure 4. Timing Diagram for SPI Register Read (4-Wire SPI Protocol)

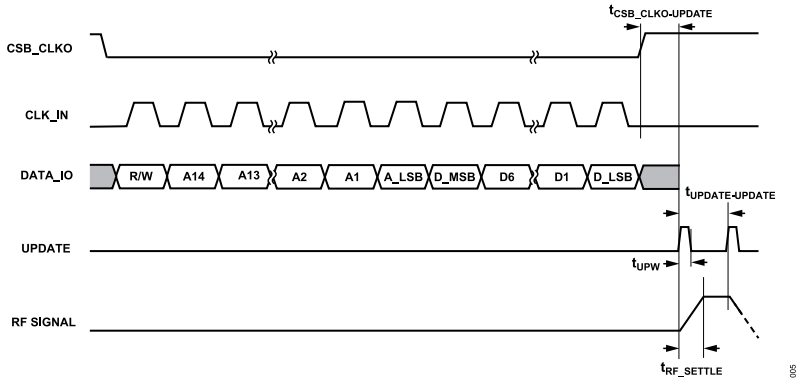

Figure 5. Timing Diagram for UPDATE Pin

SPECIFICATIONS

SPI BLOCK WRITE MODE

Data can be written to and read from the SPI registers in block write or read modes, where the register address automatically increments (given Bit 5 and Bit 2 are asserted high in Register 0x00). Data for consecutive registers can be written or read without sending new address bits. During the transaction, the rising edge of CLK_IN during the final bit (D0) of the register triggers the data to load into the register. Data writing or reading can be continued indefinitely until CSB/CLKO is raised again, ending the write or read process.

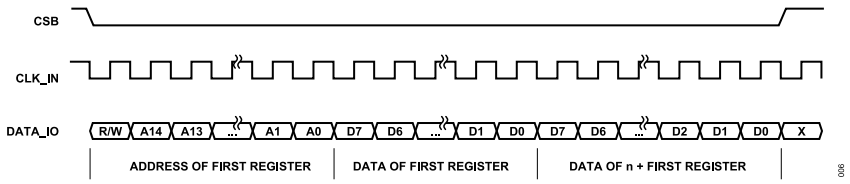

Figure 6. Timing Diagram for SPI Block Write Mode

SHORT CONTROL COMMAND

The short control command is a quick and efficient 6-bit SPI transaction used for eight different commands. The first two bits clocked in must be 0b11 to initiate a short control command. Each command is given with a 3-bit command code within the SPI transaction. After the 3-bit command code, a final don't care bit must be clocked in. Table 4 outline the various commands and their unique command code bits. The same commands are available via the normal 24-bit SPI transaction; however, these shorter versions allow much faster operation. The active edge of a short control command is the CSB/CLKO rising edge, which completes the command. Timing is shown in Figure 7, wherein the don't care bit is shown as a zero.

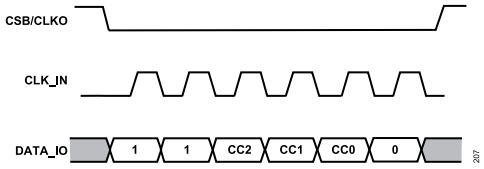

Figure 7. Short Control Command

Table 4. Short Control Commands

Short Control Command	Control Command Bits [CC2:CC0]	Description
Switch to Sequencer B	0 0 0	Sources the TDU/DSA data from Sequencer B. In addition, sets Bit 0 = 1 in Register 0x16.
Switch to Sequencer A	0 0 1	Sources the TDU/DSA data from Sequencer A. In addition, sets Bit 0 = 0 in Register 0x16.
Reset Sequencer A	0 1 0	Resets Sequencer A to its start position. In addition, sets Bit 3 in Register 0x15.
Reset Sequencer B	0 1 1	Resets Sequencer B to its start position. In addition, sets Bit 0 in Register 0x15.
Toggle Sequencer A Direction	1 0 0	Changes Sequencer A ascending/descending direction. In addition, sets Bit 3 in Register 0x14.
Toggle Sequencer B Direction	1 0 1	Changes Sequencer B ascending/descending direction. In addition, sets Bit 0 in Register 0x14.
Data Load Command	1 1 0	Loads all 32 TDU and DSA state data from the first rank registers to the second rank registers.
Update Command	1 1 1	Advances sequencer while in SPI mode.

SPECIFICATIONS

SHIFT REGISTER MODE

The ADAR4002 offers an extremely simple serial shift register mode by asserting the MODE pin high. In this mode, there are no register addresses, no sequencer functionality, and no short commands. The shift register has dual rank data registers and is controlled with the UPDATE pin. The digital pins of the ADAR4002 are configured for a daisy-chain operation, with the possibility of one ADAR4002 driving another, in as long a chain as required. Data comes in on CLK_IN and DATA_IO and shifts out on CSB/CLKO and DATA_O. Data is serially shifted through the full chain of the devices. Once the correct TDU and DSA data are in the correct devices, an update signal is given to load the data into the second rank register of the several devices. The second rank register data is immediately applied to the various TDUs and DSAs on all the daisy chained ADAR4002 devices. Shift register mode timing is shown in Figure 8.

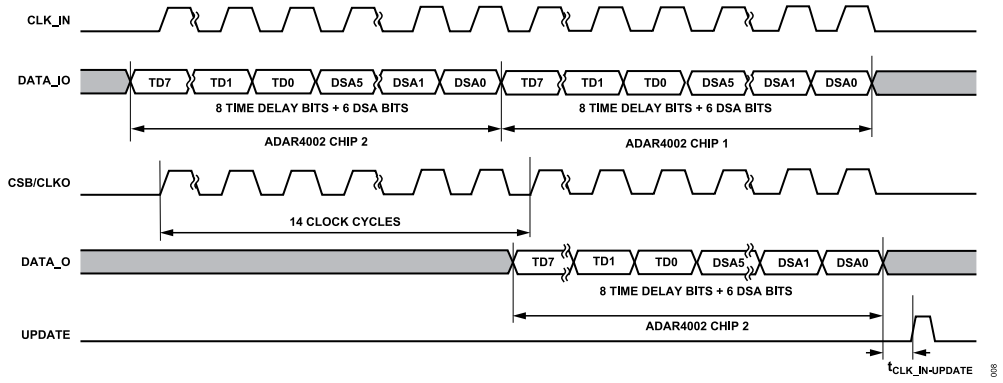

Figure 8. Timing Diagram for Two ADAR4002 Chips Daisy-Chained Together While in Shift Register Mode (Chip 1 Drives Chip 2)

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V1P2 to GND	1.35 V
V1P0 to GND	1.15 V
CSB/CLKO, CLK_IN, DATA_IO, DATA_O, UPDATE, and MODE	−0.5 V to +1.8 V
Maximum RF Input Power (RF1 or RF2)	18 dBm
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Reflow Soldering, Peak	260°C
Maximum Junction (T_J)	125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. The PCB thermal design requires careful attention.

θ_{JA} is the junction to the ambient with the exposed pad soldered down, θ_{JB} is junction to board, θ_{JC_TOP} is the junction to the top of the package, and θ_{JC_BOTTOM} is the junction to the exposed pad.

Table 6. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JB}	θ_{JC_TOP}	θ_{JC_BOTTOM}	Unit
CP-14-6	63.9	24.9	68.5	15.4	°C/W

[1] Simulated based on PCB specified in JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2014

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADAR4002

Table 7. ADAR4002, 14-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	±2	2
CDM	±1.25	C5

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

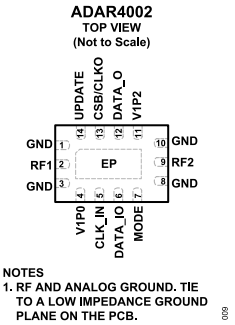

Figure 9. ADAR4002 Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 8, 10	GND	RF and Analog Ground. Tie all ground pads together to a low impedance plane on the circuit board.
2	RF1	RF Input or Output Looking into the DSA. Internal DC bias is 0 V. AC coupling is required if the bias of the connected device differs so that the ADAR4002 internal bias is not disturbed.
4	V1P0	Digital Supply. Apply 1.0 V.
5	CLK_IN	Serial Clock Input for Both Digital Modes (1.0 V Logic).
6	DATA_IO	Dual Direction Pin. DATA_IO is used for both SPI mode and shift register mode. While in the 3-wire SPI protocol, this pin is the serial data input and output. While in the 4-wire SPI protocol, this pin is the serial data input. While in shift register mode, this pin is the register data input (1.0 V logic).
7	MODE	Digital Mode Select for Digital Input and Output Data (1.0 V Logic). If MODE is low (ground), it is in SPI mode, and if MODE is high, it is in shift register mode.
9	RF2	RF Input or Output Looking into the TDU. Internal DC bias is 0 V. AC coupling is required if the bias of the connected device differs so that the ADAR4002 internal bias is not disturbed.
11	V1P2	RF Supply Voltage. Apply 1.2 V.
12	DATA_O	Serial Data Output for Both Digital Modes. While in the 4-wire SPI protocol, this pin is the serial data output. While in shift register mode, this pin is the shift register data output (1.0 V logic).
13	CSB/CLKO	While in SPI mode, chip select (CSB). While in shift register mode, clock output (1.0 V logic).
14	UPDATE	While in SPI mode, UPDATE advances the sequencer. While in shift register mode, UPDATE loads data from the shift register to TDU and DSA (1.0 V logic).
EP	Exposed Pad	RF and Analog Ground. Tie to a low impedance ground plane on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

V1P2 = 1.2 V, V1P0 = 1.0 V, T_A = 25°C, frequency = 10 GHz, TDU code = 0, and DSA code = 0, unless otherwise specified. IP2 tone spacing = 1 GHz, and IP3 tone spacing = 10 MHz. Low-side tone reported for IP2. Port 1 = RF1 and Port 2 = RF2. Gain is S21 and reverse gain is S12. Error plots reference an ideal line. Variation plots are self referenced and are a measure of change from the self reference.

TIME DELAY SWEEP, TIME DELAY RANGE 0

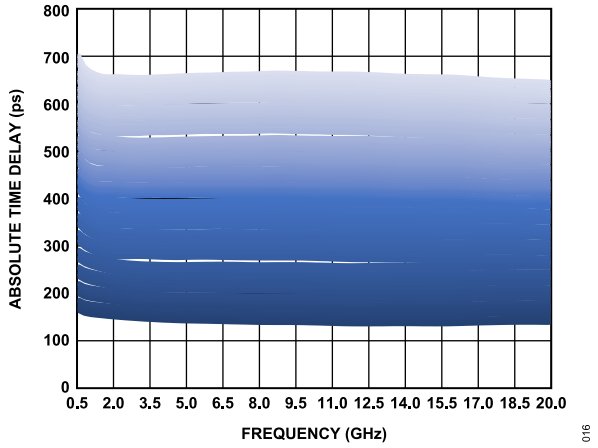

Figure 10. Absolute Time Delay vs. Frequency over TDU Code 0 to TDU Code 127, Darkest Blue Is TDU = 0 and Lightest Blue is TDU = 127

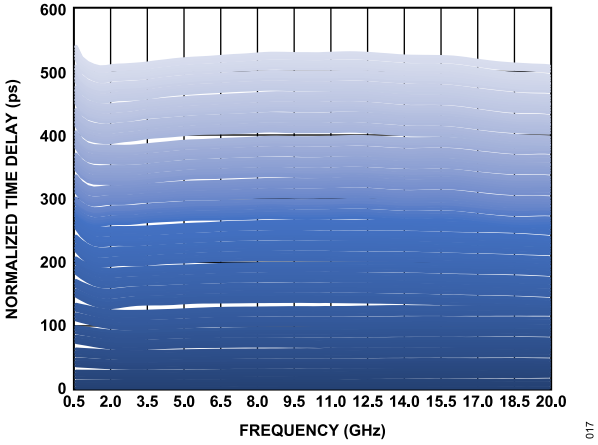

Figure 11. Normalized Time Delay vs. Frequency over TDU Code 0 to TDU Code 127, Darkest Blue Is TDU = 0 and Lightest Blue is TDU = 127

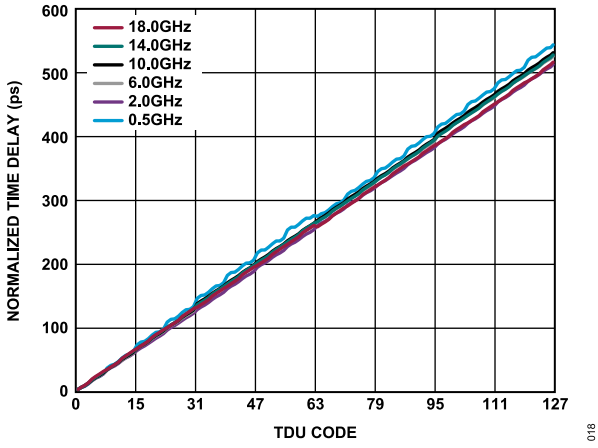

Figure 12. Normalized Time Delay vs. TDU Code over Frequencies 0.5 GHz, 2.0 GHz, 6.0 GHz, 10.0 GHz, 14.0 GHz, and 18.0 GHz

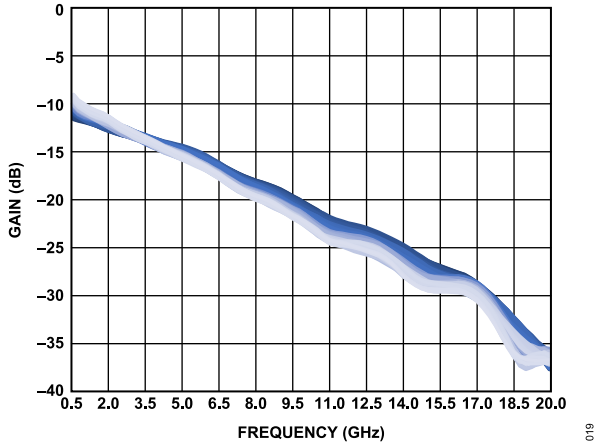

Figure 13. Gain vs. Frequency over TDU Code 0 to TDU Code 127, Darkest Blue Is TDU = 0 and Lightest Blue is TDU = 127

TYPICAL PERFORMANCE CHARACTERISTICS

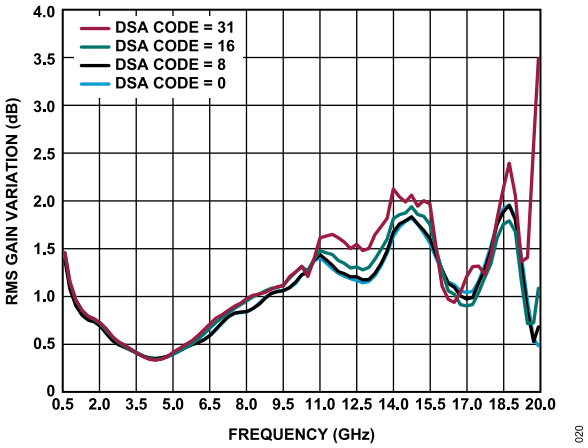

Figure 14. RMS Gain Variation vs. Frequency, Computed over Time Delay Code 0 to Code 127 at DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31

TYPICAL PERFORMANCE CHARACTERISTICS

TIME DELAY SWEEP, TIME DELAY RANGE 1

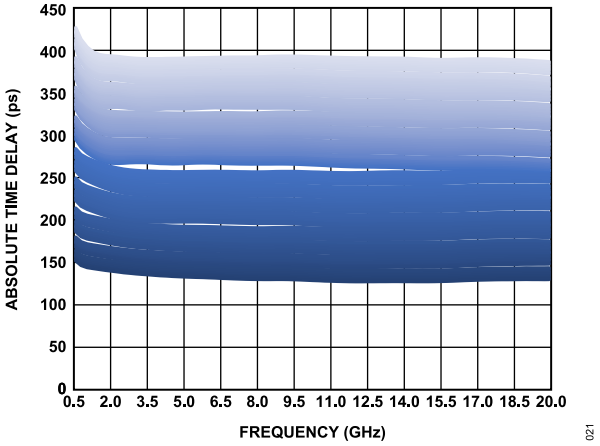

Figure 15. Absolute Time Delay vs. Frequency over TDU Code 0 to TDU Code 127, Darkest Blue Is TDU = 0 and Lightest Blue is TDU = 127

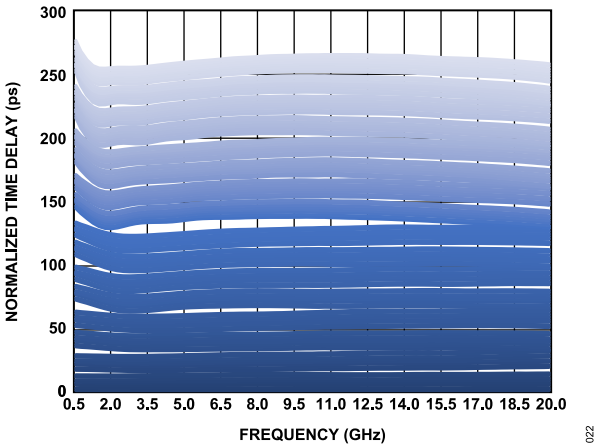

Figure 16. Normalized Time Delay vs. Frequency over TDU Code 0 to TDU Code 127, Darkest Blue Is TDU = 0 and Lightest Blue is TDU = 127

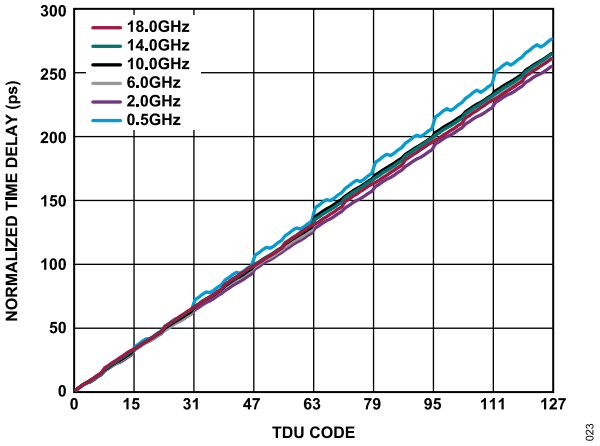

Figure 17. Normalized Time Delay vs. TDU Code over Frequencies 0.5 GHz, 2.0 GHz, 6.0 GHz, 10.0 GHz, 14.0 GHz, and 18.0 GHz

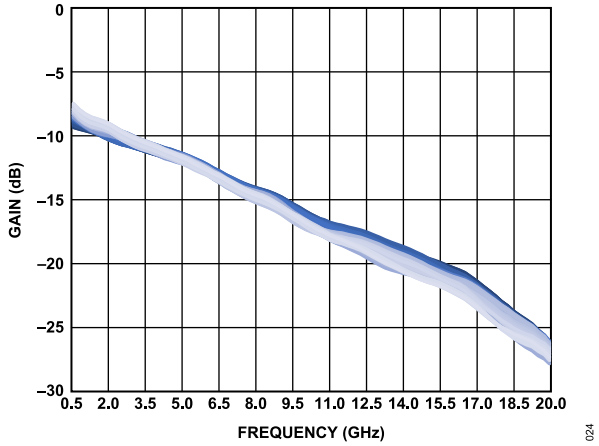

Figure 18. Gain vs. Frequency over TDU Code 0 to TDU Code 127, Darkest Blue Is TDU = 0 and Lightest Blue is TDU = 127

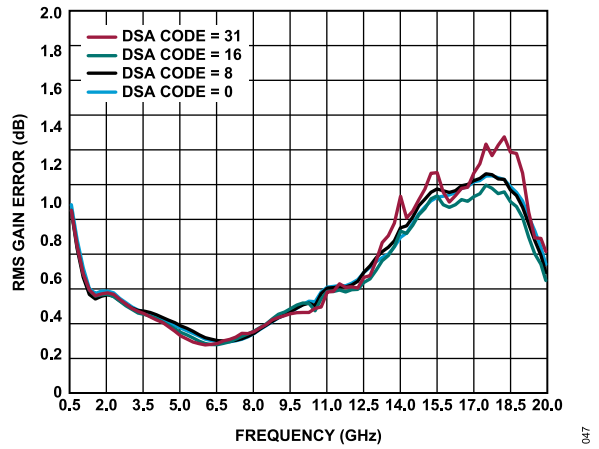

Figure 19. RMS Gain Variation vs. Frequency, Computed over TDU Code 0 to TDU Code 127 at DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31

TYPICAL PERFORMANCE CHARACTERISTICS

DSA ATTENUATION SWEEP, TIME DELAY RANGE 0

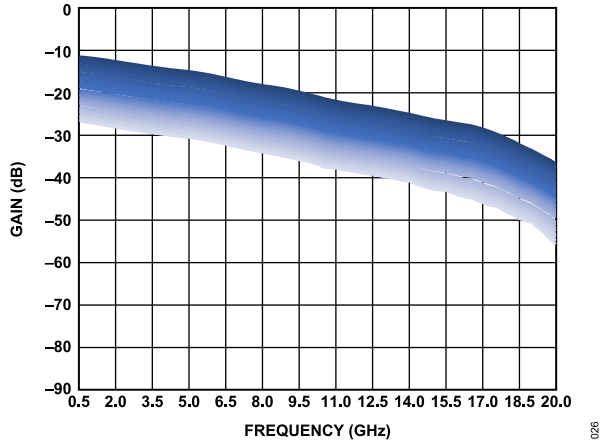

Figure 20. Gain vs. Frequency over DSA Code 0 to DSA Code 31, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 31

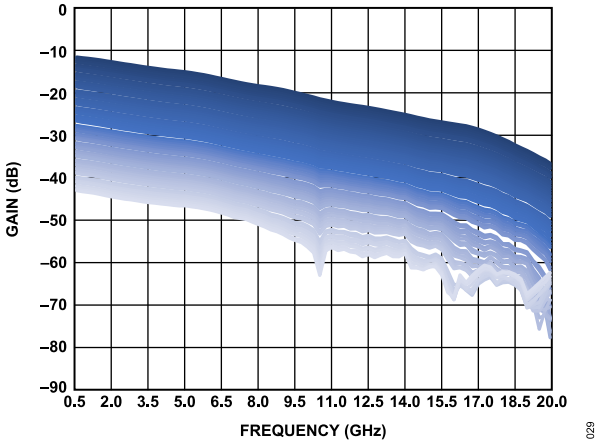

Figure 23. Gain vs. Frequency over DSA Code 0 to DSA Code 63, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

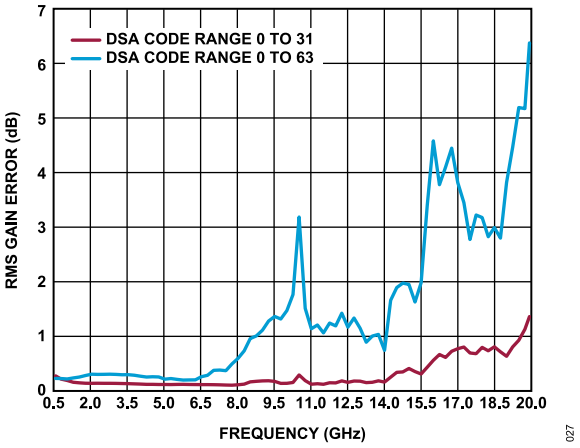

Figure 21. RMS Gain Error vs. Frequency, Computed over DSA Code 0 to DSA Code 31 and DSA Code 0 to DSA Code 63

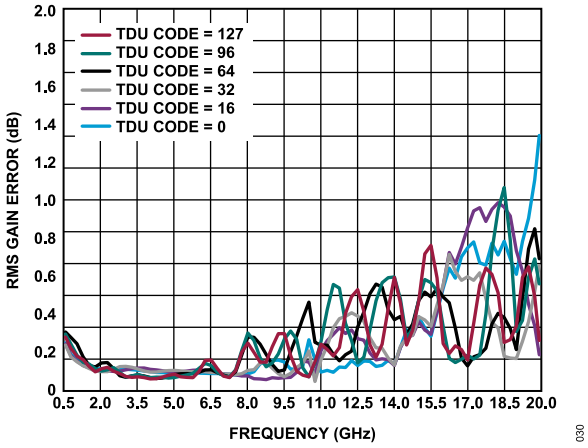

Figure 24. RMS Gain Error vs. Frequency, Computed over DSA Code 0 to DSA Code 31 at TDU Code 0, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127

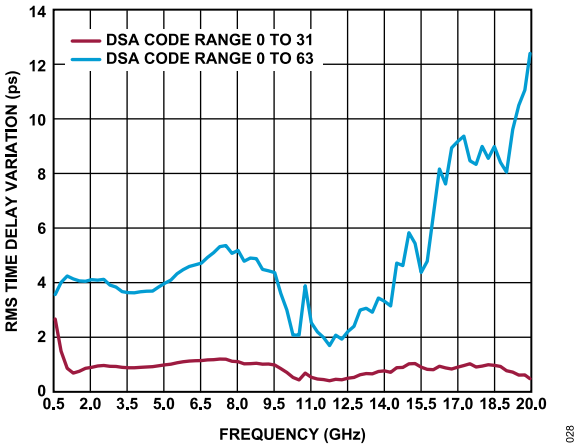

Figure 22. RMS Time Delay Variation vs. Frequency, Computed over DSA Code 0 to DSA Code 31 and DSA Code 0 to DSA Code 63

TYPICAL PERFORMANCE CHARACTERISTICS

DSA ATTENUATION SWEEP, TIME DELAY RANGE 1

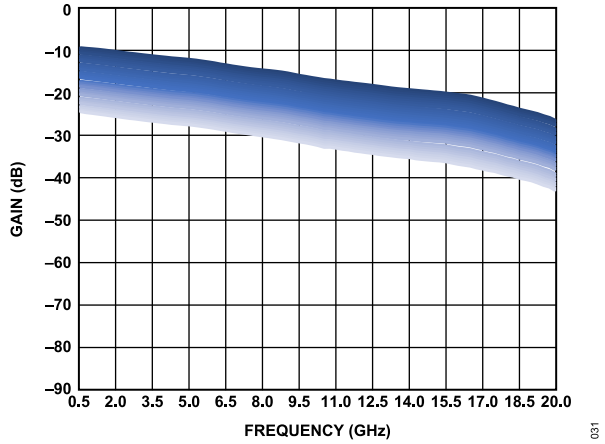

Figure 25. Gain vs. Frequency over DSA Code 0 to DSA Code 31, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 31

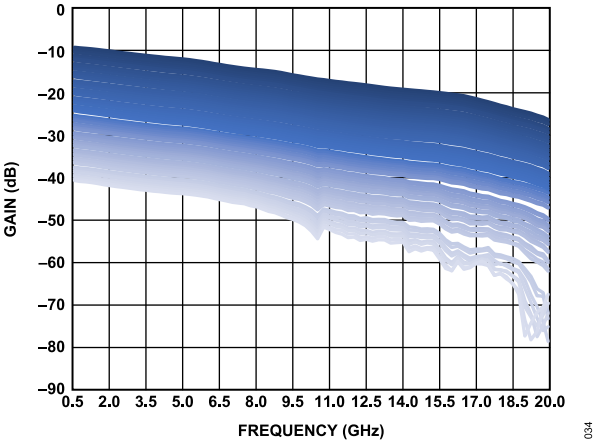

Figure 28. Gain vs. Frequency over DSA Code 0 to DSA Code 63, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

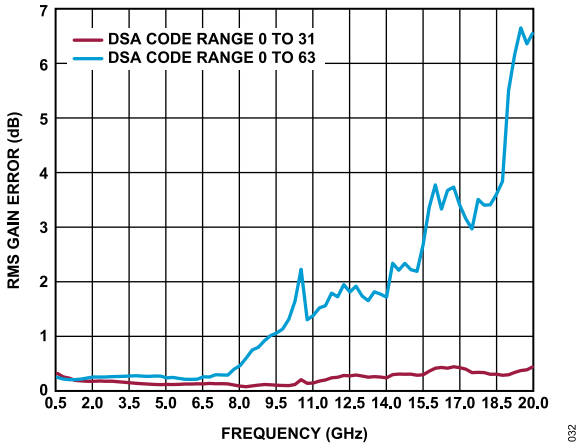

Figure 26. RMS Gain Error vs. Frequency, Computed over DSA Code 0 to DSA Code 31 and DSA Code 0 to DSA Code 63

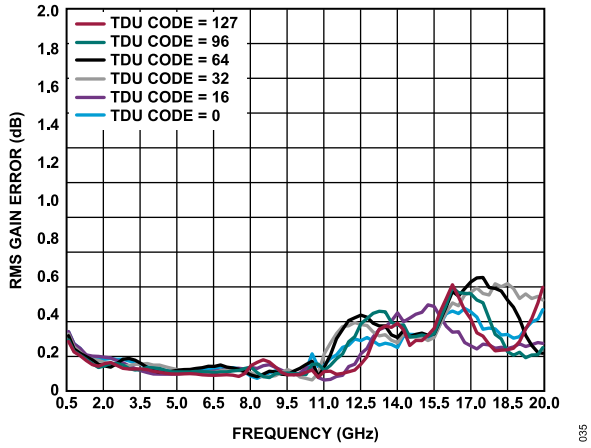

Figure 29. RMS Gain Error vs. Frequency, Computed over DSA Code 0 to DSA Code 31 at TDU Code 0, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127

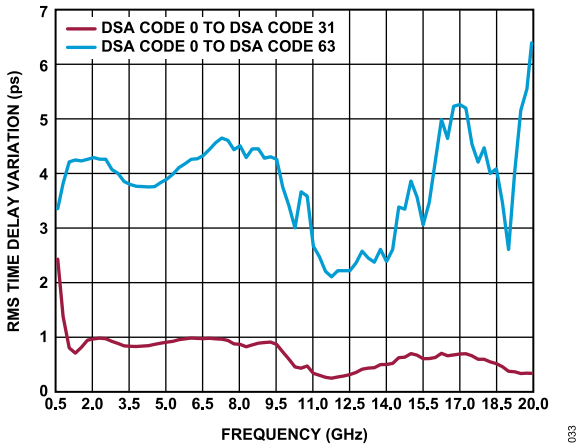

Figure 27. RMS Time Delay Variation vs. Frequency, Computed over DSA Code 0 to DSA Code 31 and DSA Code 0 to DSA Code 63

TYPICAL PERFORMANCE CHARACTERISTICS

DSA SWEEPS

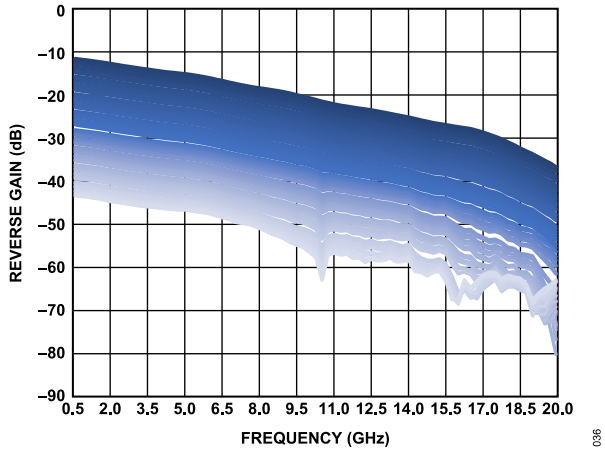

Figure 30. Reverse Gain vs. Frequency over DSA Code 0 to DSA Code 63, Time Delay Range 0, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

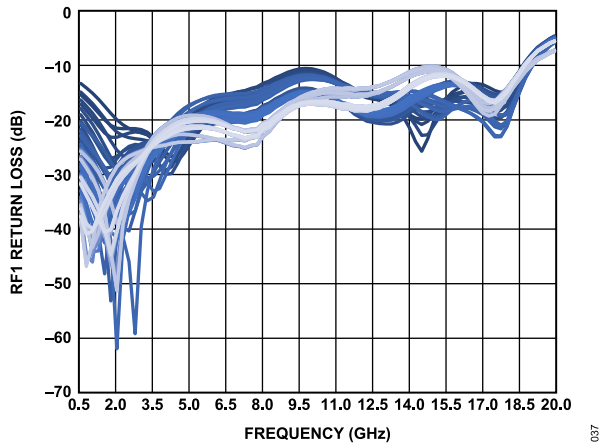

Figure 31. RF1 Return Loss vs. Frequency over DSA Code 0 to DSA Code 63, Time Delay Range 0, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

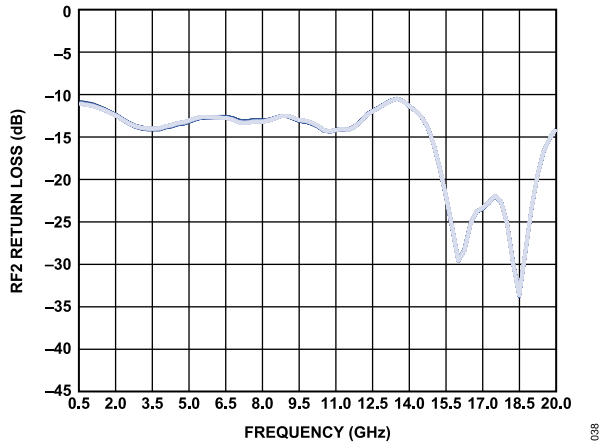

Figure 32. RF2 Return Loss vs. Frequency over DSA Code 0 to DSA Code 63, Time Delay Range 0, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

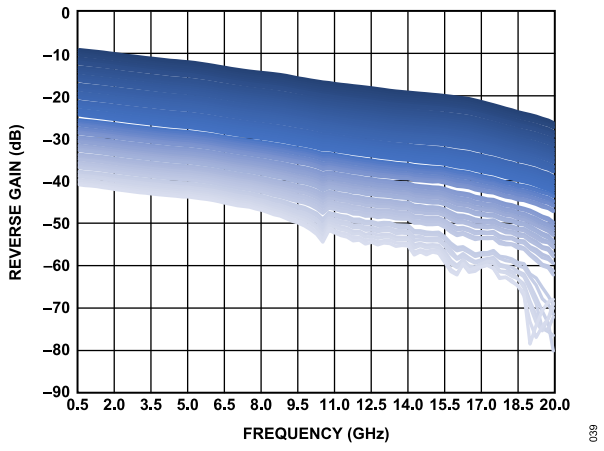

Figure 33. Reverse Gain vs. Frequency over DSA Code 0 to DSA Code 63, Time Delay Range 1, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

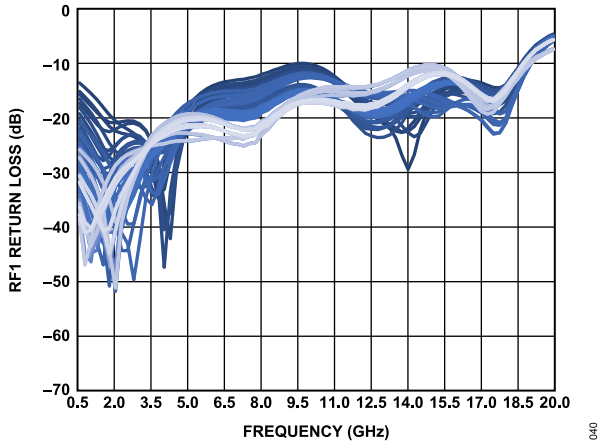

Figure 34. RF1 Return Loss vs. Frequency over DSA Code 0 to DSA Code 63, Time Delay Range 1, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

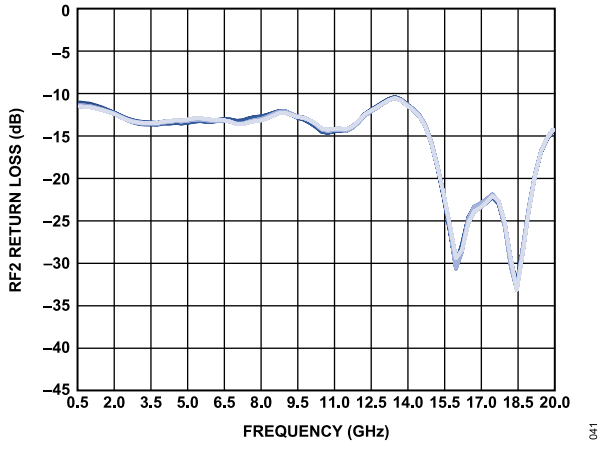

Figure 35. RF2 Return Loss vs. Frequency over DSA Code 0 to DSA Code 63, Time Delay Range 1, Darkest Blue Is DSA = 0 and Lightest Blue is DSA = 63

TYPICAL PERFORMANCE CHARACTERISTICS

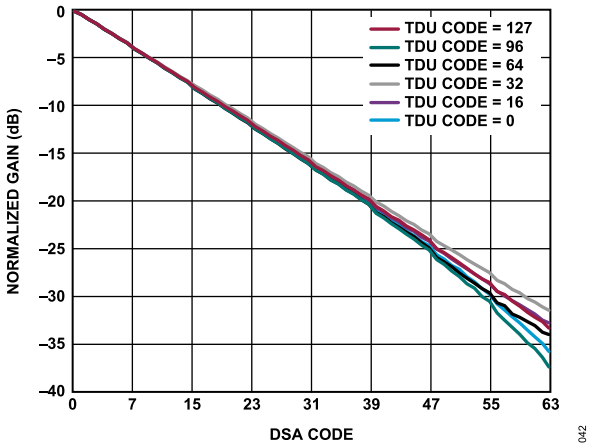

Figure 36. Normalized Gain vs. DSA Code over TDU Code 0, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 0

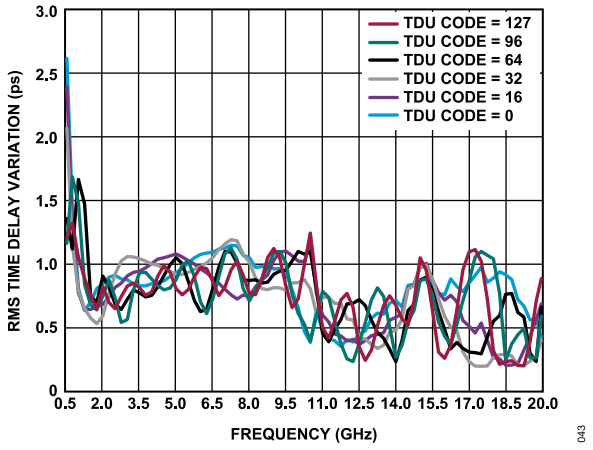

Figure 37. RMS Time Delay Variation vs. Frequency, Computed over DSA Code 0 to DSA Code 31 at TDU Code 0, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 0

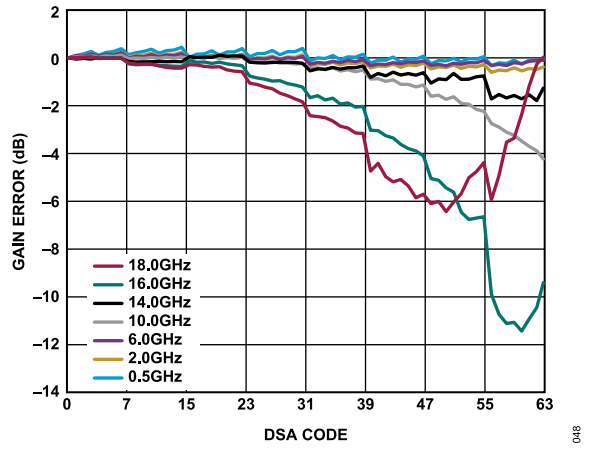

Figure 38. Gain Error vs. DSA Code over Frequency, Time Delay Range 0

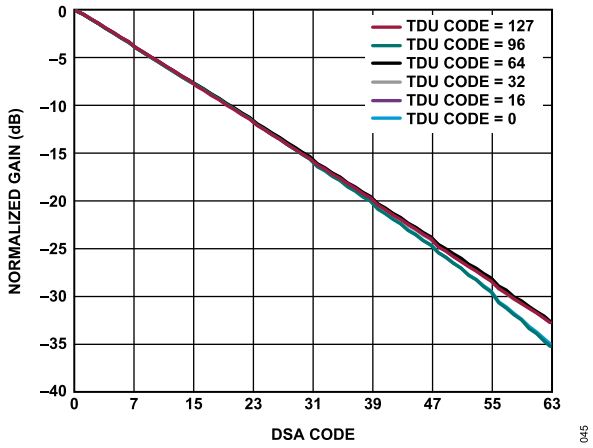

Figure 39. Normalized Gain vs. DSA Code over TDU Code 0, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 1

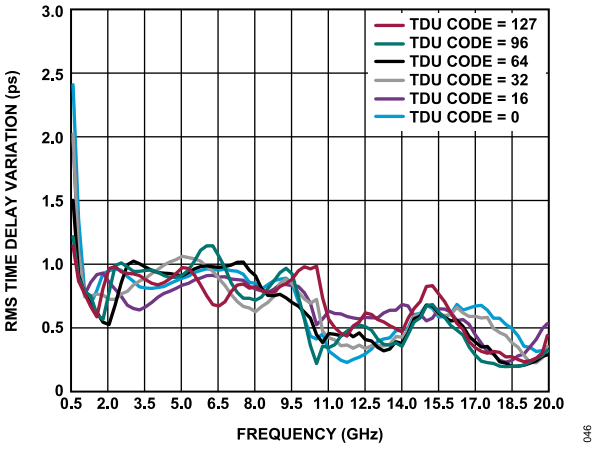

Figure 40. RMS Time Delay Variation vs. Frequency, Computed over DSA Code 0 to DSA Code 31 at TDU Code 0, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 1

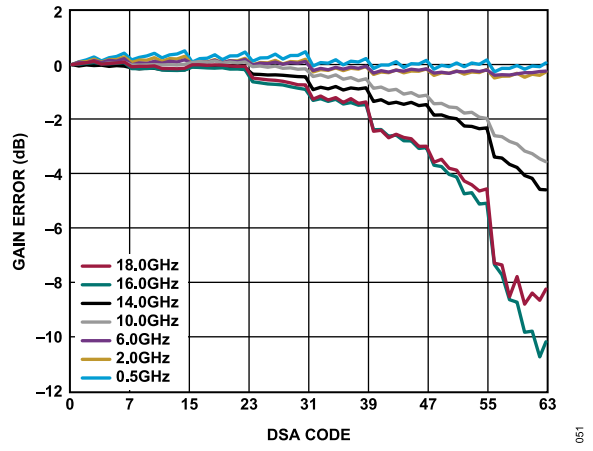

Figure 41. Gain Error vs. DSA Code over Frequency, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

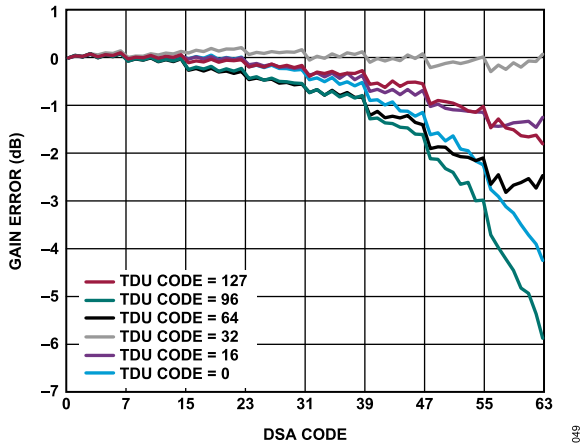

Figure 42. Gain Error vs. DSA Code over TDU Code 0, TDU Code 8, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 0

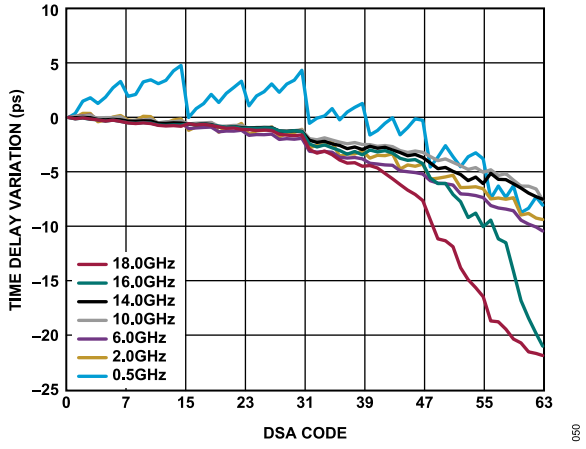

Figure 43. Time Delay Variation vs. DSA Code over Frequency, Time Delay Range 0

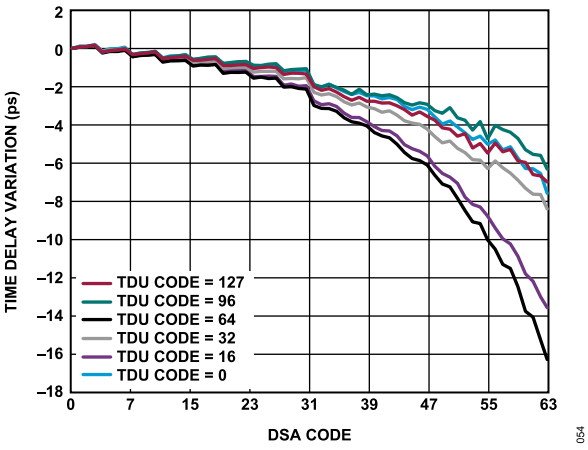

Figure 44. Time Delay Variation vs. DSA Code over TDU Code 0, TDU Code 8, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 0

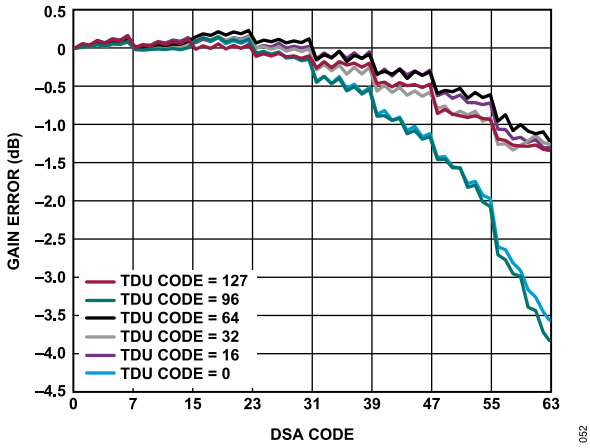

Figure 45. Gain Error vs. DSA Code over TDU Code 0, TDU Code 8, TDU Code 16, and TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 1

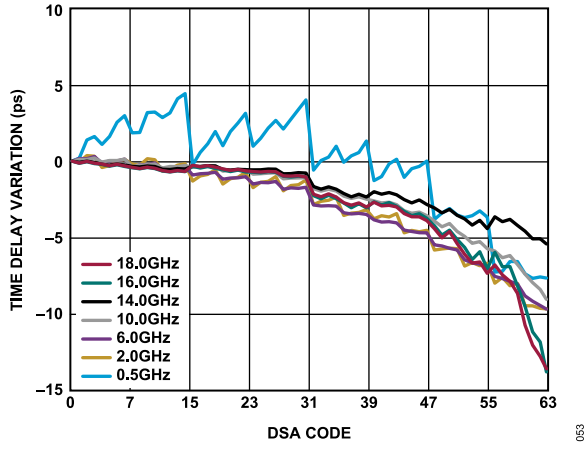

Figure 46. Time Delay Variation vs. DSA Code over Frequency, Time Delay Range 1

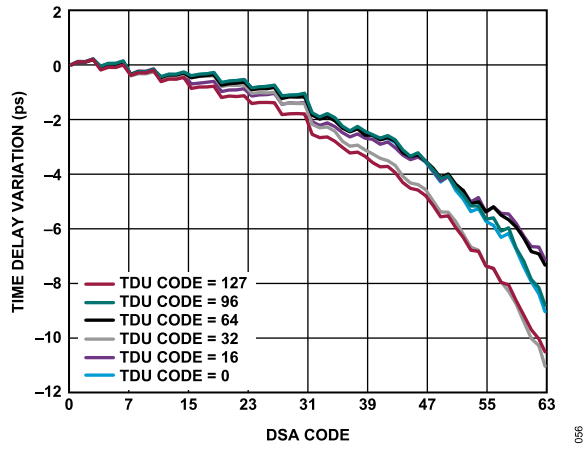

Figure 47. Time Delay Variation vs. DSA Code over TDU Code 0, TDU Code 8, TDU Code 16, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

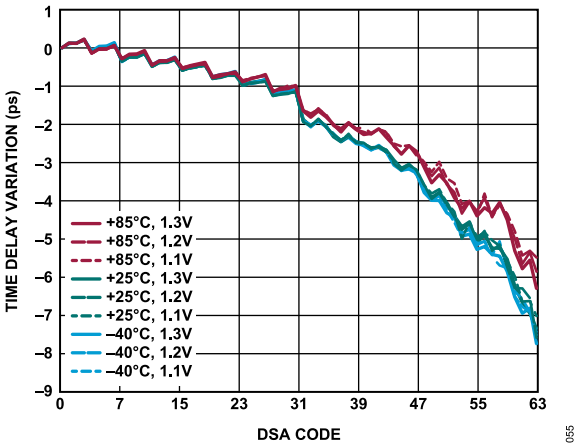

Figure 48. Time Delay Variation vs. DSA Code over Temperature and Supply Voltage, Time Delay Range 0

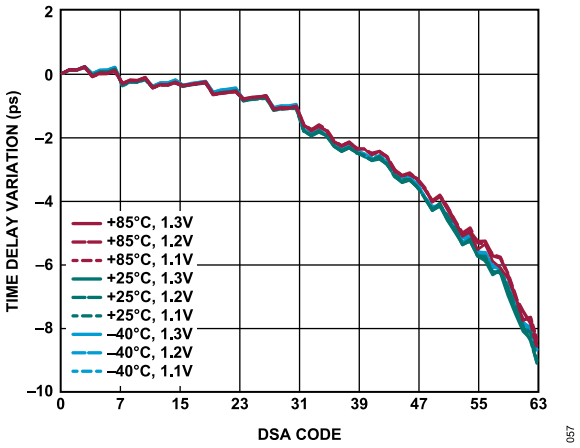

Figure 49. Time Delay Variation vs. DSA Code over Temperature and Supply Voltage, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

TDU SWEEPS

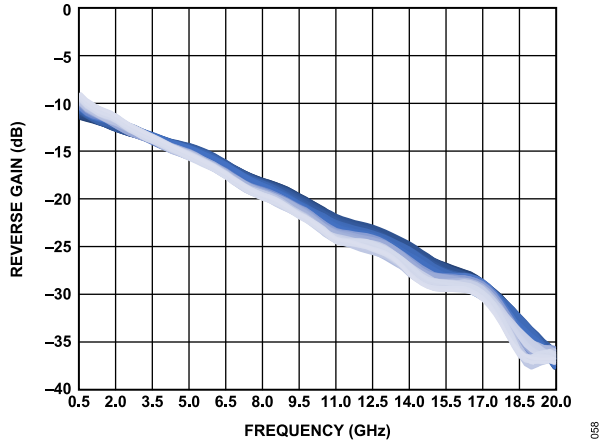

Figure 50. Reverse Gain vs. Frequency over TDU Code 0 to TDU Code 127, Time Delay Range 0, Darkest Blue Is TDU = 0 and Lightest Blue Is TDU = 127

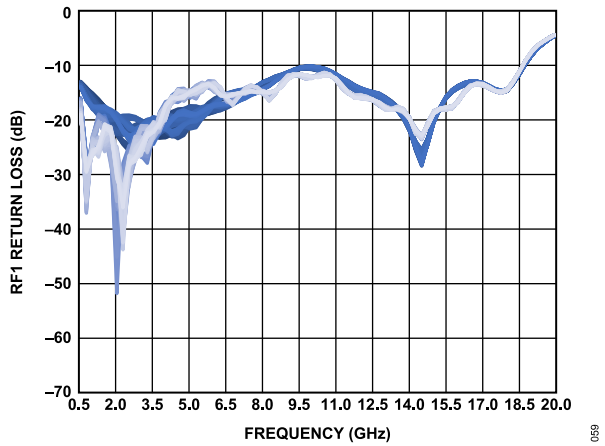

Figure 51. RF1 Return Loss vs. Frequency over TDU Code 0 to TDU Code 127, Time Delay Range 0, Darkest Blue Is TDU = 0 and Lightest Blue Is TDU = 127

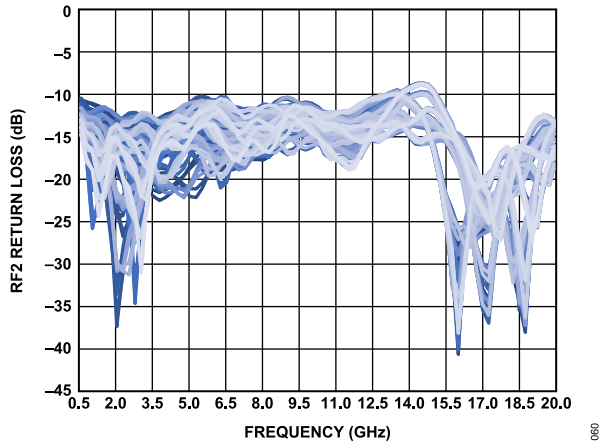

Figure 52. RF2 Return Loss vs. Frequency over TDU Code 0 to TDU Code 127, Time Delay Range 0, Darkest Blue Is TDU = 0 and Lightest Blue Is TDU = 127

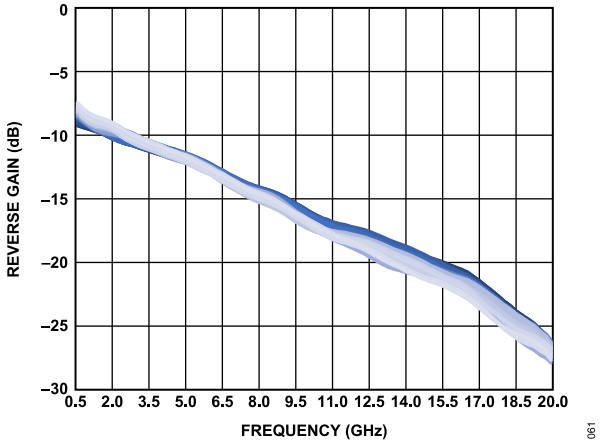

Figure 53. Reverse Gain vs. Frequency over TDU Code 0 to TDU Code 127, Time Delay Range 1, Darkest Blue Is TDU = 0 and Lightest Blue Is TDU = 127

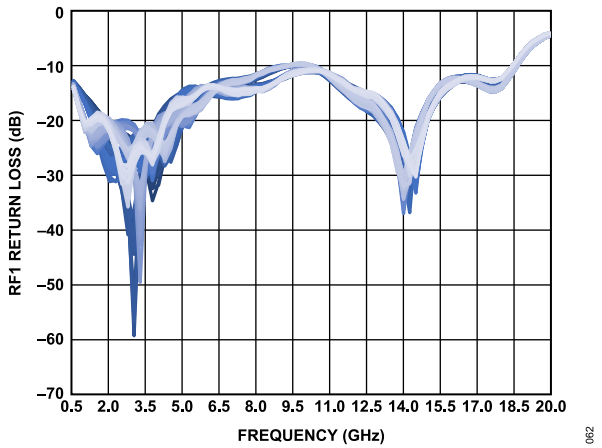

Figure 54. RF1 Return Loss vs. Frequency over TDU Code 0 to TDU Code 127, Time Delay Range 1, Darkest Blue Is TDU = 0 and Lightest Blue Is TDU = 127

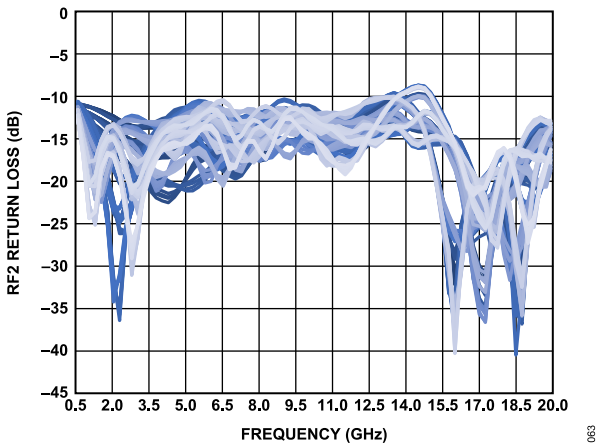

Figure 55. RF2 Return Loss vs. Frequency over TDU Code 0 to TDU Code 127, Time Delay Range 1, Darkest Blue Is TDU = 0 and Lightest Blue Is TDU = 127

TYPICAL PERFORMANCE CHARACTERISTICS

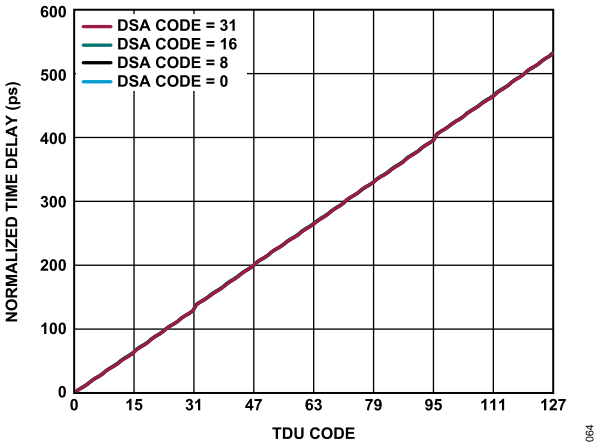

Figure 56. Normalized Time Delay vs. TDU Code over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 0

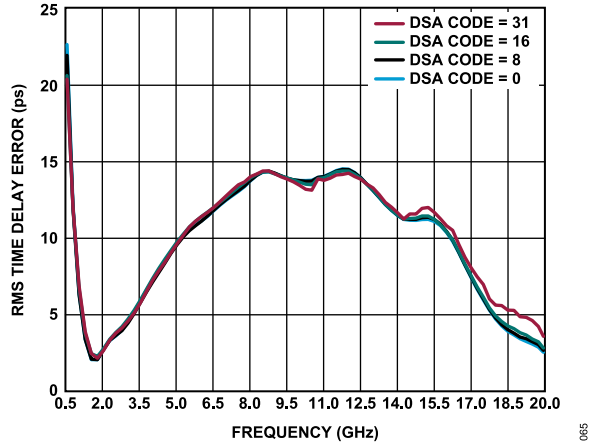

Figure 57. RMS Time Delay Error vs. Frequency, Computed over TDU Code 0 to TDU Code 127 at DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 0

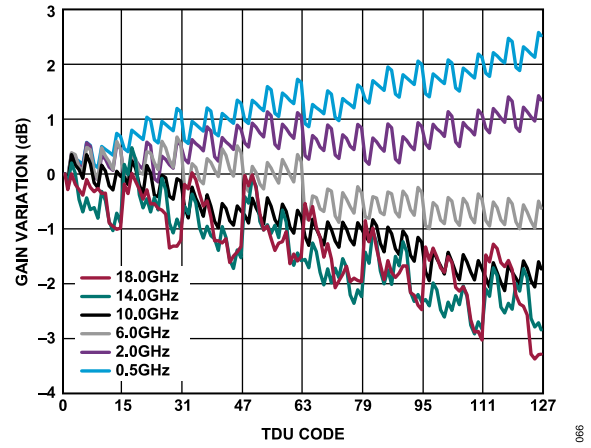

Figure 58. Gain Variation vs. TDU Code over Frequency, Time Delay Range 0

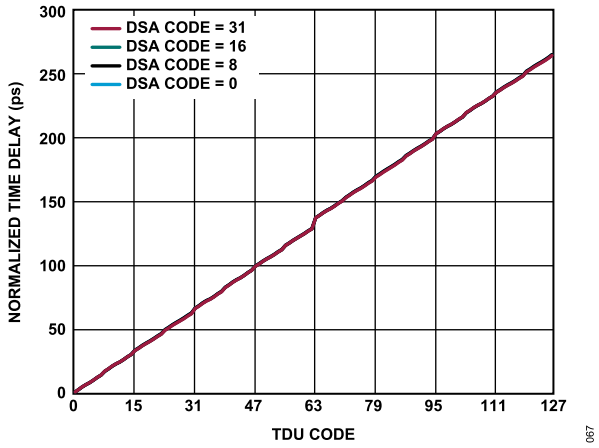

Figure 59. Normalized Time Delay vs. TDU Code over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 1

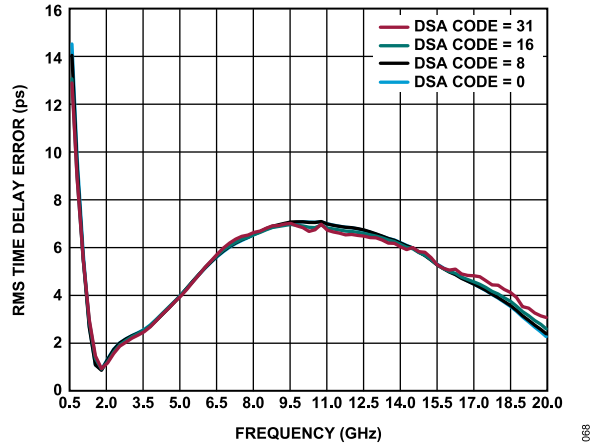

Figure 60. RMS Time Delay Error vs. Frequency Computed, over TDU Code 0 to TDU Code 127 at DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 1

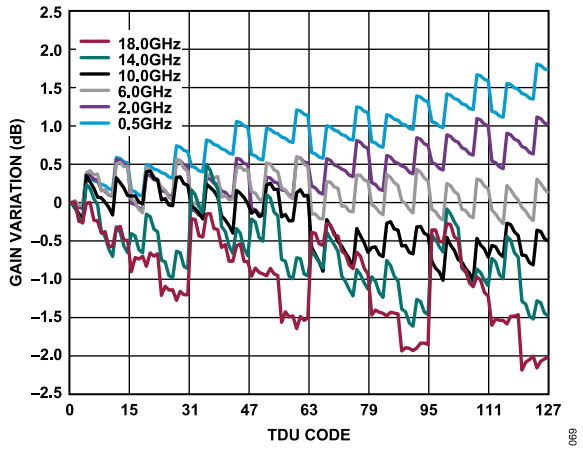

Figure 61. Gain Variation vs. TDU Code over Frequency, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

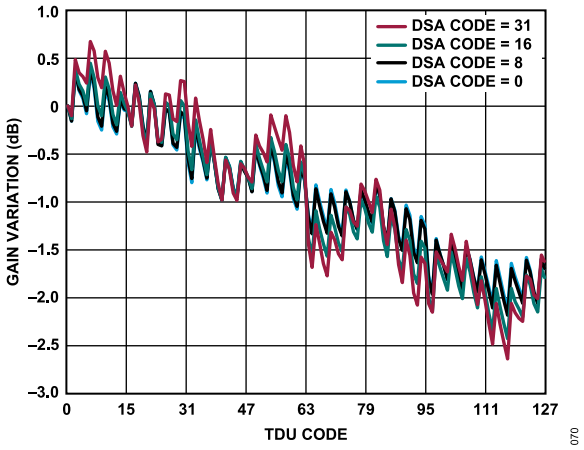

Figure 62. Gain Variation vs. TDU Code over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 0

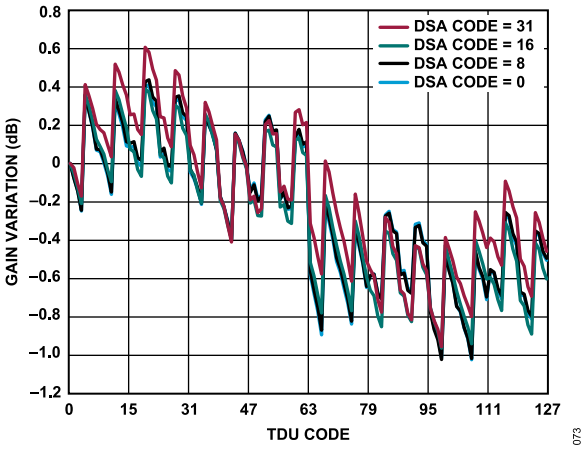

Figure 65. Gain Variation vs. TDU Code over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 1

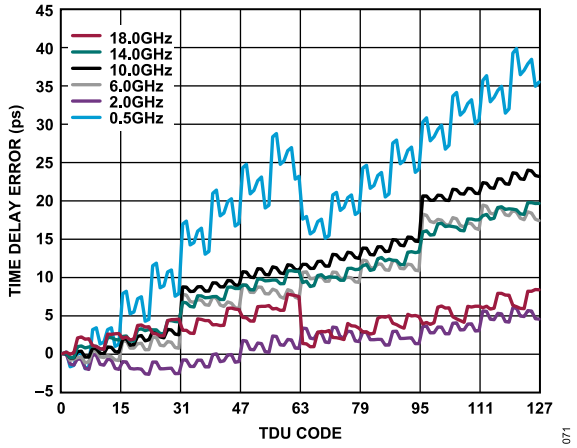

Figure 63. Time Delay Error vs. TDU Code over Frequency, Time Delay Range 0

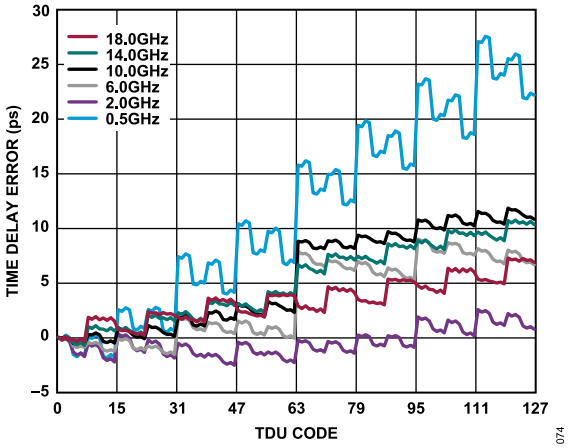

Figure 66. Time Delay Error vs. TDU Code over Frequency, Time Delay Range 1

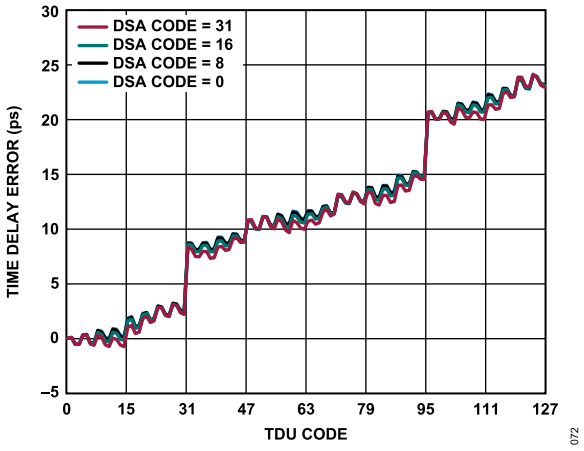

Figure 64. Time Delay Error vs. TDU Code over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 0

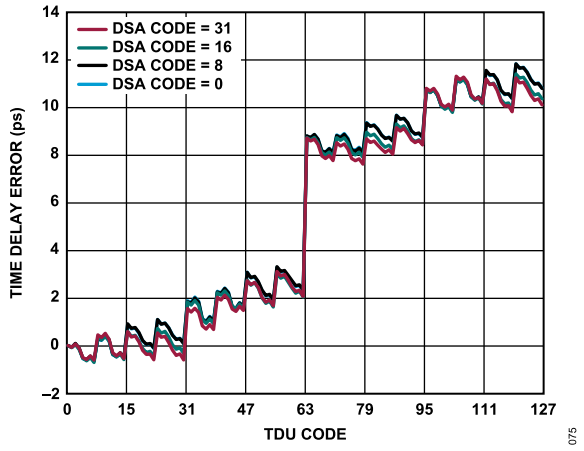

Figure 67. Time Delay Error vs. TDU Code over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE SUPPLY AND TEMPERATURE SWEEPS

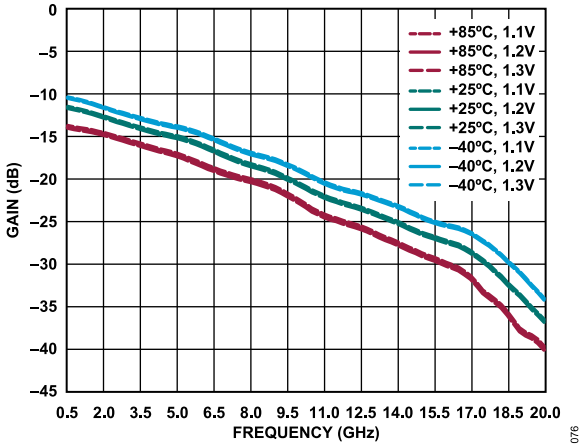

Figure 68. Gain vs. Frequency over Temperature and Supply Voltage, Time Delay Range 0

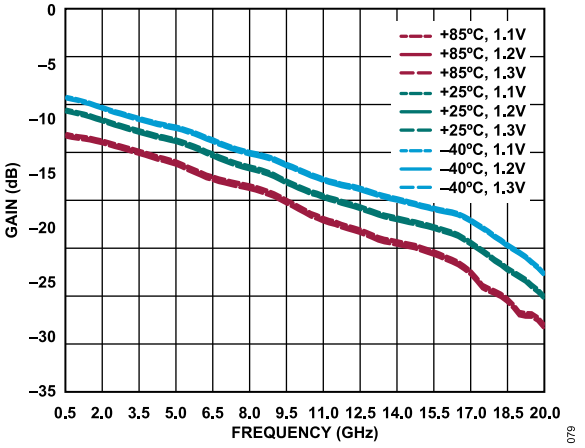

Figure 71. Gain vs. Frequency over Temperature and Supply Voltage, Time Delay Range 1

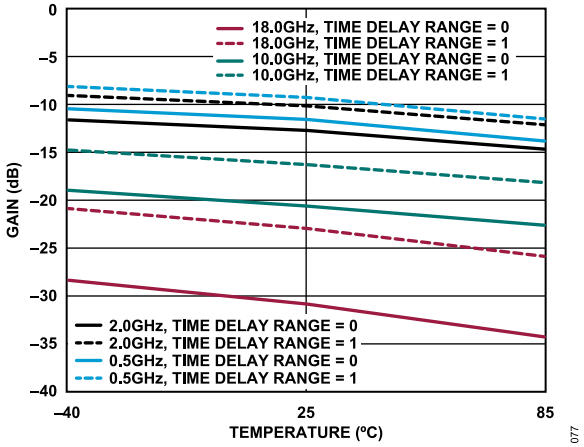

Figure 69. Gain vs. Temperature over Frequency and Time Delay Range

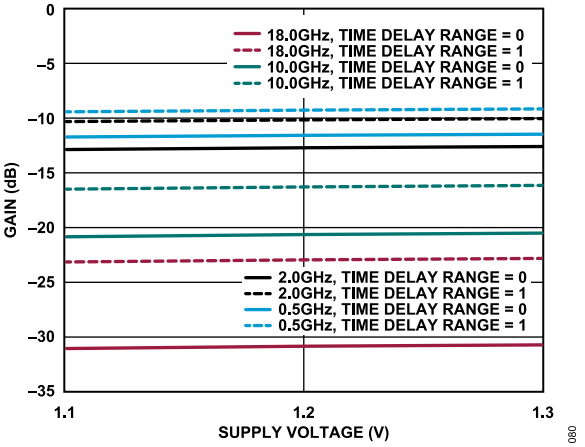

Figure 72. Gain vs. Supply Voltage over Frequency and Time Delay Range

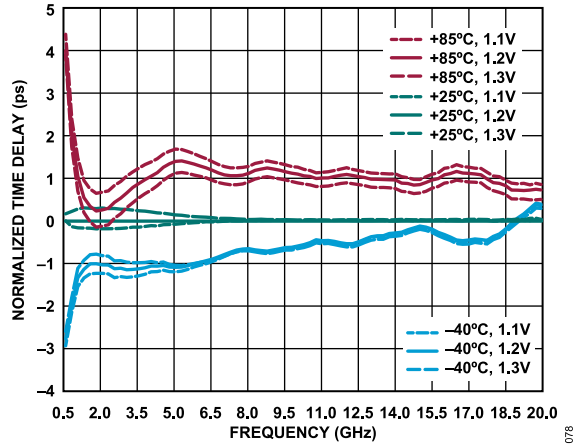

Figure 70. Normalized Time Delay vs. Frequency over Temperature and Supply Voltage, Time Delay Range 0

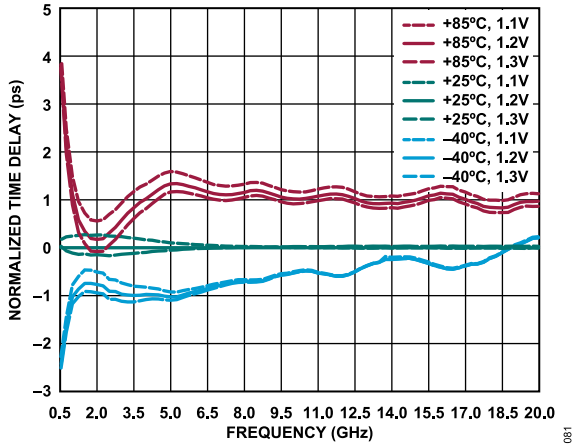

Figure 73. Normalized Time Delay vs. Frequency over Temperature and Supply Voltage, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

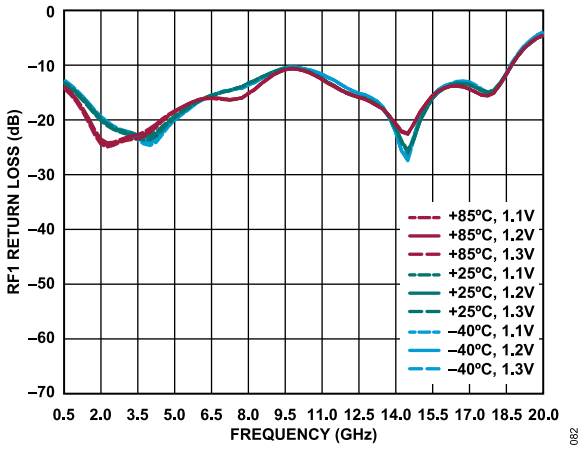

Figure 74. RF1 Return Loss vs. Frequency over Temperature and Supply Voltage, Time Delay Range 0

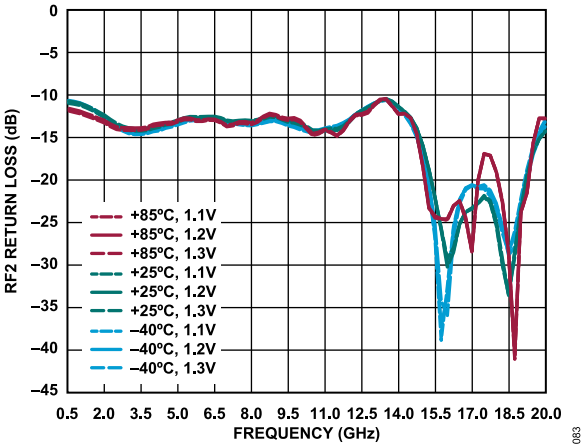

Figure 75. RF2 Return Loss vs. Frequency over Temperature and Supply Voltage, Time Delay Range 0

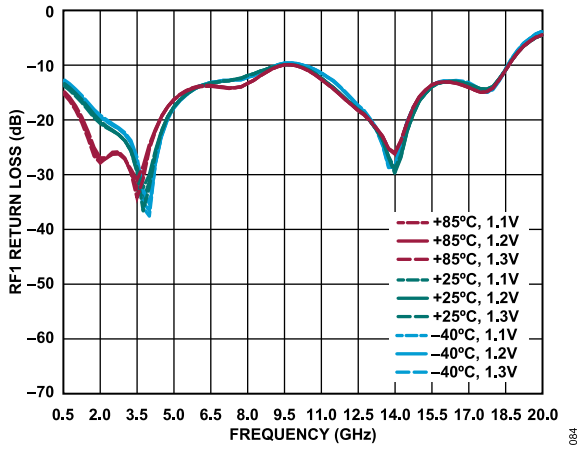

Figure 76. RF1 Return Loss vs. Frequency over Temperature and Supply Voltage, Time Delay Range 1

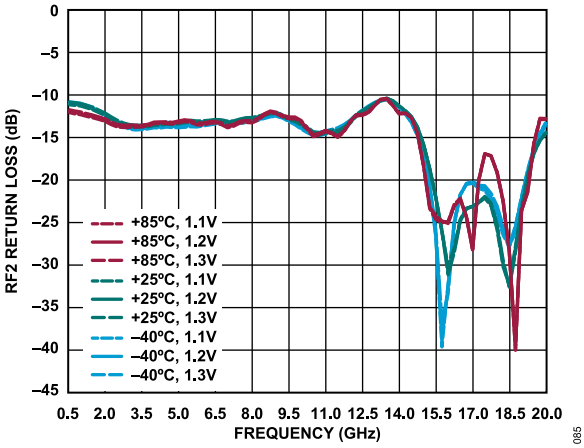

Figure 77. RF2 Return Loss vs. Frequency over Temperature and Supply Voltage, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

POLAR PLOTS

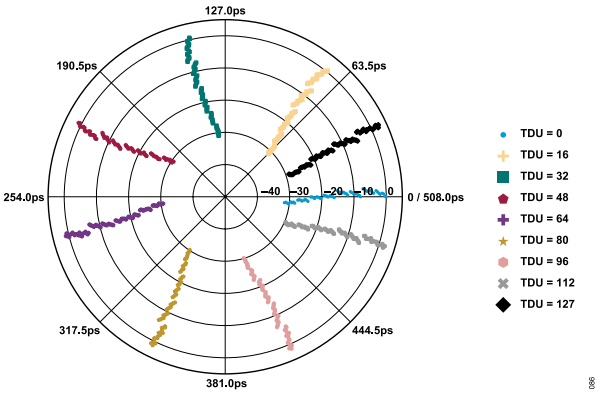

Figure 78. Gain vs. DSA Code over TDU Codes at 500 MHz, Time Delay Range 0

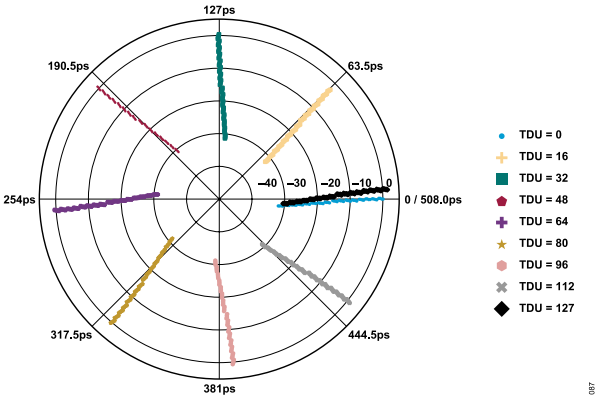

Figure 79. Gain vs. DSA Code over TDU Codes at 2 GHz, Time Delay Range 0

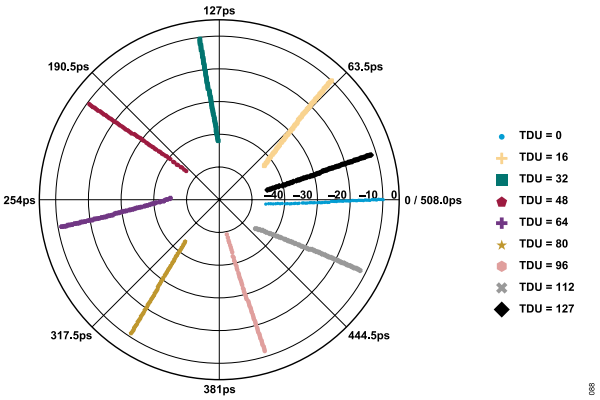

Figure 80. Gain vs. DSA Code over TDU Codes at 10 GHz, Time Delay Range 0

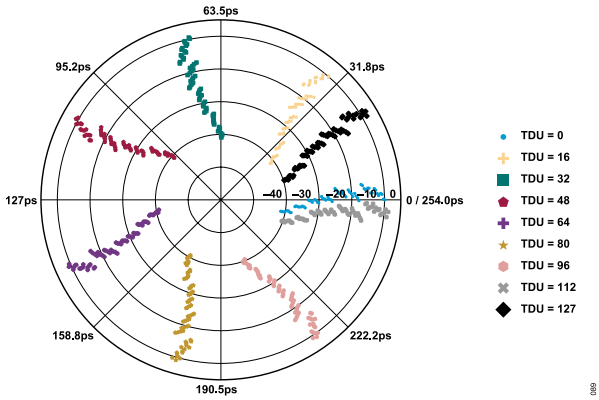

Figure 81. Gain vs. DSA Code over TDU Codes at 500 MHz, Time Delay Range 1

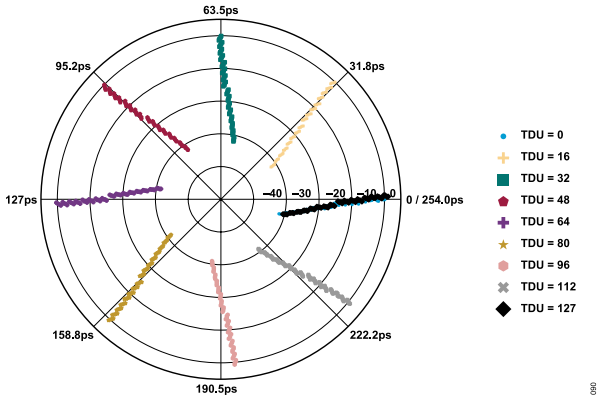

Figure 82. Gain vs. DSA Code over TDU Codes at 2 GHz, Time Delay Range 1

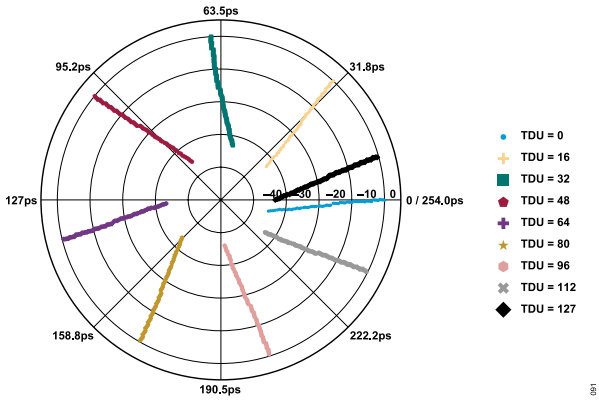

Figure 83. Gain vs. DSA Code over TDU Codes at 10 GHz, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

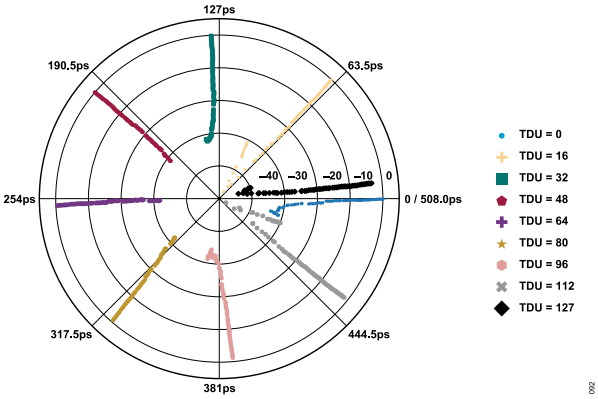

Figure 84. Gain vs. DSA Code over TDU Codes at 18 GHz, Time Delay Range 0

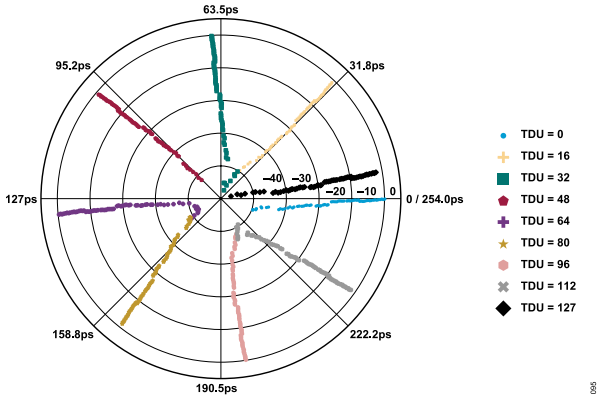

Figure 87. Gain vs. DSA Code over TDU Codes at 18 GHz, Time Delay Range 1

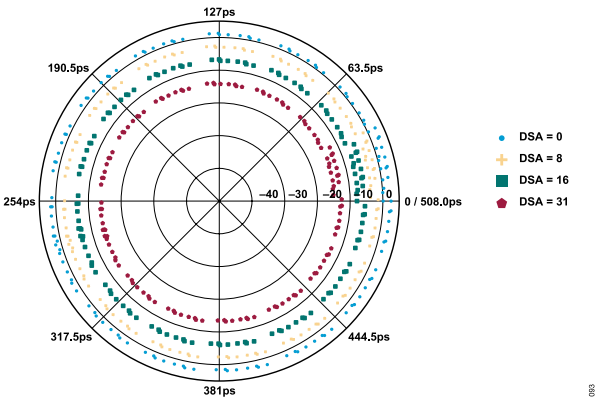

Figure 85. Time Delay vs. TDU Code over DSA Codes at 500 MHz, Time Delay Range 0

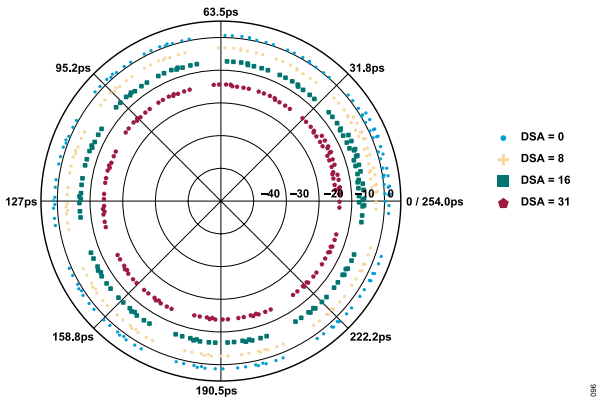

Figure 88. Time Delay vs. TDU Code over DSA Codes at 500 MHz, Time Delay Range 1

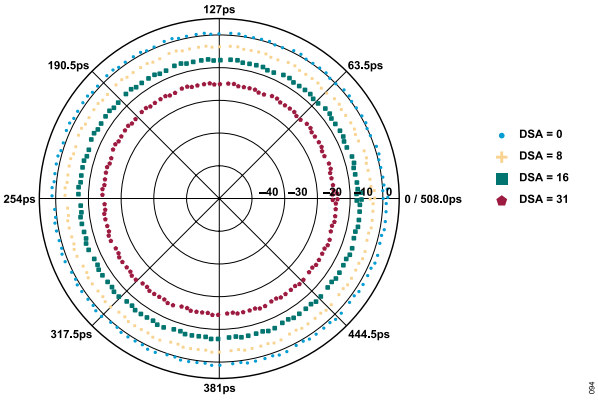

Figure 86. Time Delay vs. TDU Code over DSA Codes at 2 GHz, Time Delay Range 0

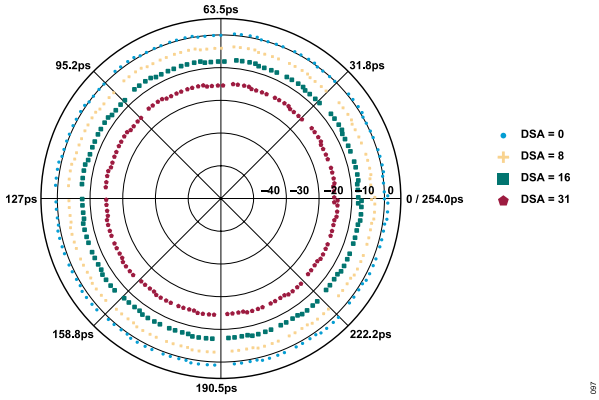

Figure 89. Time Delay vs. TDU Code over DSA Codes at 2 GHz, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

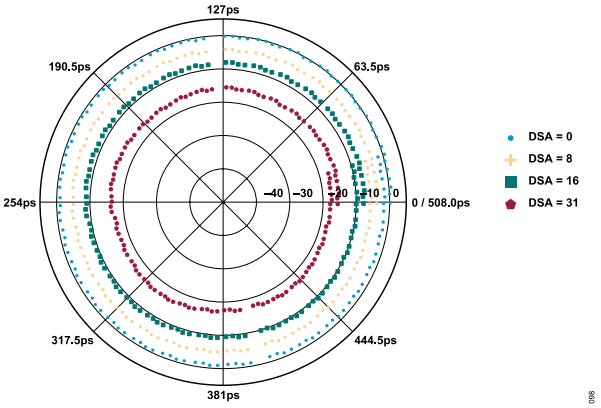

Figure 90. Time Delay vs. TDU Code over DSA Codes at 10 GHz, Time Delay Range 0

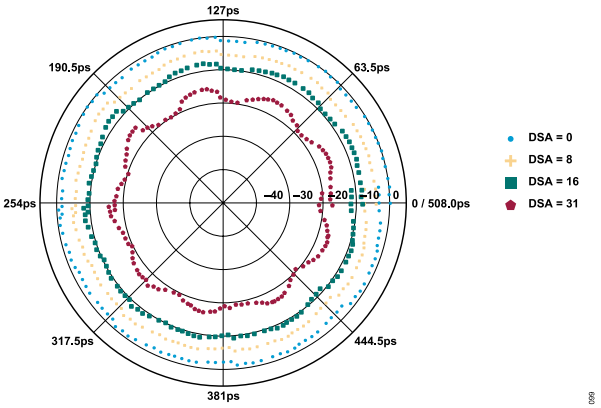

Figure 91. Time Delay vs. TDU Code over DSA Codes at 18 GHz, Time Delay Range 0

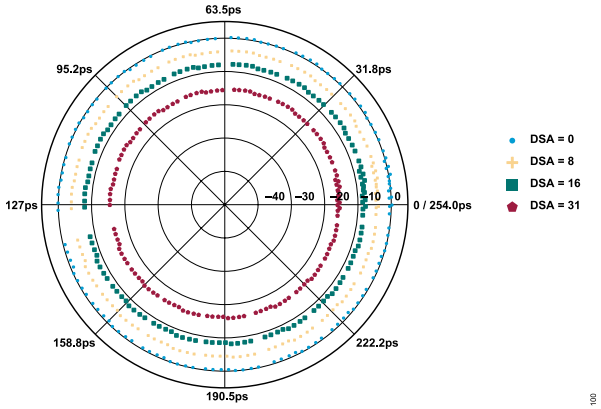

Figure 92. Time Delay vs. TDU Code over DSA Codes at 10 GHz, Time Delay Range 1

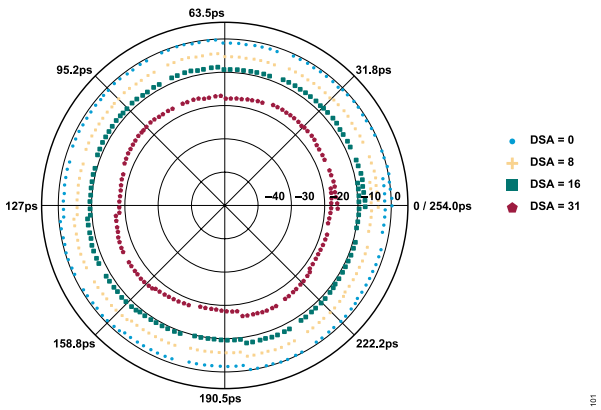

Figure 93. Time Delay vs. TDU Code over DSA Codes at 18 GHz, Time Delay Range 1

TYPICAL PERFORMANCE CHARACTERISTICS

NOISE FIGURE

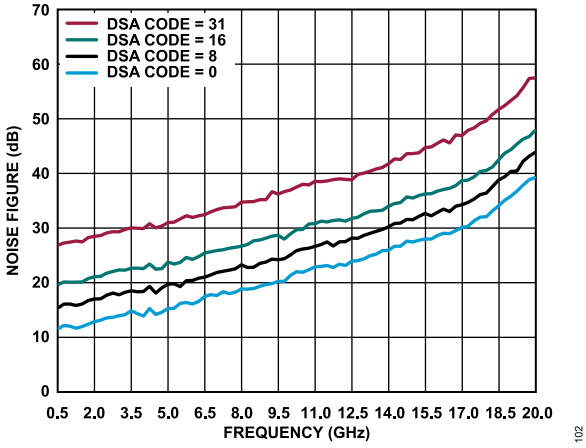

Figure 94. Noise Figure vs. Frequency over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 0

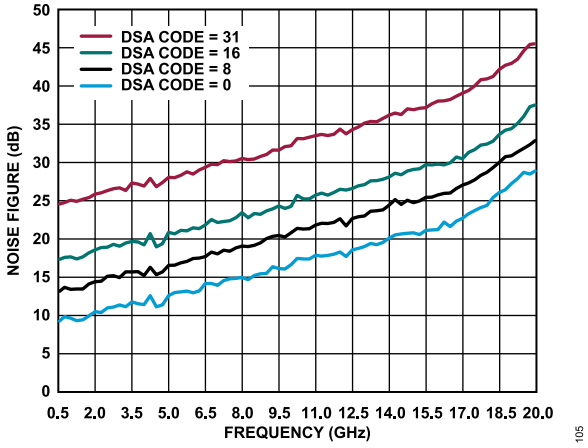

Figure 97. Noise Figure vs. Frequency over DSA Code 0, DSA Code 8, DSA Code 16, and DSA Code 31, Time Delay Range 1

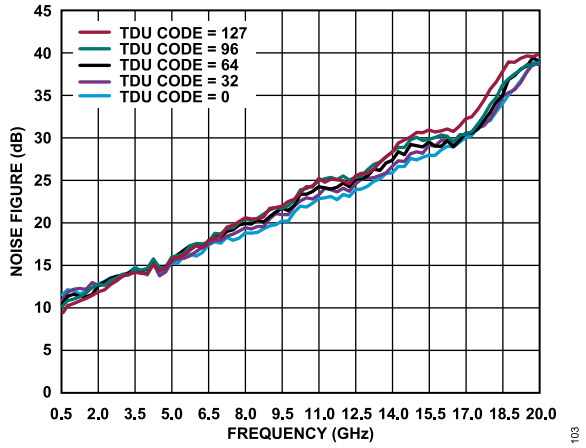

Figure 95. Noise Figure vs. Frequency over TDU Code 0, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 0

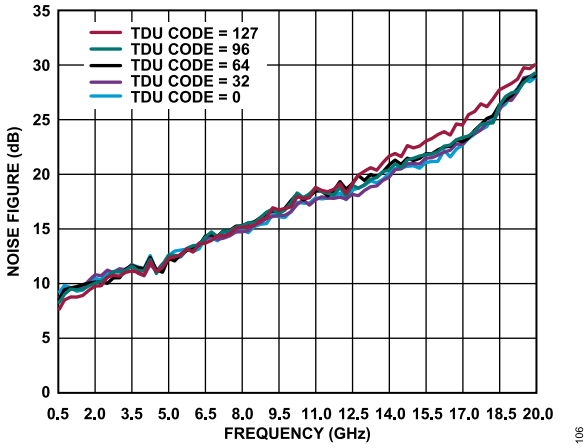

Figure 98. Noise Figure vs. Frequency over TDU Code 0, TDU Code 32, TDU Code 64, TDU Code 96, and TDU Code 127, Time Delay Range 1

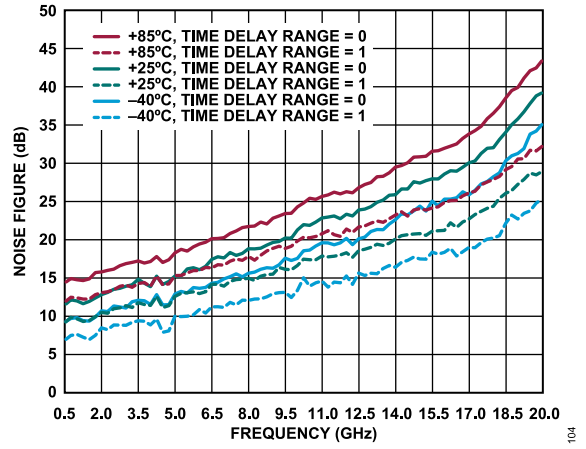

Figure 96. Noise Figure vs. Frequency over Temperature and Time Delay Range

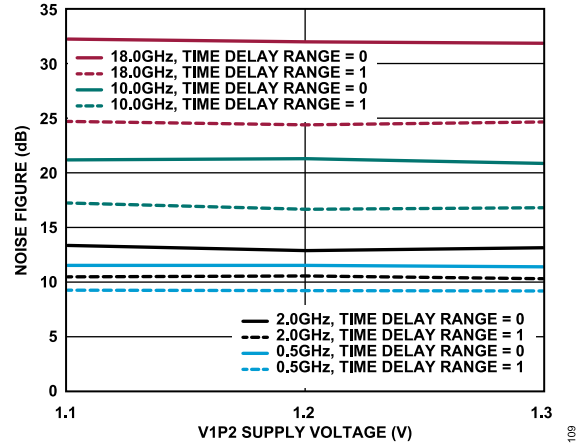

Figure 99. Noise Figure vs. V1P2 Supply Voltage over Frequency and Time Delay Range

TYPICAL PERFORMANCE CHARACTERISTICS

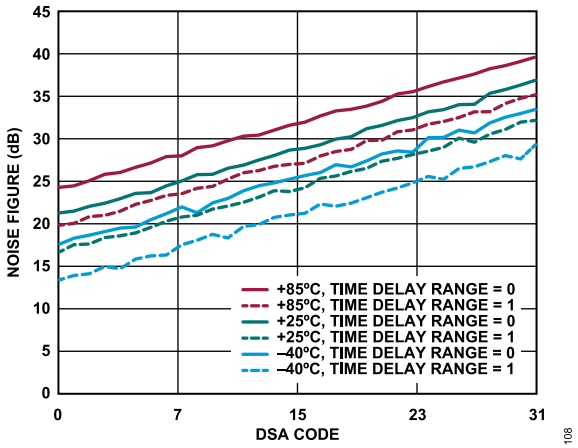

Figure 100. Noise Figure vs. DSA Code over Temperature and Time Delay Range

TYPICAL PERFORMANCE CHARACTERISTICS

COMPRESSION AND LINEARITY

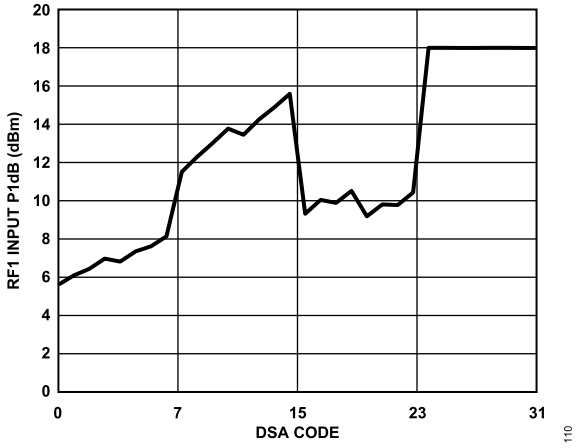

Figure 101. RF1 Input P1dB vs. DSA Code at 10 GHz, Time Delay Range 0

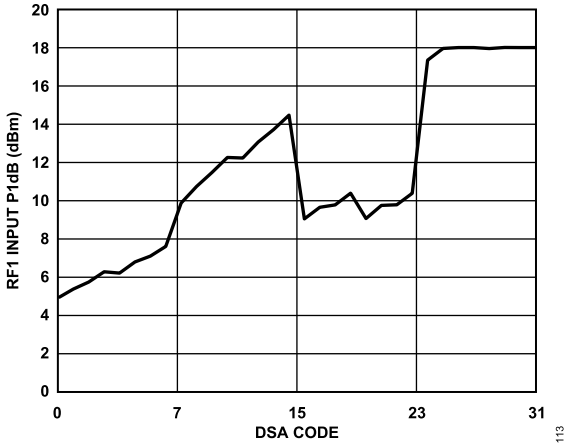

Figure 104. RF1 Input P1dB vs. DSA Code at 10 GHz, Time Delay Range 1

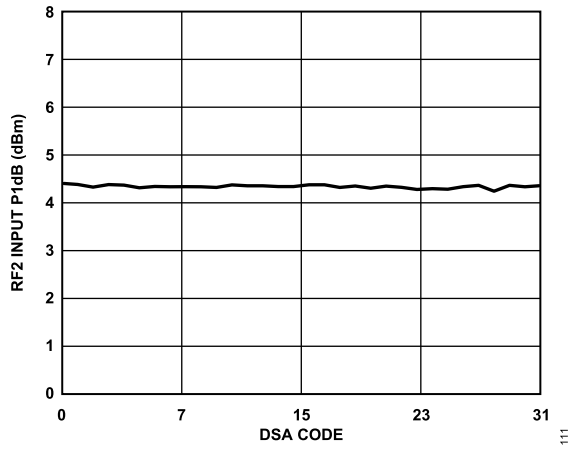

Figure 102. RF2 Input P1dB vs. DSA Code at 10 GHz, Time Delay Range 0

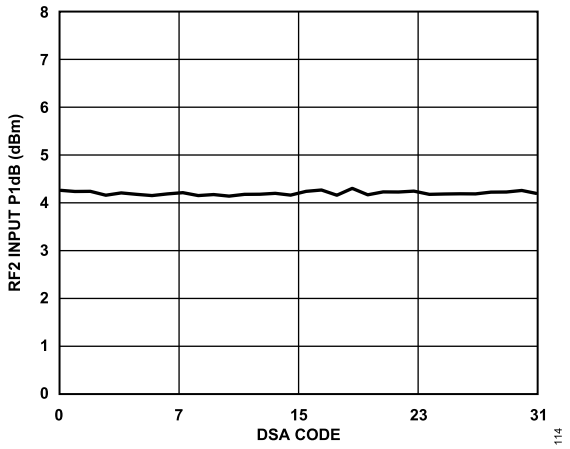

Figure 105. RF2 Input P1dB vs. DSA Code at 10 GHz, Time Delay Range 1

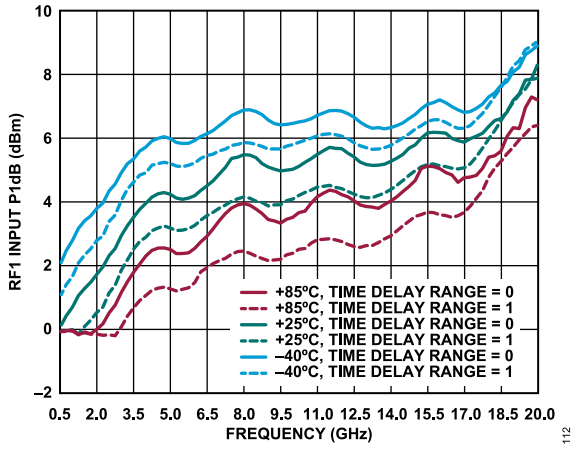

Figure 103. RF1 Input P1dB vs. Frequency over Temperature and Time Delay Range

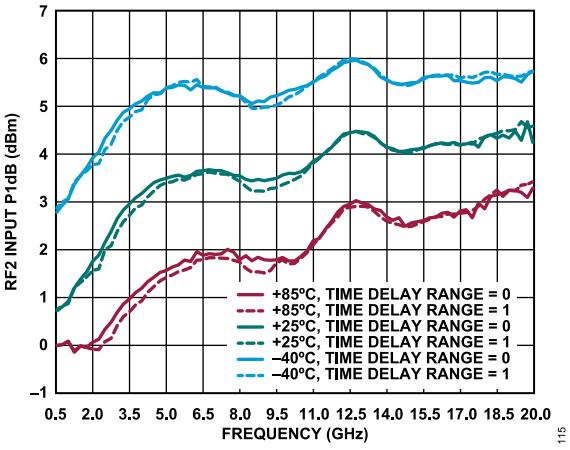

Figure 106. RF2 Input P1dB vs. Frequency over Temperature and Time Delay Range

TYPICAL PERFORMANCE CHARACTERISTICS

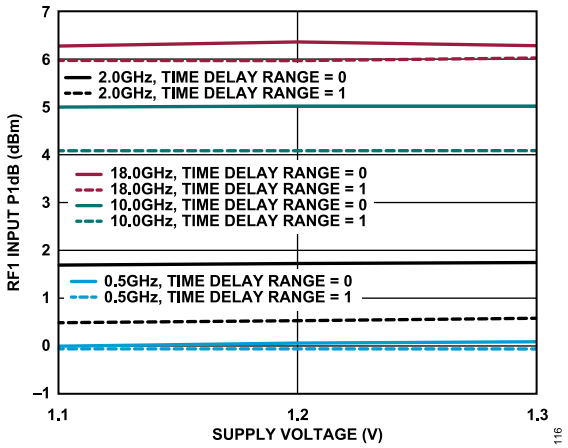

Figure 107. RF1 Input P1dB vs. Supply Voltage over Frequency and Time Delay Range

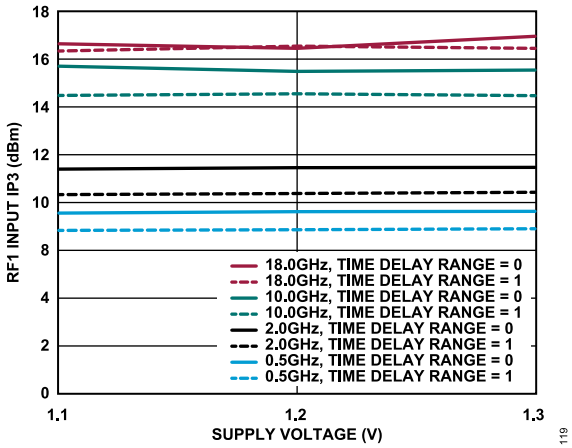

Figure 110. RF1 Input IP3 vs. Supply Voltage over Frequency and Time Delay Range

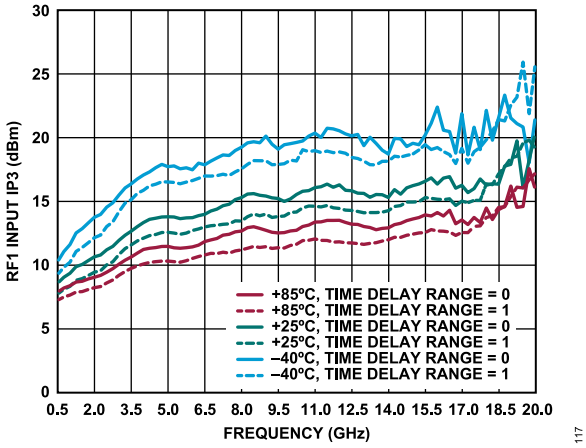

Figure 108. RF1 Input IP3 vs. Frequency over Temperature and Time Delay Range

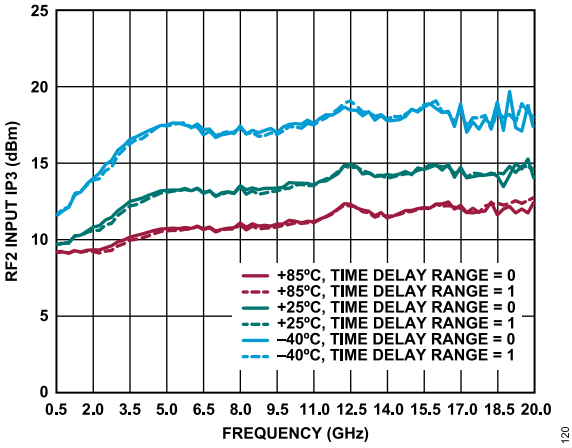

Figure 111. RF2 Input IP3 vs. Frequency over Temperature and Time Delay Range

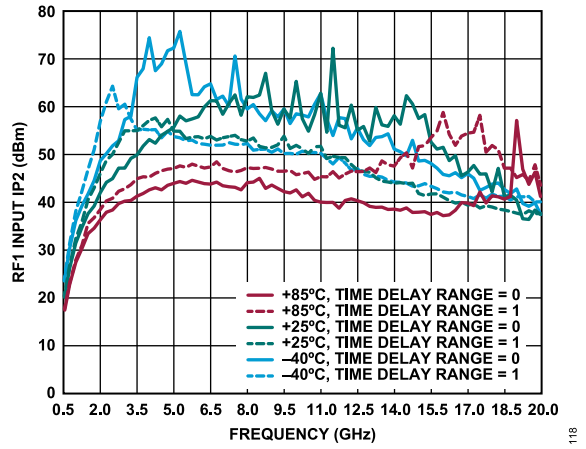

Figure 109. RF1 Input IP2 vs. Frequency over Temperature and Time Delay Range

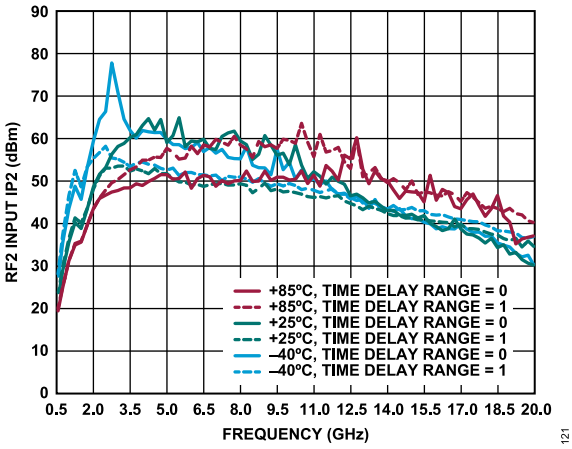

Figure 112. RF2 Input IP2 vs. Frequency over Temperature and Time Delay Range

TYPICAL PERFORMANCE CHARACTERISTICS

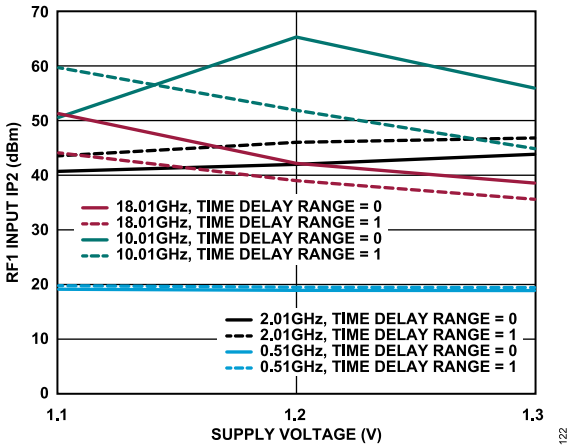

Figure 113. RF1 Input IP2 vs. Supply Voltage over Frequency and Time Delay Range

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AND SETTLING TIME

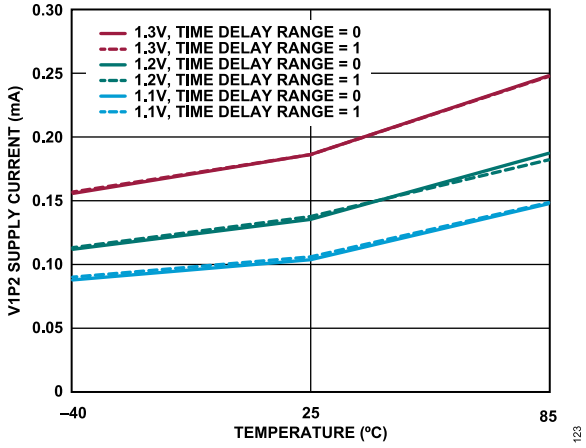

Figure 114. V1P2 Supply Current vs. Temperature over Supply Voltage and Time Delay Range

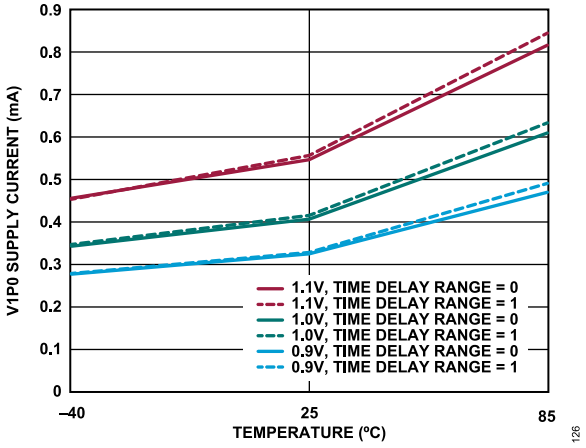

Figure 117. V1P0 Supply Current vs. Temperature over Supply Voltage and Time Delay Range

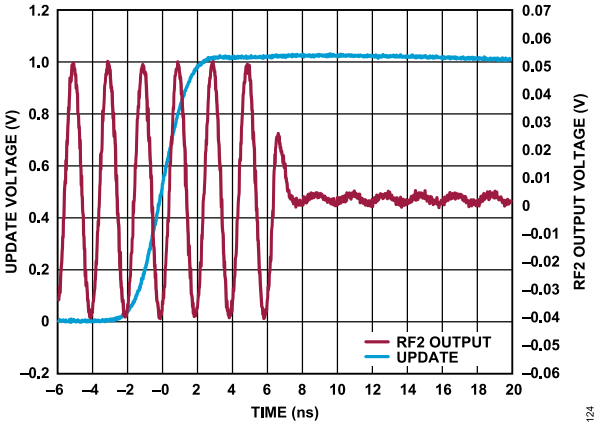

Figure 115. DSA Switching Time from Code 0 to Code 63 at 500 MHz, Time Delay Range 0

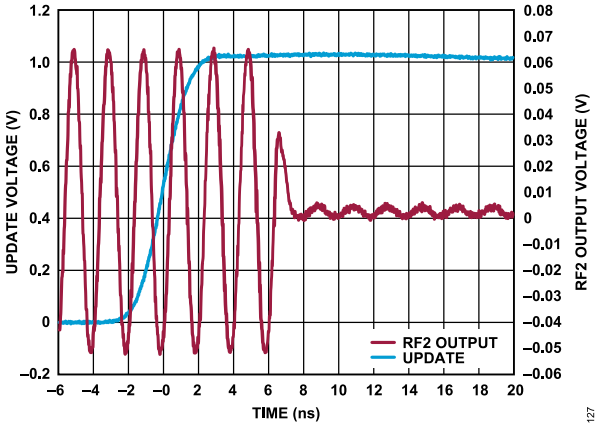

Figure 118. DSA Switching Time from Code 0 to Code 63 at 500 MHz, Time Delay Range 1

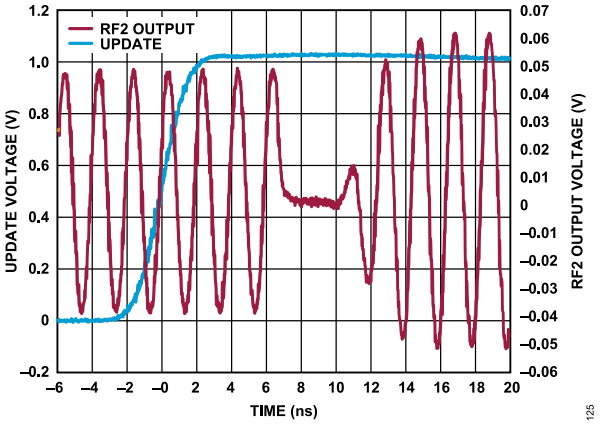

Figure 116. TDU Switching Time from Code 0 to Code 127 at 500 MHz, Time Delay Range 0

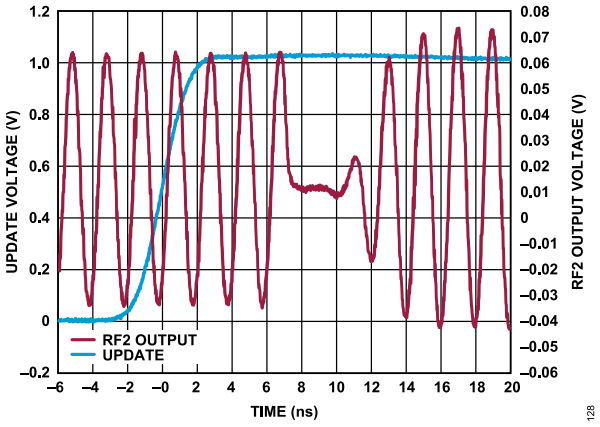

Figure 119. TDU Switching Time from Code 0 to Code 127 at 500 MHz, Time Delay Range 1

EQUIVALENT CIRCUITS

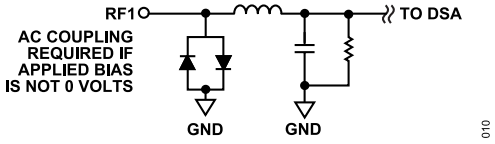

Figure 120. RF1 Equivalent Circuit

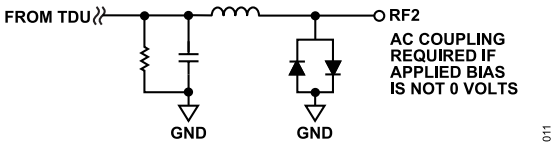

Figure 121. RF2 Equivalent Circuit

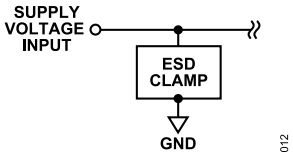

Figure 122. V1P2 and V1P0 Equivalent Circuit

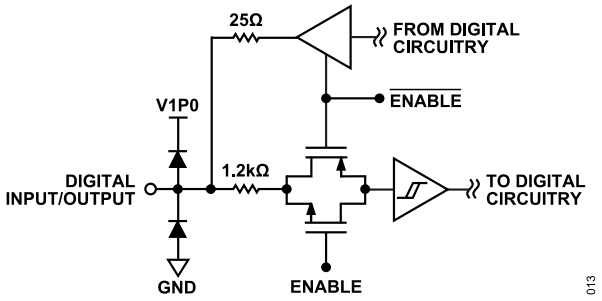

Figure 123. DATA_IO and CSB/CLKO Equivalent Circuit

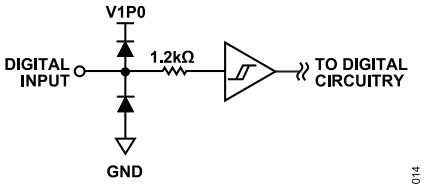

Figure 124. CLK_IN, MODE, and UPDATE Equivalent Circuit

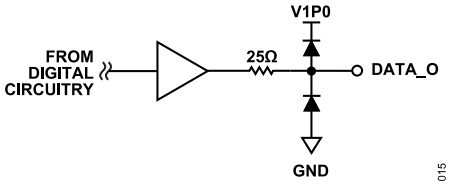

Figure 125. DATA_O Equivalent Circuit

TERMINOLOGY

Attenuation

The quantity of attenuation set by the DSA, which is often abbreviated as ATTN or ATT.

Attenuator

The attenuator is the single DSA unit used in the ADAR4002.

Block Write

A block write is a SPI write to several consecutive registers, wherein only the address of the first register is clocked in, with all subsequent consecutive register addresses omitted from the SPI transaction. See SPI Block Write Mode for more details. Block write can be used with the StreamWrite registers to significantly reduce clock cycles.

Data Load Command

The data load command is a command that transfers all TDU and DSA data from the first rank registers to the second rank registers. This command is initiated by any DATA_LOAD bit in the DSAxx registers or in Register 0x98, or with the short control command using the data load command bits, 0b110.

Digital Stepped Attenuator (DSA)

The DSA is used in the ADAR4002 to set the attenuation.

First Rank Registers

The first rank registers are a set of registers where the SPI data is initially stored when clocked into the ADAR4002. A data load command is needed to transfer the TDU and DSA data from the first rank registers to the second rank registers.

Second Rank Registers

The second rank registers are the second set of registers that hold the TDU and DSA data, which is applied directly to the TDU and DSA blocks from these registers. A data load command is needed to transfer the TDU and DSA data from the first rank registers to the second rank registers.

Sequencer

The sequencer is a state machine that increments or decrements the TDU and DSA state one position per update command. The sequencer sources TDU and DSA data from the second rank registers and is used in SPI mode only. There are two selectable sequencers, Sequencer A and Sequencer B.

Sequencer A

Sequencer A is one of the two sequencers that the ADAR4002 features. Sequencer A has its own dedicated start and stop sequence values found in Register 0x10 (SEQUENCERA_START) and Register 0x11 (SEQUENCERA_STOP), respectively. Sequencer A has full access to the second rank register TDU and DSA data.

Sequencer B

Sequencer B is one of the two sequencers that the ADAR4002 features. Sequencer B has its own dedicated start and stop TDU and DSA state sequence values found in Register 0x12 (SEQUENCERB_START) and Register 0x13 (SEQUENCERB_STOP), respectively. Sequencer B has full access to the second rank register TDU and DSA data.

Sequencer Direction

The sequencer direction is the ascension or descension through the TDU and DSA register addresses that contain the time delay and attenuation data.

Sequencer Reset Command

The sequencer reset command resets the indicated sequencer to its start TDU and DSA state.

Shift Register Mode

The shift register mode is one of the two digital modes wherein the TDU and DSA data is clocked into the first 14-bit shift register using the CLK_IN and DATA_IO pins, and is then loaded into the second 14-bit shift register by a pulse on the UPDATE pin. Pull the MODE pin logic high to put the ADAR4002 into shift register mode.

Short Control Command

A short control command is a 6-bit SPI write, initiated by a 0b11 in the first two bits clocked in, that can perform eight unique actions including sequencer selection, sequencer reset, sequencer direction, data load command, and an update command. More information can be found in Figure 7 and Table 4.

SPI Mode

SPI mode is one of the two digital modes wherein the TDU and DSA data, as well as all the control, is done by the SPI port. Pull the MODE pin logic low to put the ADAR4002 into SPI mode.

StreamWrite

A StreamWrite is a SPI write to a register or registers between 0x60 and 0x97. These registers contain the same TDU and DSA data found within Register 0x20 to Register 0x5F; however, the data flows from one register to the next, which reduces the needed clock cycles. A change to the TDU and DSA data in Register 0x60 to Register 0x97 is automatically reflected in Register 0x20 to Register 0x5F, and vice versa, when the SPI transaction is complete, which is not to be confused with the block write functionality, which eliminates the need to clock in the address data after the first register of consecutive register writes. StreamWrite can be used with block write.

Time Delay

The time delay of the ADAR4002 is from RF1 to RF2, either absolute or normalized. The time delay is varied by the TDU.

TERMINOLOGY

Time Delay Range

The time delay range is the total available time delay of the TDU. The time delay is user programmable to either 508 ps or 254 ps via Bit 7 of each TDxx register.

Time Delay Unit (TDU)

The TDU is used in the ADAR4002 to set the time delay.

TDU and DSA

The TDU and DSA are the variable time delay and attenuation block that includes one DSA and one TDU.

Update Command

The update command is a command that advances the selected sequencer while in SPI mode.

Variable Amplitude and Phase (VAP) Block

The VAP block is a block that contains a programmable TDU and DSA.

VAP Vector

The VAP vector is the 14 bits of combined data that make up a single TDU and DSA state.

THEORY OF OPERATION

RF PATH

The ADAR4002 is a low power, broadband, bidirectional, single-channel IC for use in applications requiring programmable time delay and/or attenuation. Both the RF1 and RF2 ports are internally matched to 50 Ω. The ADAR4002 is intended to operate over a frequency range of 2 GHz to 18 GHz, but the device can operate down to 500 MHz and up to 19 GHz with limited degradation in performance. The DSA is connected to the RF1 port, while RF2 is connected to the TDU. Driving the RF1 port allows improved P1dB performance vs. DSA code, relative to driving RF2. See the Typical Performance Characteristics section for more detail.

TDU AND DSA

The TDU has 7-bit resolution, with two selectable time delay ranges, 508 ps and 254 ps, which creates step sizes of 4 ps and 2 ps, respectively. Time Delay Range 0 is recommended for applications extending down to 2 GHz where 508 ps of time delay provides approximately 365° of phase shift. While Time Delay Range 1 is recommended for applications 4 GHz and above, where 254 ps of time delay provides 365° of phase shift at 4 GHz. Range 1 also provides less loss relative to Range 0, which is advantageous as the ADAR4002 insertion loss increases with frequency. Table 9 shows a summary of the time delay control.

Table 9. Time Delay Control Summary

Range	Maximum Time Delay	Step Size
0	508 ps	4 ps
1	254 ps	2 ps

The DSA has 6-bit resolution with an attenuation range of 31.5 dB and step size of 0.5 dB.

The DSA and TDU are digitally controlled by either the register and on-chip sequencers (SPI mode) or the shift register mode. Both modes clock data into and out of the chip via a shared set of digital pins. The MODE pin controls the digital mode of the chip. See the Digital Section for more details.

THEORY OF OPERATION

DIGITAL SECTION

The ADAR4002 contains registers for overall control, DSA data, and TDU data storage. There are two sequencers that can independently sequence through the several DSA and TDU states found in the registers. Each sequencer has its own programmable start and stop value. The ADAR4002 has two digital modes that the device can operate in SPI mode or shift register mode. Both modes are described in the Digital Modes and Interface section.

DIGITAL MODES AND INTERFACE

The ADAR4002 is in SPI mode when the MODE pin is held at logic low. In SPI mode, the TDU and DSA values are set via the 3-wire or 4-wire SPI bus (the CSB/CLKO, CLK_IN, DATA_IO, and DATA_O pins). Note that in SPI mode, the CSB/CLKO pin function is the CSB pin. In addition, the 3-wire SPI does not use the DATA_O pin, and the DATA_IO becomes a bidirectional data input and output pin. Two ranks of registers are present, loaded from first rank to second rank on a data load command, either via a SPI write or a short control command. Advancing the TDU and DSA state to the next state using the sequencer is done either with a standard 24-bit SPI write, a 6-bit short control command, or a pulse of the UPDATE pin. For multiple ADAR4002 chips to share the SPI lines and enable individual chip control, each chip must have at least its own dedicated CSB/CLKO, CLK_IN, or DATA_IO line to be unique. For the fastest parallel data transfer, multiple ADAR4002 chips can share CSB/CLKO and CLK_IN, with different DATA_IO for each chip.

When the MODE pin is held at logic high, the ADAR4002 is in shift register mode. In this mode, the TDU and DSA values are set via the 2-wire serial interface, with the CLK_IN and DATA_IO pins, along with the UPDATE pin that serves as the data load from the first shift register to the second shift register. The output pins, CSB/CLKO and DATA_O, allow for a daisy-chain connection of multiple ADAR4002 chips, and the DATA_O pin of one chip drives the DATA_IO pin of the next chip, and the CSB/CLKO pin drives the CLK_IN pin of the next chip. Changing the TDU and DSA to a different state is accomplished by clocking new TDU and DSA data in on the CLK_IN and DATA_IO pins, and then strobing the UPDATE pin after the 14th data bit is clocked in. Shift register mode allows the user to configure multiple chips with zero digital overhead, that is, there are no address bits nor padding bits, and programs the chips in a serial daisy-chain connection as shown in Figure 130. The length of this chain is only limited by the delay through the chain, or the number of clock cycles required to program all of the ADAR4002 chips.

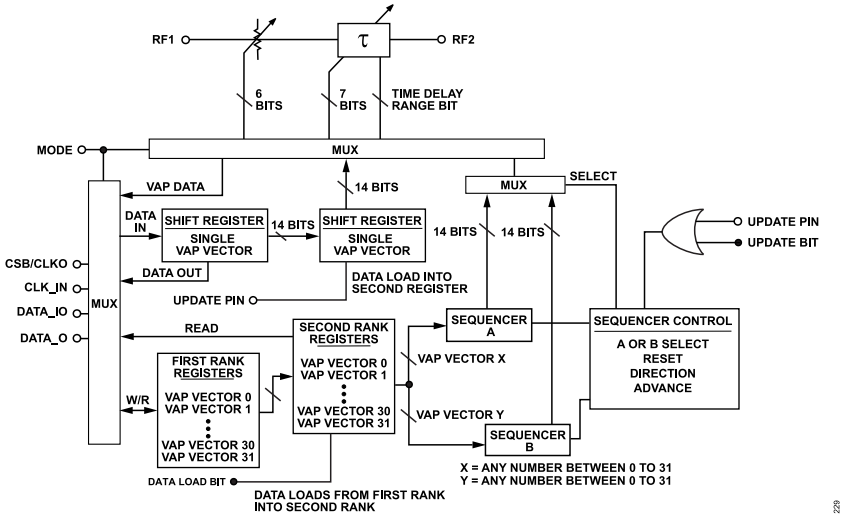

Figure 126. Digital Block Diagram

THEORY OF OPERATION

SPI TRANSACTION PROTOCOLS

The ADAR4002 in SPI mode provides three different possible SPI transaction protocols, which include the following:

- Standard Analog Devices, Inc., 24-bit SPI write and read protocols
- SPI block write and read mode
- Short control command

These first two protocols follow the Analog Devices standard 16-bit address header followed by an 8-bit data-word, or several consecutive 8-bit data-words for the SPI block write and read mode. These two protocols are used for all writes to the registers. Note that for 4-wire SPI readback on the DATA_O pin, DATA_O must be enabled by setting Bits[4:3] high in Register 0x00. Otherwise, the ADAR4002 is in 3-wire SPI mode with Bits[4:3] low in Register 0x00. By default upon power-up, the ADAR4002 is in 4-wire SPI mode. Timing diagrams for the Analog Devices SPI mode are shown in Figure 2 through Figure 6. The register map is shown in Table 14.

Short control commands are initiated by unique values set on the first two bits that are clocked in on the SPI and make the transaction length 6 bits. If the first two data bits are 0b11 and the SPI transaction is 6 bits in length, this command is recognized as a short control command. Following the leading 0b11 bits, the decoding structure of the short control command is shown in Table 4.

SPI MODE

In SPI mode, registers provide storage of up to 32 TDU and DSA states. There are two sequencer state machines (Sequencer A and Sequencer B) that allow the user to sequentially step through the 32 states. The sequencers are independent of each other, each having separate start and stop values, as well as a sequence direction. The user can switch between the sequencers, change direction on either sequencer, or reset either sequencer to its start value at any time using a SPI write or short control command.

Two ranks of registers store the TDU and DSA data. The sequencers source their data from the second rank registers, which allows the data in the first rank registers to be completely rewritten while simultaneously sequencing through the second rank register data. This dual-rank, two sequencer setup is flexible and ideal for situations with a set of transmit TDU and DSA values and a set of receive TDU and DSA values, as well as for situations in which the user wants to write a future set of TDU and DSA values while simultaneously sequencing through a previously written set.

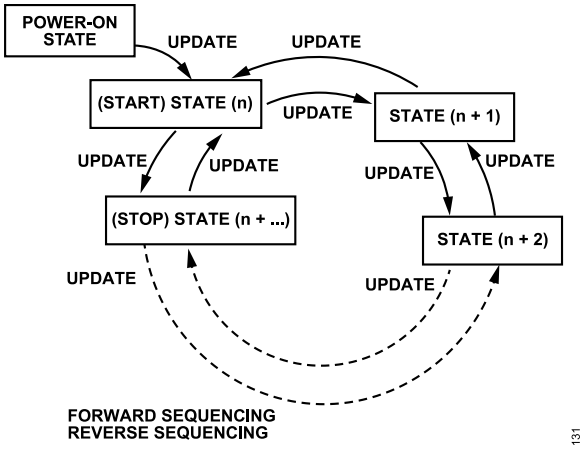

Figure 127. Sequencer State Machine Block Diagram

DATA LOAD

All the TDU and DSA data (the 32 TDU and DSA states) from the first rank registers are loaded to the second rank registers by asserting any DATA_LOAD bit in each DSA register (Bit 0) or in Register 0x98, or by using the short control command. The DATA_LOAD bit automatically clears on the next CLK_IN edge after being set in any of the DSA registers, Register 0x98, or if accomplished with a short control command.

The active edge for the DATA_LOAD command is the next rising edge of CLK_IN following the assertion of the DATA_LOAD bit. If a DATA_LOAD command is to be immediately followed by an update using the UPDATE pin, an extra clock cycle must be added after the DATA_LOAD bit is asserted, to ensure the DATA_LOAD command has taken effect before the update rising edge. The extra clock cycle can be while the CSB/CLKO is low or high. If the next command is any SPI transaction, no extra SPI clock is necessary.

UPDATE

While in SPI mode, to apply TDU and DSA data from the second rank registers to the actual TDU and DSA blocks, an update command is required, which applies whether the user is initially loading the TDU and DSA state that corresponds to the sequencer start value or advancing the sequencer to its next TDU and DSA state.

An update command is accomplished by asserting the UPDATE bit in Register 0x99, using the update short control command or by a rising edge (low-to-high) on the UPDATE pin.

The active edge that triggers the loading of the TDU and DSA state from the second rank registers to the TDU and DSA blocks varies. If issuing an update command with a regular SPI write, the active edge is the eighth CLK_IN rising edge on the eighth data bit. The active edge on an update short control command is the CSB/CLKO rising edge, which completes the command. The active edge on the UPDATE pin is any rising edge.

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The UPDATE bit auto clears on the next CLK_IN edge after being set, whether in Register 0x99 or via the short control command.

SHIFT REGISTER MODE

In shift register mode, two sets of 14 serially connected, storage flip-flops allows writing bits during RF activity, without upsetting the current data applied to the TDU and DSA blocks. A rising edge on the UPDATE pin loads the bits from the first shift register flip-flops to the second set, which holds and applies the data to the DSA and TDU blocks.

This mode offers zero overhead bits for addresses and a minimum of 14 bits per chip for time delay and attenuation control, but without any sequencer capability or stored TDU and DSA values (other than in the two sets of flip-flops). Readback can be done via the DATA_O pin, which is connected to the output of the 14^{TH} flip-flop of the first shift register.

The output of one ADAR4002 (CSB_CLKO and DATA_O) can drive another ADAR4002 (CLK_IN and DATA_IO) directly. Note that, there is a minimal 2 ns propagation delay between CLK_IN and the CSB_CLKO and DATA_O outputs. The required number of clock cycles to set the TDU and DSA data for an individual ADAR4002 is 14 clocks, which is as follows:

- 1 bit for the time delay range
- 7 bits for the time delay
- 6 bits for the DSA attenuation

The total number of clock cycles for N ADAR4002 chips is N x 14 clock cycles. A two chip example is shown in Figure 8. The length of the chain is only set by the accumulated delay through the chain or acceptable write length for each write. For simultaneous data loading, a single update signal to all chips is recommended, with appropriate delay-matched buffering of the signal as required to each chip.

See Figure 131 for an example connection schematic in shift register mode.

SPI REGISTERS

All configuration registers are detailed in the register summary (see Table 14). These configuration registers include the standard Analog Devices SPI setup registers, sequencer setup and readback registers, start and stop pointers for the sequencer state machines, and the 32 TDU and DSA states for the sequencers. Table 10 outlines the addresses of each register section.

Table 10. Configuration Register Outline

Register Section	Start Address	Stop Address
Analog Devices SPI Setup	0x00	0x0F
Sequencer Configuration	0x10	0x18
TDU and DSA Data	0x20	0x5F
StreamWrite TDU and DSA Data	0x60	0x97
Global DATA_LOAD and UPDATE	0x98	0x99

Table 10. Configuration Register Outline (Continued)

Register Section	Start Address	Stop Address
Second Rank Readback	0xA0	0xDF
TDU and DSA Readback	0xF0	0xF1

The following sections outline some commonly used registers.

Register 0x00: SPI Configuration

The SPI configuration register contains soft-reset functionality (sets all register values to their default), setup for LSB first bit orientation, address ascension and descension, and activation of the DATA_O pin, as follows:

- Soft reset: Bit 7 and Bit 0
- LSB first: Bit 6 and Bit 1
- Address ascension and descension: Bit 5 and Bit 2
- DATA_O enable and disable: Bit 4 and Bit 3

By default at power-up or on a soft reset, this register is set to 0x3C, which sets the address ascension and enables the DATA_O pin.

Register 0x20 Through Register 0x5F: Time Delay and Attenuation

The time delay control bits are a 7-bit data-word along with a time delay range selection bit. The time delay range is controlled with Bit 7 set to 0 for standard resolution and a 508 ps maximum time delay and Bit 7 set to 1 for high resolution and a 254 ps maximum time delay.

The decoding of the time delay bits (FIRSTRANK_TIMEDELAYxx, Bits[6:0]) on each time delay register (Register TDxx) is the following:

- Minimum time delay: 0x00
- Maximum time delay: 0x7F

The attenuator bits (FIRSTRANK_DSAxx, Bits[7:2]) are a 6-bit word that provides 0.5 dB resolution with 31 dB of attenuation range.

The decoding of the attenuator bits (FIRSTRANK_DSAxx, Bits[7:2]) on each DSA register (Register DSAxx) is the following:

- Minimum attenuation: 0x00
- Maximum attenuation: 0x3F

Register 0x60 Through 0x97: Streamwrite Time Delay and Attenuation

The ADAR4002 allows a streamwrite of the time delay range selection bit, the 7-bit time delay value, and the 6-bit DSA attenuation value, with no extra zero padding bits. This streamwrite functionality is found in Register 0x60 through Register 0x97. If writing to many TDU and DSA values at once in SPI block write format and using the streamwrite registers, repeated address bits as well as excess

THEORY OF OPERATION

zero padding bits can be eliminated from the SPI transaction to reduce data transfer time.

Note that any changes in these streamwrite registers also change the corresponding data in the regular TDU and DSA data registers (Register 0x20 through Register 0x5F), and vice versa. Also note that the data is arranged in an ascending address block write. Bit 5 and Bit 2 must be asserted high in Register 0x000 for address ascension.

Register 0xF0 and Register 0xF1

The current time delay and DSA values being applied to the TDU and DSA blocks can be read back from Registers 0xF0 and Register 0xF1.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADAR4002 has two power supply domains: a 1.2 V supply for the RF and analog circuitry and an 1.0 V supply for the digital blocks. These power supply domains must be decoupled to ground as shown in Figure 128.

There are only two RF pins: RF1 and RF2 (Pin 2 and Pin 9, respectively). These pins are matched to 50 Ω and thus must be connected to a transmission line with a characteristic impedance of 50 Ω. The RFx pins each have a pair of ground pins surrounding them, which creates a ground-signal-ground type connection, making it simple to interface with PCB transmission lines. RF1 and RF2 must be AC-coupled so that their internal bias is not disturbed.

The MODE pin controls the state of the digital mode of the partADAR4002 as follows:

- When MODE is pulled to ground, the ADAR4002 is in SPI mode.
- When MODE is pulled to 1 V, the ADAR4002 is in shift register mode.

The CLK_IN, CSB/CLKO, DATA_IO, and DATA_O constitute the SPI or shift register pins. When in SPI mode, the functions of these pins are as follows:

- CLK_IN is the SPI clock input.
- CSB/CLKO is the: SPI chip select input.
- DATA_IO is the SPI data input only in a 4-wire SPI protocol, or the SPI data input and output in a 3-wire SPI protocol.
- DATA_O is the SPI data output in a 4-wire SPI protocol.

Note that the ADAR4002 has no device address pins, so to share SPI lines and allow individual control, each ADAR4002 must have its own dedicated CSB/CLKO line, CLK_IN line, or DATA_IO line, to be individually addressed while in SPI mode (see Figure 129). For the fastest, parallel data transfer, multiple ADAR4002 chips can share CSB/CLKO and CLK_IN with different DATA_IO for each chip.

When the ADAR4002 is in shift register mode, the functions of these pins are as follows:

- CLK_IN is the clock input.
- CSB_CLKO is the clock output.
- DATA_IO is the data input.
- DATA_O is the data output.

The shift register allows the user to daisy-chain several ADAR4002 chips together. A single shift register write can contain all the DSA and TDU data of the daisy-chained chips. This setup is shown in Figure 131.

The UPDATE pin advances the sequencer to the next DSA and TDU value if in SPI mode or loads the DSA and TDU data if in shift register mode.

All digital pins can be driven to 1.2 V without any issues. For additional information, see the Logic Voltages Greater Than 1.2 V section.

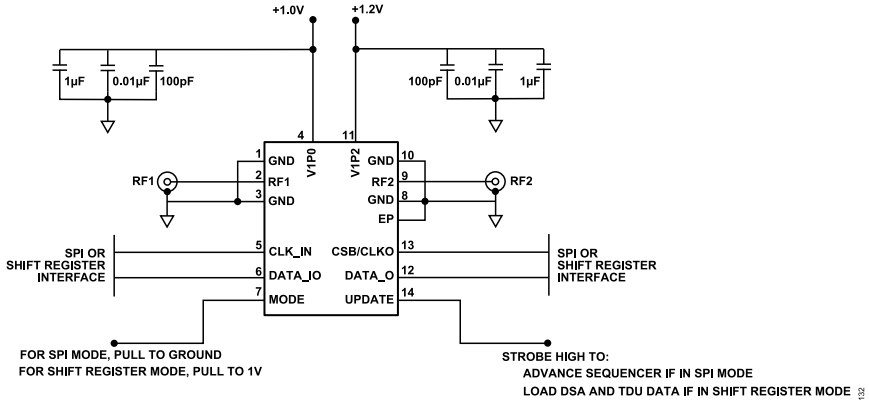

Figure 128. Basic Connection in SPI Mode

APPLICATIONS INFORMATION

DEVICE SETUP

Basic SPI Setup with Single DSA and TDU Register

To set the ADAR4002 up in SPI mode and use both sequencers, first ensure that the MODE pin is pulled to ground. Then, perform the following writes in Table 11. To change DSA and TDU data write new data into Register 0x20 and Register 0x21, followed by a data load and update. This setup is useful when first learning the device and/or for debugging.

Table 11. SPI Setup for Single Register

Address	Data	Notes
0x00	0xBD	Soft reset, MSB first, DATA_O enabled
0x00	0x18	SDO active (for 4-wire SPI)
0x10	0x00	Sequencer A start at 0
0x11	0x00	Sequencer A stop at 0
0x14	0x11	Sequencer A and Sequencer B direction ascending
0x16	0x00	Sequencer A selection (data = 0x01 for Sequencer B selection)
0x20	0x00	Minimum time delay for TD00, Time Delay Range 0
0x21	0x00	Minimum attenuation for DSA00
0x98	0x01	Load data from the first rank to second rank registers
0x99	0x01	Update, applies data to DSA and TDU blocks

SPI Setup and Example Use of Sequencers

To set the ADAR4002 up in SPI mode and use both sequencers, first ensure that the MODE pin is pulled to ground. Then, perform the following writes in Table 12.

Table 12. SPI Setup and Example Use of Sequencers

Address	Data	Notes
0x00	0xBD	Soft reset, MSB first, DATA_O enabled
0x00	0x18	SDO active (for 4-wire SPI)
0x10	0x00	Sequencer A start at 0
0x11	0xF	Sequencer A stop at 15
0x12	0x01	Sequencer B start at 16
0x13	0x1F	Sequencer B stop at 31
0x14	0x11	Sequencer A and Sequencer B direction ascending
0x16	0x00	Select Sequencer A
0x20 to 0x5F	0xXX	Write desired data to all 32 TDU and DSA states
0x98	0x01	Load data from the first rank to second rank registers
0x99	0x01	Update, applies TD00 and DSA00 data to the DSA and TDU blocks
0x99	0x01	Update, applies TD01 and DSA01 data to the DSA and TDU blocks
0x99	0x01	Update, applies TD02 and DSA02 data to the DSA and TDU blocks
0x16	0x01	Select Sequencer B
0x99	0x01	Update, applies TD016 and DSA16 data to the DSA and TDU blocks
0x99	0x01	Update, applies TD017 and DSA17 data to the DSA and TDU blocks
0x99	0x01	Update, applies TD018 and DSA18 data to the DSA and TDU blocks
0x15	0x11	Reset both sequencers
0x16	0x00	Select Sequencer A
0x99	0x01	Update, applies TD00 and DSA00 data to the DSA and TDU blocks

Shift Register Setup

To set the ADAR4002 to shift register mode, first pull the MODE pin to logic high. Then, use the CLK_IN and DATA_IO pins for the clock and data input, respectively. Clock the desired 14-bit TDU and DSA data sequence as shown in Figure 8, followed by a pulse on the UPDATE pin to load the data from the first shift register to the second shift register, and apply the data to the TDU and DSA.

DIGITAL INTERFACE FOR MULTIPLE CHIP OPERATION

SPI Mode Block Diagram

Figure 129 shows the SPI mode block diagram.

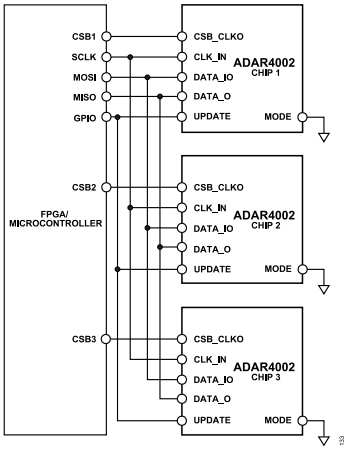

Figure 129. Multiple Chip Configuration in SPI Mode (Mode Pin = Logic Low)

APPLICATIONS INFORMATION

Shift Register Mode Digital Interface Block Diagrams

Figure 130 and Figure 131 show the shift register mode digital interface block diagrams.

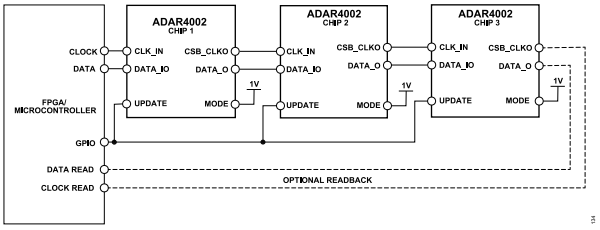

Figure 130. Multiple Chip Configuration in Shift Register Mode

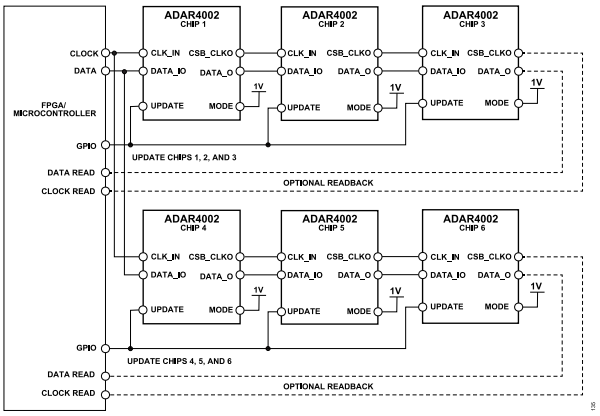

Figure 131. Shift Register Mode with Parallel Chips

POWER MANAGEMENT RECOMMENDATIONS

The ADAR4002 has two voltage supplies, a 1.2 V supply and a 1.0 V supply, and each supply has different maximum current requirements. To supply both voltages to several ADAR4002 chips, follow the power-management recommendations detailed in this section and shown in Table 13 and Figure 132.

Note that a 12 V supply is assumed available in the application, and this supply is used as the input voltage to both the LT3045 and the LTM8074, or the MAXM17631.

For the 1.0 V and 1.2 V supply, the voltage steps down from 12 V to 1.9 V for best performance with the LTM8074 (or MAXM17631). The stepped-down 1.9 V output from the LTM8074 (or MAXM17631) drives the input voltage of the LT3045, which performs the final voltage step-down to 1.0 V and 1.2 V. The LT3045 output can drive the 1.0 V and 1.2 V supply of to 1024 ADAR4002 devices at typical. The typical expected 1.2 V current and 1.0 V current are 0.3 mA and 0.4 mA respectively.

Because of the low-current consumption per the ADAR4002, the I x R voltage drop across the power distribution network on the PCB is small. Therefore, a single LDO regulator is able to power at least 100 devices to 200 devices, depending on the design of the power distribution network.

In general, a switcher and LDO regulator combination configuration is recommended where the total current is more than 100 mA for power efficiency reasons. Where the total current is less than 50 mA, using an LDO regulator with a switcher is not power efficient. If the total current is between 50 mA and 100 mA, other factors like heat dissipation, cost, and size must be considered along with the power efficiency.

Table 13. Power Management Recommendations

ADAR4002 Chips	Total 1.2 V Current, $I_{1.2V}$ (mA)	LDO	Switcher
64	19	LT3045	Not applicable
256	77	LT3045	LTM8074 or MAXM17631
1024	307	LT3045	LTM8074 or MAXM17631

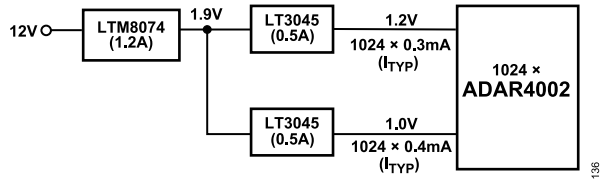

Figure 132. Recommended Power Management of up to 1024 ADAR4002 Devices at Typical Operating Conditions

APPLICATIONS INFORMATION

LOGIC VOLTAGES GREATER THAN 1.2 V

Driving CSB/CLKO and DATA_IO to voltages more than 1.2 V, appreciable current sinks into the pin, especially over temperature (see Figure 133). Keep voltage drive levels to 1.2 V or lower on these bidirectional, dual-use pins to avoid high-current draw. The high-current draw is especially pronounced for the CSB/CLKO pin in SPI mode. The CSB/CLKO pin idles high between SPI writes; therefore, high-current draw occurs between SPI writes if the drive voltage is more than 1.2 V.

The digital input only pins, CLK_IN, MODE, and UPDATE, do not draw high current when driven with larger voltages than 1.2 V. However, 1.2 V is still the recommend operational maximum for these input pins.

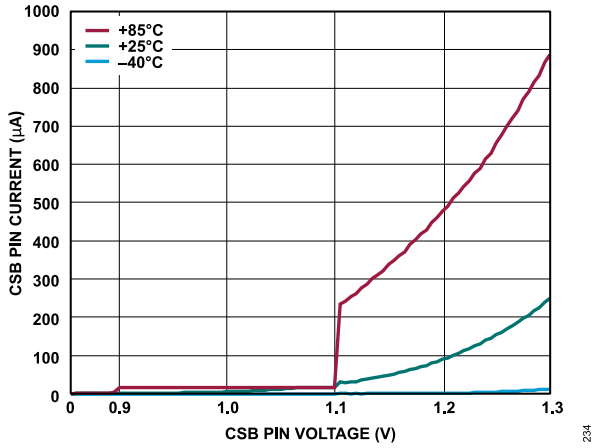

Figure 133. CSB Pin Current vs. CSB Pin Voltage Drive Level over Temperature While in SPI Mode

REGISTER MAP

Table 14. ADAR4002 Register Summary

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x00	ADI_SPI_CONFIG_A	7	SOFTRESET_	Soft Reset. Broadcast to all chips on the SPI bus.	0x0	R/W
		6	LSB_FIRST_	LSB First.	0x0	R/W
		5	ENDIAN_	Endian. Clear = descend and set = ascend.	0x1	R/W
		4	SDOACTIVE_	SDO Active	0x1	R/W
		3	SDOACTIVE	SDO Active	0x1	R/W
		2	ENDIAN	Address Ascension on Block Writes. Clear = descend and set = ascend.	0x1	R/W
		1	LSB_FIRST	LSB First.	0x0	R/W
		0	SOFTRESET	Soft Reset. Broadcast to all chips on the SPI bus.	0x0	R/W
0x01	ADI_SPI_CONFIG_B	7	SINGLE_INSTRUCTION	Single Instruction.	0x0	R/W
		6	CSB_STALL	CSB Stall.	0x0	R/W
		5	CONTROLLER_TARGET_RB	Controller and Target RB.	0x0	R/W
		4	SLOW_INTERFACE	Slow Interface Control.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		2	SOFTRESET2	Soft Reset 2.	0x0	R/W
		1	SOFTRESET1	Soft Reset 1.	0x0	R/W
		0	RESERVED	Reserved	0x0	R
0x03	CHIPTYPE	[7:0]	CHIPTYPE	Chip Type, Read Only.	0x1	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID_L	Product_ID_L, Lower Eight Bits.	0x3	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID_H	Product_ID_H, Higher Eight Bits.	0x0	R
0x06	CHIP_GRADE	[7:4]	BEOL	BEOL Version.	0x0	R
		[3:0]	FEOL	FEOL Version.	0x0	R
0x08	ADDRESS_PAGE	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	ADDR_PAGE	Not applicable.	0x0	R/W
0x0A	SCRATCHPAD	[7:0]	SCRATCHPAD	Scratch Pad.	0x0	R/W
0x0B	SPI_REV	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	SPI_REV	SPI Register Map Revision.	0x1	R
0x0C	VENDOR_ID_L	[7:0]	VENDOR_ID_L	Vendor ID Low Byte. Read only, value = 0x56.	0x56	R
0x0D	VENDOR_ID_H	[7:0]	VENDOR_ID_H	Vendor ID High Byte. Read only, value = 0x04.	0x4	R
0x10	SEQUENCERA_START	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	SEQUENCERA_START	Start Value of Sequencer A.	0x0	R/W
0x11	SEQUENCERA_STOP	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	SEQUENCERA_STOP	Stop Value of Sequencer A.	0x1F	R/W
0x12	SEQUENCERB_START	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	SEQUENCERB_START	Start Value of Sequencer B.	0x0	R/W
0x13	SEQUENCERB_STOP	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	SEQUENCERB_STOP	Stop Value of Sequencer B.	0x1F	R/W
0x14	SEQUENCER_DIRECTIONS	[7:5]	RESERVED	Reserved.	0x0	R
		4	SEQUENCERA_DIRECTION	Direction of Sequencer A. 1 = ascend, and 0 = descend.	0x1	R/W
		[3:1]	RESERVED	Reserved.	0x0	R
		0	SEQUENCERB_DIRECTION	Direction of Sequencer B. 1 = ascend, and 0 = descend.	0x1	R/W
0x15	SEQUENCER_RESET	[7:5]	RESERVED	Reserved.	0x0	R
		4	SEQUENCERA_RESET	Reset Sequencer A to SEQUENCERA_START.	0x0	R/W
		[3:1]	RESERVED	Reserved.	0x0	R
		0	SEQUENCERB_RESET	Reset Sequencer B to SEQUENCERB_START.	0x0	R/W
0x16	SEQUENCERA_B	[7:1]	RESERVED	Reserved.	0x0	R
		0	SEQUENCERA_B	Sequencer A = 0, and Sequencer B = 1.	0x0	R/W

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x17	SEQUENCERA_SEQPOINTER	[7:5]	RESERVED	Reserved	0x0	R
		[4:0]	SEQUENCERA_CURRENTVALUE	Current Sequencer Pointer of Sequencer A. Read only.	0x0	R
0x18	SEQUENCERB_SEQPOINTER	[7:5]	RESERVED	Reserved	0x0	R
		[4:0]	SEQUENCERB_CURRENTVALUE	Current Sequencer Pointer of Sequencer B. Read only.	0x0	R
0x20	TD00	7	FR_TDRANGE00	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY00, Bits[6:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x21	DSA00	[7:2]	FIRSTRANK_DSA00	6 Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x22	TD01	7	FR_TDRANGE01	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY01	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x23	DSA01	[7:2]	FIRSTRANK_DSA01	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x24	TD02	7	FR_TDRANGE02	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY02	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x25	DSA02	[7:2]	FIRSTRANK_DSA02	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x26	TD03	7	FR_TDRANGE03	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY03	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x27	DSA03	[7:2]	FIRSTRANK_DSA03	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x28	TD04	7	FR_TDRANGE04	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY04	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x29	DSA04	[7:2]	FIRSTRANK_DSA04	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x2A	TD05	7	FR_TDRANGE05	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[6:0]	FIRSTRANK_TIMEDELAY05	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x2B	DSA05	[7:2]	FIRSTRANK_DSA05	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x2C	TD06	7	FR_TDRANGE06	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY06	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x2D	DSA06	[7:2]	FIRSTRANK_DSA06	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x2E	TD07	7	FR_TDRANGE07	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY07	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x2F	DSA07	[7:2]	FIRSTRANK_DSA07	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x30	TD08	7	FR_TDRANGE08	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY08	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x31	DSA08	[7:2]	FIRSTRANK_DSA08	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x32	TD09	7	FR_TDRANGE09	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY09	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x33	DSA09	[7:2]	FIRSTRANK_DSA09	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x34	TD10	7	FR_TDRANGE10	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY10	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x35	DSA10	[7:2]	FIRSTRANK_DSA10	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x36	TD11	7	FR_TDRANGE11	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY11	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x37	DSA11	[7:2]	FIRSTRANK_DSA11	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x38	TD12	7	FR_TDRANGE12	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY12	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x39	DSA12	[7:2]	FIRSTRANK_DSA12	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x3A	TD13	7	FR_TDRANGE13	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY13	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x3B	DSA13	[7:2]	FIRSTRANK_DSA13	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x3C	TD14	7	FR_TDRANGE14	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY14	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x3D	DSA14	[7:2]	FIRSTRANK_DSA14	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x3E	TD15	7	FR_TDRANGE15	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY15	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x3F	DSA15	[7:2]	FIRSTRANK_DSA15	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x40	TD16	7	FR_TDRANGE16	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY16	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x41	DSA16	[7:2]	FIRSTRANK_DSA16	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x42	TD17	7	FR_TDRANGE17	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY17	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x43	DSA17	[7:2]	FIRSTRANK_DSA17	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x44	TD18	7	FR_TDRANGE18	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY18	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x45	DSA18	[7:2]	FIRSTRANK_DSA18	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x46	TD19	7	FR_TDRANGE19	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY19	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x47	DSA19	[7:2]	FIRSTRANK_DSA19	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x48	TD20	7	FR_TDRANGE20	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY20	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x49	DSA20	[7:2]	FIRSTRANK_DSA20	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x4A	TD21	7	FR_TDRANGE21	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY21	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x4B	DSA21	[7:2]	FIRSTRANK_DSA21	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x4C	TD22	7	FR_TDRANGE22	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY22	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x4D	DSA22	[7:2]	FIRSTRANK_DSA22	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x4E	TD23	7	FR_TDRANGE23	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY23	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x4F	DSA23	[7:2]	FIRSTRANK_DSA23	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x50	TD24	7	FR_TDRANGE24	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY24	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x51	DSA24	[7:2]	FIRSTRANK_DSA24	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x52	TD25	7	FR_TDRANGE25	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY25	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x53	DSA25	[7:2]	FIRSTRANK_DSA25	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x54	TD26	7	FR_TDRANGE26	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY26	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x55	DSA26	[7:2]	FIRSTRANK_DSA26	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x56	TD27	7	FR_TDRANGE27	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY27	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x57	DSA27	[7:2]	FIRSTRANK_DSA27	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x58	TD28	7	FR_TDRANGE28	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY28	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x59	DSA28	[7:2]	FIRSTRANK_DSA28	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x5A	TD29	7	FR_TDRANGE29	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY29	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x5B	DSA29	[7:2]	FIRSTRANK_DSA29	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x5C	TD30	7	FR_TDRANGE30	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY30	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x5D	DSA30	[7:2]	FIRSTRANK_DSA30	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x5E	TD31	7	FR_TDRANGE31	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY31	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x5F	DSA31	[7:2]	FIRSTRANK_DSA31	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x60	STREAMWRITE00	7	FR_TDRANGE00	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY00, Bits[6:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x61	STREAMWRITE01	[7:2]	FIRSTRANK_DSA00	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE01	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY01, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x62	STREAMWRITE02	[7:2]	FIRSTRANK_TIMEDELAY01, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[1:0]	FIRSTRANK_DSA01, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x63	STREAMWRITE03	[7:4]	FIRSTRANK_DSA01, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE02	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY02, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x64	STREAMWRITE04	[7:4]	FIRSTRANK_TIMEDELAY02, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA02, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x65	STREAMWRITE05	[7:6]	FIRSTRANK_DSA02, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE03	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY03, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x66	STREAMWRITE06	[7:6]	FIRSTRANK_TIMEDELAY03, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA03	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x67	STREAMWRITE07	7	FR_TDRANGE04	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY04	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x68	STREAMWRITE08	[7:2]	FIRSTRANK_DSA04	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE05	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY05, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x69	STREAMWRITE09	[7:2]	FIRSTRANK_TIMEDELAY05, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA05, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x6A	STREAMWRITE0A	[7:4]	FIRSTRANK_DSA05, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE06	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY06, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x6B	STREAMWRITE0B	[7:4]	FIRSTRANK_TIMEDELAY06, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA06, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x6C	STREAMWRITE0C	[7:6]	FIRSTRANK_DSA06, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE07	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY07, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x6D	STREAMWRITE0D	[7:6]	FIRSTRANK_TIMEDELAY07, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA07	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x6E	STREAMWRITE0E	7	FR_TDRANGE08	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY08	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x6F	STREAMWRITE0F	[7:2]	FIRSTRANK_DSA08	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE09	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY09, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x70	STREAMWRITE10	[7:2]	FIRSTRANK_TIMEDELAY09, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA09, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x71	STREAMWRITE11	[7:4]	FIRSTRANK_DSA09, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE10	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY10, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x72	STREAMWRITE12	[7:4]	FIRSTRANK_TIMEDELAY10, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA10, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x73	STREAMWRITE13	[7:6]	FIRSTRANK_DSA10, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE11	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY11, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x74	STREAMWRITE14	[7:6]	FIRSTRANK_TIMEDELAY11, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA11	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x75	STREAMWRITE15	7	FR_TDRANGE12	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY12	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x76	STREAMWRITE16	[7:2]	FIRSTRANK_DSA12	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE13	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY13, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x77	STREAMWRITE17	[7:2]	FIRSTRANK_TIMEDELAY13, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA13, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x78	STREAMWRITE18	[7:4]	FIRSTRANK_DSA13, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE14	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY14, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x79	STREAMWRITE19	[7:4]	FIRSTRANK_TIMEDELAY14, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA14, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x7A	STREAMWRITE1A	[7:6]	FIRSTRANK_DSA14, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE15	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY15, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x7B	STREAMWRITE1B	[7:6]	FIRSTRANK_TIMEDELAY15, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA15	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x7C	STREAMWRITE1C	7	FR_TDRANGE16	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY16	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x7D	STREAMWRITE1D	[7:2]	FIRSTRANK_DSA16	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE17	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY17, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x7E	STREAMWRITE1E	[7:2]	FIRSTRANK_TIMEDELAY17, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA17, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x7F	STREAMWRITE1F	[7:4]	FIRSTRANK_DSA17, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE18	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY18, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x80	STREAMWRITE20	[7:4]	FIRSTRANK_TIMEDELAY18, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA18, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x81	STREAMWRITE21	[7:6]	FIRSTRANK_DSA18, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE19	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY19, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x82	STREAMWRITE22	[7:6]	FIRSTRANK_TIMEDELAY19, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[5:0]	FIRSTRANK_DSA19	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x83	STREAMWRITE23	7	FR_TDRANGE20	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY20	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x84	STREAMWRITE24	[7:2]	FIRSTRANK_DSA20	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE21	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY21, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x85	STREAMWRITE25	[7:2]	FIRSTRANK_TIMEDELAY21, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA21, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x86	STREAMWRITE26	[7:4]	FIRSTRANK_DSA21, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE22	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY22, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x87	STREAMWRITE27	[7:4]	FIRSTRANK_TIMEDELAY22, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA22, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x88	STREAMWRITE28	[7:6]	FIRSTRANK_DSA22, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE23	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY23, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x89	STREAMWRITE29	[7:6]	FIRSTRANK_TIMEDELAY23, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA23	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x8A	STREAMWRITE2A	7	FR_TDRANGE24	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY24	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x8B	STREAMWRITE2B	[7:2]	FIRSTRANK_DSA24	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE25	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY25, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x8C	STREAMWRITE2C	[7:2]	FIRSTRANK_TIMEDELAY25, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA25, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x8D	STREAMWRITE2D	[7:4]	FIRSTRANK_DSA25, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		3	FR_TDRANGE26	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY26, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x8E	STREAMWRITE2E	[7:4]	FIRSTRANK_TIMEDELAY26, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA26, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x8F	STREAMWRITE2F	[7:6]	FIRSTRANK_DSA26, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE27	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY27, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x90	STREAMWRITE30	[7:6]	FIRSTRANK_TIMEDELAY27, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA27	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
0x91	STREAMWRITE31	7	FR_TDRANGE28	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[6:0]	FIRSTRANK_TIMEDELAY28	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x92	STREAMWRITE32	[7:2]	FIRSTRANK_DSA28	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W
		1	FR_TDRANGE29	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		0	FIRSTRANK_TIMEDELAY29, Bit 6	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x93	STREAMWRITE33	[7:2]	FIRSTRANK_TIMEDELAY29, Bits[5:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[1:0]	FIRSTRANK_DSA29, Bits[5:4]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
0x94	STREAMWRITE34	[7:4]	FIRSTRANK_DSA29, Bits[3:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
		3	FR_TDRANGE30	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[2:0]	FIRSTRANK_TIMEDELAY30, Bits[6:4]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x95	STREAMWRITE35	[7:4]	FIRSTRANK_TIMEDELAY30, Bits[3:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[3:0]	FIRSTRANK_DSA30, Bits[5:2]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0xF	R/W
0x96	STREAMWRITE36	[7:6]	FIRSTRANK_DSA30, Bits[1:0]	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3	R/W
		5	FR_TDRANGE31	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R/W
		[4:0]	FIRSTRANK_TIMEDELAY31, Bits[6:2]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
0x97	STREAMWRITE37	[7:6]	FIRSTRANK_TIMEDELAY31, Bits[1:0]	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R/W
		[5:0]	FIRSTRANK_DSA31	6 Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R/W

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x98	STREAMWRITE_DATALOAD	[7:1]	RESERVED	Reserved.	0x0	R
		0	DATA_LOAD	Load Signal for Second Rank of Registers. This bit auto clears after being set.	0x0	R/W
0x99	SPI_UPDATE	[7:1]	RESERVED	Reserved.	0x0	R
		0	UPDATE	Update Sequencer via SPI Bit. this bit auto-clears after being set	0x0	R/W
0xA0	SECONDRANKRB_TD00	7	SR_TDRANGE00	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY00	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xA1	SECONDRANKRB_DSA00	[7:2]	SECONDRANKRB_DSA00	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xA2	SECONDRANKRB_TD01	7	SR_TDRANGE01	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY01	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xA3	SECONDRANKRB_DSA01	[7:2]	SECONDRANKRB_DSA01	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xA4	SECONDRANKRB_TD02	7	SR_TDRANGE02	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY02	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xA5	SECONDRANKRB_DSA02	[7:2]	SECONDRANKRB_DSA02	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xA6	SECONDRANKRB_TD03	7	SR_TDRANGE03	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY03	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xA7	SECONDRANKRB_DSA03	[7:2]	SECONDRANKRB_DSA03	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xA8	SECONDRANKRB_TD04	7	SR_TDRANGE04	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY04	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xA9	SECONDRANKRB_DSA04	[7:2]	SECONDRANKRB_DSA04	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xAA	SECONDRANKRB_TD05	7	SR_TDRANGE05	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY05	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xAB	SECONDRANKRB_DSA05	[7:2]	SECONDRANKRB_DSA05	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xAC	SECONDRANKRB_TD06	7	SR_TDRANGE06	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R

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Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[6:0]	SECONDRANKRB_TIMEDELAY06	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xAD	SECONDRANKRB_DSA06	[7:2]	SECONDRANKRB_DSA06	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation. n	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xAE	SECONDRANKRB_TD07	7	SR_TDRANGE07	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY07	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xAF	SECONDRANKRB_DSA07	[7:2]	SECONDRANKRB_DSA07	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xB0	SECONDRANKRB_TD08	7	SR_TDRANGE08	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY08	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xB1	SECONDRANKRB_DSA08	[7:2]	SECONDRANKRB_DSA08	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xB2	SECONDRANKRB_TD09	7	SR_TDRANGE09	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY09	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xB3	SECONDRANKRB_DSA09	[7:2]	SECONDRANKRB_DSA09	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xB4	SECONDRANKRB_TD10	7	SR_TDRANGE10	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY10	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xB5	SECONDRANKRB_DSA10	[7:2]	SECONDRANKRB_DSA10	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xB6	SECONDRANKRB_TD011	7	SR_TDRANGE11	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY11	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xB7	SECONDRANKRB_DSA11	[7:2]	SECONDRANKRB_DSA11	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xB8	SECONDRANKRB_TD12	7	SR_TDRANGE12	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY12	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xB9	SECONDRANKRB_DSA12	[7:2]	SECONDRANKRB_DSA12	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xBA	SECONDRANKRB_TD13	7	SR_TDRANGE13	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY13	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0xBB	SECONDRANKRB_DSA13	[7:2]	SECONDRANKRB_DSA13	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xBC	SECONDRANKRB_TD14	7	SR_TDRANGE14	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY14	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xBD	SECONDRANKRB_DSA14	[7:2]	SECONDRANKRB_DSA14	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xBE	SECONDRANKRB_TD15	7	SR_TDRANGE15	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY15	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xBF	SECONDRANKRB_DSA15	[7:2]	SECONDRANKRB_DSA15	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xC0	SECONDRANKRB_TD16	7	SR_TDRANGE16	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY16	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xC1	SECONDRANKRB_DSA16	[7:2]	SECONDRANKRB_DSA16	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xC2	SECONDRANKRB_TD17	7	SR_TDRANGE17	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY17	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xC3	SECONDRANKRB_DSA17	[7:2]	SECONDRANKRB_DSA17	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xC4	SECONDRANKRB_TD18	7	SR_TDRANGE18	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY18	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xC5	SECONDRANKRB_DSA18	[7:2]	SECONDRANKRB_DSA18	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xC6	SECONDRANKRB_TD19	7	SR_TDRANGE19	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY19	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xC7	SECONDRANKRB_DSA19	[7:2]	SECONDRANKRB_DSA19	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xC8	SECONDRANKRB_TD20	7	SR_TDRANGE20	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY20	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xC9	SECONDRANKRB_DSA20	[7:2]	SECONDRANKRB_DSA20	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[1:0]	RESERVED	Reserved.	0x0	R
0xCA	SECONDRANKRB_TD21	7	SR_TDRANGE21	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY21	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xCB	SECONDRANKRB_DSA21	[7:2]	SECONDRANKRB_DSA21	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xCC	SECONDRANKRB_TD22	7	SR_TDRANGE22	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY22	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xCD	SECONDRANKRB_DSA22	[7:2]	SECONDRANKRB_DSA22	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xCE	SECONDRANKRB_TD23	7	SR_TDRANGE23	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY23	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xCF	SECONDRANKRB_DSA23	[7:2]	SECONDRANKRB_DSA23	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xD0	SECONDRANKRB_TD24	7	SR_TDRANGE24	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY24	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xD1	SECONDRANKRB_DSA24	[7:2]	SECONDRANKRB_DSA24	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xD2	SECONDRANKRB_TD025	7	SR_TDRANGE25	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY25	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xD3	SECONDRANKRB_DSA25	[7:2]	SECONDRANKRB_DSA25	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xD4	SECONDRANKRB_TD26	7	SR_TDRANGE26	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY26	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xD5	SECONDRANKRB_DSA26	[7:2]	SECONDRANKRB_DSA26	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xD6	SECONDRANKRB_TD27	7	SR_TDRANGE27	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY27	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xD7	SECONDRANKRB_DSA27	[7:2]	SECONDRANKRB_DSA27	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R

REGISTER MAP

Table 14. ADAR4002 Register Summary (Continued)

Addr	Name	Bits	Bit Name	Description	Reset	Access
0xD8	SECONDRANKRB_TD28	7	SR_TDRANGE28	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY28	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xD9	SECONDRANKRB_DSA28	[7:2]	SECONDRANKRB_DSA28	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xDA	SECONDRANKRB_TD29	7	SR_TDRANGE29	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY29	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xDB	SECONDRANKRB_DSA29	[7:2]	SECONDRANKRB_DSA29	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xDC	SECONDRANKRB_TD30	7	SR_TDRANGE30	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY30	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xDD	SECONDRANKRB_DSA30	[7:2]	SECONDRANKRB_DSA30	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xDE	SECONDRANKRB_TD31	7	SR_TDRANGE31	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	SECONDRANKRB_TIMEDELAY31	7-Bit Time Delay Control. Default = 0x00, minimum time delay.	0x0	R
0xDF	SECONDRANKRB_DSA31	[7:2]	SECONDRANKRB_DSA31	6-Bit Attenuation Control. Default = 0x3F, maximum attenuation.	0x3F	R
		[1:0]	RESERVED	Reserved.	0x0	R
0xF0	VAP_RB_TIMEDELAY	7	VAP_RB_TDRANGE	Time Delay Range. 0 = Range 0, 508 ps, and 1 = Range 1, 254 ps.	0x0	R
		[6:0]	VAP_RB_TIMEDELAY, Bits[6:0]	Readback for Active VAP Output—Time Delay.	0x0	R
0xF1	VAP_RB_DSA	[7:2]	VAP_RB_DSA	Readback for Active VAP Output—DSA.	0x0	R
		[1:0]	RESERVED	Reserved.	0x0	R

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-14-6	LFCSP	16-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAR4002ACPZ	−40°C to +85°C	14-Lead LFCSP (2 mm x 3 mm x 0.75 mm with an EP)	CP-14-6
ADAR4002ACPZ-R7	−40°C to +85°C	14-Lead LFCSP (2 mm x 3 mm x 0.75 mm with an EP)	CP-14-6

[1] Z = RoHS Compliant Part.

Updated: June 04, 2025

EVALUATION BOARDS

Model[1]	Description
ADAR4002-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.