Data Sheet

ADAR3003

27GHz to 31GHz, 1-Beam and 4-Element, Dual Polarized, Transmit Ka Band Beamformer

FEATURES

- 27GHz to 31GHz RF range
- Programmable amplifier bias
  - Power consumption range (quiescent): 571mW to 805mW
  - Gain range: 20.8dB to 23.3dB at 29.2GHz
  - Output P1dB range: 13.1dBm to 11.8dB at 29.2GHz
- Power consumption at OP1dB: 1.01W (nominal bias)
- Specifications at 29.2GHz and nominal bias
  - RMS gain error over DSA 0 to DSA Code 31: 0.98dB
  - RMS phase error over PSU Code 0 to PSU Code 63: 4.7°
  - Maximum path gain: 22.7dB
  - OIP3: 20.2dBm
  - OP1dB: 12.1dBm
  - Output P_{SAT}: 14.5dBm
  - Output NSD: −127.8dBm/Hz
  - Noise figure: 22.7dB
- Isolation (element to element): < −30.7dB
- 0° to 360° phase adjustment range
- 5.625 phase resolution
- ≥31.5dB gain adjustment range
- ≤0.5dB gain resolution
- User-programmable sequencer for beamstate selection
- Memory for 128 prestored beamstates
  - 64 beamstates per beam polarization
- FIFO memory for 32 beamstates
  - 16 beamstates per beam polarization
- Variable SPI length for flexible and efficient beam commands
  - Update, reset, and mute from 1 beam up to 16 beams
- Integrated 8-bit ADC for temperature sensor and RF detectors
- 3-wire or 4-wire SPI
- Package: 128-ball 5mm × 5mm WLCSP

APPLICATIONS

- Mobile Ka band satellite communications (satcom) applications
  - Air terminals
  - Ground terminals
  - Maritime terminals

For more information on the ADAR3003, contact beamformer@analog.com.

FUNCTIONAL BLOCK DIAGRAM

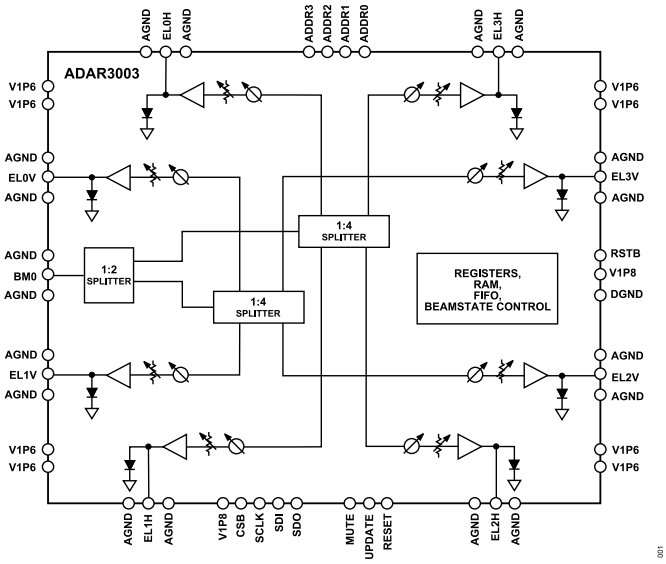

Figure 1. ADAR3003 Functional Block Diagram

GENERAL DESCRIPTION

The ADAR3003 is a 27GHz to 31GHz transmit, 1-beam input, and 4-dual polarized element outputs, beamforming chip for polarized phased arrays. Each of the eight RF paths provide a ≥31.5 dB gain adjustment range and 360° phase adjustment range, with a gain and phase resolution of less than ≤0.5 dB and 5.625°, respectively, via the variable amplitude and phase (VAP) blocks. Each VAP contains a digital stepped attenuator (DSA) and phase shifter unit (PSU). Each path has an integrated RF power detector at its output, with a 18dB measurement range.

Access of all the on-chip control registers and memory is through a simple 3-wire or 4-wire serial port interface (SPI). In addition, four address pins allow SPI control of up to 16 devices on the same serial lines. The random access memory (RAM) has storage for up to 128 beamstates, organized into 64 beamstates per beam polarization. The on-chip sequencer selects and advances the beamstate being sourced from either the RAM or the first-in, first-out (FIFO).

The ADAR3003 is available in a 128-ball 5mm × 5mm wafer level chip-scale package (WLCSP) and is specified from −40°C to +85°C.

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