17.7 GHz to 21.2 GHz, 2-Beam and 4-Element, Dual Polarized, Receive Ka-Band Beamformer

FEATURES

- 17.7 GHz to 21.2 GHz frequency range
- Noise figure (using electronic gain) = 2.0 dB
- Low power consumption = 398.5 mW nominal
  - 8 programmable amplifier bias settings
- RMS gain error = 0.2 dB
- RMS phase error = 2.3 degrees
- Coherent gain = 25.1 dB at 19.5 GHz
  - All 8 inputs driven
- Single path gain = 7.1 dB at 19.5 GHz
- IIP3 = −21.6 dBm at 19.5 GHz
- IP1dB = -29.4 dBm at 19.5 GHz
- Cross polarization isolation = 25 dB
- 0 degree to 360 degree phase adjustment range
- 5.625 degree step size/resolution
- ≥31 dB gain adjustment range
- ≤0.5 dB gain resolution
- Memory for 256 prestored beam positions
  - 64 beamstates per beam polarization
- User programmable sequencer for beamstate selection
- FIFO memory for 64 beam positions
  - 16 beamstates per beam polarization
- Variable SPI length for flexible and efficient beam commands
  - Update, reset, and mute from 1 up to 16 aperture beams
- 8-bit ADC for integrated temperature sensors and AMUX pin
- 3-wire or 4-wire SPI
- 176-ball, 6.6 mm x 6.6 mm WLCSP

APPLICATIONS

- Mobile Ka-band satellite communication (satcom) applications
  - Air terminals
  - Ground terminals
  - Maritime terminals

GENERAL DESCRIPTION

The ADAR3002 is a 17.7 GHz to 21.2 GHz receive, 2-beam and 4-dual polarized elements, beamforming chip for polarized phased arrays. Each of the 16 RF paths provides a ≥31 dB gain adjustment range and 360 degree phase adjustment, with resolution of less than ≤0.5 dB and 5.625 degrees, respectively, through variable amplitude and phase (VAP) blocks. Each VAP contains a digital stepped attenuator (DSA) and phase shifter unit (PSU).

Access to on-chip control registers and memory is through a simple 3-wire or 4-wire serial port interface (SPI). Four chip address pins allow SPI control of up to 16 devices on the same serial lines. The random access memory (RAM) has storage for up to 256 beamstates, organized into 64 beamstates per beam polarization. The sequencer selects and advances the beamstate being sourced from either the RAM or FIFO.

ADAR3002 is available in a 176-ball 6.6 mm x 6.6 mm wafer level chip scale package (WLCSP) and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

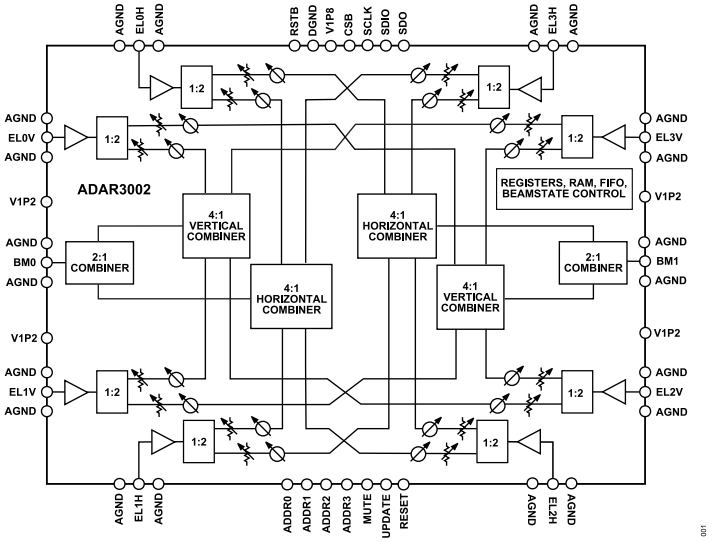

Figure 1. Functional Block Diagram

NOTES