FEATURES

Dual-channel differential input/output
Integrated 36 MHz, 8-pole low-pass filter
Low power dissipation
- 213 mW typical at 3 V supply
2 integrated fully differential ADC drivers
30 dB maximum differential gain
  - Adjustable down to 14 dB
Gain error: ±0.2 dB
Gain drift: 0.01 dB/°C typical
2.7 V to 3.3 V supply range
84-ball, 6 mm × 12 mm CSP_BGA package with 0.8 mm ball pitch
Operating temperature range: −40°C to +85°C
Built-in supply decoupling capacitors

APPLICATIONS

IF broadband demodulators
Medical imaging (CW ultrasound beam forming)
Phased array systems
  - Radar
  - Adaptive antennas
Communications receivers
Radio Links
Wireless local loop
IF broadband demodulators
RF instrumentation
Satellite modems
Baseband data acquisition system
  - Multichannel digitizer instruments
  - Ultrasonic non-destructive test

GENERAL DESCRIPTION

The ADAQ8088 is a dual-channel analog system in package (SIP) that integrates three common signal processing and conditioning blocks to support a variety of demodulator applications and data acquisition applications. The device integrates all active and passive components to form a complete signal chain between the output of an I/Q demodulator and the input to an analog-to-digital converter (ADC). The device also forms the complete signal chain between a transducer output and the input to an ADC in baseband data acquisition systems. No external components are required for proper functionality.

Each channel contains a preamplifier, followed by an 8-pole, low-pass filter with a 36 MHz, 3 dB frequency and a differential ADC driver optimized to drive 12-bit to 14-bit pipeline ADCs with speeds up to 150 MSPS. Encapsulated in a 6 mm × 12 mm CSP_BGA package, the ADAQ8088 minimizes space requirements in high density multichannel systems.

The ADAQ8088 operating temperature range is from −40°C to +85°C.
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## REVISION HISTORY

2/2021—Revision 0: Initial Version
**SPECIFICATIONS**

VCC = 3.0 V, common-mode voltage ($V_{CM}$) floating, VINAP, VINAN, VINBP, and VINBN are self biased, differential 63 mV p-p input at 1 MHz, $T_A = 25^\circ C$, unless otherwise noted.

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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<td><strong>INPUT CHARACTERISTICS</strong></td>
<td>Each input to GND</td>
<td>249/1</td>
<td>mA</td>
<td>V/pF</td>
<td></td>
</tr>
<tr>
<td>Input Impedance</td>
<td>( V_{CC} = 2.7 ) V</td>
<td>1.15</td>
<td>V</td>
<td>dc</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3.0 ) V</td>
<td>1.25</td>
<td>V</td>
<td>dc</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3.3 ) V</td>
<td>1.38</td>
<td>V</td>
<td>dc</td>
<td></td>
</tr>
<tr>
<td>Open Circuit Voltage at VIN Pins</td>
<td>( V_{CC} = 2.7 ) V</td>
<td>-550</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3.0 ) V</td>
<td>-610</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3.3 ) V</td>
<td>-670</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>Each input to GND, ( V_{CC} = 2.7 ) V</td>
<td>±3.5</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3.0 ) V</td>
<td>±4.0</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3.3 ) V</td>
<td>±4.5</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>Each input to GND</td>
<td>7.5</td>
<td>µV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Common-Mode Voltage Range</td>
<td>( V_{OS} )</td>
<td>+0.7</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential RTI Vos</td>
<td>( T_A = -40^\circ C ) to ( +85^\circ C )</td>
<td>36</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bandwidth Drift</td>
<td>( T_A = -40^\circ C ) to ( +85^\circ C )</td>
<td>0.1</td>
<td>MHz/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)</td>
<td>( V_{OUT} = 2 ) V p-p differential, ( R_L = 1 ) kΩ</td>
<td>-63</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>( T_A = -40^\circ C ) to ( +85^\circ C )</td>
<td>180</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gain</td>
<td>With no external resistors</td>
<td>30</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Error</td>
<td>Channel to channel, at 10 MHz</td>
<td>±0.2</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Drift</td>
<td>( T_A = -40^\circ C ) to ( +85^\circ C )</td>
<td>0.01</td>
<td>dB/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Match Error</td>
<td>Channel to channel, at 10 MHz</td>
<td>0.5</td>
<td>Degrees</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td>( R_L = 806 ) Ω, either output pin</td>
<td>2.15</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>( R_L = 806 ) Ω, either output pin</td>
<td>0.17</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Current</td>
<td>-60</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Balance Error</td>
<td>-60</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Resistance</td>
<td>In series with each output</td>
<td>10</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crosstalk</td>
<td></td>
<td>80</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
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<td><strong>NOISE AND HARMONIC PERFORMANCE</strong></td>
<td>At 1 MHz</td>
<td>7</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
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<tr>
<td>RTI Voltage Noise Density</td>
<td>At 10 MHz</td>
<td>6</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RTO Voltage Noise Density</td>
<td>Gain = 30 dB, ( f = 1 ) MHz</td>
<td>220</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gain = 30 dB, ( f = 10 ) MHz</td>
<td>190</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1/f Corner</td>
<td></td>
<td>20</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>$V_{CM}$ CHARACTERISTICS</strong></td>
<td>( V_{CM} ) Gain</td>
<td>0.5</td>
<td>2</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CM} ) Range</td>
<td>5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CM} ) Input Resistance</td>
<td>18</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**POWER SUPPLY**

| Operating Range | 2.7 | 3.3 | V | |
| Quiescent Current | 71 | 88 | mA | |
| PSRR | 70 | dB | |
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
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<tbody>
<tr>
<td>Analog Inputs</td>
<td>3.5 V</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.5 V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−55°C to +125°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>Lead Temperature Soldering</td>
<td>260°C reflow as per JEDEC J-STD-020</td>
</tr>
<tr>
<td>Electrostatic Discharge (ESD) Ratings</td>
<td>500 V</td>
</tr>
<tr>
<td>Human Body Model (HBM)</td>
<td>2k V</td>
</tr>
<tr>
<td>Field Induced Charged Device Model</td>
<td>500 V</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_{JA}$ (°C/W)</th>
<th>$\theta_{JC, TOP}$ (°C/W)</th>
<th>$\theta_{JC, BOTTOM}$ (°C/W)</th>
<th>$\theta_{JB}$ (°C/W)</th>
<th>$\Psi_{JT}$ (°C/W)</th>
<th>$\Psi_{JB}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC-84-4</td>
<td>33</td>
<td>21.1</td>
<td>12.2</td>
<td>13.7</td>
<td>11</td>
<td>13</td>
</tr>
</tbody>
</table>

1 Test Condition 1: Thermal impedance simulated values are based on use of a 2S2P with vias JEDEC PCB excluding the $\theta_{JC, TOP}$ which uses 1S0P JEDEC PCB.

Thermal resistance values specified in table 3 are simulated based on JEDEC specs (unless specified otherwise) and should be used in compliance with JESD51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

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<th>Pin No.</th>
<th>Mnemonic</th>
<th>Type¹</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>VINAP</td>
<td>AI</td>
<td>Analog Input for Channel A.</td>
</tr>
<tr>
<td>A2, A3, A5, A6, A10, A11, C2, C3, C11, D2, D3, D11, F2, F3, F5, F6, F10, F11</td>
<td>DNC</td>
<td>DNC</td>
<td>Do Not Connect. Do not connect to these pins.</td>
</tr>
<tr>
<td>A4, A7, A8, B1 to B14 E1 to E14, F4, F7, F8</td>
<td>GND</td>
<td>P</td>
<td>Analog Ground.</td>
</tr>
<tr>
<td>A9</td>
<td>VCMA</td>
<td>AI</td>
<td>$V_{CM}$ Input from the ADC.</td>
</tr>
<tr>
<td>A12, A13</td>
<td>RA21, RA22</td>
<td>AI</td>
<td>External Resistors for Channel A.</td>
</tr>
<tr>
<td>A14</td>
<td>VOUTAP</td>
<td>AO</td>
<td>Analog Output for Channel A.</td>
</tr>
<tr>
<td>C1</td>
<td>VINAN</td>
<td>AI</td>
<td>Analog Input for Channel A.</td>
</tr>
<tr>
<td>C4 to C10, D4 to D10</td>
<td>VCC</td>
<td>P</td>
<td>Power Supplies, 2.7 V to 3.3 V.</td>
</tr>
<tr>
<td>C12, C13</td>
<td>RA11, RA12</td>
<td>AI</td>
<td>External Resistors for Channel A.</td>
</tr>
<tr>
<td>C14</td>
<td>VOUTAN</td>
<td>AO</td>
<td>Analog Output for Channel A.</td>
</tr>
<tr>
<td>D1</td>
<td>VINBP</td>
<td>AI</td>
<td>Analog Input for Channel B.</td>
</tr>
<tr>
<td>D12, D13</td>
<td>RB11, RB12</td>
<td>AI</td>
<td>External Resistors for Channel B.</td>
</tr>
<tr>
<td>D14</td>
<td>VOUTBP</td>
<td>AO</td>
<td>Analog Output for Channel B.</td>
</tr>
<tr>
<td>F1</td>
<td>VINBN</td>
<td>AI</td>
<td>Analog Input for Channel B.</td>
</tr>
<tr>
<td>F9</td>
<td>VCMB</td>
<td>AI</td>
<td>$V_{CM}$ Input from the ADC.</td>
</tr>
<tr>
<td>F12, F13</td>
<td>RB21, RB22</td>
<td>AI</td>
<td>External Resistors for Channel B.</td>
</tr>
<tr>
<td>F14</td>
<td>VOUTBN</td>
<td>AO</td>
<td>Analog Output for Channel B.</td>
</tr>
</tbody>
</table>

¹ AI is analog input, DNC is do not connect, P is power, and AO is analog output.
TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 3 V; V_{CM} is floating, typically 1.25 V; R_{LOAD} = 1 kΩ; T = 25°C, inputs and outputs are measured differentially, unless otherwise noted.

**Figure 3.** Gain vs. Input Power, Input Frequency at 1 MHz and 10 MHz

**Figure 4.** V_{OUT} vs. Input Power with Gain Set to 30 dB, Input Frequency at 1 MHz and 10 MHz

**Figure 5.** Frequency Response, Input = −20 dBm

**Figure 6.** Normalized Gain vs. Input Power, Input Frequency at 1 MHz and 10 MHz

**Figure 7.** 1 dB Gain Compression with Gain Set to 30 dB, Input Frequency at 1 MHz and 10 MHz

**Figure 8.** Gain Flatness, Input = −20 dBm
Figure 9. Phase Response with Gain Set to 30 dB, Input = −20 dBm

Figure 10. Normalized Frequency Response, Input = −20 dBm

Figure 11. Frequency Response vs. Supply, Input = −20 dBm

Figure 12. I/Q Channel Crosstalk

Figure 13. Step Response with Gain Set to 30 dB

Figure 14. Distortion
**Figure 15. Noise Floor**

**Figure 16. Amplitude Aggressor**

**Figure 17. Frequency Aggressor**
THEORY OF OPERATION

Figure 18. ½ ADAQ8088 Simplified Schematic

CIRCUIT INFORMATION

The ADAQ8088 system in package (SiP) is an analog signal chain designed to interface baseband I/Q from quadrature demodulators to 12-bit to 14-bit pipeline ADCs.

INPUT RESISTANCE

The equivalent input impedance of each input of the ADAQ8088 is a 249 Ω resistor connected to VCC/2.

Each baseband output of the demodulator is loaded with the input impedance of the ADAQ8088. To avoid saturating the ADAQ8088 inputs, ac couple demodulators with high dc bias on the I/Q outputs to the ADAQ8088.

LOW PASS FILTER

An 8-pole Butterworth low-pass filter provides steep roll-off beyond the filter corner frequency of 36 MHz typical.

NOISE

Input referred broad band noise density of the ADAQ8088 is 6 nV/√Hz

1/f corner is located at 20 kHz.

OUTPUT STAGE

The output stage is optimized to drive 12-bit to 14-bit pipeline ADCs with speeds of 150 MSPS or lower.

The output resistance of the ADAQ8088 is set to 10 Ω. Additional resistors in series with each output and a differential capacitor placed as close to the ADC inputs as possible provides additional filtering.

DC bias of the outputs is set by the voltage on the VCMA pin and the VCMB pin. Floating these pins self adjusts the outputs to 1.25 V (internally biased). Additionally, these pins are typically connected to the chosen ADC VCM output pin.

RESOLUTION

Two 15 Ω resistors, each in series with an output pin of the ADAQ8088 and a 10 pF capacitor across the ADC input pins, allows just over a 10-bit effective resolution at full-scale input for an ADC with a 4 ns acquisition time.

The 190 nV/√Hz RTO noise density of the ADAQ8088 at a gain value of 30 dB, integrated over the 36 MHz signal bandwidth, allows an effective signal resolution of 9 bits which is suitable for a 10-bit ADC with 2 V p-p FS analog input.

Reducing the gain to 20 dB increases the effective resolution to 10.5 bits in an ADC with 2 V p-p FS analog input.

POWER SUPPLY DECOUPLING

The ADAQ8088 features built in, 0.1 μF supply decoupling capacitors on VCC.
GAIN
With no external component, the gain of the ADAQ8088 is set to 30 dB. This gain can be reduced with external resistors ($R_{\text{EXT}}$) connected between the following pins: RA11 and RA12, RA21 and RA22, RB11 and RB12, and RB21 and RB22.

The maximum gain is 30 dB with no resistors. The minimum gain is 14 dB when $R_{\text{EXT}} = 110 \, \Omega$. Figure 19 shows the gain vs. $R_{\text{EXT}}$ value.

Gain can be further reduced by a factor of $249/(249 + R)$ with external resistors connected in series with each input.

![Figure 19. Gain vs. External Resistor Value](image1)

![Figure 20. Gain (dB) vs. External Resistor Value](image2)
APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 21 shows an example of how the ADAQ8088 can be directly coupled to a demodulator. Place the 61.9 Ω resistors close to the ADAQ8088 input pins. The parallel combination of the resistors and the 249 Ω input impedance of the ADAQ8088 provides a 50 Ω termination for the demodulator outputs. If the ADC is located physically some distance from the ADAQ8088 and is driven with a transmission line, place the 40.2 Ω series resistors close to the ADAQ8088 output pins. These resistors, along with the device internal impedance, provide a 50 Ω series termination. The value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

Figure 22 shows an example of how the ADAQ8088 can be used as part of an ultrasonic non-destructive test.

Figure 23 shows an example of how the ADAQ8088 works on high accuracy, wide bandwidth, multichannel digitizer instruments.

Figure 21. ADAQ8088 Direct Coupled to Demodulator, Driving 12-Bit to 14-Bit ADCs with Speeds up to 150 MSPS
Figure 22. Ultrasonic Non-Destructive Test
Figure 23. Multichannel Digitizer Instrument
OUTLINE DIMENSIONS

Figure 24. 84-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-84-4)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model¹</th>
<th>Temperature Range</th>
<th>Ordering Quantity</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADAQ8088BBCZ</td>
<td>−40°C to +85°C</td>
<td>Tray, 280</td>
<td>84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]</td>
<td>BC-84-4</td>
</tr>
</tbody>
</table>

¹ Z = RoHS Compliant Part.