16-Bit, 15 MSPS, µModule Data Acquisition Solution

Preliminary Technical Data

ADAQ23875

FEATURES

- Integrated fully differential ADC driver with signal scaling
  - Wide input common range
  - High common-mode rejection
- Single-ended to differential conversion
  - ±2.048 V input range with 4.096 V REFBUF
- Critical passive components
  - 0.005% precision matched resistor array for FDA
- 9 mm × 9 mm, 0.8 mm pitch, 100-ball BGA package
  - 2.5× footprint reduction versus discrete solution
- Low power, dynamic power scaling, power-down mode
  - 143 mW typical at 15 MSPS
- Throughput: 15 MSPS, no pipeline delay
- INL: ±0.4 LSB typical, ±1 LSB maximum
- SINAD: 89 dB typical at 1 kHz
- THD: −119 dB at 1 kHz, −100 dB at 500 kHz
- Gain error: 0.005% typical
- Gain error drift: 1 ppm/°C typical
- On-board reference buffer with VCM generation
- Serial LVDS interface
- Wide operating temperature range: −40°C to +85°C

APPLICATIONS

- ATE
- Data acquisition
- Hardware in the Loop (HiL)
- Power analyzers
- Non-destructive test (acoustic emissions)
- Mass spectrometry
- Travelling-wave fault location
- Medical imaging and instruments

GENERAL DESCRIPTION

The ADAQ23875 is a precision, high speed, µModule® data acquisition solution that reduces the development cycle of a precision measurement systems by transferring the design burden of component selection, optimization, and layout from designer to the device.

Using System-in-Package (SIP) technology, the ADAQ23875 reduces end system component count by combining multiple common signal processing and conditioning blocks in a single device, including a low noise, fully differential ADC driver, a stable reference buffer, and a high speed, 16-bit, 15 MSPS successive approximation register (SAR) ADC.

The ADAQ23875 also incorporates the critical passive components with superior matching and drift characteristics using Analog Devices, Inc., iPassive® technology to minimize temperature dependent error sources and to offer optimized performance. The fast settling of the ADC driver stage and no latency of the SAR ADC provide a unique solution for high channel count multiplexed signal chain architectures and control loop applications.

The small footprint, 9 mm × 9 mm BGA package enables smaller form factor instruments without sacrificing any performance. The system integration solves many design challenges while the device still provides the flexibility of a configurable ADC driver feedback loop to allow gain or attenuation adjustments as well as fully differential or single-ended to differential input. A single 5 V supply operation is possible while achieving optimum performance from the device.

The ADAQ23875 features a serial LVDS digital interface with one-lane or two-lane output modes, allowing the user to optimize the interface data rate for each application. The specified operation of the µModule is from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

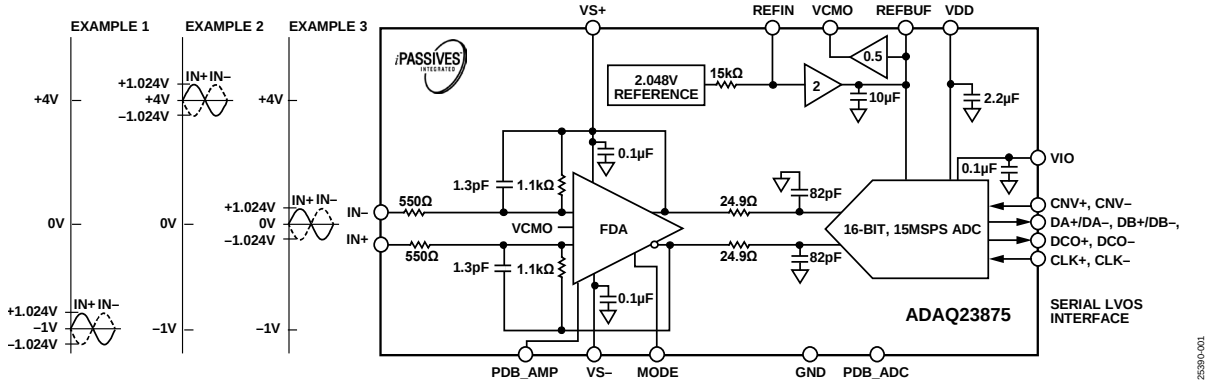

Figure 1. ADAQ23875 Configured for Gain = 2, ±2.048 V Differential Input Range

Rev. PrH Document Feedback

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SPECIFICATIONS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS− = −1 V± 5%, VS− = 0 V[1] (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, 15 MSPS, gain =2, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[2]
RESOLUTION		18			Bits
ANALOG Input Impedance, Z_{IN}	V_{IN} = 4.096 V p-p				
	Single-ended to differential configuration		550		Ω
	Differential configuration		1100		Ω
Input Capacitance	IN1+, IN1−		TBD		pF
Differential Input Voltage Range, V_{IN}[3]	Gain = 2, V_{IN} = 4.096 V p-p	−2.048		+2.048	V
THROUGHPUT					
Complete Cycle		66.6			ns
Conversion Time		54	58	63	ns
Acquisition Phase[4]			t_{CYC} − 39		ns
Throughput Rate[5]		0		15	MSPS
Transient Response[6]	Full-scale step		52		ns
DC ACCURACY	Single ended and differential configuration				
No Missing Codes		16			Bits
Integral Linearity Error		−1	±0.4	+1	LSB
Differential Linearity Error		−1	±0.2	+1	LSB
Transition Noise			0.73		LSB_{RMS}
Gain Error		−0.045	±0.005	+0.045	%FS
Gain Error Drift			1	TBD	ppm/°C
Offset Error		−1.5		+1.5	mV
Offset Error Drift			TBD	TBD	ppm/°C
Common Mode Rejection Ratio (CMRR), Input Referred	$\Delta V_{ICM}/\Delta V_{OSDIFF}$		106		dB
Power Supply Rejection Ratio (PSRR)					
Positive			106		dB
Negative			106		dB
1/f Noise[7]	Bandwidth = 0.1 Hz to 10 Hz		TBD		µV p-p
Input Current Noise	f = 100 kHz		1		pA/√Hz
AC ACCURACY[8]	Single ended and differential configuration				
Dynamic Range	f_{IN} = 1 kHz, −60 dB input	TBD	90		dB
Total RMS Noise	All Gains		91.6		μV_{RMS}
Signal-to-Noise Ratio	f_{IN} = 1 kHz	87.5	89.3		dB
	f_{IN} = 100 kHz		88.5		dB
	f_{IN} = 500 kHz		88		dB
	f_{IN} = 1 MHz		87.5		dB
Signal-to-Noise + Distortion (SINAD)	f_{IN} = 1 kHz	87.3	89		dB
	f_{IN} = 100 kHz		88		dB
	f_{IN} = 500 kHz		87.5		dB
	f_{IN} = 1 MHz		87		dB
Total Harmonic Distortion	f_{IN} = 1 kHz		−119		dB
	f_{IN} = 100 kHz		−111		dB
	f_{IN} = 500 kHz		−100		dB
	f_{IN} = 1 MHz		−80		dB
Spurious-Free Dynamic Range	f_{IN} = 1 kHz		114		dB
−3 dB Input Bandwidth, RC Filter			136		MHz
Aperture Delay[9]			0		ns
Aperture Jitter[9]			0.25		ps_{RMS}

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[2]
REFERENCE					
REFIN, Internal Reference Output Voltage	IOUT = 0 µA	2.028	2.048	2.068	V
Temperature Coefficient			±5	±20	ppm/°C
Output Impedance			15		kΩ
Line Regulation	VDD = 4.75 V to 5.25 V		0.3		mV/V
Input Voltage Range	REFIN overdriven	2.028	2.048	2.068	V
REFBUF, Reference Buffer Output Voltage	REFIN = 2.048 V	4.056	4.096	4.136	V
Input Voltage Range	REFBUF overdriven[10]	4.056	4.096	4.136	V
Load Current	REFBUF = 4.096 V (REFBUF overdriven)		1.6	1.8	mA
	REFBUF = 4.096 V (REFBUF overdriven)		0.5		mA
VCMO					
Common-Mode Output	REFBUF = 4.096 V, IOUT = 0 µA	2.028	2.048	2.028	V
Output Impedance	−1 mA < IOUT < +1 mA		15		Ω
DIGITAL INPUTS					
Logic Levels					
Input Low Voltage, V_{IL}	VIO = 2.5 V			0.6	V
Input High Voltage, V_{IH}	VIO = 2.5 V	1.7			V
Digital Input Current	VIN = 0 V to 2.5 V	−10		+10	µA
Input Pin Capacitance			3		pF
CNV+/CNV− and CLK+/CLK− (LVDS Clock Input)					
Differential Input Voltage, V_{ID}		175	350	650	mV
Common Mode Input Voltage, V_{ICM}		0.8	1.25	1.7	V
DCO+/DCO−, DA+/DA−, DB+/DB− (LVDS Outputs)					
V_{OD}, Differential Output Voltage	100 Ω differential load	247	350	454	mV
V_{OS}, Common Mode Output Voltage	100 Ω differential load	1.125	1.25	1.375	V
POWER-DOWN MODE					
ADC Driver (PDB_AMP)/ ADC (PDB_ADC)					
Low	Power-down mode		<1		V
High	Enabled, normal operation		>1.7		V
Turn-On Time	Specified performance		TBD	TBD	µs
POWER REQUIREMENTS					
VDD		4.75	5	5.25	V
VS+		3	5	VS− + 10	V
VS−		VS+ − 10	0	+0.1	V
VIO		2.375	2.5	2.625	V
Total Standby Current[11, 12]	Static, all devices enabled		45	52	mA
	Static, all devices disabled		0.1	0.4	µA
ADAQ23875 Current Draw					
VDD			3.8	4.1	mA
VS+/VS−			4	5.5	mA
VIO			40	42	mA
ADAQ23875 Power Dissipation	VDD = 5 V, VS+ = 5 V, VS− = 0 V				
VDD			19	21.53	mW
VS+/VS−	Gain = 2		24	33	mW
VIO	One-Lane mode[13]		100	110.25	mW
Total			143	164.78	mW

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[2]
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] For gain = 2, limit the differential input range, V_{IN}, to 95% to allow enough footroom for the ADC driver with VS− = 0 V to achieve the above specified performance.
[2] The LSB unit means least significant bit. The weight of the LSB, referred to input, changes depending on the input voltage range.
[3] The differential input ranges, V_{IN} should be within allowed input common-mode range as per Figure 3 to Figure 7and is dependent on the VS+/VS− supply rails used.
[4] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADAQ23875 running at a throughput rate of 15 MSPS.
[5] A throughput rate of 15 MSPS can only be achieved with a minimum SCK rate of TBD MHz.
[6] Transient response is the time required for the ADAQ23875 to acquire a full-scale input step to within ±1 LSB accuracy. Guaranteed by design, not subject to test.
[7] See the 1/f noise plot in Figure TBD.
[8] All ac specifications expressed in decibels are referenced to the full-scale input range (FSR) and are tested with an input signal at 1 dB below full scale, unless otherwise specified.
[9] Guaranteed by design, not subject to test.
[10] When REFBUF is overdriven, the internal reference buffer must be turned off by setting REFIN = 0 V. Refer to the Voltage Reference Input section.
[11] With all digital inputs forced to VIO or GND as required.
[12] During the acquisition phase.
[12] In two-lane mode, the VIO power dissipation is about 10 mW higher than one-lane mode.

TIMING SPECIFICATIONS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS− = −1 V ± 5%, VS− = 0 V[1] (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, 15 MSPS, gain = 0.37, 0.73, 0.87, 1.38, 2.25, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_{SMPL}	0.02		15	MSPS
Conversion Time—CNV Rising Edge to Data Available	t_{CONV}	54	58	63	ns
Acquisition Phase	t_{ACQ}		t_{CYC} -39		ns
Time Between Conversions	t_{CYC}	66.6		50,000	ns
CNV High Time	t_{CNVH}	5			ns
CNV Low Time	t_{CNVL}	8			ns
CNV↑ to First CLK↑ from the Same Conversion	$t_{FIRSTCLK}$	65			ns
CNV↑ to First CLK↓ from the Previous Conversion	$t_{LASTCLK}$			49	ns
CLK TO DCO Delay	t_{CLKDCO}	0.7	1.3	2.3	ns
SCK Low Time	t_{SCKL}	1.25			ns
SCK High Time	t_{SCKH}	1.25			ns
CLK to DA/DB Delay	t_{CLKD}	0.7	1.3	2.3	ns
DCO to DA/DB skew	t_{SKEW}	-200	0	200	ns
Sampling Delay Time	t_{AP}		0		ns
Sampling Delay Jitter	t_{JITTER}		0.25		ns

Timing Diagram

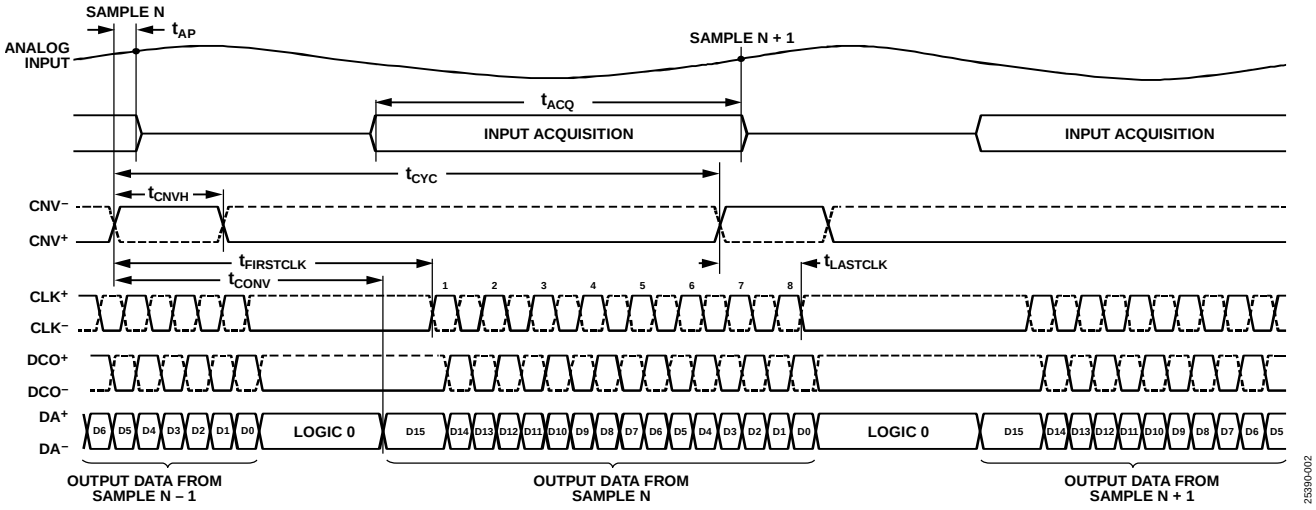

Figure 2. One-Lane Output Mode

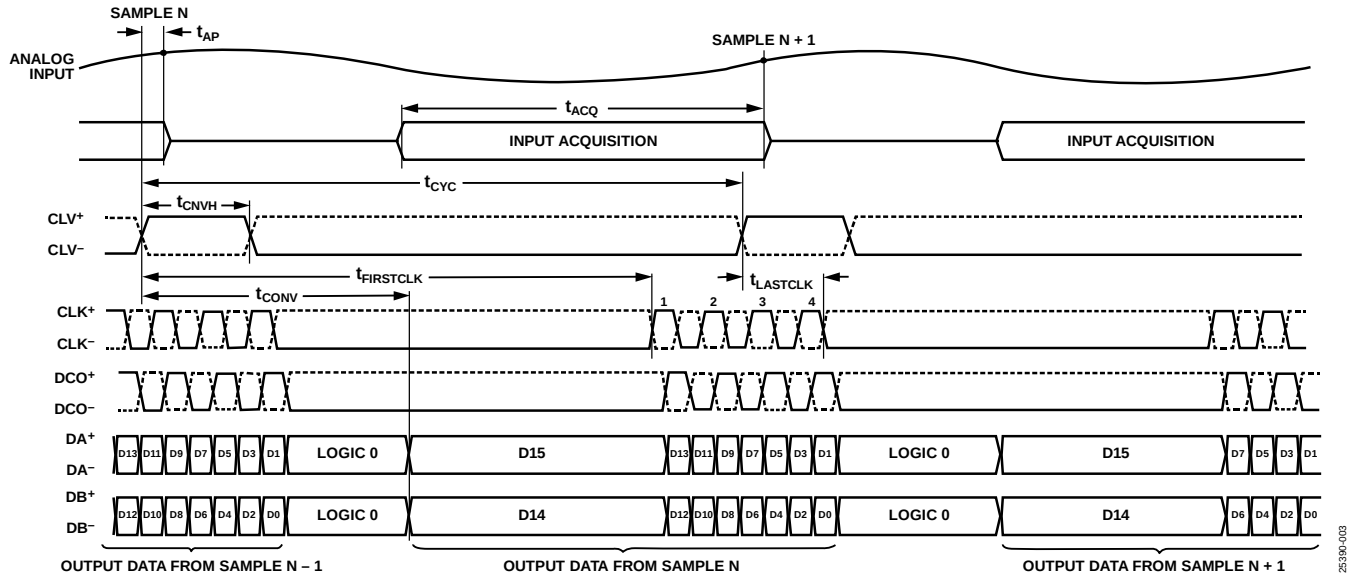

Figure 3. Two-Lane Output Mode

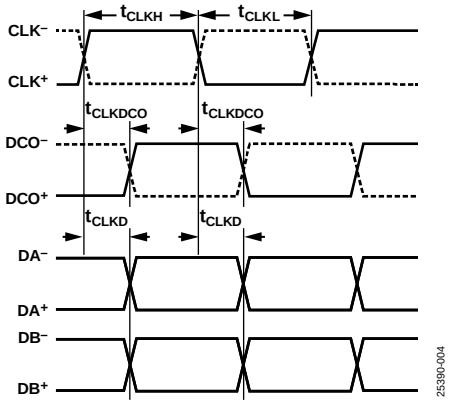

Figure 4. Data Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Inputs	
IN1+, IN1− to GND	−12 V to +12 V or ±10 mA[1]
Supply Voltage	
VDD to GND	6 V
VIO to GND	2.8 V
VS+ to VS−	11 V
VS+ to GND	−0.3 V to +11 V
VS− to GND	−11 V to +0.3 V
REFBUF to GND	−0.3 V to VDD + 0.3 V
REFIN to GND	−0.3 V to +2.8 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020

[1] Whichever occurs first. Current condition tested over a 10 ms time interval.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Unit
BC-100-7	48.4	35.1	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of 2S2P JEDEC PCB.
[2] θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.
[3] θ_{JC} is the junction to case thermal resistance.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Table 5. ADAQ23875, 100-Ball CSP_BGA

ESD Model	Withstand Threshold (V)
HBM	1250
FICDM	750

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

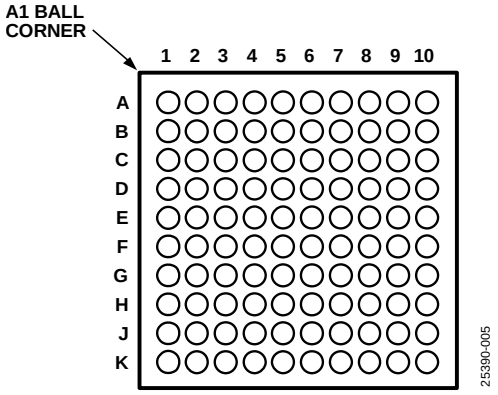

Figure 5. 100-Ball CSP BGA Top View

Table 6. 100-Ball CSP BGA Pin Configuration

	1	2	3	4	5	6	7	8	9	10
A	GND	IN1−	IN1+	GND	GND	GND	GND	VIO	GND	CNV+
B	PDB_AMP	IN1−	IN1+	GND	GND	GND	GND	TWOLANES	GND	CNV−
C	GND	MODE	GND	VS+	VS−	GND	GND	GND	GND	GND
D	GND	GND	GND	GND	GND	VCMO	GND	GND	GND	CLK+
E	GND	GND	GND	VS+	GND	GND	GND	GND	GND	CLK−
F	NC	NC	GND	GND	GND	GND	GND	GND	GND	GND
G	GND	GND	GND	GND	GND	GND	GND	GND	GND	DCO+
H	VS+	GND	GND	GND	GND	GND	GND	GND	GND	DCO−
J	VS−	GND	REFBUF	REFBUF	GND	GND	GND	GND	GND	DA+
K	GND	GND	REFIN	GND	PDB_ADC	VDD	TESTPAT	DB−	DB+	DA−

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, A4, A5, A6, A7, A9, B4, B5, B6, B7, B9, C1, C3, C6, C7, C8, C9, C10, D1, D2, D3, D4, D5, D7, D8, D9, E1, E2, E3, E5, E6, E7, E8, E9, F3, F4, F5, F6, F7, F8, F9, F10, G1, G2, G3, G4, G5, G6, G7, G8, G9, H2, H3, H4, H5, H6, H7, H8, H9, J2,J5, J6, J7, J8, J9, K1, K2, K4	GND	P	Power Supply Ground.
A2, B2	IN1−	AI	Negative Input of Fully Differential ADC Driver Connected to 550 Ω Resistor.
A3, B3	IN1+	AI	Positive Input of Fully Differential ADC Driver Connected to 550 Ω Resistor.
A8	VIO	P	2.5 V Analog and Output Power Supply. The range of VIO is 2.375 V to 2.625 V. Bypass this pin to GND with an at least 2.2 µF (0402, X5R) ceramic capacitor.
A10	CNV+	DI	Conversion Start LVDS Input. A rising edge on CNV+ puts the internal sample and hold in hold mode and starts a conversion cycle. CNV+ can be also driven with 2.5 V CMOS signal if CNV− is connected to GND.
B1	PDB_AMP	DI	Active Low. Connect this pin to GND to power down the fully differential ADC driver. Otherwise, connect this pin to VS+.
B8	TWOLANES	DI	Digital Input that Enables Two-Lane Output Mode. When TWOLANES is connected high (two-lane output mode), the ADAQ23875 outputs two bits at a time on DA−/DA+ and DB−/DB+. When TWOLANES is low (one-lane output mode), the ADAQ23875 outputs one bit at a time on DA−/DA+, and DB−/DB+ are disabled. Logic levels are determined by VIO.
B10	CNV−	DI	Conversion Start LVDS Input. A rising edge on CNV+ puts the internal sample and hold into the hold mode and starts a conversion cycle. CNV+ can be also driven with 2.5 V CMOS signal if CNV− is connected to GND.

Pin No.	Mnemonic	Type[1]	Description
C2	MODE	DI	Power Mode for Fully Differential Amplifier. Connect this pin to VS+ for full performance. Connect this pin to GND for power-down mode.
C4, E4, H1	VS+	P	Differential Amplifier and Reference Buffer Positive Supply. Bypass this pin to GND with an at least 2.2 µF (0402, X5R) ceramic capacitor.
C5, J1	VS−	P	Differential Amplifier Negative Supply. Bypass this pin to GND with an at least 2.2 µF (0402, X5R) ceramic capacitor.
D6	VCMO	AO	Differential Amplifier Output Common-Mode Voltage. Nominally REFBUF/2.
D10	CLK+	DI	LVDS Clock Input. This is an externally applied clock that serially shifts out the conversion result.
E10	CLK−	DI	LVDS Clock Input. This is an externally applied clock that serially shifts out the conversion result.
F1, F2	NC		Do Not Connect.
G10	DCO+	DO	LVDS Data Clock Output. This is an echoed version of CLK+/CLK− that can be used to latch the data outputs.
H10	DCO−	DO	LVDS Data Clock Output. This is an echoed version of CLK+/CLK− that can be used to latch the data outputs.
J3, J4	REFBUF	AO	Reference Buffer Output Voltage. As a required component of SAR architecture, a 10 µF ceramic bypass capacitor is already laid out within the ADAQ23875 between REFBUF and GND. Therefore, adding a second, smaller capacitor in parallel with the 10 µF capacitor may degrade performance and is not recommended.
J10	DA+	DO	Serial LVDS Data Output. In one-lane output mode, DB−/DB+ are not used and their LVDS driver is disabled to reduce power consumption.
K3	REFIN	P	Internal Reference Output/Reference Buffer Input. The output voltage of the internal reference, nominally 2.048 V, is output on this pin. An external reference can be applied to REFIN if a more accurate reference is required. If the internal reference buffer is not used, connect REFIN to GND to power down the buffer and connect an external buffered reference to REFBUF.
K5	PDB_ADC	DI	Digital Input that Enables the Power-Down Mode. When PDB_ADC is low, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) is shutdown. When PDB_ADC is high, the part operates normally. Logic levels are determined by VIO.
K6	VDD	P	5 V Analog Power Supply. The range of VDD is 4.75 V to 5.25 V. Short the two pins together and bypass them to GND with at least 2.2 µF (0402, X5R) ceramic capacitors.
K7	TESTPAT	DI	Digital Input that Forces the LVDS Data Outputs to be a Test Pattern. When TESTPAT is high, the digital outputs are test pattern. When TESTPAT is low, the digital outputs are the ADAQ23875 conversion result. Logic levels are determined by VIO.
K8	DB−	DO	Serial LVDS Data Output. In one-lane output mode, DA−/DA+ are not used and their LVDS driver is disabled to reduce power consumption.
K9	DB+	DO	Serial LVDS Data Outputs. In one-lane output mode, DA−/DA+ are not used and their LVDS driver is disabled to reduce power consumption.
K10	DA−	DO	Serial LVDS Data Outputs. In one-lane output mode, DB−/DB+ are not used and their LVDS driver is disabled to reduce power consumption.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, NC is no connection, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS− = −1 V ± 5%, VS− = 0 V[1] (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, 15 MSPS, gain = 2, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

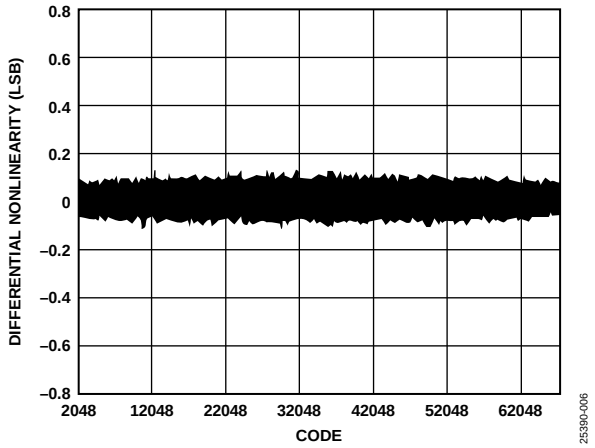

Figure 6. DNL vs. Code, f_S = 15 MSPS

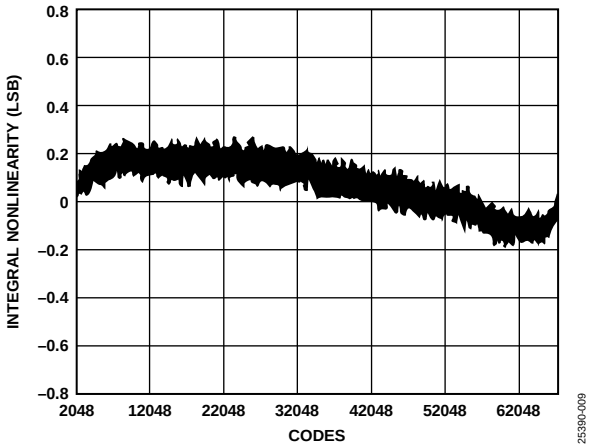

Figure 9. INL vs. Code, f_S = 15 MSPS

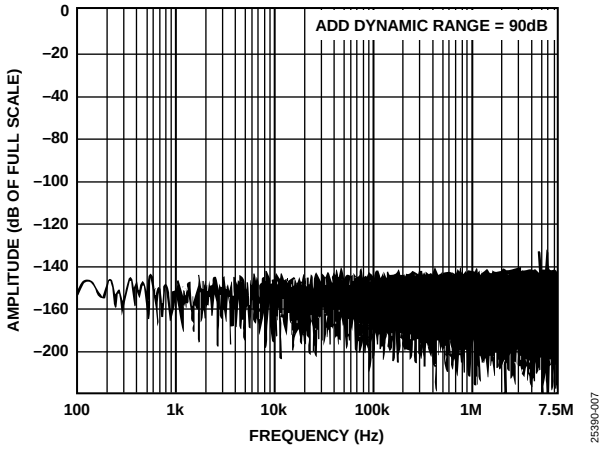

Figure 7. FFT, f_S = 15 MSPS, IN1+/IN1− Shorted to GND

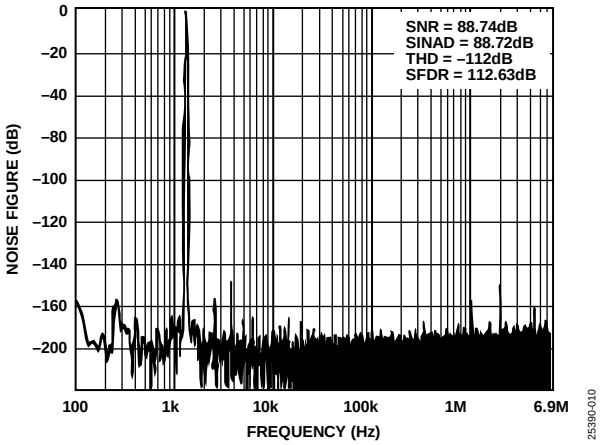

Figure 10. FFT, f_{IN} = 1 kHz, 13.8 MSPS, −0.5 dBFS, REFBUF = 4.096 V

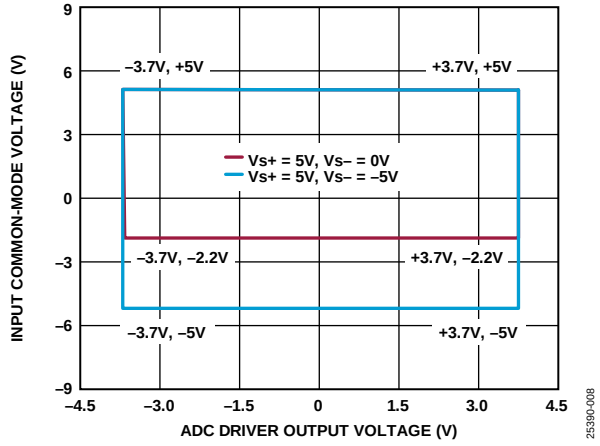

Figure 8. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 2, ±1.024 V Differential Input

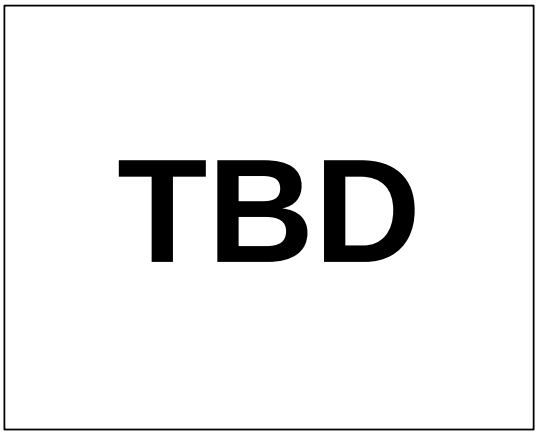

Figure 11.

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line

Differential Nonlinearity (DNL)
In an ideal µModule, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

Gain Error
The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

ENOB is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the µModule to acquire a full-scale input step to ±1 LSB accuracy.

Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the power in the µModule output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the input common-mode voltage of frequency, f.

$$CMRR \text{ (dB)} = 10\log(P_{\mu Module\_IN}/P_{\mu Module\_OUT})$$

where:
$P_{\mu Module\_IN}$ is the common-mode power at the frequency, f, applied to the inputs.
$P_{\mu Module\_OUT}$ is the power at the frequency, f, in the µModule output.

Power Supply Rejection Ratio (PSRR)
PSRR is the ratio of the power in the µModule output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the µModule VDD supply of frequency, f.

$$PSRR \text{ (dB)} = 10\log(P_{VDD\_IN}/P_{\mu Module\_OUT})$$

where:
P_{VDD_IN} is the power at the frequency, f, at the VDD pin.
$P_{\mu Module\_OUT}$ is the power at the frequency, f, in the µModule output.

THEORY OF OPERATION

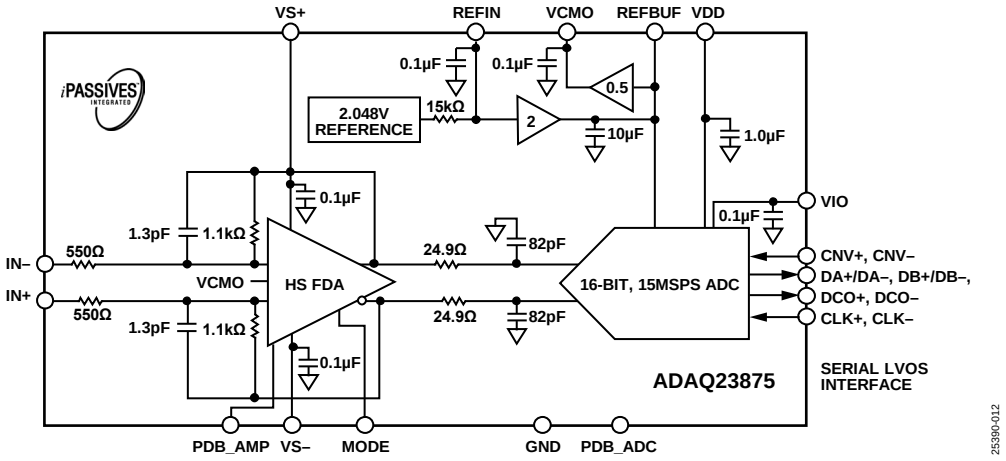

Figure 12. ADAQ23875 µModule Simplified Block Diagram

CIRCUIT INFORMATION

The ADAQ23875 is a precision, high speed µModule data acquisition solution that reduces the development cycle of a precision measurement systems by transferring the design burden of component selection, optimization, and layout from designer to the device. The ADAQ23875 reduces end system component count by combining multiple common signal processing and conditioning blocks in a single device including a low noise, fully differential ADC driver, a stable reference buffer, and a high speed, 16-bit, 15 MSPS successive approximation register (SAR) ADC. It also incorporates the Analog Devices proprietary iPASSIVES™ technology components necessary for optimum performance. The superior matching and drift characteristics of the resistors minimizes temperature dependent error sources. The ADAQ23875 includes a precision internal 2.048 V reference as well as an internal reference buffer. The ADAQ23875 also has a high speed serial LVDS interface that can output one or two bits at a time. The fast 15 MSPS throughput with no pipeline latency makes the ADAQ23875 ideally suited for a wide variety of high speed applications. The ADAQ23875 dissipates only 185 mW at 15 MSPS and has a power-down mode to reduce the power consumption to TBD µW during inactive periods.

TRANSFER FUNCTION

The ADAQ23875 µModule digitizes the full-scale voltage of 2× REFBUF into 2^{16} levels, resulting in an LSB size of 125 µV with REFBUF = 4.096 V. The output data is in twos complement format. The ideal transfer function is shown in Figure 13. The ideal offset binary transfer function can be obtained from the twos complement transfer function by inverting the most significant bit (MSB) of each output code.

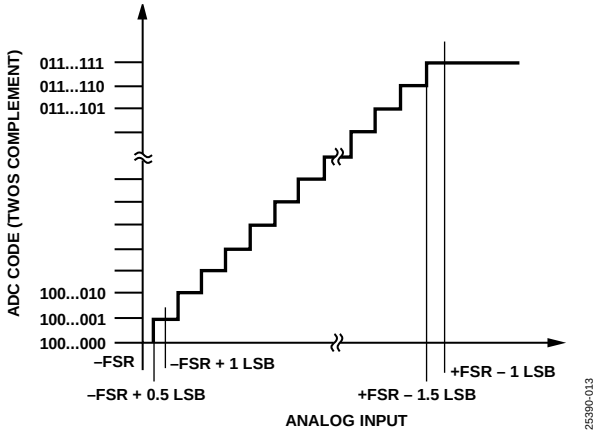

Figure 13. ADAQ23875 Transfer Function (FSR Is Full-Scale Range)

Table 8. Output Codes and Ideal Input Voltages

Description	Inputs Voltages	Digital Output Code (Twos Complement, Hex.)
FSR – 1 LSB	$(32{,}767 \times V_{REF})/(32{,}768 \times \text{gain})$	0x7FFF
Midscale + 1 LSB	$V_{REF}/(32{,}768 \times \text{gain})$	0x0001
Midscale	0 V	0x0000
Midscale – 1 LSB	$-V_{REF}/(32{,}768 \times \text{gain})$	0xFFFF
–FSR + 1 LSB	$-(32{,}767 \times V_{REF})/(32{,}768 \times \text{gain})$	0x8001
–FSR	$-V_{REF} \times \text{gain}$	0x8000

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAM

Figure 14 shows the typical application examples of differential signals applied to each of the ADAQ23875 inputs for a given gain with varying common-mode voltage. Figure 15 shows the typical application example of a single-ended signal applied to one of the ADAQ23875 inputs for a given gain with a fixed common-mode voltage of 0 V.

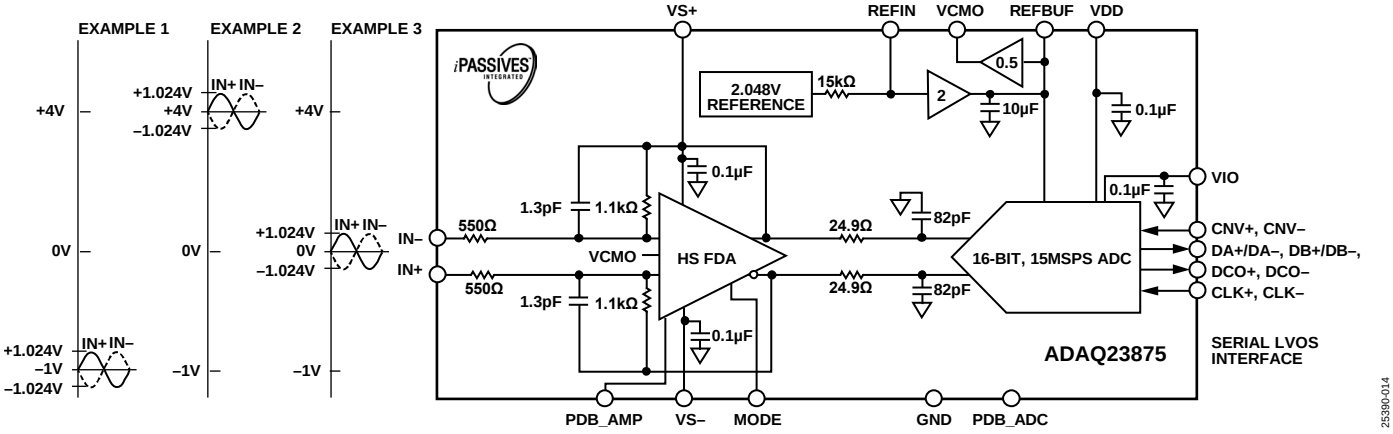

Figure 14. ADAQ23875 Differential Input Configuration with Gain = 2, ±2.048 V Input Range

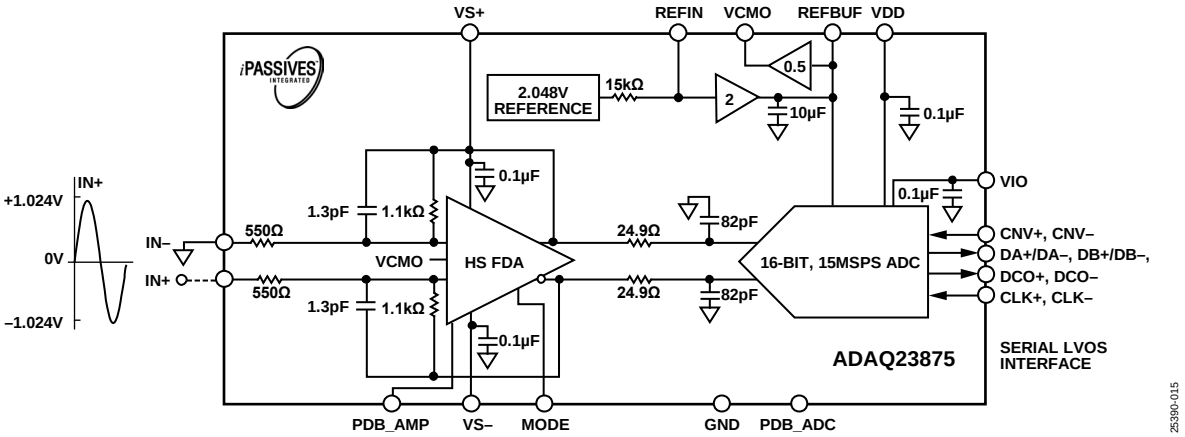

Figure 15. ADAQ23875 Single-Ended Input Configuration with Gain = 2, ±2.048 V Input Range

VOLTAGE REFERENCE INPUT

The ADAQ23875 µModule has an internal low noise, low drift (20 ppm/°C), band gap reference connected to REFIN. An internal reference buffer gains the REFIN voltage by 2× to 4.096 V at the REFBUF pin. The voltage difference between REFBUF and GND determines the full-scale input range of the ADAQ23875. The reference and reference buffer can also be externally driven if desired. Also housed in the ADAQ23875 is a 10 µF decoupling capacitor between REFBUF and GND that is ideally laid out within the device. This decoupling capacitor is a required component of the SAR architecture. Adding a second, smaller capacitor in parallel with the 10 µF capacitor may degrade performance and is not recommended.

Internal Reference with Internal Reference Buffer

To use the internal reference and internal reference buffer, bypass REFIN pin to GND with a 0.1µF ceramic capacitor.

External Reference with Internal Reference Buffer

If more accuracy and/or lower drift is desired, REFIN can be directly overdriven by an external 2.048 V reference as shown in Figure 16. Analog Devices offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power, and high accuracy, the LTC6655-2.048 is well suited for use with the ADAQ23875 when overdriving the internal reference. The LTC6655-2.048 offers 0.025% (maximum) initial accuracy and 2 ppm/°C (maximum) temperature coefficient for high precision applications.

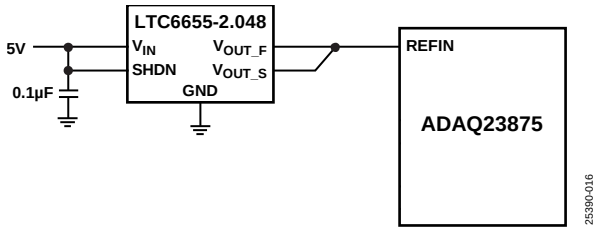

Figure 16. Using the LTC6655-2.048 as an External Reference

External Reference Buffer

The internal reference buffer can also be overdriven with an external 4.096 V reference at REFBUF as shown in Figure 17. To do so, REFIN must be grounded to disable the reference buffer. The external reference must have a fast transient response and be able to drive the 0.5 mA to 1.6 mA load at the REFBUF pin. The LTC6655-4.096 is recommended when overdriving REFBUF.

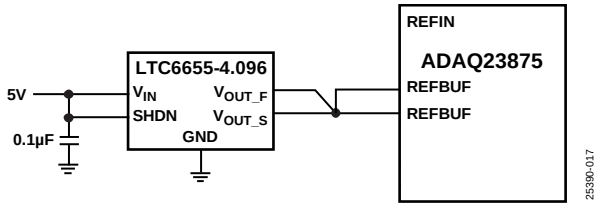

Figure 17. Overdriving REFBUF Using the LTC6655-4.096

COMMON-MODE OUTPUT

The VCMO pin is an output that provides one half the voltage present on the REFBUF pin. This voltage is used to set the common mode of a differential amplifier driving the analog inputs. If VCMO is not used, it can be left floating, but the parasitic capacitance on the pin must be under 10 pF.

POWER SUPPLY

The ADAQ23875 uses four power supplies: an internal ADC core supply (VDD), a digital input/output interface supply (VIO), a fully differential ADC driver positive supply (VS+), and a negative supply (VS–). Figure 18 shows the typical total power consumption including individual consumption for each of the VS+, VDD, and VIO supplies. It is recommended to bypass each of the supply pins (VDD, VIO, VS+, and VS–) with a 2.2 µF (0402, X5R) ceramic decoupling capacitor connected to GND. See the Board Layout section.

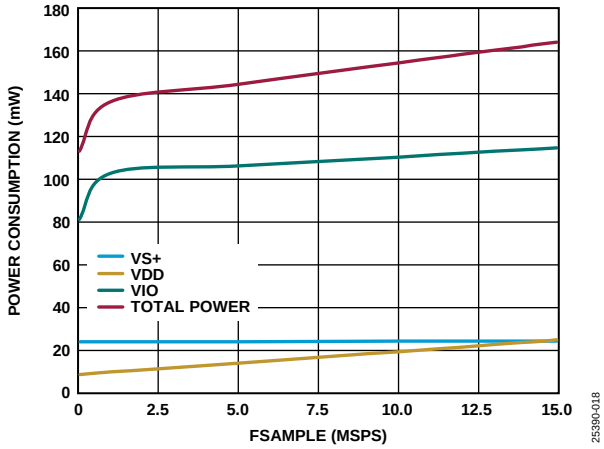

Figure 18. IN1+, IN1– Connected to GND, VS+ = 5 V, VS– = –1 V, REFBUF = 4.096 V

Power Supply Sequencing

The ADAQ23875 does not have any specific power supply sequencing requirements. The internal ADC core of ADAQ23875 has a power-on-reset (POR) circuit that resets the ADAQ23875 at initial power-up or whenever VDD drops well below the minimum values. After the supply voltage re-enters the nominal supply voltage range, the POR reinitializes the ADAQ23875.

Power-Down Mode

The power-down mode of fully differential ADC driver is asserted by applying a low logic level (GND) to the PDB_AMP pin to minimize the quiescent current consumed when the ADAQ23875 is not being used. When the PDB_AMP pin is connected to GND, the fully differential ADC driver output is high impedance. When PDB_ADC is low logic level, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) is shut down. When PDB_AMP and PDB_ADC are connected to a high logic level, the ADAQ23875 operates normally. The logic levels for both the PDB_AMP and PDB_ADC pins are determined by VS+ and VIO, respectively.

DIGITAL INTERFACE

The ADAQ23875 conversion is controlled by the CNV+ and CNV– inputs, which can be driven directly with an LVDS signal. Alternatively, the CNV+ pin can be driven with a 0 V to 2.5 V CMOS signal when CNV– is connected to GND. A rising edge on CNV+ samples the analog inputs and initiates a conversion. The pulse width of CNV+ should meet the t_{CNVH} and t_{CNVL} specifications in the timing table.

After the ADAQ23875 is powered on, or exits power-down mode, conversion data is invalid for the first two conversion cycles. The subsequent conversion results are accurate as long as the time between conversions meets the t_{CYC} specification. If the analog input signal has not completely settled when it is sampled, the ADAQ23875 noise performance is affected by jitter on the rising edge of CNV+. In this case, drive the rising edge of CNV+ with a clean, low jitter signal. Note that the ADAQ23875 is less sensitive to jitter on the falling edge of CNV+. In applications that are insensitive to jitter, CNV can be driven directly from an FPGA.

The ADAQ23875 has an internal clock that is trimmed to achieve a maximum conversion time of 63 ns. With a typical acquisition time of 27.7 ns, throughput performance of 15 MSPS is achieved.

The ADAQ23875 has a serial LVDS digital interface that is easy to connect to an FPGA. Three LVDS pairs are required: CLK±, DCO±, and DA±. A fourth LVDS pair, DB±, is optional (see Figure 19). Route the LVDS signals on the PC board as 100 Ω differential transmission lines and terminated at the receiver with 100 Ω resistors. The optional LVDS output, DB±, is enabled, and data is output two bits at a time on DA± and DB±. Enabling the DB± output increases the supply current from VIO by about 3.6 mA. In two-lane mode, four clock pulses are required for CLK± (see Figure 23).

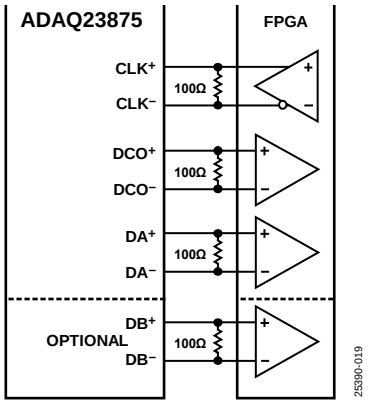

Figure 19. Digital Output Interface to an FPGA

One-Lane Output Mode

A conversion is started by the rising edge of CNV+. When the conversion is complete, the most significant data bit is output on DA±. Data is then ready to be shifted out by applying a burst of eight clock pulses to the CLK± input. The data on DA± is updated by every edge of CLK±. An echoed version of CLK± is output on DCO±. The edges of DA± and DCO± are aligned, so DCO± can be used to latch DA± in the FPGA. The timing of a single conversion is shown in Figure 20 and Figure 21. Data must be clocked out after the current conversion is complete, and before the next conversion finishes. The valid time window for clocking out data is shown in Figure 22. Note that it is allowed to be still clocking out data when the next conversion begins.

Two-Lane Output Mode

At high sample rates, the required LVDS interface data rate can reach >400 Mbps. Most FPGAs can support this rate, but if a lower data rate is desired, the two-lane output mode can be used. When the TWOLANES input pin is connected high (VIO), the ADAQ23875 outputs two bits at a time on DA–/DA+ and DB–/DB+, as shown in Figure 23.

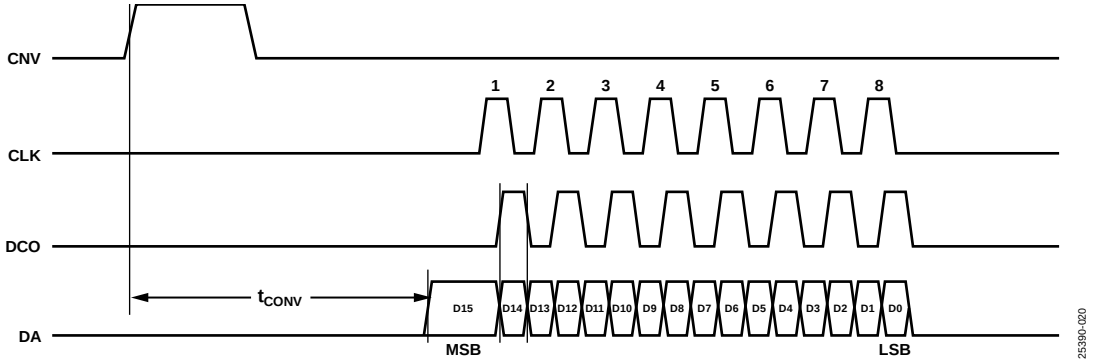

Figure 20. Timing Diagram for a Single Conversion in One-Lane Mode

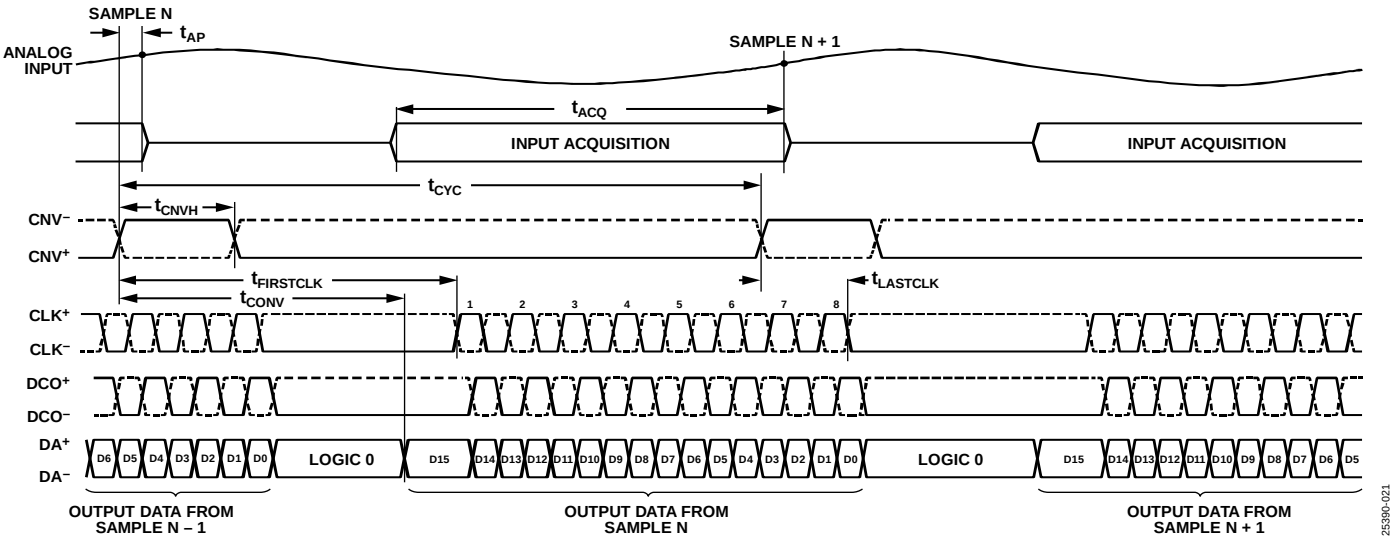

Figure 21. Timing Diagram for Multiple Conversions in One-Lane Output Mode

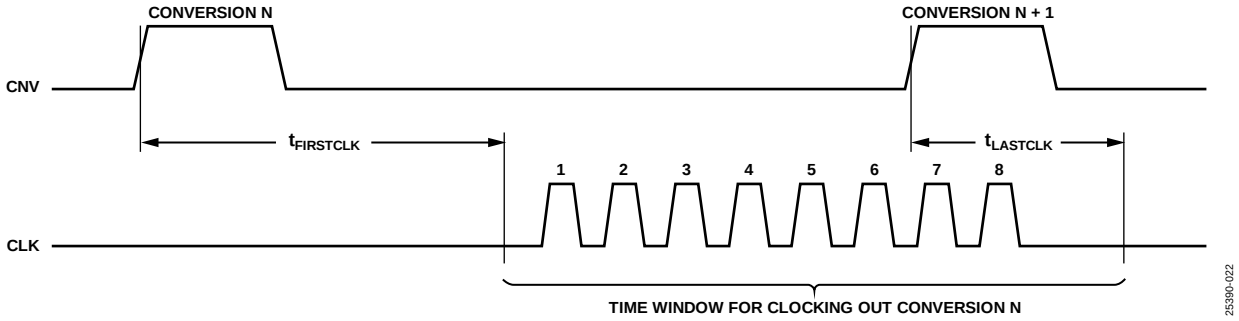

Figure 22. Valid Time Window for Clocking Out Data

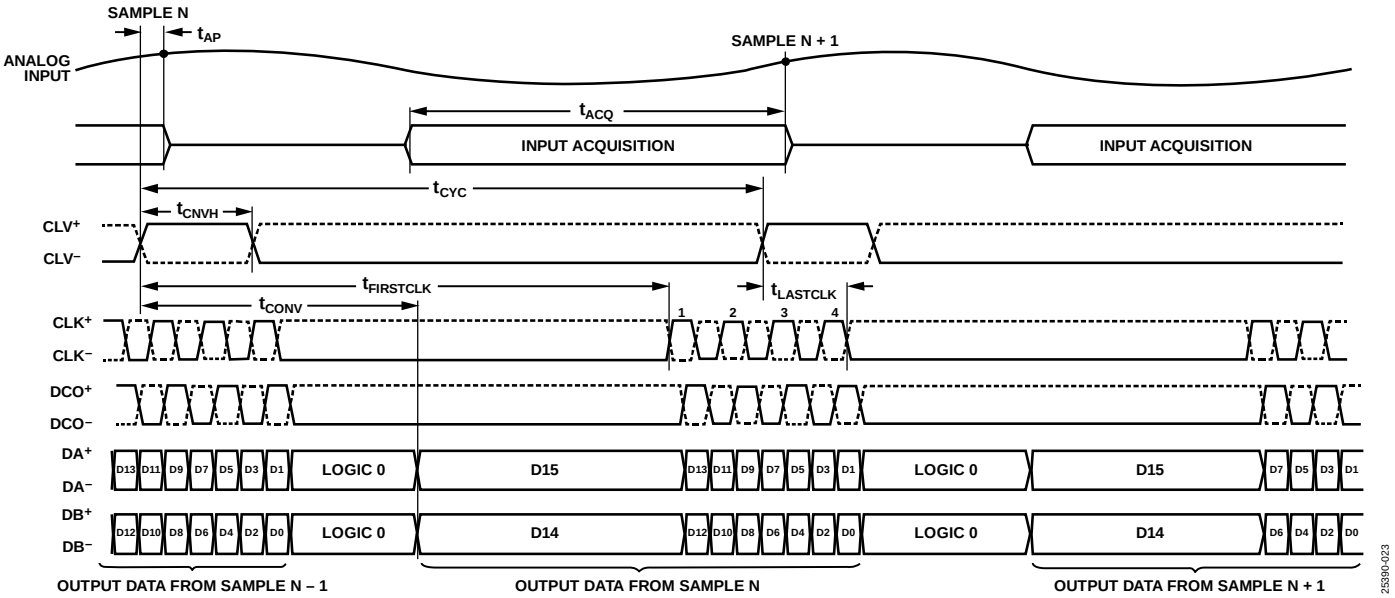

Figure 23. Two-Lane Output Mode

Output Test Patterns

The test pattern is enabled when the TESTPAT pin is brought high (VIO) to allow in-circuit testing of the digital interface of the ADAQ23875 and forces its LVDS data outputs to be a test pattern. The ADAQ23875 digital data outputs known values as a test pattern as follows:

- One-lane mode: 1010 0000 0111 1111
- Two-lane mode: 1100 1100 0011 1111

When the TESTPAT pin connected low (GND), the ADAQ23875 digital data outputs the conversion results.

BOARD LAYOUT

The printed circuit board (PCB) layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ23875. A multilayer board with an internal, clean ground plane in the first layer beneath the ADAQ23875 is recommended. Care must be taken with the placement of individual components and routing of various signals on the board. It is especially recommended to route input and output signals symmetrically. Solder the ground pins of the ADAQ23875 directly to the ground plane of the PCB using multiple vias. Remove the ground and power planes beneath the input and output pins of ADAQ23875 to avoid undesired parasitic capacitance.

The sensitive analog and digital sections must be separated on PCB while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as CNV± or CLK±, and digital outputs DA±, DB± should not run near or cross over analog signal paths to prevent noise coupling to the ADAQ23875.

Good quality ceramic bypass capacitors of at least 2.2 µF (0402, X5R) must be placed between each of supply pins VDD, VIO, VS+, and VS− of the ADAQ23875 and GND to minimize EMI susceptibility and reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ23875, saving extra board space and cost.

Mechanical Stress Shift

The mechanical stress of mounting a device to a board may cause subtle changes to the SNR and internal voltage reference. The best soldering method is to use IR reflow or convection soldering with a controlled temperature profile. Hand soldering with a heat gun or a soldering iron is not recommended

OUTLINE DIMENSIONS

100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-7)
Dimensions shown in millimeters

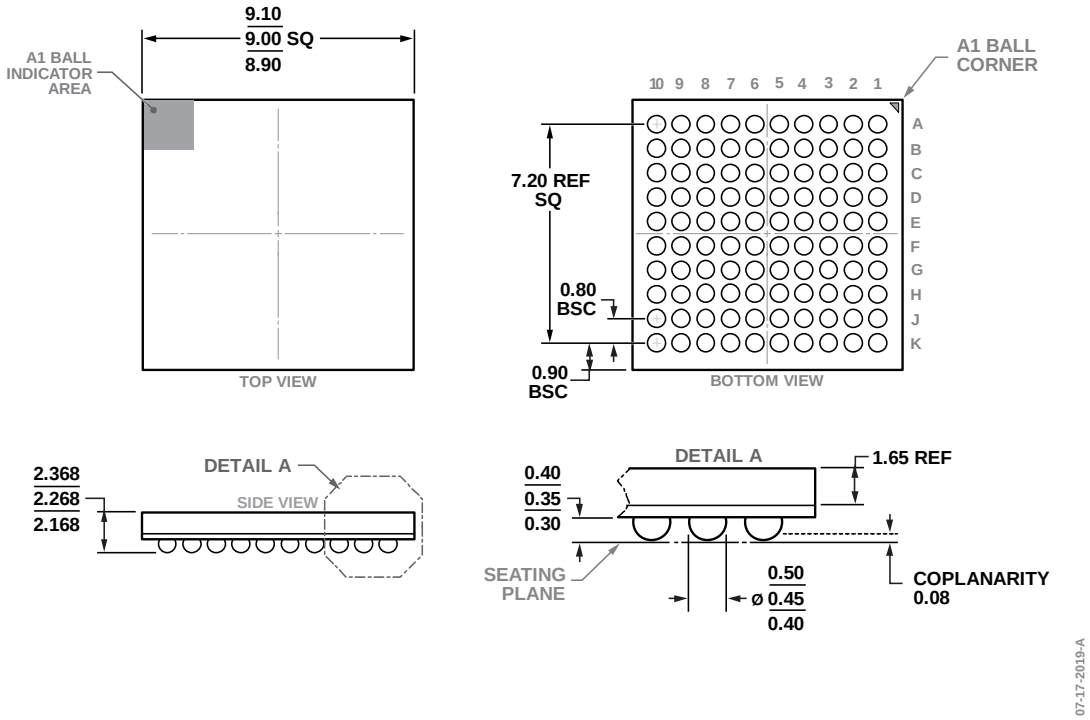

Figure 24. 100-Ball, 9 mm × 9 mm Chip Scale Package Ball Grid Array [CSP_BGA]

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PR25390-10/20(PrA)