Data Sheet

ADA4356

Programmable Transimpedance, Current to Bits Receiver µModule

FEATURES

- High performance, current input, data-acquisition µModule that includes
  - Programmable-gain transimpedance amplifier (PGTIA)
  - Fully differential amplifier (FDA)
  - Programmable analog low-pass filter (LPF)
  - 14-bit 125MSPS ADC
  - Three selectable gains
  - Integrated 1.8V LDO for the ADC
- Small form factor: 12.00mm × 6.00mm BGA
- Operation from a single 3.3V supply
- PGTIA selectable gains single 20ns pulse sensitivity
  - T_Z = 133kΩ, 250nA to 10µA
  - T_Z = 11kΩ, 1µA to 100µA
  - T_Z = 4.54kΩ, 10µA to 300µA
- Optional external current divider circuit enables current detections up to 60mA
- Fast input overload recovery
- Analog filter for noise reduction and anti-alias filtering
  - Selectable 1.0MHz and 100MHz LPF bandwidth
- Low input referred current noise: 3.5nA RMS
  - T_Z = 133kΩ, 1MHz analog filter
- 14-bit ADC with sample rate up to 125MSPS
  - Serial LVDS data output
  - Serial peripheral interface (SPI) controls
- Quiescent power: 546mW, LDO enabled
- Temperature range: −40°C to +85°C

APPLICATIONS

- Time of flight (ToF)
- Current to bits conversion
- Range finder
- Fiber optic sensing
- Optical time domain reflectometry (OTDR)

GENERAL DESCRIPTION

The ADA4356 is a low-noise, wide dynamic-range, current input, analog-to-digital converter (ADC) µModule. For space savings in size conscious applications, the ADA4356 includes all the required active and passive components to realize a complete current-to-bits data-acquisition solution with programmable gain and filter characteristics.

The high-speed transimpedance amplifier (TIA) front-end amplifier in the ADA4356 supports 20ns pulse widths, which allows high spatial resolution for the ToF measurements, and exhibits fast overdrive recovery from large input signals. The ADA4356 includes three selectable TIA feedback resistor values for programmable TIA gain.

An internal analog low-pass filter offers either 100MHz or 1MHz cutoff frequencies to reduce broadband noise and serve as an anti-aliasing filter for the ADC inputs. For lower bandwidth signals, the 1MHz filter configuration offers additional noise reduction.

Following the TIA and filter blocks, a 14-bit pipeline ADC converts the analog signal at 125MSPS and outputs the digitized signals through two serial, low voltage, differential signaling (LVDS) data lanes operating at rates up to 1GBPS per lane. The data clock output (DCO) operates at frequencies of up to 500MHz and supports double data rate (DDR) operation.

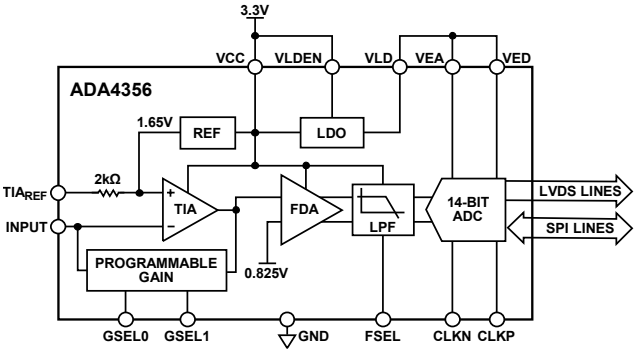

Figure 1. Simplified Block Diagram

Rev. 0; 10/25

TECHNICAL SUPPORT

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SIMPLIFIED APPLICATION DIAGRAM

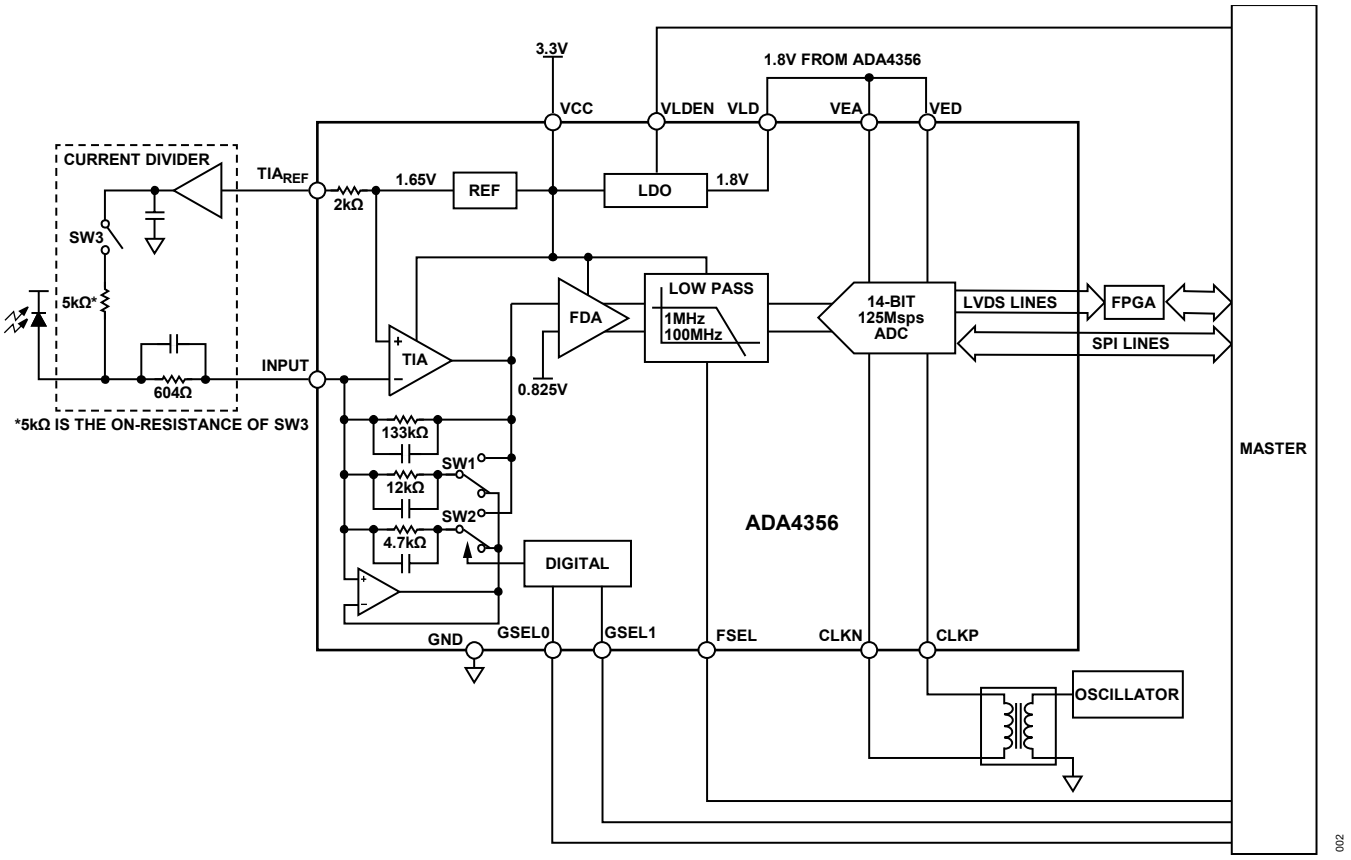

Figure 2. Simplified Application Block Diagram

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGES
0	10/25	Initial release	—

SPECIFICATIONS

Table 1. Performance Specifications

(T_A = 25°C, V_{CC} = 3.3V, LDO enabled (see the power connection scheme shown in *Figure 3*), FSEL = 0, and the source capacitance (C_S) = 0.5pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
Input Referred Current Noise, C_S = 5pF	i_N	T_Z = 4.54kΩ[1]		68		nA rms
		T_Z = 11kΩ[2]		33		nA rms
		T_Z = 133kΩ		8.4		nA rms
		T_Z = 133kΩ, FSEL = 1		3.5		nA rms
		T_Z = 4.54kΩ, 65,536 averages		270		pA rms
		T_Z = 11kΩ, 65,536 averages		130		pA rms
		T_Z = 133kΩ, 65,536 averages		31		pA rms
		T_Z = 133kΩ, FSEL = 1, 65,536 averages		14		pA rms
Equivalent Voltage Noise at Output, C_S = 5pF	v_N	T_Z = 4.54kΩ		310		µV rms
		T_Z = 11kΩ		363		µV rms
		T_Z = 133kΩ		1.11		mV rms
		T_Z = 133kΩ, FSEL = 1		0.465		mV rms
Input Voltage	V_{IN}			1.65		V
Noninverting TIA internal reference voltage	TIA_{REF}[3]	No load		1.65		V
Input Bias Current	I_B			±1		nA
Linear Input Current Range	I_{IN}	T_Z = 4.54kΩ		+3 to +300		µA
		T_Z = 11kΩ		+1 to +100		µA
		T_Z = 133kΩ		+0.1 to +10		µA
T_Z Gain Accuracy	$\Delta T_Z/T_Z$	All gains		±1	±5	%
Input Capacitance	C_{IN}			2		pF
ADC Input Bias Voltage	V_{BIAS}	I_{IN} = 0µA, all gains[3]		825		mV
AC PERFORMANCE						

(T_A = 25°C, V_{CC} = 3.3V, LDO enabled (see the power connection scheme shown in *Figure 3*), FSEL = 0, and the source capacitance (C_S) = 0.5pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Referred Supply Sensitivity		All gains		0.5		nA/mV
TIA Bandwidth	TIA_{BW}	T_Z = 4.54kΩ		38		MHz
		T_Z = 11kΩ		22		MHz
		T_Z = 133kΩ		3.5		MHz
LPF Bandwidth	LPF_{BW}	FSEL = 0		100		MHz
		FSEL = 1		1		MHz
ADC PERFORMANCE						
ADC Internal Reference Voltage	V_{REF}		0.98	1	1.02	V
Resolution	N		14			Bits
Sampling Rate	F_S		20		125	MSPS
No Missing Code				Guaranteed		
DIGITAL OUTPUTS, ANSI-644						
Logic Compliance				LVDS		
Differential Output Voltage	V_{OD}		290	345	400	mV
Output Offset Voltage	V_{OS}		1.15	1.25	1.35	V
Output Coding (Default)				Two's complement		
TEMPERATURE						
Operation Temperature Range			−40		+85	°C

1 T_Z = 4.54kΩ is 4.7kΩ ‖ 133kΩ.

2 T_Z = 11kΩ is 12kΩ ‖ 133kΩ.

3 See *Figure 2*.

Table 2. Power Specifications

(T_A = 25°C and V_{CC} = 3.3V, unless otherwise noted. VEA and VED are the internal ADC 1.8 V supply rails (See *Figure 3*), and VLD is the 1.8 V integrated LDO output.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
VCC Range	V_{CC}		3.1	3.3	3.6	V
VCC Current	I_{VCC}	LDO enabled[1]		165		mA
		LDO disabled[2]		72		mA
ADC Digital Circuit Supply	VED	LDO disabled[2]		1.8 ± 5%		V
VED Current	I_{VED}			47		mA
ADC Analog Circuit Supply	VEA	LDO disabled[2]		1.8 ± 5%		V
VEA Current	I_{VEA}			47		mA
On-Chip LDO Output	VLD	LDO enabled[1]		1.8		V
Quiescent Power	P_Q	LDO enabled[1]		546		mW
		LDO disabled[2]		406		mW
		ADC power-down mode		238		mW
		ADC standby mode		322		mW

[1] See *Figure 3*.

[2] See *Figure 4*.

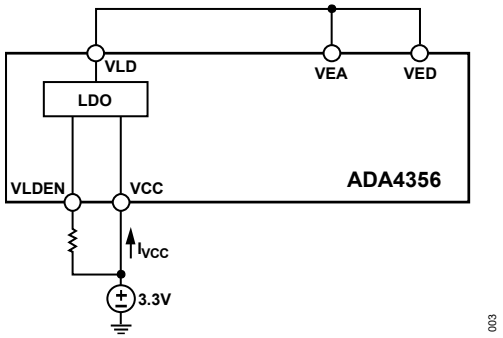

Figure 3. On-Chip LDO Enabled

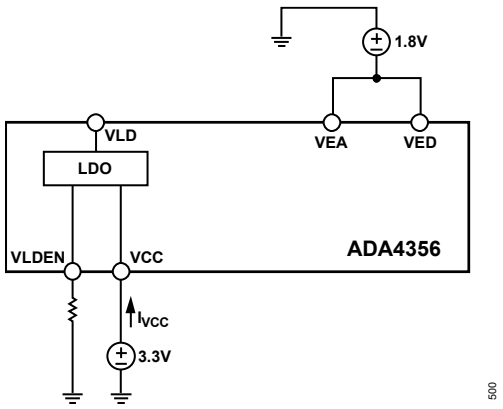

Figure 4. On-Chip LDO Disabled

Table 3. CLK, SPI, and Control Specifications

(T_A = 25°C, V_{CC} = 3.3V, and LDO enabled (see the power scheme shown in *Figure 3*), unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLKP AND CLKN)						
External Clock Frequency			10		1000	MHz
Conversion Rate			10		125	MSPS
Logic Compliance				MOS, LVDSL, VPECL		
Differential Input Voltage		For LVDS and LVPECL	0.2		3.6	Vp-p
Input Voltage Range			GND − 0.2		VEA + 0.2	V
Input Common-Mode Voltage	V_{CM}			0.9		V
Input Resistance (Differential)	$R_{IN,CLK}$			15		kΩ
Input Capacitance	$C_{IN,CLK}$			4		pF
SPI CLOCK						
SCLK Frequency					25	MHz
SPI INPUTS (SCLK, $\overline{CS}$, AND SDIO)						
Input High Voltage	V_{INH}		1.2		VEA + 0.2	V
Input Low Voltage	V_{INL}		0		0.8	V
SCLK Input Resistance	$R_{IN,SCLK}$			30		kΩ
SCLK Input Capacitance	$C_{IN,SCLK}$			2		pF
$\overline{CS}$ Input Resistance	$R_{IN,CS}$			26		kΩ
$\overline{CS}$ Input Capacitance	$C_{IN,CS}$			2		pF

(T_A = 25°C, V_{CC} = 3.3V, and LDO enabled (see the power scheme shown in *Figure 3*), unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDIO Input Resistance	$R_{IN,SDIO}$			26		kΩ
SDIO Input Capacitance	$C_{IN,SDIO}$			5		pF
SPI OUTPUT (SDIO)						
Logic 1 Output Voltage	V_{OH}	High output current (I_{OH}) = 800µA		1.79		V
Logic 0 Output Voltage	V_{OL}	Low output current (I_{OL}) = 50µA			0.05	V
OTHER CONTROL INPUTS (GSEL0, GSEL1, FSEL, AND VLDEN)						
Input High Voltage	V_{INH}		2		VCC	V
Input Low Voltage	V_{INL}		0		0.4	V
Input Low Current	I_{INL}	Input voltage (V_{IN}) = V_{INL}		40		nA
Input High Current	I_{INH}	Input voltage (V_{IN}) = V_{INH}		40		nA
Input Capacitance	$C_{IN,SEL}$			2		pF

Table 4. ADC SPI Timing Requirements

(T_A = 25°C and V_{CC} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING REQUIREMENTS (See *Figure 5*, unless otherwise noted)						
Setup Time	t_{DS}	Between the data and the rising edge of SCLK	2			ns
Hold Time	t_{DH}	Between the data and the rising edge of SCLK	2			ns
SCLK Period	t_{CLK}		40			ns
Setup Time	t_S	Between $\overline{CS}$ and SCLK	2			ns
Hold Time	t_H	Between $\overline{CS}$ and SCLK	2			ns
SCLK	t_{HIGH}	Pulse width high	10			ns
	t_{LOW}	Pulse width low	10			ns
SDO Switching[1]	t_{EN_SDIO}	SDIO switch time from input to output relative to the SCLK falling edge	10			ns
SDO Switching[1]	t_{DIS_SDIO}	SDIO switch time output to input relative to the SCLK rising edge	10			ns

[1] This parameter is not shown in *Figure 5*.

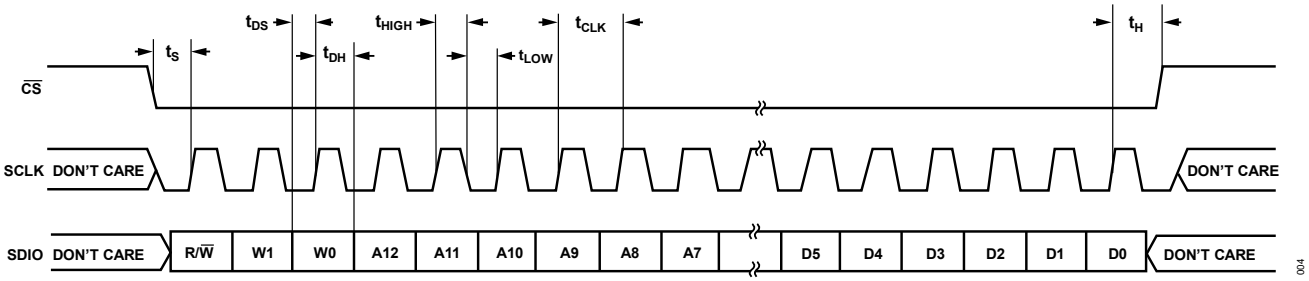

Figure 5. Serial Port Interface Timing Diagram

Table 5. ADC LVDS Output Specifications[1, 2]

(Full temperature range, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK[3]						
Input Rate			10		1000	MHz
Conversion Rate[4]	f_{conv}		10		125	MSPS
Pulse Width	t_{EH}	High		6.25 to 4.0		ns
	t_{EL}	Low		6.25 to 4.0		ns
OUTPUT PARAMETERS[3]						
Propagation Delay	t_{PD}		1.5	2.3	3.1	ns
Rise Time[5]	t_R	20% to 80%		300		ps
Fall Time[5]	t_F	80% to 20%		300		ps
Frame Clock Output (FCO) Propagation Delay	t_{FCO}		1.5	2.3	3.1	ns
DCO Propagation Delay[6]	t_{CPD}			t_{FCO} + (t_{SAMPLE}/16)		ns
DCO to Data Delay[6]	t_{DATA}		(t_{SAMPLE}/16) − 300	t_{SAMPLE}/16	(t_{SAMPLE}/16) + 300	ps
DCO to FCO Delay[6]	t_{FRAME}		(t_{SAMPLE}/16) − 300	t_{SAMPLE}/16	(t_{SAMPLE}/16) + 300	ps
Lane Delay	t_{LD}			90		ps
Data to Data Skew[5]	$t_{DATA-MAX}$ − $t_{DATA-MIN}$			±50	±200	ps
Wake-Up Time		Standby, 25°C		250		ns
		Power-down, 25°C		375		µs
Pipeline Latency				16		Clock Cycles
APERTURE						
Aperture Delay	t_A	25°C		1		ns
Aperture Uncertainty (Jitter)[5]	t_J	25°C		174		fs rms

(Full temperature range, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Out-of-Range Recovery Time		25°C		1		Clock Cycles

1 For the definitions and for more details on how these tests are completed, refer to the Application Note AN-835: *Understanding High Speed ADC Testing and Evaluation*.

2 These parameters are measured on standard FR4 materials.

3 The clock can be adjusted via the SPI.

4 The conversion rate is the clock rate after the divider. Valid for 2-lane operation.

5 This parameter is not shown in *Figure 6* through *Figure 11*.

6 $t_{SAMPLE}/16$ is based on the number of bits in two LVDS data lanes. $t_{SAMPLE} = 1/f$.

ADC LVDS Output Timing Diagrams

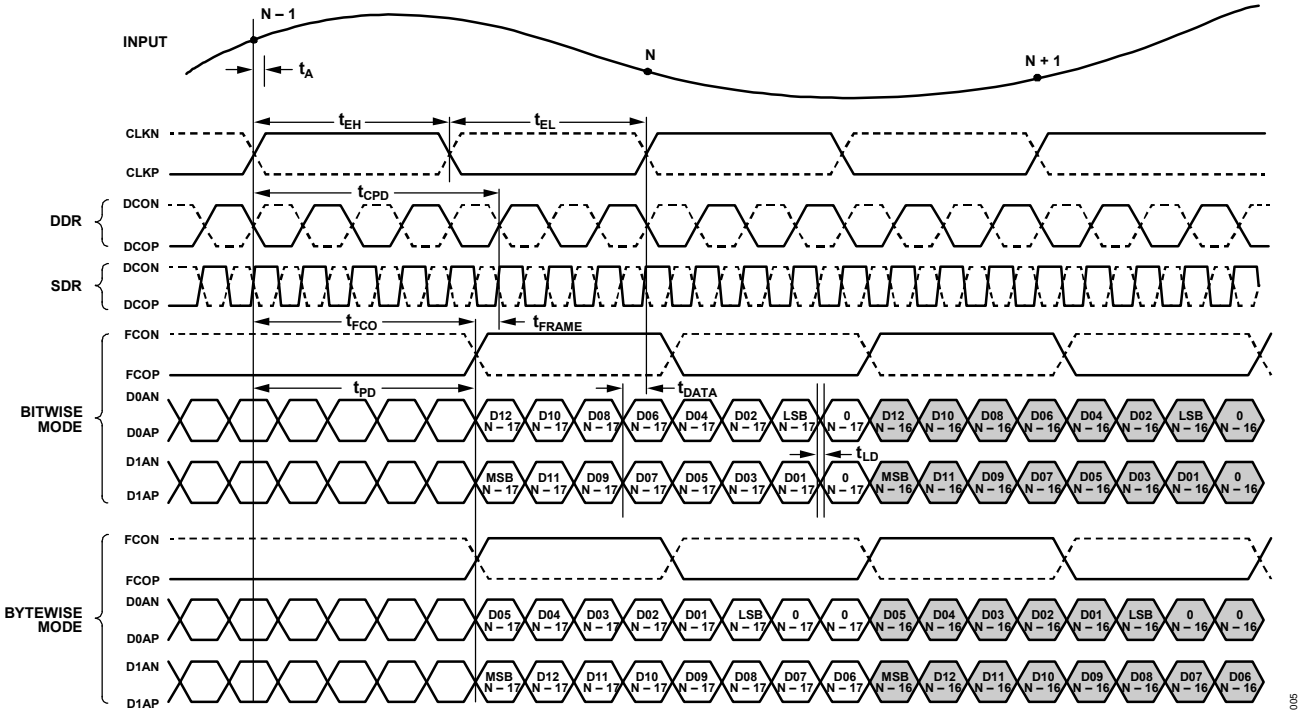

Figure 6. 16-Bit DDR/Single Data Rate (SDR), 2-Lane, 1× Frame Mode (Default)

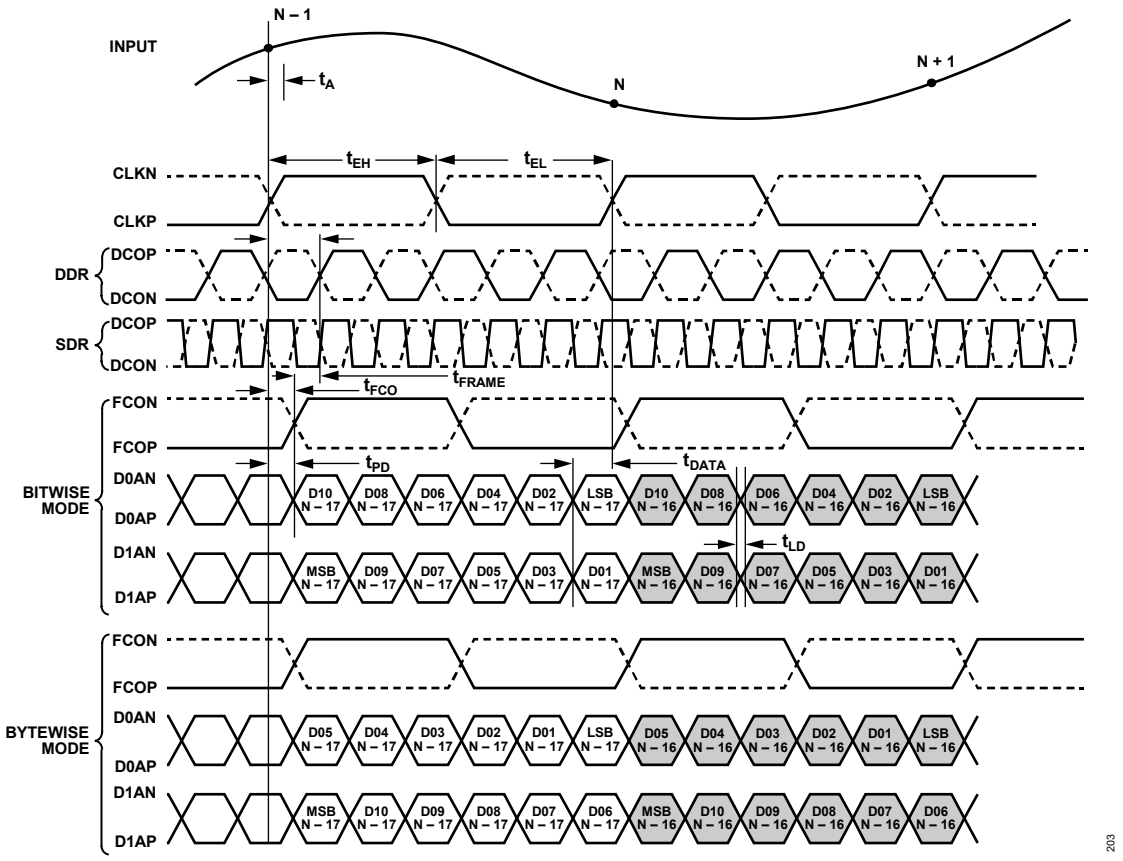

Figure 7. 12-Bit DDR/SDR, 2-Lane, 1× Frame Mode

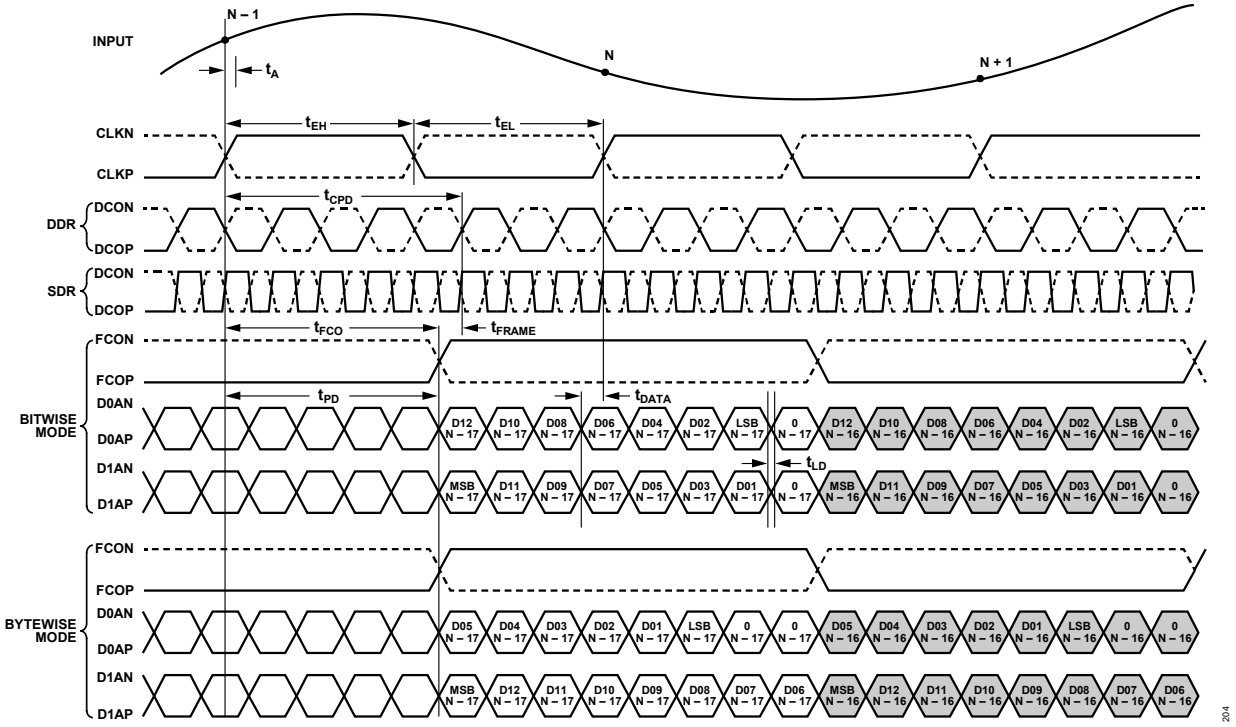

Figure 8. 16-Bit DDR/SDR, 2-Lane, 2× Frame Mode

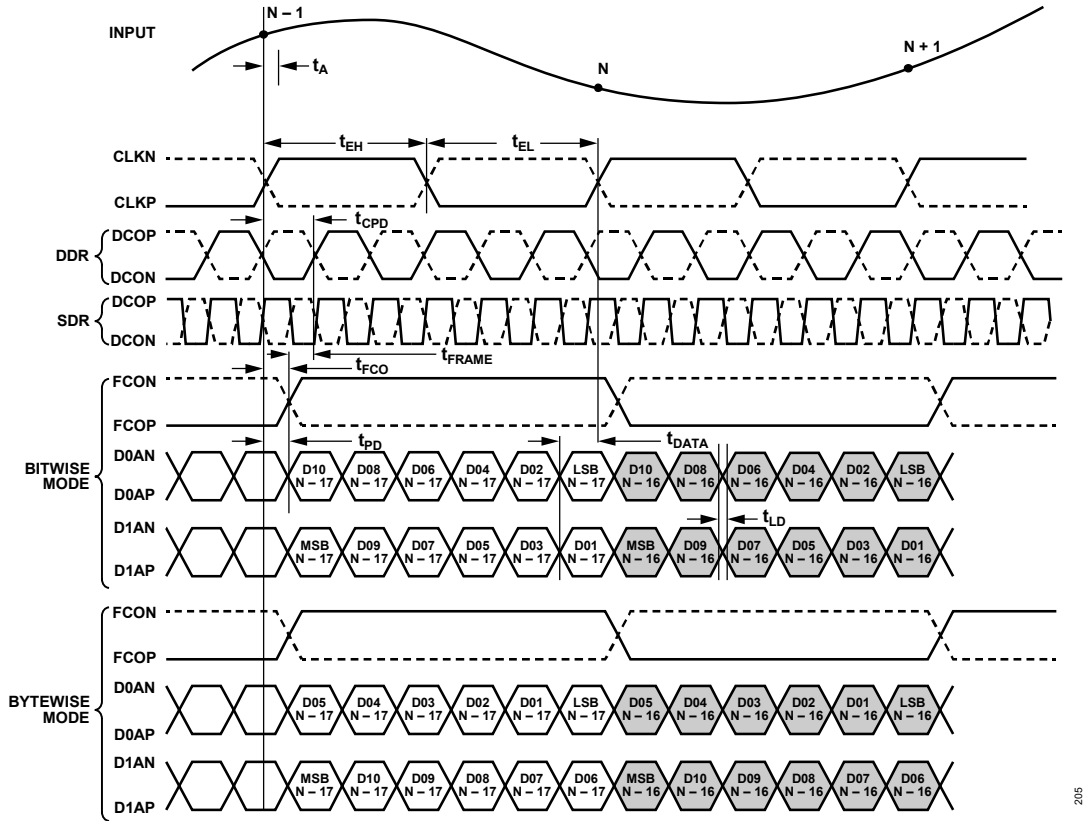

Figure 9. 12-Bit DDR/SDR, 2-Lane, 2× Frame Mode

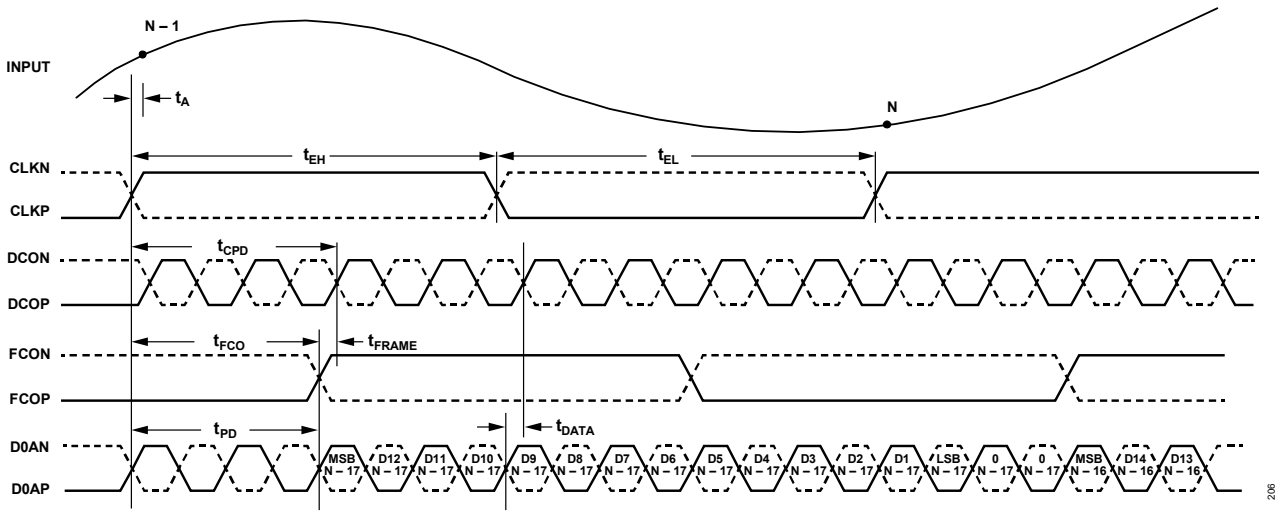

Figure 10. Wordwise DDR, 1-Lane, 1× Frame, 16-Bit Output Mode

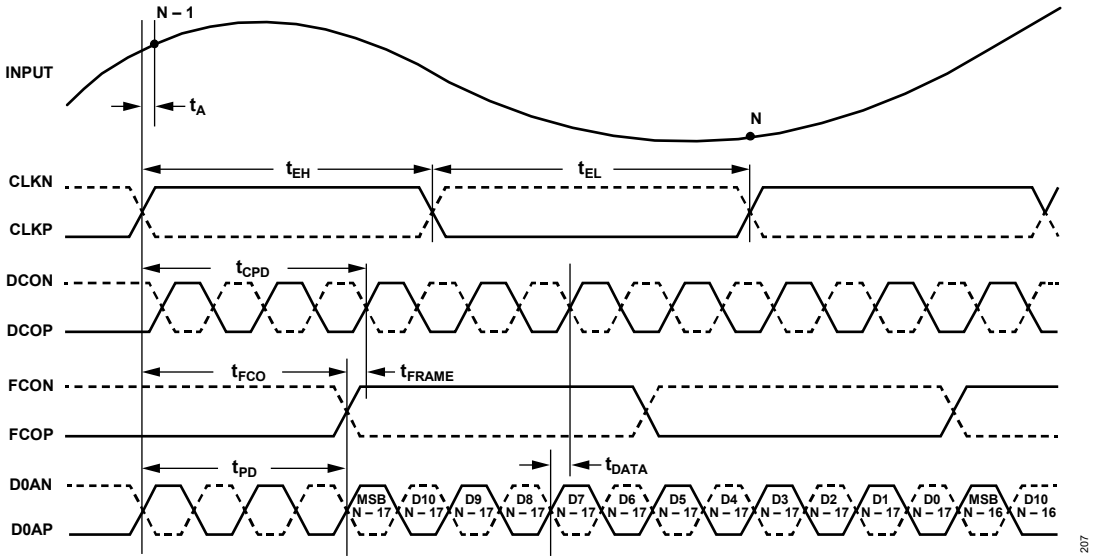

Figure 11. Wordwise DDR, 1-Lane, 1× Frame, 12-Bit Output Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 6. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC} to GND	−0.3V to +4.0V
VEA, VED to GND	−0.3V to +2.0V
VLD to GND	−0.3V to V_{CC}
CLKP, CLKN, SPI[1] to GND	−0.3V to +2.0V
INPUT to GND	−0.2V to V_{CC} + 0.2V
Analog Input Current	40mA
Control[2] to GND	−0.3V to V_{CC} + 0.3V or 1mA, whichever occurs first
Digital Output[3] to GND	−0.3V to +2.0V
Environmental Temperature	
Storage Range (Ambient)	−65°C to +125°C
Maximum Junction	+125°C
Assemble (Soldering, 10sec)	300°C
Electrostatic Discharge (ESD)	
Human Body Model, INPUT (Ball E1) and TIA_{REF} (Ball F1) Balls	500V
Human Body Model, All Other Balls	3000V
Field Induced Charge Device Model (FICDM)	1250V

1 Includes SCLK, SDIO, and $\overline{CS}$.

2 Includes FSEL, GSEL1, GSEL0, and VLDEN.

3 Includes D0AP, D0AN, D1AP, D1AN, DCOP, DCON, FCOP, and FCON.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Thermal resistance values specified in *Table 7* are calculated based on standard JEDEC specifications.

Table 7. Thermal Resistance

PACKAGE TYPE	Θ_{JA}	Θ_{JC_TOP}	Ψ_{JT}	UNIT
BC-84-4	52.6	22.0	17.7	°C/W

Only use θ_{JA} and θ_{JC_TOP} to compare thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. One common mistake is to use θ_{JA} and θ_{JC} to estimate the junction temperature in the system environment. Instead, using Ψ_{JT} is a more appropriate way to estimate the worst-case junction temperature of the device in the system environment. First, take an accurate thermal measurement of the top center of the device (on the mold compound in this case) while the device operates in the system environment. This measurement is known in the following equation as T_{TOP}. Then, use this equation to solve for the worst-case T_J in that given environment as follows:

$$T_J = \Psi_{JT} \times P + T_{TOP}$$

where:

Ψ_{JT} is the junction-to-top thermal characterization number as specified in the data sheet.

P refers to the total power dissipation in the chip (W).

T_{TOP} refers to the package top temperature (°C) and is measured at the top center of the package in that given environment.

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

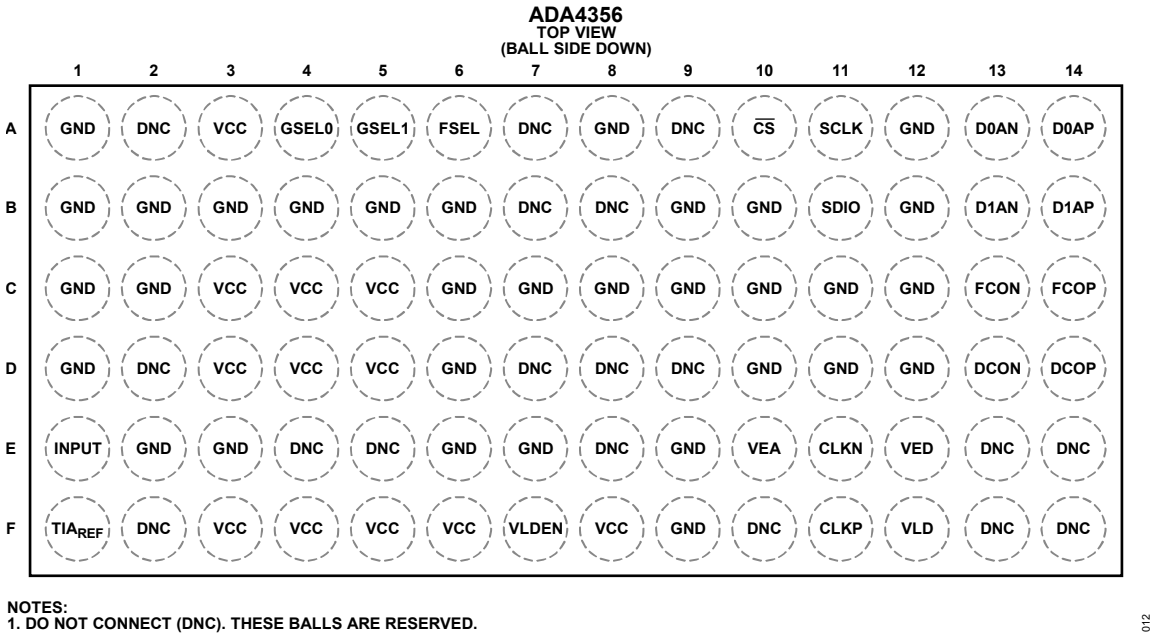

Figure 12. Ball Configuration

Table 8. Ball Descriptions

BALL	NAME	DESCRIPTION	TYPE
A1, A8, A12, B1, B2, B3, B4, B5, B6, B9, B10, B12, C1, C2, C6, C7, C8, C9, C10, C11, C12, D1, D6, D10, D11, D12, E2, E3, E6, E7, E9, F9	GND	Ground.	P[1]
A3, C3, C4, C5, D3, D4, D5, F3, F4, F5, F6, F8	VCC	3.3V Power Supply.	P[1]
E10	VEA	1.8V Analog Power Supply to ADC.	P[1]
E12	VED	1.8V Digital Power Supply to ADC.	P[1]
F1	TIA_{REF}	1.65V reference voltage for TIA DC Bias. See the *Extending Input Current Range* section.	AO[2]
F12	VLD	1.8V LDO Output. Connect VLD to VEA and VED to power the ADC from the internal LDO. Leave VLD floating if the ADC is powered from an external source. Do not connect VLD to external circuitry.	PO[3]

BALL	NAME	DESCRIPTION	TYPE
F7	VLDEN	VLD Output Enable. Set VLDEN = 1 to enable the VLD output.	DI[4]
A6	FSEL	LPF Bandwidth Select. FSEL selects 100MHz (FSEL = 0) or 1.0MHz (FSEL = 1) LPF bandwidth.	DI[4]
A10	$\overline{CS}$	Chip Select. Set $\overline{CS}$ = 0 to enable SPI mode. $\overline{CS}$ has an internal 15kΩ pull-up resistor.	DI[4]
B11	SDIO	Serial Data Input/Output. In SPI mode, SDIO is a bidirectional SPI data input/output with a 31kΩ internal pull-down resistor.	DIO[5]
A11	SCLK	SPI Clock Input in SPI Mode. SCLK has a 30 kΩ internal pull-down resistor.	DI[4]
D13, D14	DCON, DCOP	Data Clock Outputs, Differential LVDS Signal.	DO[6]
C13, C14	FCON, FCOP	Frame Clock Outputs, Differential LVDS Signal.	DO[6]
B13, B14	D1AN, D1AP	Lane 1 Digital Outputs, Differential LVDS Signal.	DO[6]
A13, A14	D0AN, D0AP	Lane 0 Digital Outputs, Differential LVDS Signal.	DO[6]
F11, E11	CLKP, CLKN	ADC Sampling Clock Inputs, Differential LVDS Signal.	DI[4]
A4, A5	GSEL0, GSEL1	TIA Gain Selection. For the truth table, see *Table 11*.	DI[4]
E1	INPUT	Analog Input. Input to Programmable Gain Transimpedance Amplifier (PGTIA).	AI[7]
A2, A7, A9, B7, B8, D2, D7,D8, D9, E4, E5, E8, E13, E14, F2, F10, F13, F14	DNC	Do Not Connect. These balls are reserved.	N/A[8]

1 P means power.

2 AO means analog output.

3 PO means power output.

4 DI means digital input.

5 DIO means digital input/output.

6 DO means digital output.

7 AI means analog input.

8 N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V, no averaging, and LDO enabled (see the power scheme shown in *Figure 3*), unless otherwise noted.

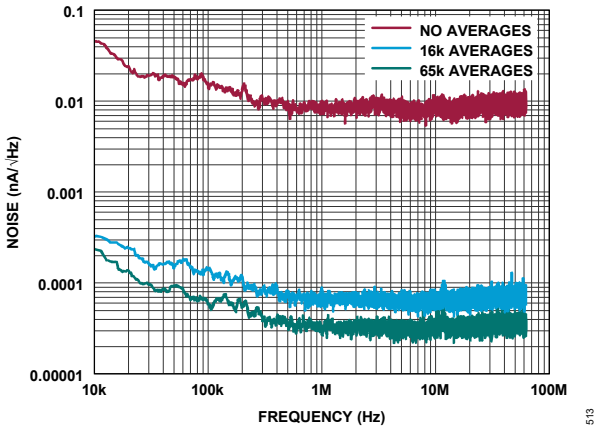

Figure 13. Noise Spectral Density, T_Z = 4.54kΩ, LPF = 100MHz

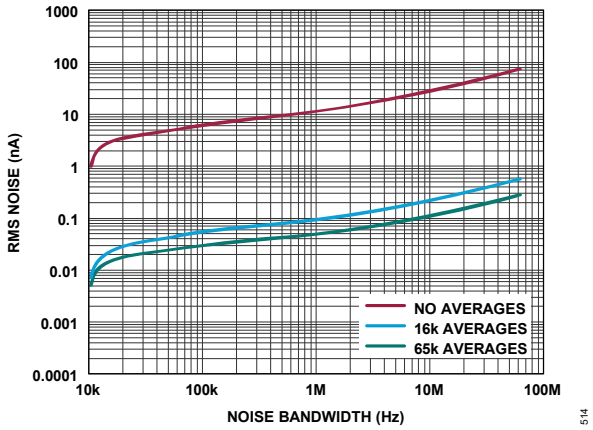

Figure 14. RMS Noise vs. Noise Bandwidth, T_Z = 4.54kΩ, LPF = 100MHz

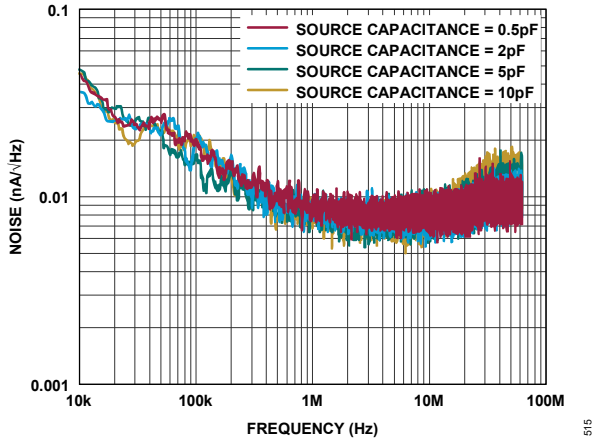

Figure 15. Noise Spectral Density for Various Source Capacitances, TZ = 4.54kΩ, LPF = 100MHz

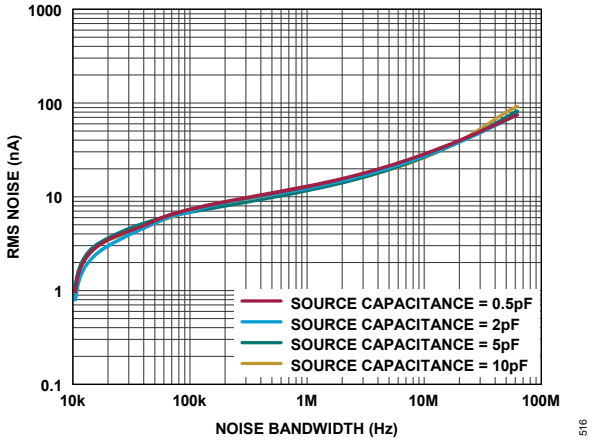

Figure 16.RMS Noise vs. Noise Bandwidth for Various Source Capacitances, T_Z = 4.54kΩ, LPF = 100MHz

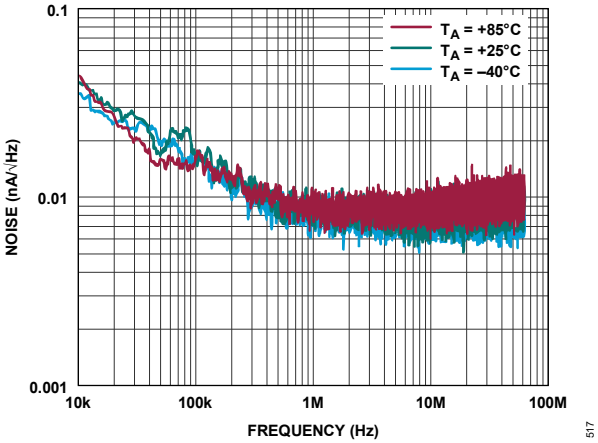

Figure 17. Noise Spectral Density for Various Temperatures, T_Z = 4.54kΩ, LPF = 100MHz

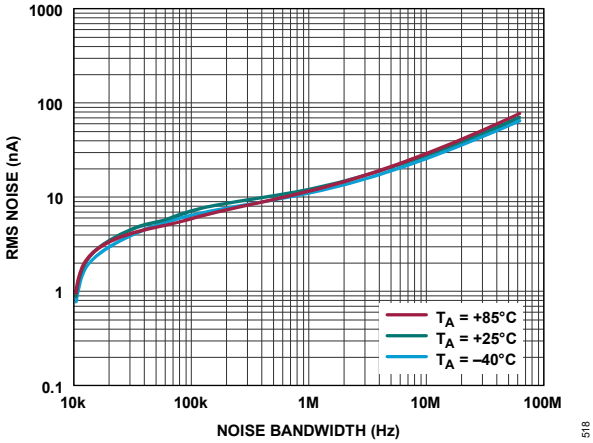

Figure 18. RMS Noise vs. Noise Bandwidth for Various Temperatures, T_Z = 4.54kΩ, LPF = 100MHz

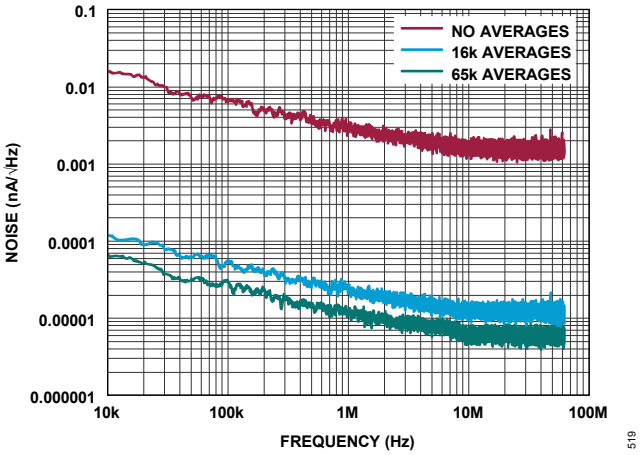

Figure 19. Noise Spectral Density, T_Z = 11kΩ, LPF = 1MHz

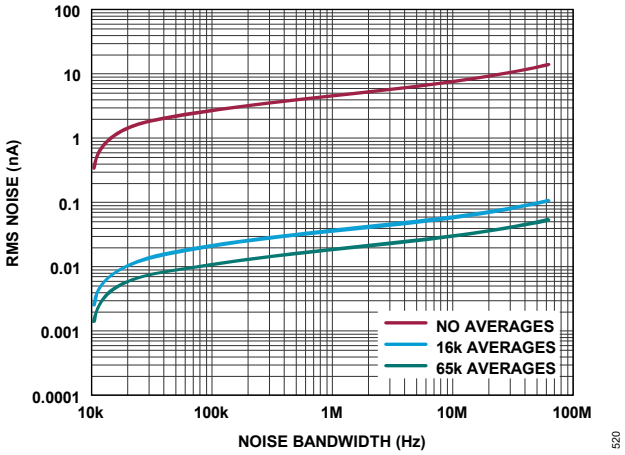

Figure 20. RMS Noise vs. Noise Bandwidth, T_Z = 11kΩ, LPF = 1MHz

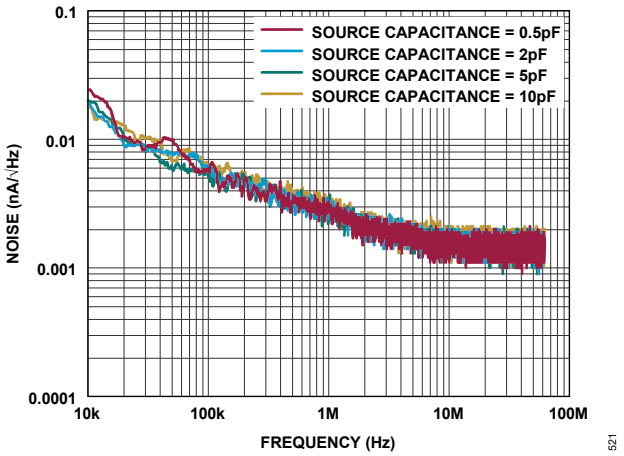

Figure 21. Noise Spectral Density for Various Source Capacitances, T_Z = 11kΩ, LPF = 1MHz

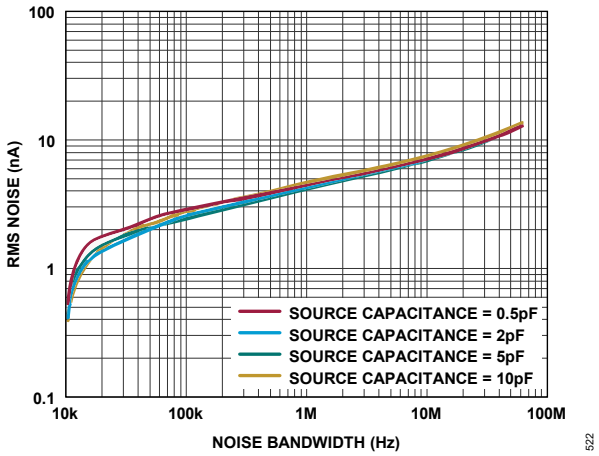

Figure 22. RMS Noise vs. Noise Bandwidth for Various Source Capacitances, T_Z = 11kΩ, LPF = 1MHz

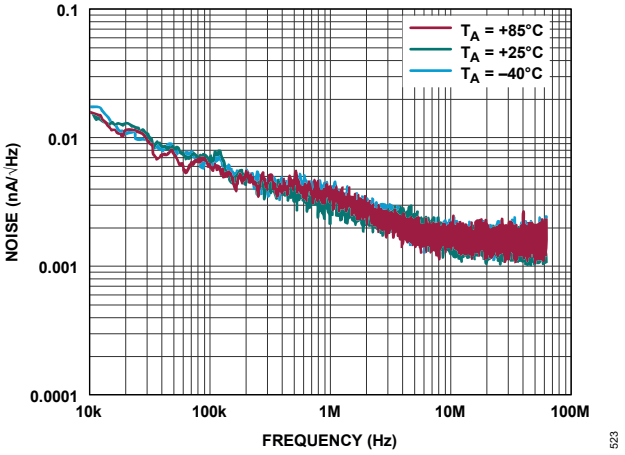

Figure 23. Noise Spectral Density for Various Temperatures, T_Z = 11kΩ, LPF = 1MHz

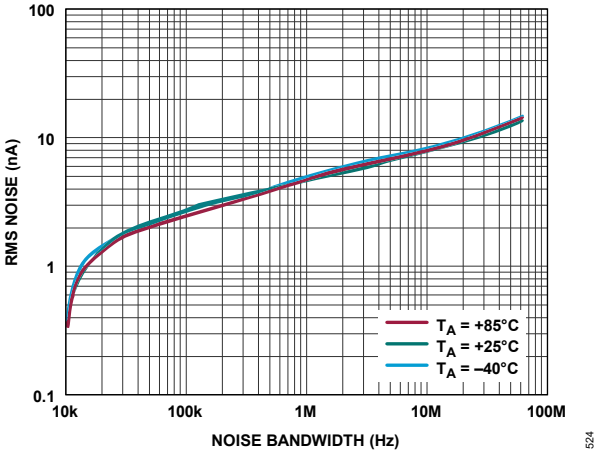

Figure 24. RMS Noise vs. Noise Bandwidth for Various Temperatures, T_Z = 11kΩ, LPF = 1MHz

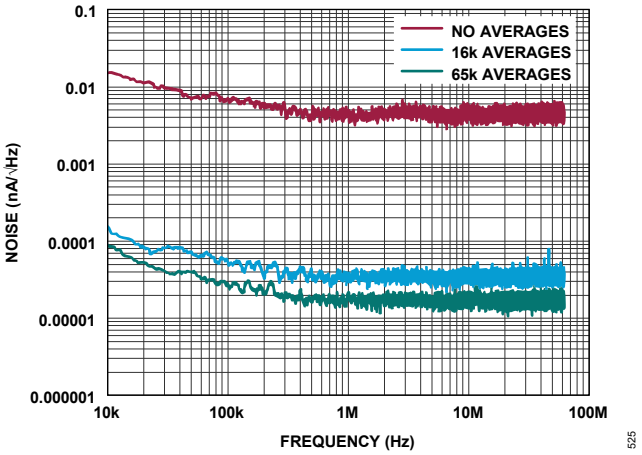

Figure 25. Noise Spectral Density, T_Z = 11kΩ, LPF = 100MHz

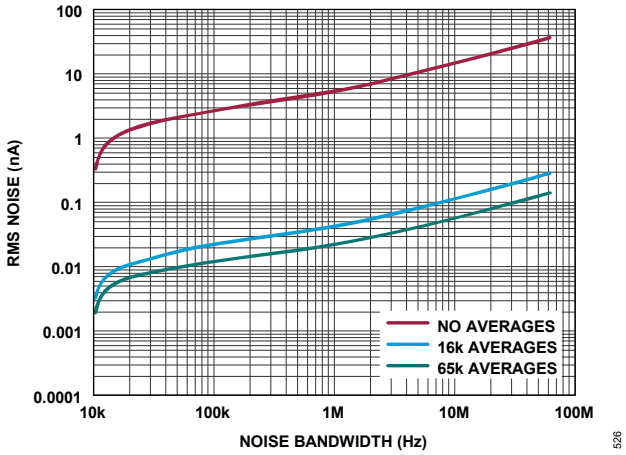

Figure 26. RMS Noise vs. Noise Bandwidth, T_Z = 11kΩ, LPF = 100MHz

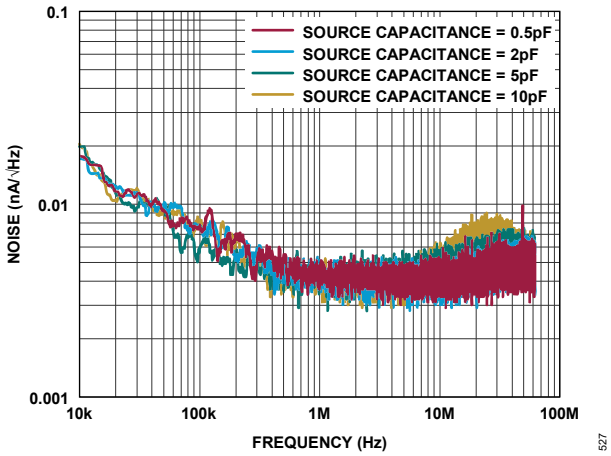

Figure 27. Noise Spectral Density for Various Source Capacitances, T_Z = 11kΩ, LPF = 100MHz

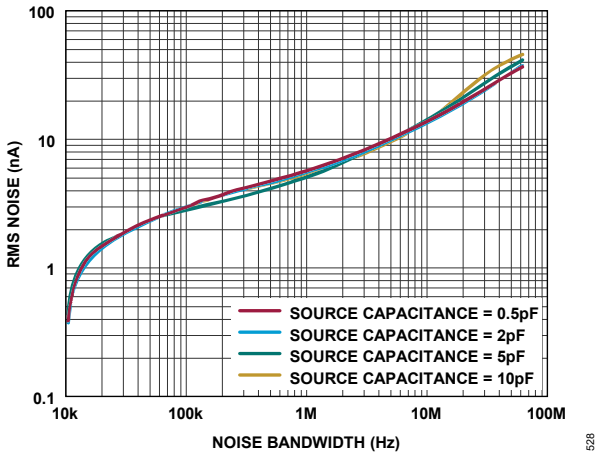

Figure 28. RMS Noise vs. Noise Bandwidth for Various Source Capacitances, T_Z = 11kΩ, LPF = 100MHz

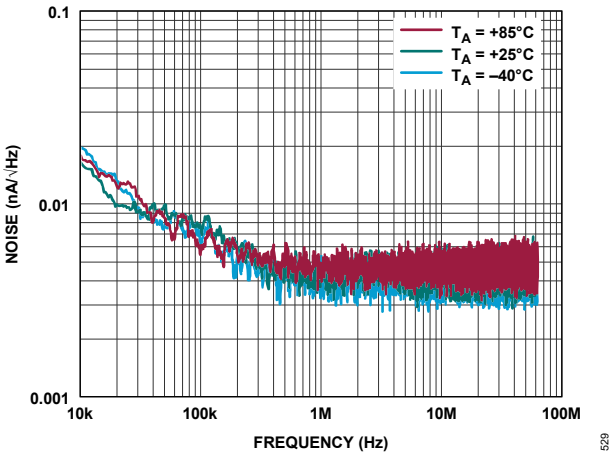

Figure 29. Noise Spectral Density for Various Temperatures, T_Z = 11kΩ, LPF = 100MHz

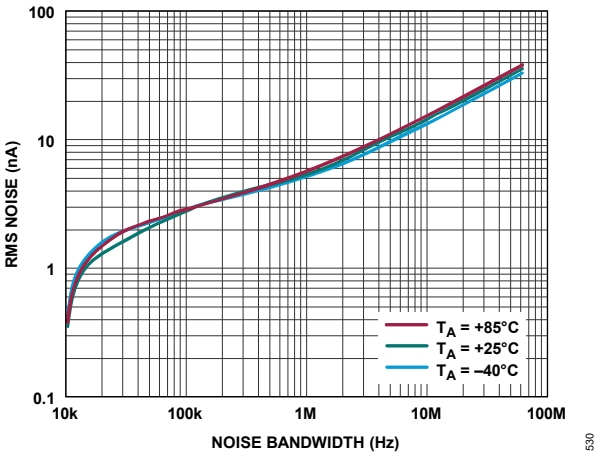

Figure 30. RMS Noise vs. Noise Bandwidth for Various Temperatures, T_Z = 11kΩ, LPF = 100MHz

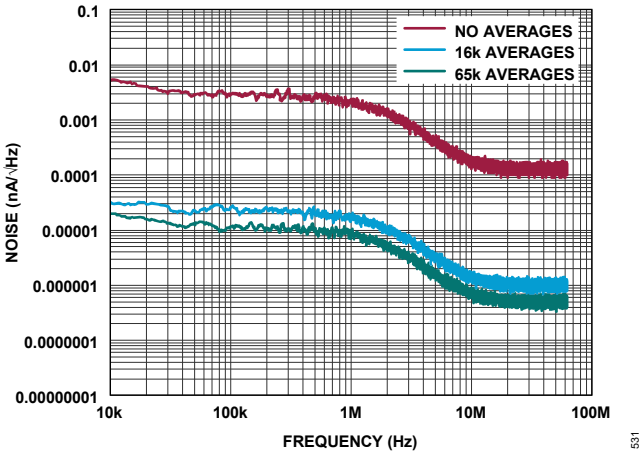

Figure 31. Noise Spectral Density, T_Z = 133kΩ, LPF = 1MHz

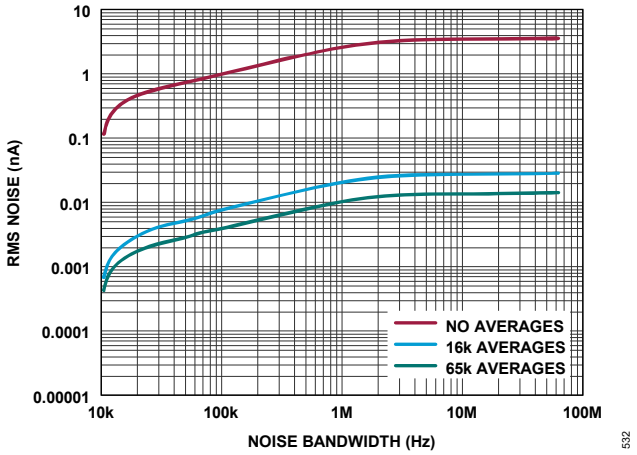

Figure 32. RMS Noise vs. Noise Bandwidth, T_Z = 133kΩ, LPF = 1MHz

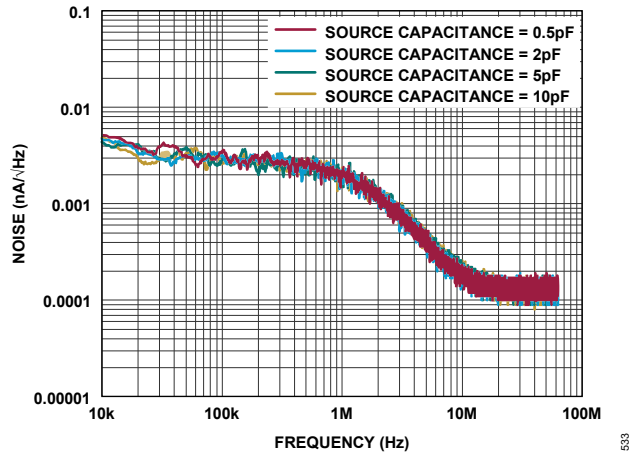

Figure 33. Noise Spectral Density for Various Source Capacitances, T_Z = 133kΩ, LPF = 1MHz

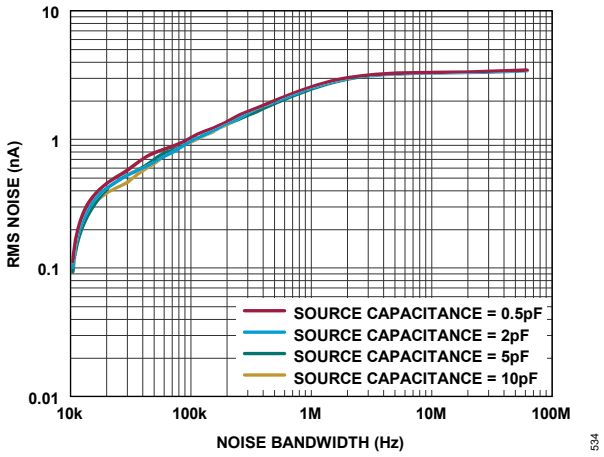

Figure 34. RMS Noise vs. Noise Bandwidth for Various Source Capacitances, T_Z = 133kΩ, LPF = 1MHz

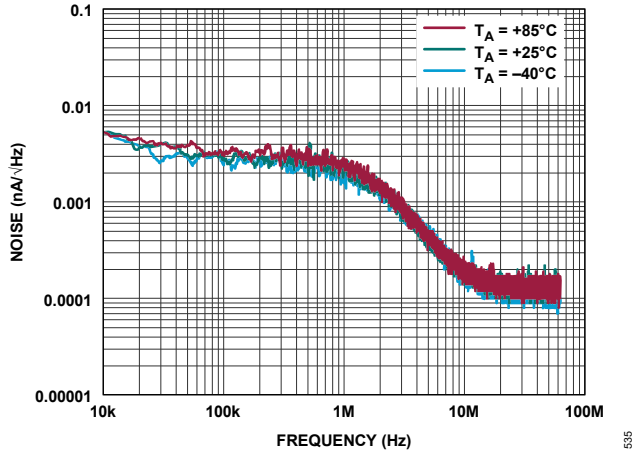

Figure 35. Noise Spectral Density for Various Temperatures, T_Z = 133kΩ, LPF = 1MHz

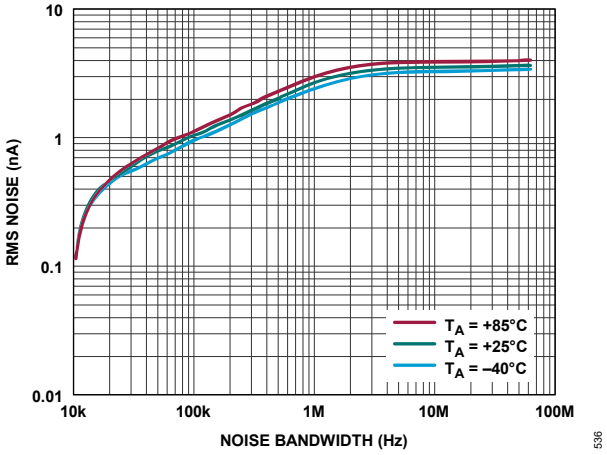

Figure 36. RMS Noise vs. Noise Bandwidth for Various Temperatures, T_Z = 133kΩ, LPF = 1MHz

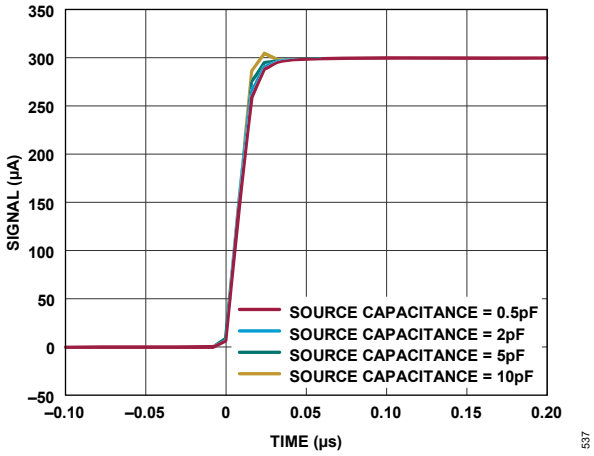

Figure 37. Pulse Response Rising Edge for Various Source Capacitances, T_Z = 4.54kΩ, LPF = 100MHz

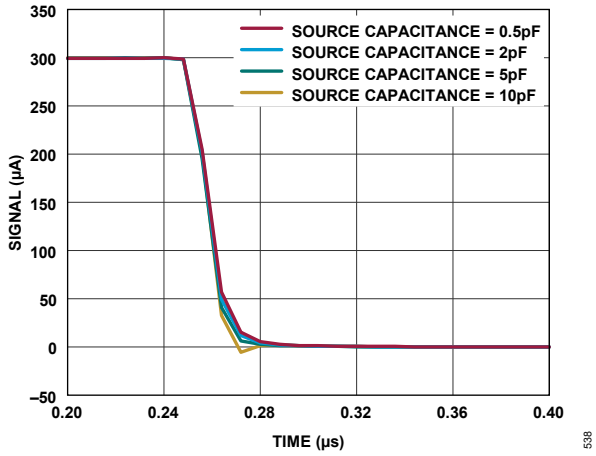

Figure 38. Pulse Response Falling Edge for Various Source Capacitances, T_Z = 4.54kΩ, LPF = 100MHz

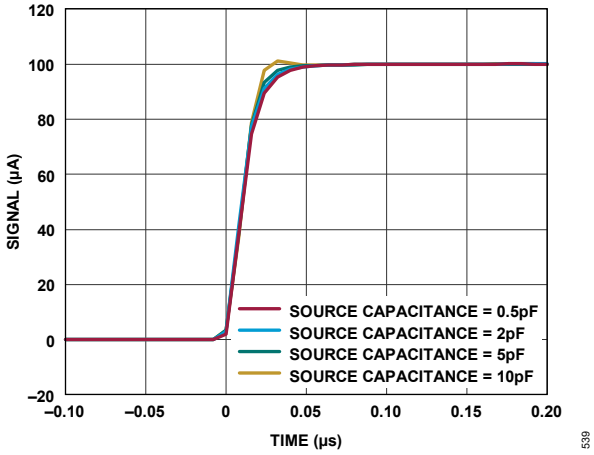

Figure 39. Pulse Response Rising Edge for Various Source Capacitances, T_Z = 11kΩ, LPF = 100MHz

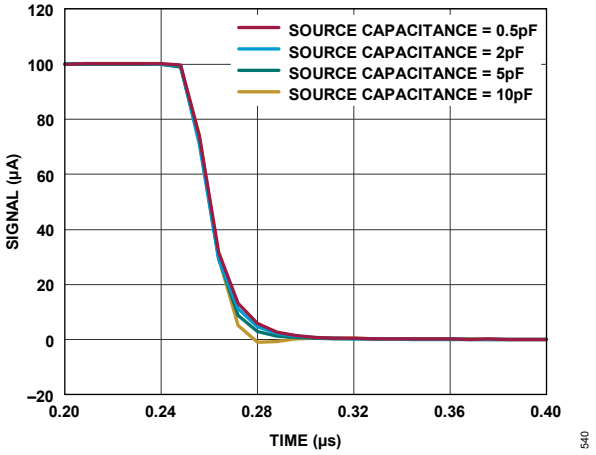

Figure 40. Pulse Response Falling Edge for Various Source Capacitances, T_Z = 11kΩ, LPF = 100MHz

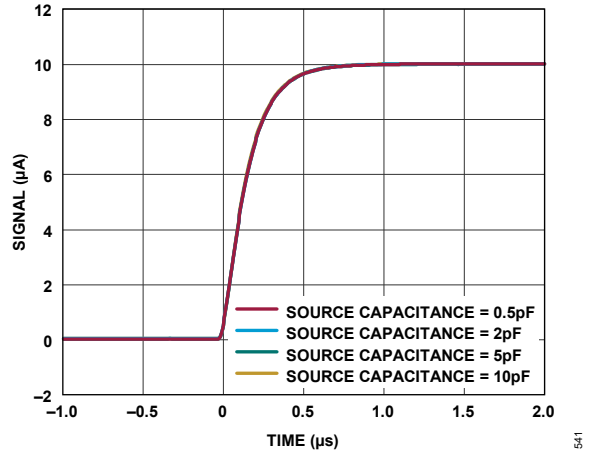

Figure 41. Pulse Response Rising Edge for Various Source Capacitances, T_Z = 133kΩ, LPF = 1MHz

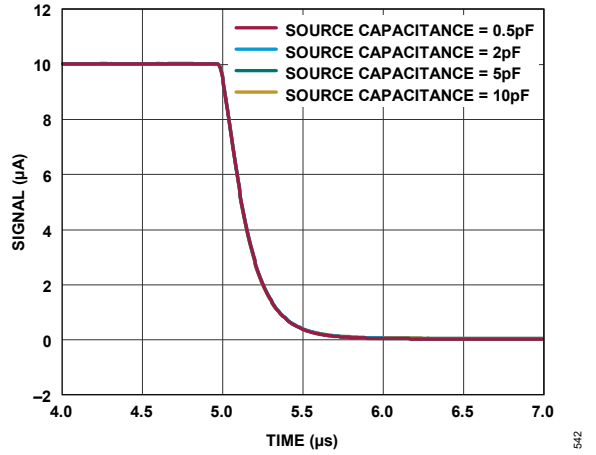

Figure 42. Pulse Response Falling Edge for Various Source Capacitances, T_Z = 133kΩ, LPF = 1MHz

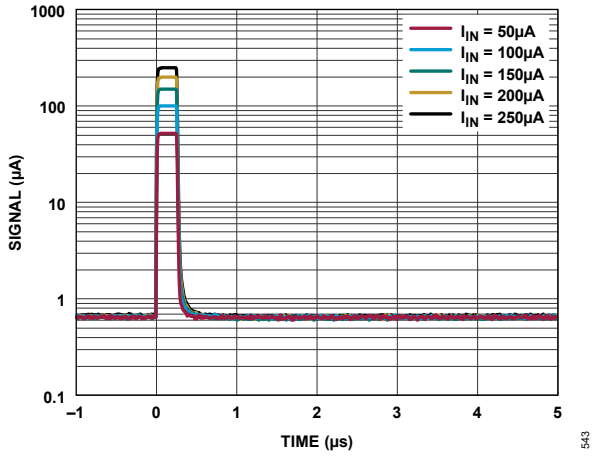

Figure 43. Settling Time for Various Input Currents, T_Z = 4.54kΩ, 250ns Pulse Width, LPF = 100MHz

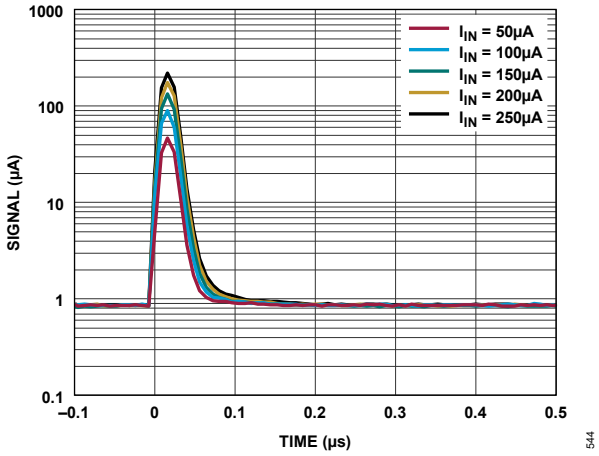

Figure 44. Settling Time for Various Input Currents, T_Z = 4.54kΩ, 20ns Pulse Width, LPF = 100MHz

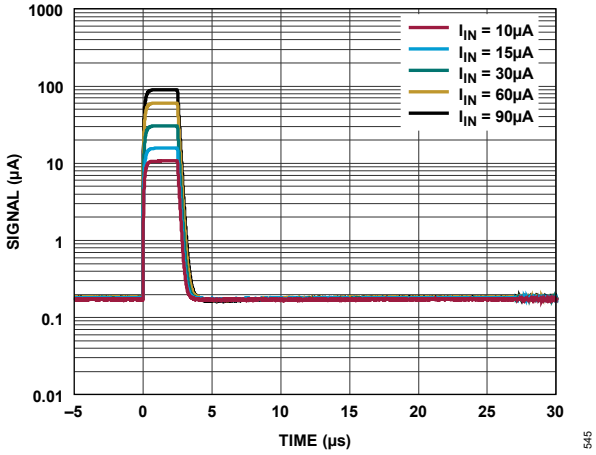

Figure 45. Settling Time for Various Input Currents, T_Z = 11kΩ, 2.5µs Pulse Width, LPF = 1MHz

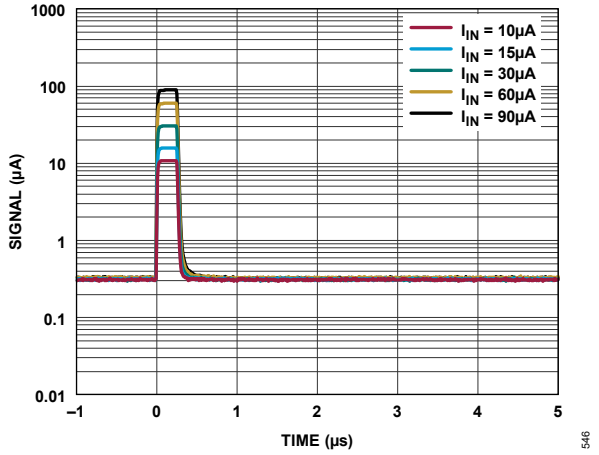

Figure 46. Settling Time for Various Input Currents, T_Z = 11kΩ, 250ns Pulse Width, LPF = 100MHz

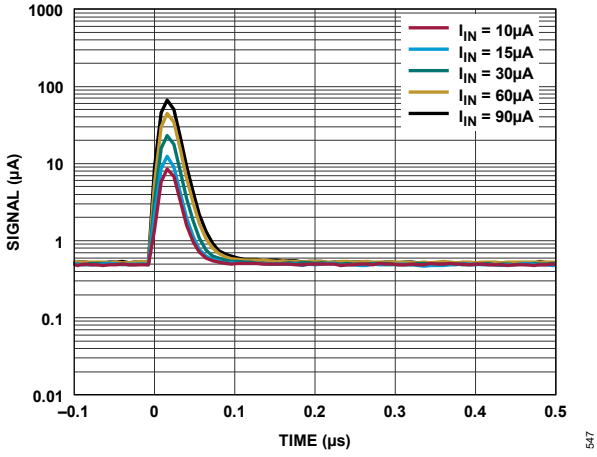

Figure 47. Settling Time for Various Input Currents, T_Z = 11kΩ, 20ns Pulse Width, LPF = 100MHz

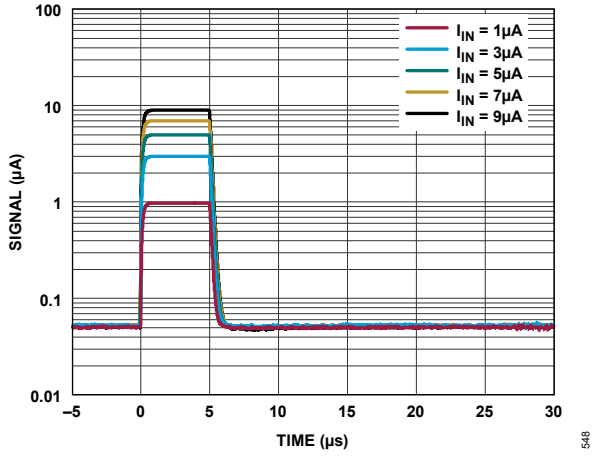

Figure 48. Settling Time for Various Input Currents, T_Z = 133kΩ, 5µs Pulse Width, LPF = 1MHz

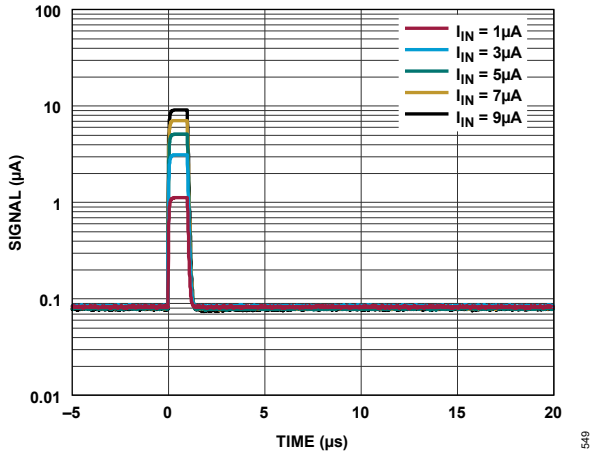

Figure 49. Settling Time for Various Input Currents, T_Z = 133kΩ, 1µs Pulse Width, LPF = 100MHz

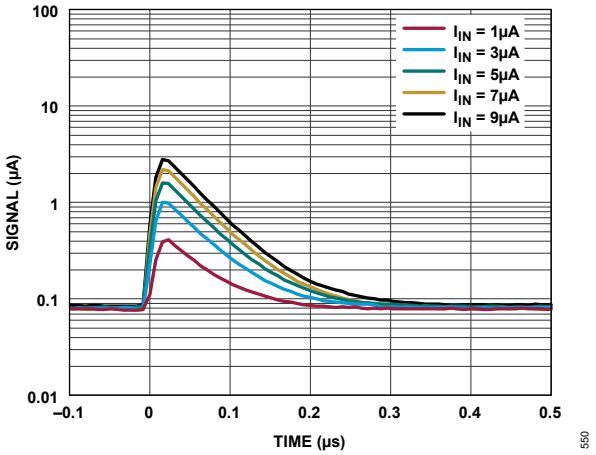

Figure 50. Settling Time for Various Input Currents, T_Z = 133kΩ, 20ns Pulse Width, LPF = 100MHz

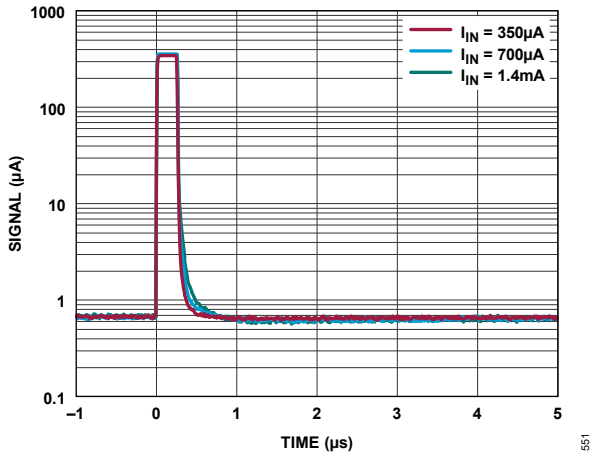

Figure 51. Overload Recovery, T_Z = 4.54kΩ, 250ns Pulse Width, LPF = 100MHz

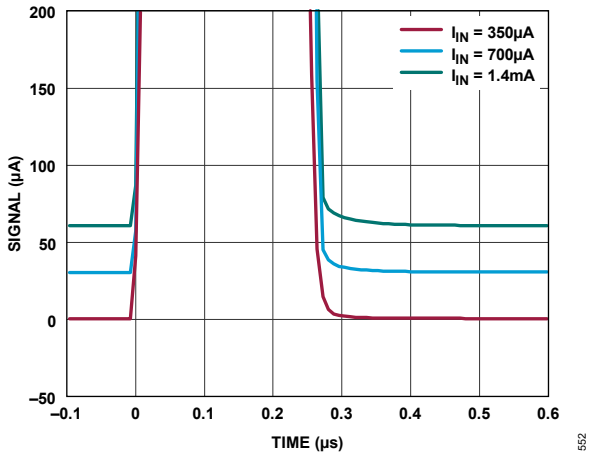

Figure 52. Overload Recovery (Zoomed In), T_Z = 4.54kΩ, 250ns Pulse Width, LPF = 100MHz (Traces Offset Vertically for Readability)

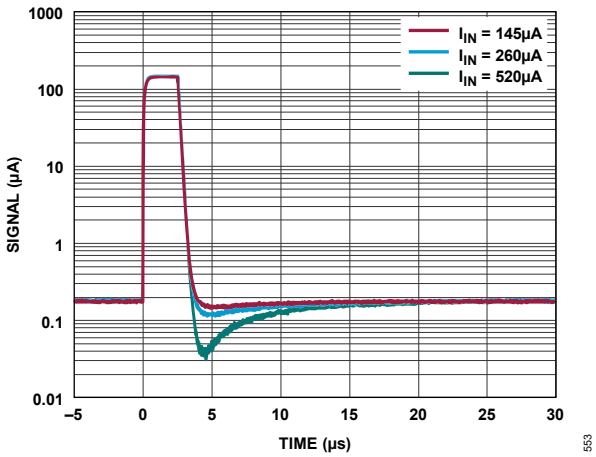

Figure 53. Overload Recovery, T_Z = 11kΩ, 2.5µs Pulse Width, LPF = 1MHz

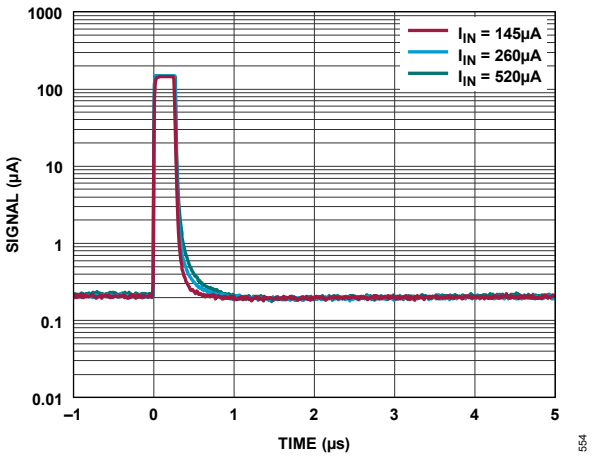

Figure 54. Overload Recovery, T_Z = 11kΩ, 250ns Pulse Width, LPF = 100MHz

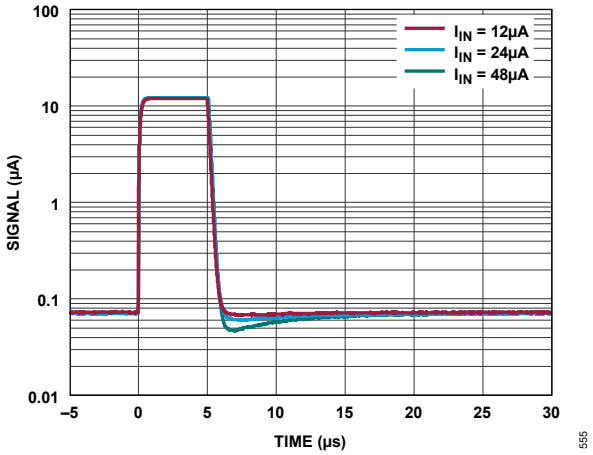

Figure 55. Overload Recovery, T_Z = 133kΩ, 5µs Pulse Width, LPF = 1MHz

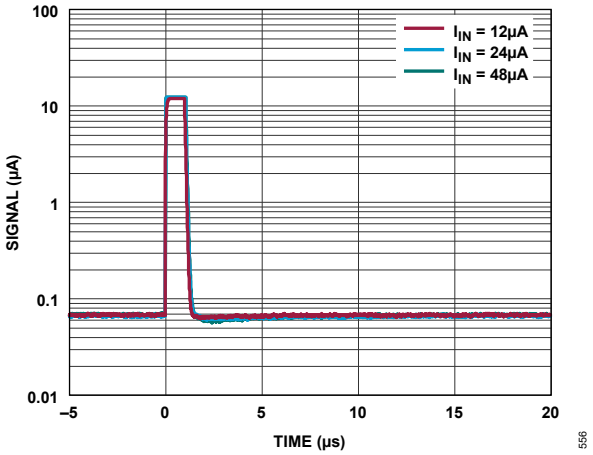

Figure 56. Overload Recovery, T_Z = 133kΩ, 1µs Pulse Width, LPF = 100MHz

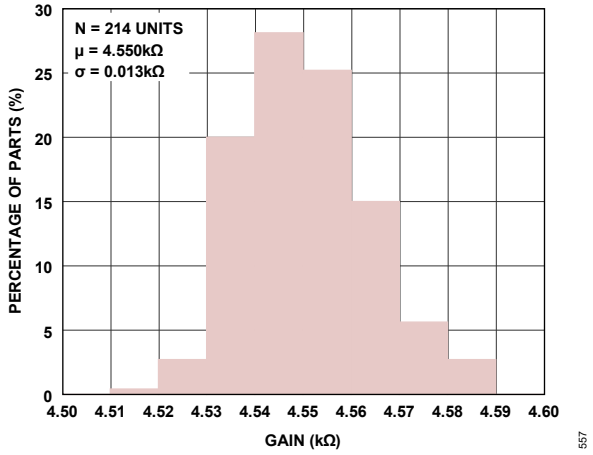

Figure 57. TIA Gain Distribution, T_Z = 4.54kΩ

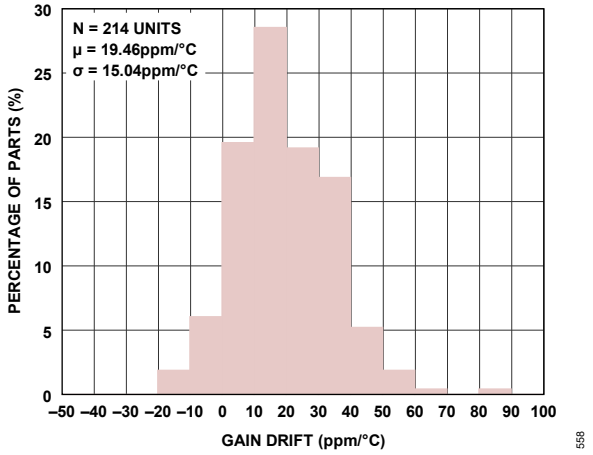

Figure 58. TIA Gain Drift Distribution, T_Z = 4.54kΩ

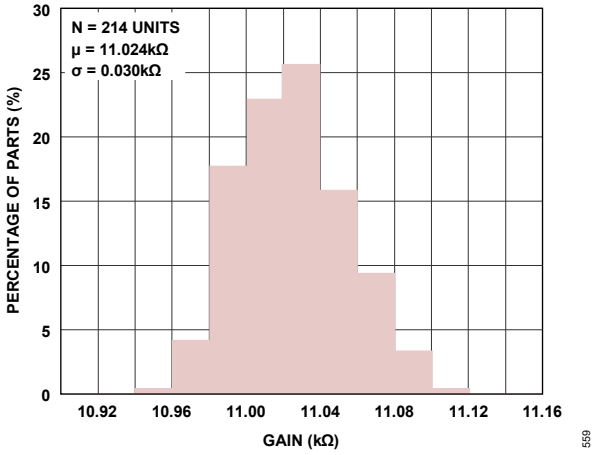

Figure 59. TIA Gain Distribution, T_Z = 11kΩ

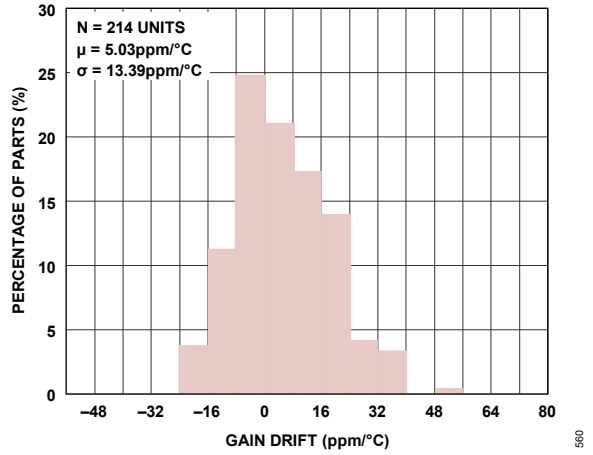

Figure 60. TIA Gain Drift Distribution, T_Z = 11kΩ

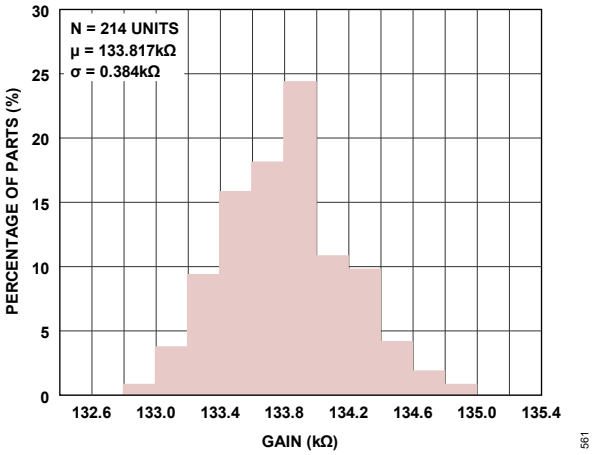

Figure 61. TIA Gain Distribution, T_Z = 133kΩ

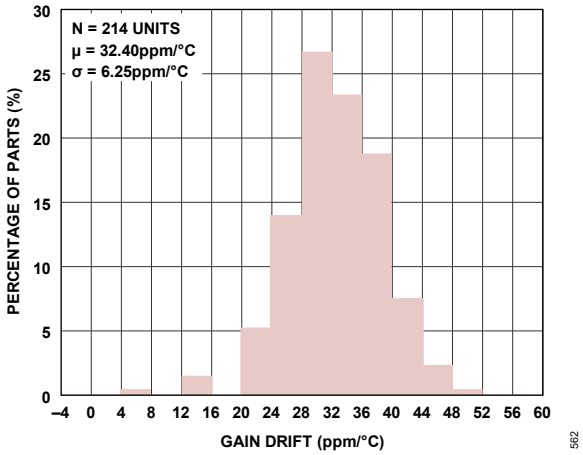

Figure 62. TIA Gain Drift Distribution, T_Z = 133kΩ

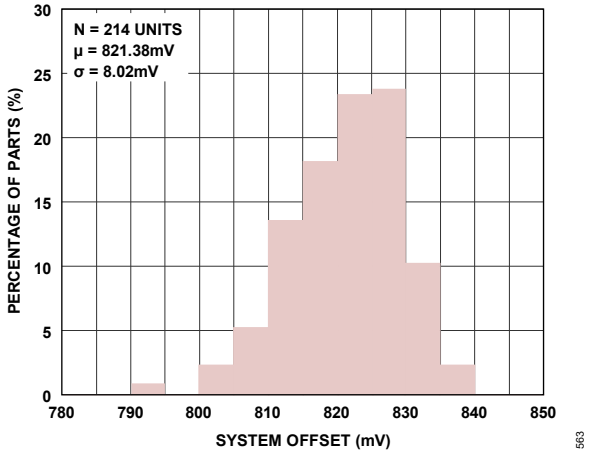

Figure 63. System Offset Distribution, T_Z = 4.54kΩ

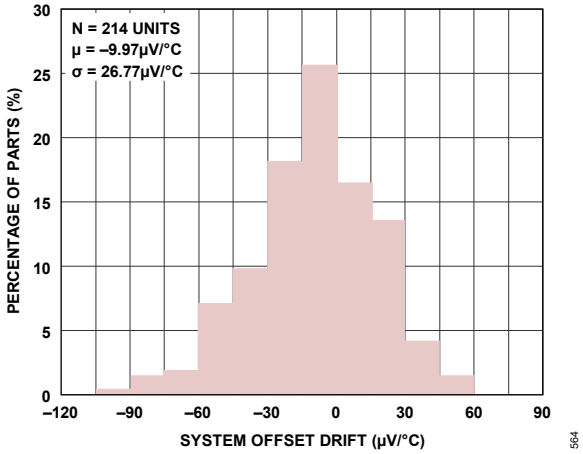

Figure 64. System Offset Drift Distribution, T_Z = 4.54kΩ

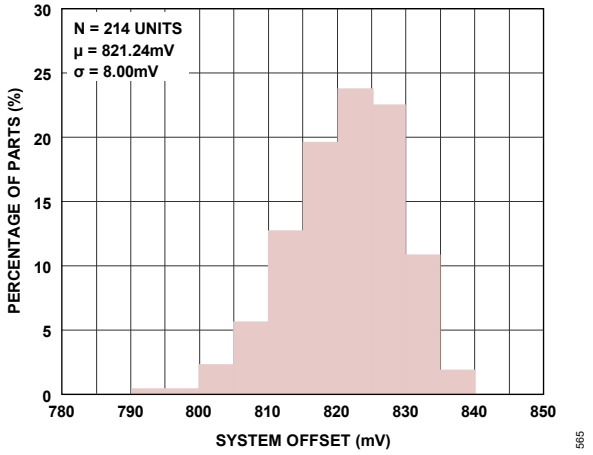

Figure 65. System Offset Distribution, T_Z = 11kΩ

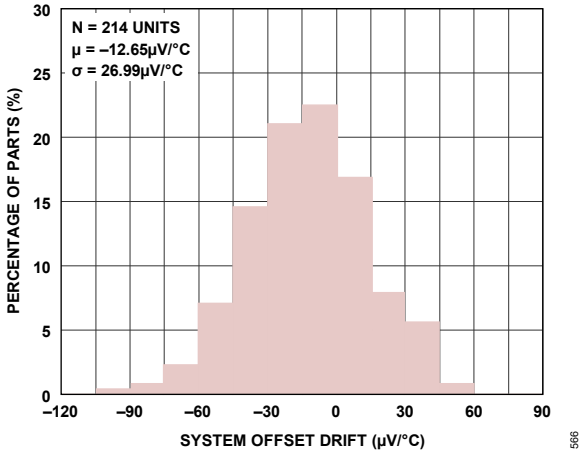

Figure 66. System Offset Drift Distribution, T_Z = 11kΩ

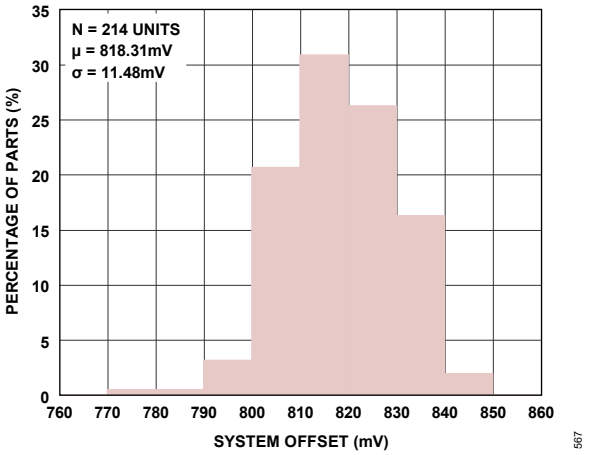

Figure 67. System Offset Distribution, T_Z = 133kΩ

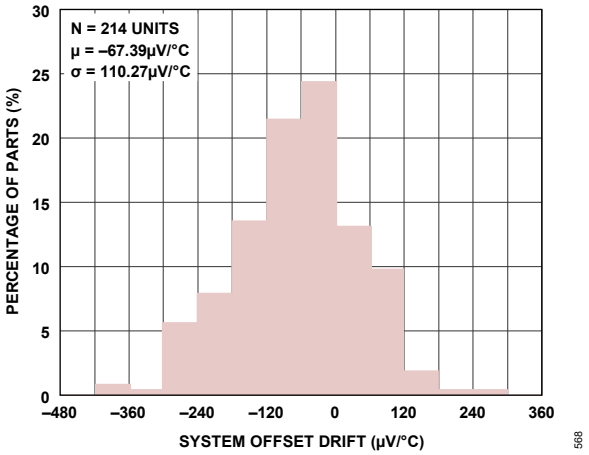

Figure 68. System Offset Drift Distribution, T_Z = 133kΩ

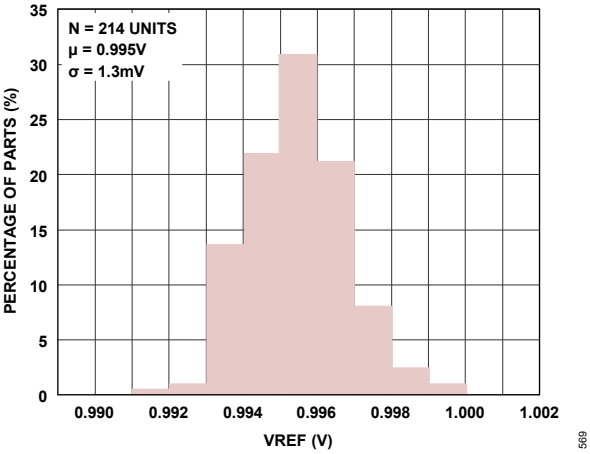

Figure 69. ADC Internal Reference Voltage (VREF) Distribution

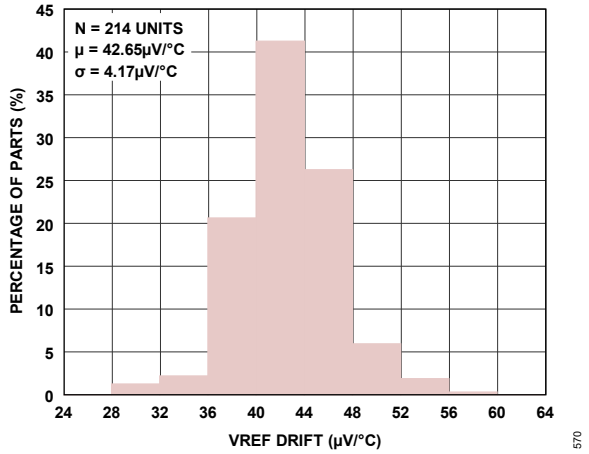

Figure 70. ADC Internal VREF Drift Distribution

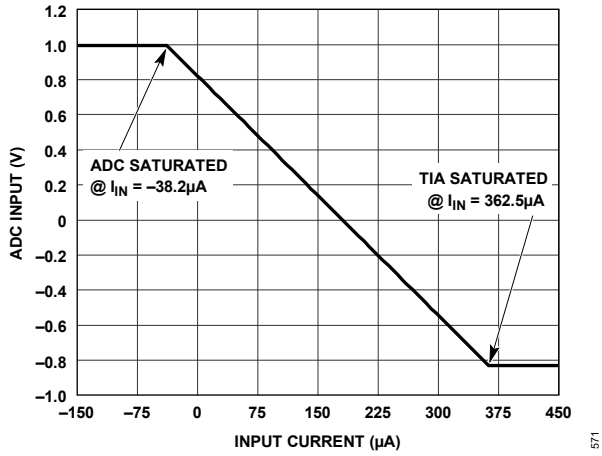

Figure 71. ADC Input Voltage vs. Input Current, T_Z = 4.54kΩ

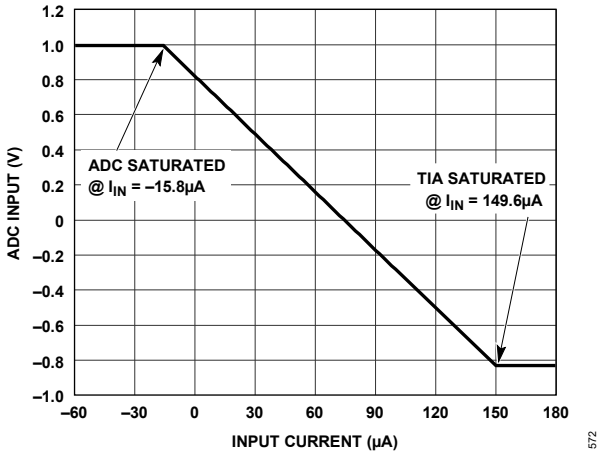

Figure 72. ADC Input Voltage vs. Input Current, T_Z = 11kΩ

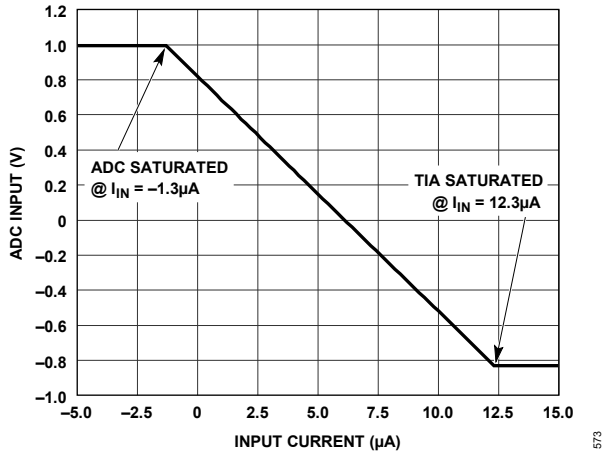

Figure 73. ADC Input Voltage vs. Input Current, T_Z = 133kΩ

EQUIVALENT CIRCUITS

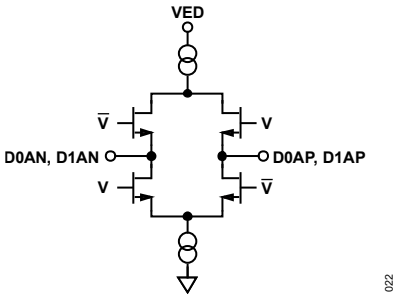

Figure 74. Equivalent Digital Output Circuit

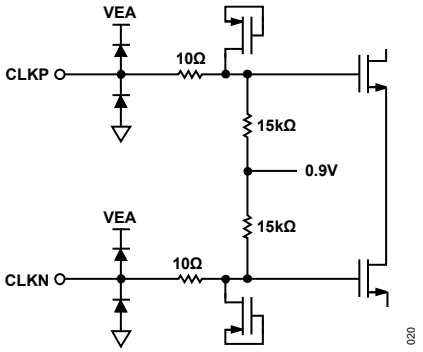

Figure 75. Equivalent Clock Input Circuit

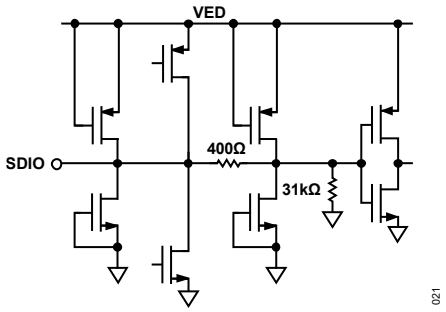

Figure 76. Equivalent SDIO Input Circuit

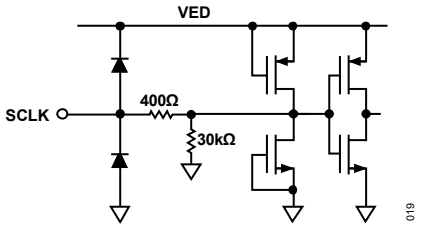

Figure 77. Equivalent SCLK Input Circuit

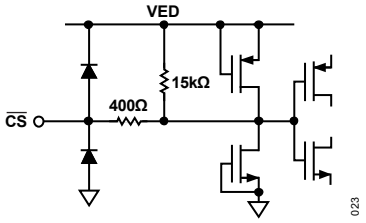

Figure 78. Equivalent $\overline{CS}$ Input Circuit

THEORY OF OPERATION

The ADA4356 integrates a field effect transistor (FET) input TIA with three switchable gains (4.54kΩ, 11kΩ, and 133kΩ). The gain switches are designed to minimize error sources that result in slow settling time and slow overload recovery. The internal overload current protection allows the input current to exceed the full-scale current while still providing fast overload recovery. Additionally, the overload current protection enables analog input current levels up to 40mA to be sustained with no damage to the TIA. The positive node of the TIA is biased to 1.65V, as shown in *Figure 2*.

Figure 79 shows the overall system transfer function. Because the photodiode provides unipolar current (sink or source), the overall transfer function has 0.825V offset to maximize the input range of the ADC. When the input current is 0µA, the ADC differential input is 0.825V. As the input current increases, the TIA output decreases toward GND. When the input current reaches $1.65V/T_Z$, the TIA output is at GND, limiting the ADC differential input voltage to −0.825V. The positive full-scale input current is $1.65V/T_Z$, and there is room to measure negative input current down to $-0.175V/T_Z$.

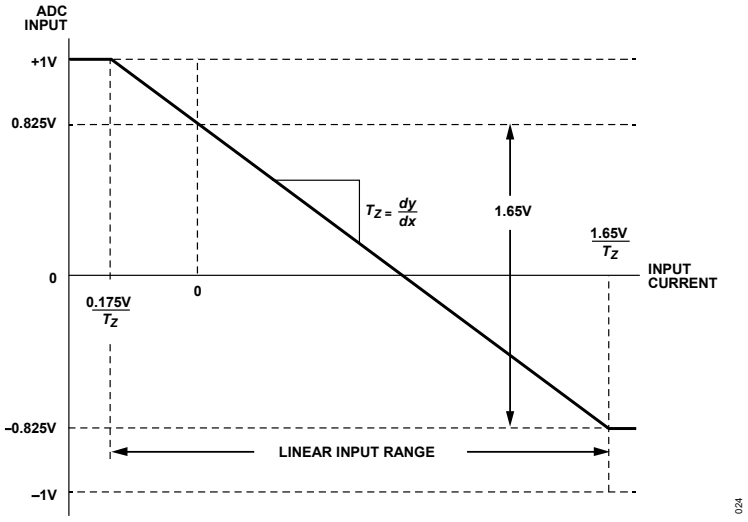

Figure 79. Overall Transfer Function

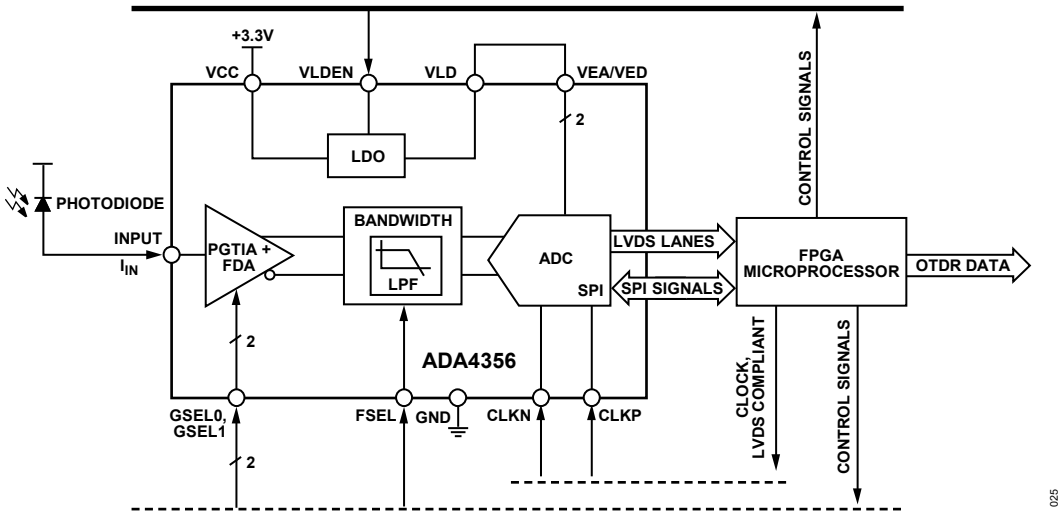

Figure 80. Typical Application Block Diagram with a Single VCC Supply, FPGA Control, and Data Process

APPLICATIONS INFORMATION

Power and Power Control

The 12mm × 6mm CSP_BGA has multiple balls designated to support the ADA4356 power requirements, with 12 balls assigned to VCC, and one ball each to VEA, VED, and VLD. The ADA4356 has internal 0.1µF bypass capacitors on all supplies, so additional external supply decoupling is not required.

VCC is a 3.3V supply that powers the ADA4356's analog core and internal LDO. Connect all VCC balls (A3, C3 to C5, D3 to D5, F3 to F6, and F8) to a clean 3.3V supply.

VLD (F12) is the internal 1.8V LDO's output. This LDO is provided as one option to power the internal ADC's analog and digital supplies. To enable this LDO, pull VLDEN (F7) high.

VEA (E10) and VED (E12) are the analog and digital supply balls, respectively, for the internal ADC. These balls should be connected to a clean 1.8V supply. To power the ADC via the internal 1.8V LDO, connect VLD to both VEA and VED, and enable VLDEN (see *Figure 3*).

To use an external 1.8V supply to power the internal ADC instead of the provided LDO, disable the internal LDO by pulling VLDEN low, and connect VEA and VED to an external 1.8V supply (see *Figure 4*).

The ADA4356 has 32 balls assigned as GND. There is no connection between the GND balls inside the package. Therefore, connect all GND balls to a low-impedance GND plane on the PCB.

Transimpedance Amplifier Input

The performance of the TIA inside the ADA4356 is affected by the total capacitance C_S present at the INPUT ball. Higher C_S reduces TIA bandwidth and increases noise.

C_S is the sum of the input photodiode capacitance (usually the largest), the TIA's own input capacitance (2.0pF), stray capacitance from the board layout, and any other capacitances present at INPUT (E1).

For more details on how to reduce the board layout capacitance at the TIA input, see the *PCB Design Tips* section.

Extending Input Current Range

The linear current input range of the ADA4356 is limited by saturation of the TIA's output. Given the input bias at 1.65V and supply of 3.3V, assuming current is being sunk into the photodiode, the output of the TIA can swing approximately 1.5V above the bias voltage before reaching nonlinearity and saturating.

For the lowest gain of T_Z = 4.54kΩ, the output saturates at an input current of 1.5V/4.54kΩ, or about 330µA. Similarly, T_Z = 11kΩ saturates 136µA, and T_Z = 133kΩ saturates at 11.3µA.

Table 9 lists recommended maximum input currents for linear TIA operation, along with the corresponding input-referred current noise i_N with no filtering or averaging and a total input capacitance of 5pF.

Table 9. Recommended Maximum Input Current for Linear TIA Operation

GAIN RANGE (kΩ)	MAXIMUM LINEAR INPUT CURRENT (µA)	INPUT REFERRED CURRENT NOISE, Cs = 5pF, FSEL = 0
4.54	300	68nA rms
11	100	33nA rms
133	10	8.4nA rms

Current Divider Circuit

For the applications with a maximum source current that exceeds the above ranges, additional external circuitry is required to linearly divide the TIA input current down to fit within the ADA4356's linear input range.

This current division is not possible with a simple two-resistor current divider to ground, because the TIA input of the ADA4356 must stay biased at a DC voltage of 1.65V. Thus, a circuit is required that can linearly divide down the input current while also maintaining the TIA input DC bias voltage. Ideally, this circuit can also be switched into/out of the main TIA input path in response to dynamic source current levels.

One such circuit is shown in *Figure 81*. It consists of:

1. C_1, capacitor to shunt fast-moving currents to ground.
2. A_1, unity-gain voltage buffer to maintain 1.65V at V1, to match the bias voltage at INPUT.
3. S_1, switch to connect/disconnect this circuit from the main TIA input path,
4. R_1 and R_2, resistor divider network between the photodiode output and the TIA input of the ADA4356.

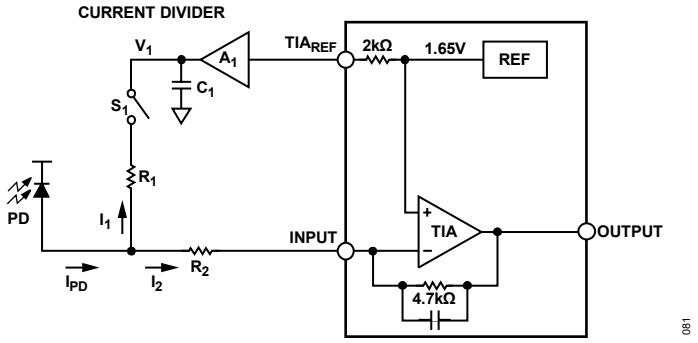

Figure 81. External High-Speed Current Divider Circuit

When switch S_1 is open, all the photodiode's source current (I_{PD}) enters the TIA at ball INPUT (E1).

When switch S_1 is closed, I_{PD} splits into two portions, I_1 and I_2, according to the ratio of R_1 and R_2.

Assuming an ideal switch S_1, ideal voltage buffer A_1, and that TIA_{REF} and INPUT are at the same potential (1.65V), the portion of I_{PD} current going into the INPUT of the ADA4356 (I_2) is given by the following equation:

$$I_2 = \frac{R_1}{R_1 + R_2} \times I_{PD}$$

The other portion of the divided-down input current (I_1) is shunted away via the divider path shown in *Figure 81.*

AC Ground V_1

In high-speed applications, the input photodiode current pulse I_{PD} may be too fast for any active device to absorb current I_1. To shunt large currents quickly, a large capacitor C1 is connected from node V_1 to ground to create an AC ground with a DC bias of 1.65V.

After C_1 absorbs the I_1 portion of I_{PD}, the DC bias at V_1 is perturbed, as shown in the LTspice simulation curves in *Figure 82*. Buffer A_1 corrects the perturbation by rapidly bringing node V_1 back to 1.65V to keep INPUT and TIA_{REF} at the same DC voltage.

The more zoomed-out simulated transient curves in *Figure 83* show multiple input current pulses on I_{PD}, and the resulting settling behavior of the AC ground at node V_1 as A_1 brings it back to 1.65V exactly.

If buffer A_1 is not present, a charge continues to accumulate on C_1 with each successive input current pulse, pushing the voltage at node V_1 up to the supply. On its own, the C_1 discharges far too slowly for the AC ground at V_1 to return to 1.65V in time for the next pulse on I_{PD}, which violates the underlying assumption of the current divider that INPUT and TIA_{REF} are always at the same DC bias.

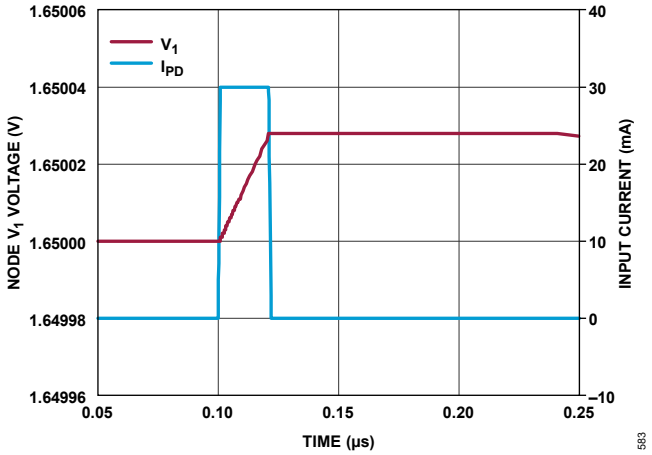

Figure 82. Simulated Input Current Pulse I_{PD} and Resulting Voltage Perturbation at Node V_1

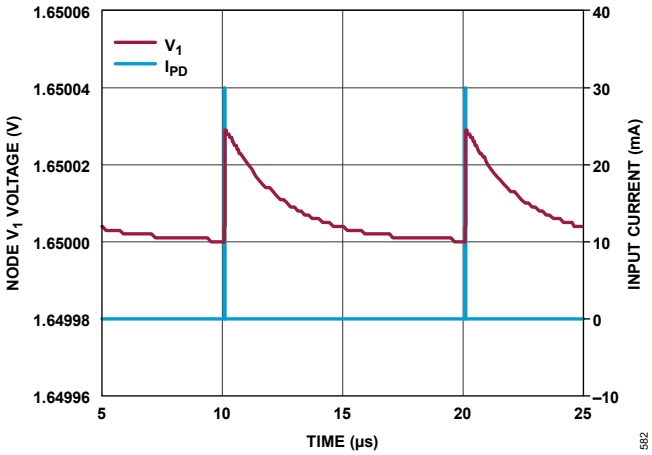

Figure 83. Simulated Input Current Pulses I_{PD} and AC Ground Settling Response at V_1

30mA Current Divider Example

Figure 84 shows an example circuit that can divide down a maximum DC input current of 30mA from I_{PD} to fit within the 300µA linear input current range of the ADA4356.

Capacitor C_1 is 22.11µF, from a combination of 22µF, 100nF, and 10nF capacitors in parallel. Resistor R_1 is the on-resistance of the chosen switch S_1, *ADG772*, which is roughly 5Ω at room temperature and with a supply voltage of 3.3V. Resistor R_2 is a discrete 604Ω. The resulting current division is:

$$I_2 = \frac{R_{ON}}{R_{ON} + R_2} \times I_{PD} = \frac{5\Omega}{5\Omega + 604\Omega} \times I_{PD} = 0.00821 \times I_{PD} \approx \frac{I_{PD}}{120}$$

Thus, I_2 = 30mA/120 = 250µA, which fits within the linear input range of 320µA.

The rest of the current, which is diverted into the AC ground at V_1, is I_1 = 30mA – I_2 = 30mA – 166µA = 29.833mA.

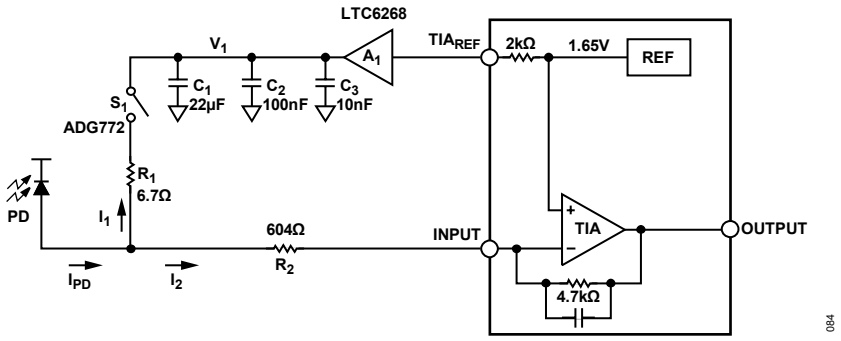

Figure 84. Example Implementation of External High-Speed Current Divider Circuit

The following subsections explain factors to consider when selecting current divider components.

TIA_{REF} Buffering Requirement

Ball TIA_{REF} (F1) is connected to the ADA4356's internal 1.65V reference via a series 2kΩ resistor for protection. Any current drawn from TIA_{REF} causes an error in the DC bias voltage, due to an IR drop across the 2kΩ resistor. Instead of drawing current directly from TIA_{REF}, it is recommended to buffer TIA_{REF}'s output with a voltage buffer A_1. This buffer can rapidly charge C_1 with high currents without introducing errors in the DC bias voltage.

Buffer Selection

Buffer A_1 must have high gain bandwidth, fast slew rate, low output impedance over the input signal frequency range, and good stability while driving large capacitors in the range of 10's of µFs. The *LTC6268*/*LTC6269* is an excellent choice for this buffer.

Resistor Selection

The value of resistor R_2 must not be too high, since current I_2 flowing through R_2 causes an IR drop that modulates the bias voltage of the photodiode. With a maximum I_2 of 300µA, selecting values of R_2 below 1kΩ keep this bias error below 300mV.

Capacitor Selection

It is recommended to place multiple smaller capacitors in parallel to create C_1, to cover a wider frequency range while handling relatively high currents.

A real capacitor's bandwidth is limited to its self-resonant frequency. All real capacitors have unavoidable parasitic package inductance. When combined with the normal capacitor value, this results in an LC tank. Above the self-resonant frequency of the LC tank, the nominal capacitor acts as an inductor.

Larger capacitor packages can handle higher currents, but have higher parasitic inductance, which lowers the self-resonant frequency of the LC tank and thus the effective frequency of the capacitor.

The self-resonant LC tank may cause instability problems at the output of buffer A_1. To reduce the risk of oscillations, it is recommended to place a small series resistor (0.1Ω) between the capacitor and ground to reduce the quality factor (Q) of the self-resonant tank.

Recommended values for a combination C_1 are 22µF, 100nF, and 10nF in parallel.

Switch Selection

Selecting a switch S_1 requires considering how switch nonidealities affect the current divider circuit.

Switch On-Resistance

Real switches have nonzero on-resistance (R_{ON}), which appears in series with R_1. Thus, switch on-resistance affects the divider ratio of R_1 and R_2. The resulting current division with nonzero switch R_{ON} is given by:

$$I_2 = \frac{(R_1 + R_{ON})}{(R_1 + R_{ON}) + R_2} \times I_{PD}$$

In the special case where $R_1 = 0\Omega$, this equation reduces to:

$$I_2 = \frac{R_{ON}}{R_{ON} + R_2} \times I_{PD}$$

The switch nonideality R_{ON} thus effectively plays the role of the resistor R_1 in the original divider in *Figure 81*.

Note that R_{ON} of a switch has a different temperature coefficient than that of a discrete resistor, which affects current division accuracy over temperature. Calibration over temperature can help address such accuracy issues.

Switch Current Limits

The maximum input current that the current divider can accept is limited by switch S_1's absolute maximum current limits. The absolute maximum current limits for current pulses are often much higher than the limit for continuous currents.

Aside from absolute maxima for switch currents, another issue with large input currents I_1 is the resulting larger transient IR drop due to the switch on-resistance ($R_{ON} \times I_1$). Since the TIA input is pinned at 1.65V, this IR drop pushes the output of the switch itself higher. An IR drop that is too big may force the switch's output too close to its own supply voltage, which can cause nonlinearity errors.

Additionally, self-heating from high currents through S_1 also causes temperature coefficient shifts in R_{ON}.

Switch Capacitance

While a larger switch has the benefits of higher current capacity and a smaller switch on-resistance R_{ON}, the trade-off is an increased switch parasitic capacitance C_{SW}. This capacitance also appears at the input of the TIA, which can affect TIA performance as explained in the *Transimpedance Amplifier Input* section.

Although resistors R_1 and R_2 may appear to isolate the INPUT node from the total input capacitance C_S and switch capacitance according to typical nodal analysis rules, this assumption does not apply here, because the TIA input is a current, not a voltage. A resistor cannot increase or decrease current, while any capacitance on the path between input source (that is, APD) and ball INPUT (E1) can divert desired input current.

Capacitor C_1 is the sole exception, because it is so large that its associated poles and zeros are multiple decades below the frequencies of interest for this application. It appears solely as an AC ground and does not affect TIA performance. Meanwhile, switch capacitance C_{SW} is typically in the pF range, and thus its associated poles and zeros are close enough to the TIA's own poles and zeros to affect bandwidth and noise.

A recommended switch that balances low on-resistance and low parasitic junction capacitance is *ADG772*.

OTDR Application

The small form factor and integrated nature of the ADA4356 micromodule make it ideally suited for space-sensitive applications, such as embedded optical time domain reflectometry (OTDR) for fiber optic cable installations in datacenters or telecommunications networks.

The 133kΩ transimpedance gain and 1MHz LPF cutoff frequency enables the ADA4356 to reach the high sensitivity and low noise levels needed for wide dynamic range long-haul OTDR applications. Conversely, the 4.54kΩ gain and

100MHz LPF cutoff frequency provides the higher bandwidth needed for narrow pulse widths that are required for closely spaced event detection necessary for datacenter applications. Additional noise floor reduction is possible via real-time averaging.

Clocks

For optimum performance, drive the ADC sample clock inputs, CLKP (F11) and CLKN (E11), with a differential signal. The clock signal is typically AC-coupled into the CLKP and CLKN balls via a transformer or capacitors. These balls are biased internally (see *Figure 75*) and require no external bias.

Clock Input Options

The ADA4356 has a flexible clock input structure. The clock input can be a CMOS, LVDS, low-voltage positive emitter coupled logic (LVPECL), or sine wave signal. Regardless of the type of signal used, clock source jitter is an important consideration, as described in the *Jitter Considerations* section.

Figure 85 and *Figure 86* show two preferred methods for clocking the ADA4356 (at clock rates up to 1GHz prior to the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

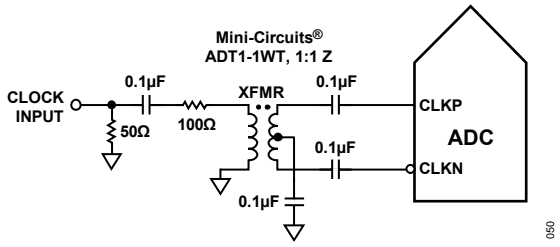

Figure 85. Transformer-Coupled Differential Clock (up to 200MHz)

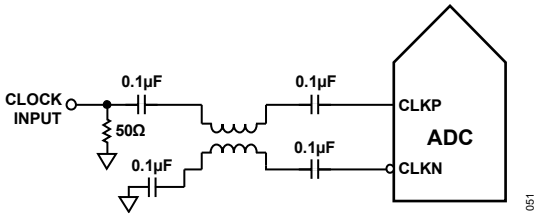

Figure 86. Balun-Coupled Differential Clock (up to 1GHz)

The RF balun configuration is recommended for clock frequencies between 125MHz and 1GHz, and the RF transformer configuration is recommended for clock frequencies from 10MHz to 200MHz.

If a low jitter clock source is not available, another option is to AC-couple(d) a differential PECL signal to the sample clock input balls, as shown in *Figure 87*. For a list of PECL drivers with excellent jitter performance that are suitable for this application, see *Table 10*.

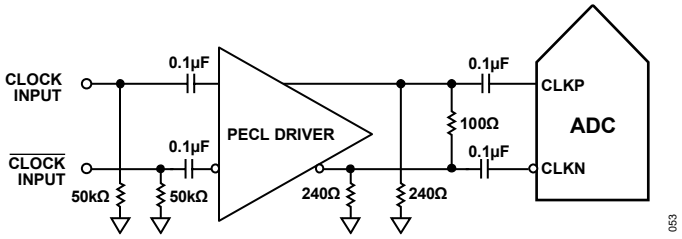

Figure 87. Differential PECL Sample Clock (up to 1GHz)

Table 10.Recommended PECL/LVDS Drivers

PART NUMBER (s)	FREQUENCIES
AD9510/*AD9511*/*AD9512* *(AD9512-EP grade available)*	1.2GHz LVPECL, 800MHz LVDS
AD9513	800MHz LVDS
AD9514/*AD9515*	1.6GHz LVPECL, 800MHz LVDS
AD9516-0/*AD9516-1*/*AD9516-2*/*AD9516-3*/*AD9516-4*/*AD9516-5*	1.6GHz LVPECL, 800MHz LVDS
AD9517-0/*AD9517-1*/*AD9517-2*/*AD9517-3*/*AD9517-4*	1.6GHz LVPECL, 800MHz LVDS

A third option is to AC-couple(d) a differential LVDS signal to the sample clock input balls, as shown in *Figure 88*. For the recommended LVDS drivers that offer excellent jitter performance, see *Table 10*.

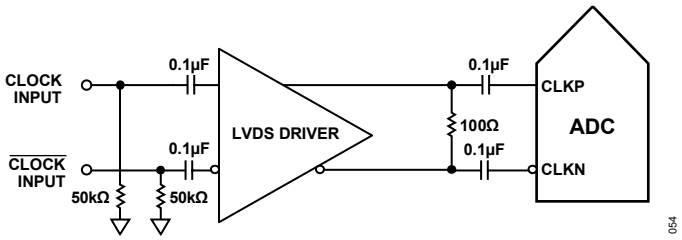

Figure 88. Differential LVDS Sample Clock (up to 1GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8V CMOS signal. In such applications, drive the CLKP ball (F11) directly from a CMOS gate, and bypass the CLKN ball (E11) to ground with a 0.1µF capacitor (see *Figure 89*).

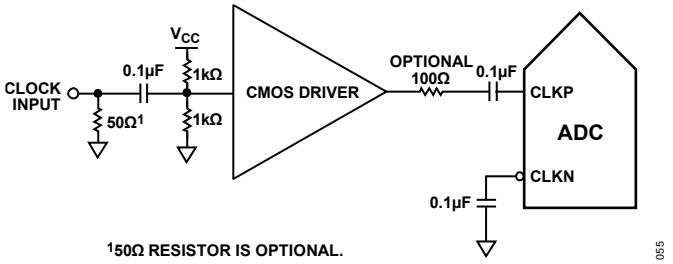

Figure 89. Single-Ended 1.8V CMOS Input Clock (up to 200MHz)

Input Clock Divider

The ADA4356 contains an input clock divider that can divide the input clock by integer values from 1 to 8. The power-on default clock divider ratio is always 1. If a different clock divide ratio is required, change SPI Register 0x0B. To achieve a given sample rate, multiply the frequency of the externally applied clock by the divide value. The increased rate of the external clock normally results in lower clock jitter, which is beneficial for intermediate frequency (IF) undersampling applications.

Clock Duty Cycle

The ADC uses both clock edges to generate a variety of internal timing signals and, as a result, can be sensitive to the clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The ADA4356 offers a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. The DCS allows the user to provide a wide range of clock input duty cycles without affecting the performance of the ADA4356. Noise and distortion performance are nearly unchanged for a

wide range of duty cycles with the DCS on. To disable the DCS function, clear the least significant bit of SPI REGISTER 0x09h to zero.

Jitter in the rising edge of the clock is still a concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates <20MHz, nominally. The loop has a time constant associated with it that must be considered in applications where the clock rate can change dynamically. A wait time of 5µs is required after a dynamic clock frequency increase or decrease before the DCS loop relocks to the input signal.

Jitter Considerations

High-speed, high-resolution ADCs are sensitive to the quality of the clock input. The following equation shows how signal-to-noise ratio (SNR) degrades at a given input frequency (f_A) due only to aperture jitter (t_J):

$$\text{SNR Degradation} = 20 \log_{10} \left(\frac{1}{2\pi \times f_A \times t_J} \right)$$

In this equation, the rms aperture jitter represents the rms of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter. The effect of jitter alone on SNR, with no other noise contributors, is shown *Figure 90*.

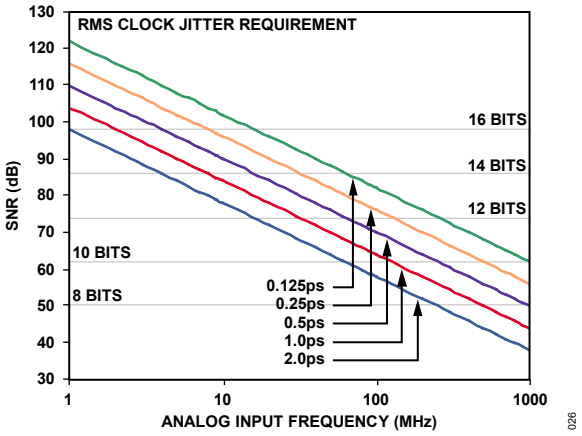

Figure 90. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter can affect the dynamic range of the ADA4356. Separate clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it is recommended to retime the clock by the original clock as the last step.

For more details on jitter performance as it relates to the internal ADC of the ADA4356, refer to the Application Note AN-501*: Aperture Uncertainty and ADC System Performance* and the Application Note AN-756*: Sampled Systems and the Effects of Clock Phase Noise and Jitter*.

Clock Stability Considerations

Immediately after power-on, the ADA4356 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the ADA4356 needs a stable clock. If the clock source to the ADC is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, invoke a digital reset via Register 0x08 after the clock source is stable. Clock instability during normal operation may also necessitate a digital reset to restore proper operation.

The pseudo code sequence for a digital reset is as follows:

1. For a digital reset, write Register 0x08 = 0x03.
2. For the normal operation, write Register 0x08 = 0x00.

Controls

The ADA4356 uses four balls to control various functions of the analog front end. Use the GSEL1 (A5) and GSEL0 (A4) balls to select T_Z (see *Table 11*), use the VLDEN (F7) ball to enable or disable the internal LDO, and use FSEL (A6) to select the filter bandwidth for the internal LPF. These control balls must be driven, as these balls have no internal pull-up or pull-down resistors.

Transimpedance Gain and Performance Controls

Each T_Z determines its corresponding maximum linear input current and input referred rms current noise (i_N), as listed in *Table 9*. The GSEL0 and GSEL1 logic levels define TIA gain setting, as shown in *Table 11*.

Table 11.Truth Table for GSEL1 and GEL0

GSEL1 (BALL A5)	GSEL0 (BALL A4)	INTERNAL GAIN SELECTION	TRANSIMPEDANCE
0	1	4.7kΩ‖133kΩ	T_Z = 4.54kΩ
1	0	12kΩ‖133kΩ	T_Z = 11kΩ
0	0	133kΩ	T_Z = 133kΩ
1	1	Reserved	Reserved

LDO Enable Controls

The internal 1.8V LDO is controlled via the VLDEN ball. The control signal vs. LDO output are shown in *Table 12*.

Table 12. LDO Control Signal Truth Table

VLDEN (BALL F7)	VLD (BALL F12)
0	No output
1	1.8V

LPF Bandwidth Selection

The ADA4356 uses an internal analog LPF to optimize settling time and noise performance. The LPF is controlled via the FSEL ball, as shown in *Table 13*. Consider the input signal pulse-width when choosing the LPF bandwidth.

Table 13. LPF Truth Table

FSEL (BALL A6)	LPF BANDWIDTH (MHz)
0	100
1	1

System Data Interface and Timing

The ADA4356 supports high speed, digital serial outputs. These serial differential outputs are LVDS-compatible data and clock lanes. These output lanes include the D0AP (A14), D0AN (A13), D1AP (B14), D1AN (B13), DCOP (D14), DCON (D13), FCOP (C14), and FCON (C13) balls.

At power-on default, the ADA4356 differential outputs conform to the ANSI-644 LVDS standard. Each of the LVDS output driver currents is set at a nominal 3.5mA. A 100Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350mV swing (or 700mV p-p differential) at the receiver.

The ADA4356 differential outputs also support a low power, reduced signal range option (similar to the IEEE 1596.3 standard) via SPI programming. When operating in reduced range mode, the LVDS output driver current reduces to 2mA. This reduction results in a 200mV swing (or 400mV p-p differential) across a 100Ω termination at the receiver.

The LVDS outputs facilitate interfacing with LVDS receivers in custom applications specific ICs (ASICs) and FPGAs for improved switching performance in noisy environments. To reduce the environmental noise impact, the PCB trace design recommends single point-to-point net topologies with a 100Ω termination resistor placed as close as possible to the receiver. Timing errors may result if there is no far end receiver termination, or if there is poor differential trace routing. To avoid such timing errors, minimize trace lengths and keep the differential output traces close together and at equal lengths.

Figure 91 shows an example of the FCO and data stream with proper trace length and position. In *Figure 91* and *Figure 92*, D0 is the differential signal, D0AP – D0AN, and D1 is the differential signal, D1AP – D1AN.

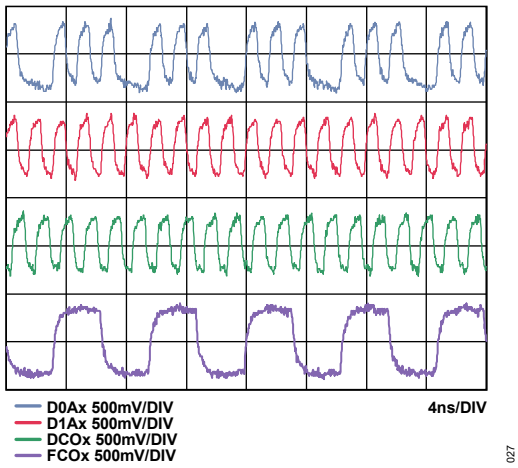

Figure 91. Output Timing Example in ANSI-644 Mode (Default)

Figure 92 shows the LVDS output timing example in reduced range mode.

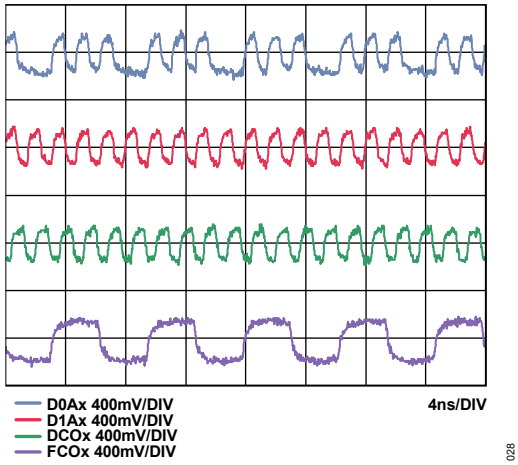

Figure 92. LVDS Output Timing Example in Reduced Range Mode

Figure 93 shows an example of the LVDS output data eye using the ANSI-644 standard (default) with trace lengths of less than 24inches on standard FR-4 material.

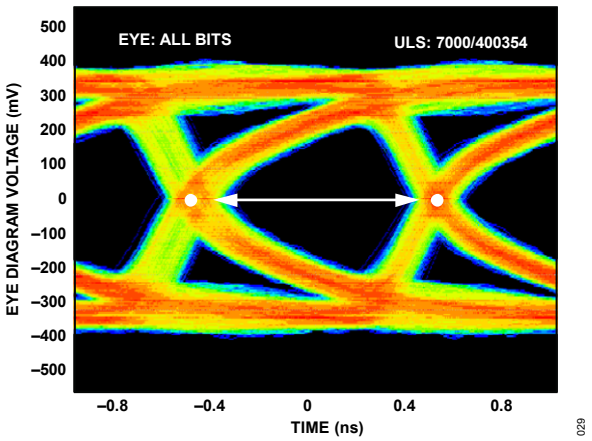

Figure 93. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less than 24inches (Approximate 6inch Trace Length Result Shown) on Standard FR-4 Material, External 100Ω Far End Termination Only

Figure 94 shows a time interval error (TIE) jitter histogram with trace lengths of less than 24inches on standard FR-4 material.

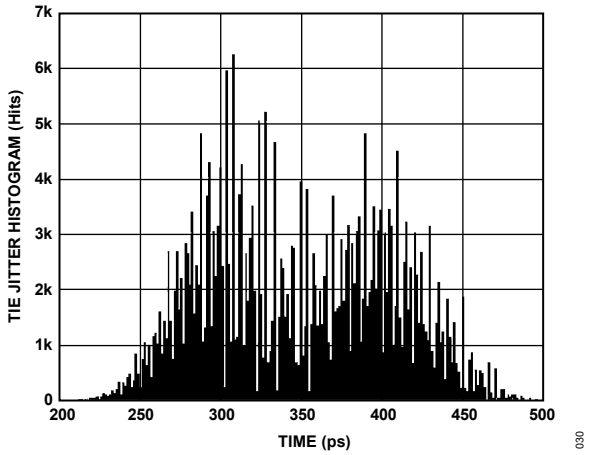

Figure 94.TIE Jitter Histogram for Trace Lengths Less than 24inches (Approximate 6inch Trace Length Result Shown) on Standard FR-4 Material

The TIE jitter histogram reflects the decrease of the data eye opening because the edge deviates from the ideal position. It is the responsibility of the user to determine if the waveforms meet the timing budget of the design.

The format of the output data is two's complement by default. For an example of the output coding format, see *Table 14*. To change the output data format to offset binary, see the *Memory Map* section.

Immediately after power-on, the ADA4356 output serial stream sets as double data rate (DDR), 2-lane, byte wise, MSB first, 1× frame, and 16-bit mode. In this default setting, the ADA4356 data rate for each serial stream is equal to (16 bits × the sample clock rate)/2 lanes, with a maximum of 1 Gbps per lane ((16 bits × 125 MSPS)/2-lanes = 1Gbps per lane).

Figure 95 shows an example of the LVDS output data eye using the ANSI-644 standard (default) with trace lengths greater than 24inches on standard FR-4 material.

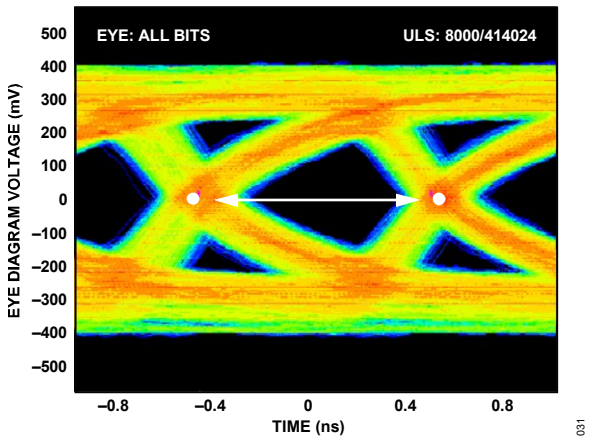

Figure 95. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater than 24inches (Approximate 36inch Trace Length Result Shown) on Standard FR-4 Material, External 100Ω Far End Termination Only

Figure 96 shows a TIE jitter histogram with trace lengths greater than 24inches on standard FR-4 material.

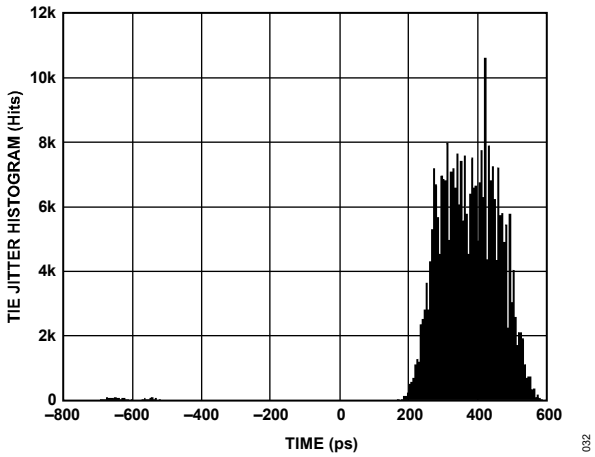

Figure 96. TIE Jitter Histogram for Trace Lengths Greater than 24inches (Approximate 36inch Trace Length Result Shown) on Standard FR-4 Material

Two output clocks assist in capturing data from the ADA4356. The DCO clocks the output data and is equal to 4× the sample clock (CLK) rate for the default mode of operation. Data is clocked out of the ADA4356 and must be captured on the rising and falling edges of the DCO that supports DDR capturing. The FCO signals the start of a new output byte and is equal to the sample clock rate in 1× frame mode. For more details, see *Figure 6*.

When the SPI is used, the DCO phase can be adjusted in approximately 60° increments relative to one data cycle (30° relative to one DCO cycle). This adjustment allows the user to refine system time margins, if required. The example DCOP and DCON timing, as shown in *Figure 6*, is 180° relative to one data cycle (90° relative to one DCO cycle).

In power-on default mode, as shown in *Figure 6*, the MSB is first in the data output serial stream. This configuration can be inverted by programming the SPI so that the LSB is first in the data output serial stream.

Digital Output Coding

There are 12 digital output test pattern options available that can be initiated through the SPI. This feature is useful when validating receiver capture and timing. For the output bit sequencing options available, see *Table 15*. Some test patterns have two serial sequential words and can be alternated in various ways depending on the test pattern chosen.

Note that some patterns do not adhere to the data format select option. In addition, custom, user-defined test patterns can be assigned in the following register addresses: Register 0x19, Register 0x1A, Register 0x1B, and Register 0x1C.

Table 14. Digital Output Coding

INPUT (V)[1]	CONDITION	OFFSET BINARY OUTPUT MODE	TWO's COMPLEMENT MODE
VIN+ − VIN−	<−1V − 0.5LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ − VIN−	−1V	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ − VIN−	0V	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ − VIN−	+1V − 1.0LSB	1111 1111 1111 1100	0111 1111 1111 1100
VIN+ − VIN−	>+1V − 0.5LSB	1111 1111 1111 1100	0111 1111 1111 1100

[1] VIN+ and VIN− are the positive and negative input voltages.

Table 15. Flexible Output Test Modes

OUTPUT TEST MODE BIT SEQUENCE	PATTERN NAME	DIGITAL OUTPUT WORD 1	DIGITAL OUTPUT WORD 2	SUBJECT to DATA FORMAT SELECT	NOTES
0000	Off (default)	Not applicable (N/A)	N/A	N/A	N/A
0001	Midscale short	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	N/A	Yes	Offset binary code shown
0010	+Full-scale short	1111 1111 1111 (12-bit) 1111 1111 1111 1100 (16-bit)	N/A	Yes	Offset binary code shown
0011	−Full-scale short	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	N/A	Yes	Offset binary code shown
0100	Checkerboard	1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit)	0101 0101 0101 (12-bit) 0101 0101 0101 0100 (16-bit)	No	N/A
0101	PN sequence long[1]	N/A	N/A	Yes	PN23 ITU 0.150 $X^{23} + X^{18} + 1$
0110	PN sequence short[1]	N/A	N/A	Yes	PN9 ITU 0.150 $X^9 + X^5 + 1$

OUTPUT TEST MODE BIT SEQUENCE	PATTERN NAME	DIGITAL OUTPUT WORD 1	DIGITAL OUTPUT WORD 2	SUBJECT to DATA FORMAT SELECT	NOTES
0111	One-/zero-word toggle	1111 1111 1111 (12-bit) 111 1111 1111 1100 (16-bit)	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	No	N/A
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No	N/A
1001	1-/0-bit toggle	1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit)	N/A	No	N/A
1010	1× sync	0000 0011 1111 (12-bit) 0000 0001 1111 1100 (16-bit)	N/A	No	N/A
1011	1-bit high	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	N/A	No	Pattern associated with the external ball
1100	Mixed frequency	1010 0011 0011 (12-bit) 1010 0001 1001 1100 (16-bit)	N/A	No	N/A

[1] All test mode options except pseudorandom number (PN) sequence short and PN sequence long can support 12-bit to 16-bit word lengths to verify data capture to the receiver.

SERIAL PERIPHERAL INTERFACE

The ADA4356 SPI allows users to configure the internal ADC for specific functions or operations through a structured register space. Registers are accessible via the SPI port. Register contents can be modified by writing to the port. Bytes that can be further divided into fields constitute register memory, which is documented in the *Memory Map* section. Details specified in this data sheet take precedence over the Application Note AN-877*: Interfacing to High Speed ADCs via SPI*, which provides general information.

Configuration Using the SPI

The ADA4356 uses a 3-wire SPI configuration, SCLK, SDIO, and $\overline{CS}$. For the functionality of each ball, see *Table 16*.

Table 16. Serial Port Interface Balls

MNEMONIC	BALL	FUNCTION
SCLK	A11	Serial clock when $\overline{CS}$ is low. The serial shift clock input, which synchronizes serial interface reads and writes.
SDIO	B11	Serial data input/output when $\overline{CS}$ is low. Serves as an input or output, which depends on the instruction sent and the relative position in the timing frame.
$\overline{CS}$	A10	Chip select. An active low control that enables the SPI mode read and write cycles.

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing is shown in *Figure 5*. For the definitions of the timing parameters, see *Table 4*.

In the ADA4356 application, $\overline{CS}$ must be held low at power-up to enable SPI mode, and then kept low, which is called streaming. $\overline{CS}$ can stall high between bytes to allow additional external timing.

During the instruction phase of an SPI operation, a 16-bit instruction is transmitted. Data follows the instruction phase, and the length of this data is determined by the W0 and W1 bits (see *Figure 5*).

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, which allows the serial port to both program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the SDIO ball to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more details on this and other features, refer to the Application Note AN-877*: Interfacing to High Speed ADCs via SPI*.

ADC SPI Start-Up Sequence

To ensure proper device operation and power dissipation, the following SPI sequence must be written after the ADA4356 is powered on and anytime a power cycle occurs:

//SPI_WRITE(Memory Map Register,

Register Value)

SPI_WRITE(0x00, 0x00);

SPI_WRITE(0x05, 0x02);

SPI_WRITE(0x22, 0x03);

SPI_WRITE(0x05, 0x31);

Hardware Interface

The balls described in *Table 16* comprise the physical interface between the user-programming device and the serial port of the ADA4356. The SCLK and the $\overline{CS}$ ball function as inputs when using the SPI. The SDIO ball is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the Application Note AN-812*: Microcontroller-Based Serial Port Interface (SPI®) Boot Circuit*.

It is recommended that the SPI port must not be active during periods when the full dynamic performance of the converter is required. Because the signals on SCLK, $\overline{CS}$, and SDIO are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the ADA4356 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI Accessible Features

Table 17 provides a brief description of the general features accessible via the SPI. These features are described in general in the Application Note AN-877*: Interfacing to High Speed ADCs via SPI*. ADA4356 device-specific features are described in *Table 18*.

Table 17. Features Accessible Using the SPI

FEATURE NAME	DESCRIPTION
Power Mode	Allows the user to set either power-down or standby mode.
Clock	Allows the user to access the DCS, set the clock divider, and set the clock divider phase.
Offset	Allows the user to digitally adjust the converter offset.

MEMORY MAP

Overview

The memory map register *Table 18* describes the ADA4356 registers. These registers configure and control the ADC only.

The memory map is divided into three sections: the chip configuration registers, the device index register, and the global ADC function registers, including setup and control.

Each register has 8-bit locations. The column with the Bit 7 (MSB) heading contains the most significant bit of the default hexadecimal value given. For example, Register 0x05, the device index register, has a hexadecimal default value of 0x33, which means that in Register 0x05, Bits[7:6] = 00, Bits[5:4] = 11, Bits[3:2] = 00, and Bits [1:0] = 11 (in binary).

For more details on this SPI port function, see the Application Note AN-877*: Interfacing to High Speed ADCs via SPI*. This application note documents the functions controlled by Register 0x00 to Register 0xFF.

Open Locations

In *Table 18*, the register bit open locations are reserved to the ADA4356. These bits must be always set to 0.

Default Values

The default values are available in *Table 18*.

After power-on, all registers have loaded their default values. To soft reset the ADA4356, use Register 0x00. All registers, except the read-only register (Register 0x02), are loaded with default values.

Logic Levels

An explanation of logic level terminology follows:

- Bit is set is synonymous with bit is set to Logic 1 or writing Logic 1 for the bit.
- "Clear a bit is synonymous with bit is set to Logic 0 or writing Logic 0 for the bit.

Memory Map Register Table

The ADA4356 uses a 3-wire interface and 16-bit addressing. Therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1.

When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset, where all the user registers revert to their default values, and Bit 2 is automatically cleared.

Table 18.Memory Map Register

REG. (HEX)	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE (HEX)	COMMENTS
CHIP CONFIGURATION REGISTERS											
0x00	SPI port configuration	0 = SDO active	LSB first	Soft reset	1 = 16-bit address	1 = 16-bit address	Soft reset	LSB first	0 = SDO active	0x18	Nibbles are mirrored to allow a given register value to perform the same function for either MSB-

REG. (HEX)	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE (HEX)	COMMENTS
											first or LSB-first mode.
0x01	Chip ID (global)	8-bit chip ID, Bits[7:0], ADA4356								0x8B	Unique chip ID used to differentiate devices; read only.
DEVICE INDEX and TRANSFER REGISTERS											
0x05	Device index	Open	Open	Clock channel DCO	Clock channel FCO	Open	Open	01 = data channel enabled, 00 = data channel disabled, Bit 1 only used after start-up or power cycle, see the *ADC SPI Start-Up Sequence* section		0x33	Bits are set to determine which channels receive the next write command. Bit 1 is only used after start-up or power cycle.
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate override	0x00	Set resolution/ sample rate override.
GLOBAL ADC FUNCTION REGISTERS											
0x08	ADC power modes (global)	Open	Open	Open	Open	Open	Open	Power mode: 00 = chip run, 01 = full power-down, 10 = standby, 11 = reset		0x00	Determines various generic modes of chip operation.
0x09	Clock (global)	Open	Open	Open	Open	Open	Open	Open	DCS: 0 = off, 1 = on	0x00	Turns DCS on or off.
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio[2:0]: 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Not applicable.
0x0D	Test mode (local except for PN sequence resets)	User input test mode: 00 = single, 01 = alternate, 10 = single once, 11 = alternate once (affects user input test mode only, Bits[3:0] = 1000)		Reset PN long gen	Reset PN short gen	Output test mode, Bits[3:0] (local): 0000 = off (default), 0001 = midscale short, 0010 = positive full-scale, 0011 = negative full-scale, 0100 = alternating checkerboard, 0101 = PN23 sequence, 0110 = PN9 sequence, 0111 = one-/zero-word toggle, 1000 = user input, 1001 = 1-/0-bit toggle, 1010 = 1× sync, 1011 = one bit high, 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output balls in place of normal data.

REG. (HEX)	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE (HEX)	COMMENTS
0x14	Output mode	Open	LVDS-ANSI/ LVDS-IEEE option: 0 = LVDS-ANSI, 1 = LVDS-IEEE reduced range link (global), see *Table 19*	Open	Open	Open	Output invert (local)	Open	Output format: 0 = offset binary, 1 = two's complement (global)	0x01	Configures the outputs and format of the data.
0x15	Output adjust	Open	Open	Output driver termination, Bits[1:0]: 00 = none, 01 = 200Ω, 10 = 100Ω, 11 = 100Ω		Open	Open	Open	Output drive: 0 = 1× drive, 1 = 2× drive	0x00	Determines LVDS or other output properties.
0x16	Output phase	Open	Input clock phase adjust, Bits[6:4] (value is the number of input clock cycles of phase delay), see *Table 20*			Output clock phase adjust, Bits[3:0] (0000 through 1011), see *Table 21*				0x03	On devices using global clock divide, Register 0x16 determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
0x19	USER_PATT1_ LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern 1LSB.
0x1A	USER_PATT1_ MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined pattern 1MSB.
0x1B	USER_PATT2_ LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined pattern 2LSB.
0x1C	USER_PATT2_ MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined

REG. (HEX)	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE (HEX)	COMMENTS
											pattern 2MSB.
0x21	Serial output data control (global)	LVDS output: 0 = MSB first (default), 1 = LSB first	SDR/DDR 1-lane/2-lane, bit wise/byte wise, Bits[6:4]: 000 = SDR 2-lane, bit wise, 001 = SDR 2-lane, byte wise, 010 = DDR 2-lane, bit wise, 011 = DDR 2-lane, byte wise (default), 100 = DDR 1-lane, word wise			Encode mode: 0 = normal encode rate mode (default), 1 = low encode mode for sample rate of <20MSPS	0 = 1× frame (default), 1 = 2× frame	Serial output number of bits: 00 = 16 bits (default), 10 = 12 bits		0x30	Serial stream control. Sample rate of <20MSPS requires that Bits[6:4] = 100 (DDR 1-lane) and Bit 3 = 1 (low encode mode).
0x22	Serial channel status (local)	Open	Open	Open	Open	Open	Open	Channel output reset	Channel power-down	0x00	Used to power down individual sections of a converter.
0x100	Resolution/sample rate override	Open	Resolution/sample rate override enable	Resolution: 01 = 14 bits 10 = 12 bits		Open	Sample rate: 000 = 20MSPS, 001 = 40MSPS, 010 = 50MSPS, 011 = 65MSPS, 100 = 80MSPS, 101 = 105MSPS, 110 = 125MSPS			0x00	Resolution/sample rate override (requires writing to the transfer register, 0xFF).
0x101	User input/output control	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disables SDIO pull-down.

Memory Map Register Descriptions

For more details on registers not described herein, and for general details on the functions controlled in Register 0x00 to Register 0xFF, refer to the Application Note AN-877*: Interfacing to High Speed ADCs via SPI*.

Chip ID (Register 0x01)

The power-on default value of this register is 0x8B.

Register 0x01 is a read-only register that is used for chip identification and for SPI authentication.

Device Index (Register 0x05)

The power-on default value of this register is 0x33.

Bits[7:6]—Open

Bit 5—Clock Channel DCO

Bit 5 is used to select the output DCO clock channel.

Bit 4—Clock Channel FCO

Bit 4 is used to select the output FCO clock channel.

Bits[3:2]—Open

Bits[1:0]—Data Channel

Setting Bit 1 enables the data channel to receive SPI write commands. To ensure Bit 0 is configured correctly, perform the SPI write commands, as shown in the *ADC SPI Start-Up Sequence* section immediately after start-up or reset.

ADC Power Modes (Register 0x08)

The power-on default value of this register is 0x00.

Bits[7:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), ADC is active.

In power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled, while the digital datapath is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital datapath clocks, and the outputs are disabled.

During a digital reset (Bits[1:0] = 11), all digital clocks and outputs (where applicable) on the chip are reset, except the SPI port. The SPI port is always left under control of the user, that is, the port is never automatically disabled or in reset, except by power-on reset.

Clock (Register 0x09)

The power-on default value of this register is 0x00.

Bits[7:1]—Open

Bit 0—DCS

This bit turns the DCS on and off.

Clock Divide (Register 0x0B)

The power-on default value of this register is 0x00.

Bits[7:3]—Open

Bits[2:0]—Clock Divide Ratio

Bits [2:0] are used to set the clock divide ratio.

Output Mode (Register 0x14)

The power-on default value of this register is 0x01.

Bit 7—Open

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting this bit selects the LVDS-IEEE (reduced range) option. The default setting for this bit is LVDS-ANSI. When LVDS-ANSI or the LVDS-IEEE reduced range link is selected, the driver current is automatically selected to give the proper output swing.

Table 19. LVDS-ANSI/LVDS-IEEE Options

BIT 6	OUTPUT MODE	OUTPUT DRIVER CURRENT
0	LVDS-ANSI (default)	Automatically selected to give proper swing.
1	LVDS-IEEE reduced range link	Automatically selected to give proper swing.

Bits[5:3]—Open

Bit 2—Output Invert

Setting this bit inverts the output bit stream.

Bit 1—Open

Bit 0—Output Format

By default, this bit is set to send the data output in two's complement format. Clearing this bit to 0 changes the output mode to offset binary.

Output Adjust (Register 0x15)

The power-on default value of this register is 0x00.

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal termination resistor.

Bits[3:1]—Open

Bit 0—Output Driver

Bit 0 of the output adjust register controls the drive strength on the LVDS driver of the FCO and DCO outputs only. The default value setsthe drive to 1×, or the drive can increase to 2× by setting the appropriate channel bit in Register 0x05 and then setting Bit 0, Register 0x15. These features cannot be used with the output driver termination select. The termination selection takes precedence over the 2× driver strength on FCO and DCO when both the output driver termination and output driver are selected.

Output Phase (Register 0x16)

The power-on default value of this register is 0x03.

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] of Register 0x16 determine at which phase the external clock sampling occurs. The input clock phase adjust is only applicable when the clock divider is used. Selecting a value for Bits[6:4] greater than Register 0x0B, Bits[2:0] is prohibited. See *Table 20*.

Bits[3:0]—Output Clock Phase Adjust

For more details, see *Table 21*.

Table 20. Input Clock Phase Adjust Options

INPUT CLOCK PHASE ADJUST, REGISTER 0x16, BITS[6:4]	NUMBER of INPUT CLOCK CYCLES of PHASE DELAY
000 (Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table 21.Output Clock Phase Adjust Options

OUTPUT CLOCK (DCO), PHASE ADJUST, REGISTER 0x16, BITS[3:0]	DCO PHASE ADJUSTMENT (APPROXIMATE DEGREES RELATIVE to the DxAP/DxAN EDGE)
0000	0
0001	60
0010	120
0011 (Default)	180
0100	240
0101	300
0110	360
0111	420
1000	480
1001	540
1010	600
1011 through 1111	600

Serial Output Data Control (Register 0x21)

The power-on default value of this register is 0x30.

The serial output data control register programs the ADA4356 in various output data modes, to accommodate different data capture solutions. *Table 22* describes the various serialization options available in the ADA4356. Note that, in single data rate (SDR) mode, the DCO frequency is double that of the frequency in DDR mode for a given sample rate. In SDR mode, to stay within the capability of the DCO LVDS driver, reduce the ADC sample rate to ≤62.5MSPS to keep the DCO frequency at ≤500MHz.

User Input/Output Control 2 (Register 0x101)

The power-on default value of this register is 0x00.

Bits[7:1]—Open

Bit 0—Disable SDIO Pull-Down

Bit 0 can be set to disable the internal 31kΩ pull-down resistor on the SDIO ball (B11), which limits the loading when many devices are connected to the SPI bus.

Table 22.Register 0x21 Options

	SERIALIZATION OPTIONS SELECTED				
REGISTER 0x21 CONTENTS	**SERIAL OUTPUT NUMBER of BITS (SONB)**	**FRAME MODE**	**SERIAL DATA MODE**	**DCO MULTIPLIER**	**TIMING DIAGRAM**
0x30	16-bit	1×	DDR 2-lane byte wise	4 × f_S	See *Figure 6* (default setting).
0x20	16-bit	1×	DDR 2-lane bit wise	4 × f_S	See *Figure 6*.
0x10	16-bit	1×	SDR 2-lane byte wise	8 × f_S	See *Figure 6*.
0x00	16-bit	1×	SDR 2-lane bit wise	8 × f_S	See *Figure 6*.
0x34	16-bit	2×	DDR 2-lane byte wise	4 × f_S	See *Figure 8*.
0x24	16-bit	2×	DDR 2-lane bit wise	4 × f_S	See *Figure 8*.
0x14	16-bit	2×	SDR 2-lane byte wise	8 × f_S	See *Figure 8*.
0x04	16-bit	2×	SDR 2-lane bit wise	8 × f_S	See *Figure 8*.
0x40	16-bit	1×	DDR 1-lane word wise	8 × f_S	See *Figure 10*.
0x32	12-bit	1×	DDR 2-lane byte wise	3 × f_S	See *Figure 7*.
0x22	12-bit	1×	DDR 2-lane bit wise	3 × f_S	See *Figure 7*.
0x12	12-bit	1×	SDR 2-lane byte wise	6 × f_S	See *Figure 7*.
0x02	12-bit	1×	SDR 2-lane bit wise	6 × f_S	See *Figure 7*.
0x36	12-bit	2×	DDR 2-lane byte wise	3 × f_S	See *Figure 9*.
0x26	12-bit	2×	DDR 2-lane bit wise	3 × f_S	See *Figure 9*.
0x16	12-bit	2×	SDR 2-lane byte wise	6 × f_S	See *Figure 9*.
0x06	12-bit	2×	SDR 2-lane bit wise	6 × f_S	See *Figure 9*.
0x42	12-bit	1×	DDR 1-lane word wise	6 × f_S	See *Figure 11*.

PCB Design Tips

Signal Integrity Recommendations

Place the photodiode signal source as close as possible to the ADA4356 input to minimize trace length and associated parasitic capacitance. Clear away all ground layers directly underneath the input trace to reduce parasitics even further. Additionally, match the lengths of all LVDS lines (DCON, DCOP, FCON, FCOP, D0AN, D0AP, D1AN, and D1AP) to eliminate potential timing issues.

Thermal Design Recommendations

The ADA4356 uses multiple VCC and GND balls to facilitate the internal power and grounding requirements. All of these balls must be connected for proper electrical connectivity within the module. Additionally, the PCB connection of the multiple VCC and GND balls is an integral part of the thermal design. All the ADA4356 VCC and GND balls must be connected to a PCB copper plane with the lowest thermal resistance possible. To achieve the best thermal performance, these planes must have as many thermal vias as practical to provide the lowest possible thermally resistive path for heat dissipation to flow through the bottom of the PCB. Solder fill or plug these vias.

Surface-Mount Design

Table 23 is provided as an aid to PCB design to accommodate CSP_BGA style surface-mount packages. For industry-standard design recommendations, refer to IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard.

Table 23. CSP_BGA Data for Use with Surface-Mount Design

PACKAGE	BALL ATTACH TYPE	SOLDER MASK OPENING	BALL PAD SIZE
84-Ball CSP_BGA (BC-84-4)	Solder mask defined	0.35mm diameter	0.40mm diameter

OUTLINE DIMENSIONS

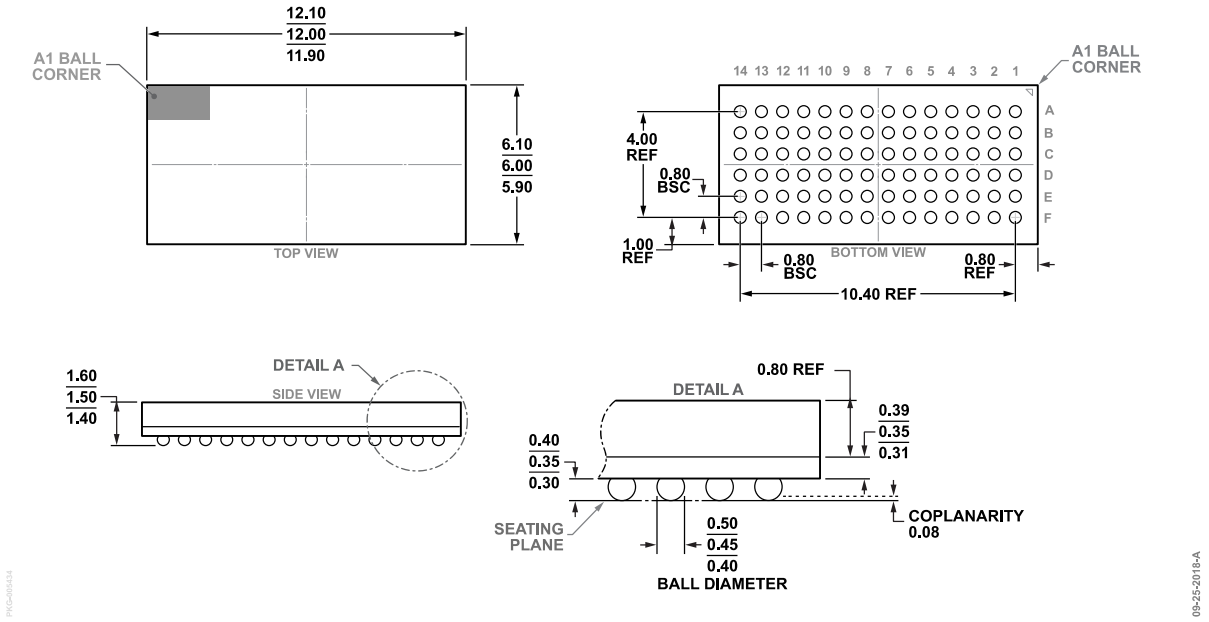

Figure 97.84-Ball Chip-Scale Package Ball Grid Array [CSP_BGA] (BC-84-4) Dimensions shown in millimeters

ORDERING GUIDE

Table 24.Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
ADA4356ABCZ	−40°C to +85°C	84-Ball Chip-Scale Package Ball Grid Array [CSP_BGA]	BC-84-4

[1] Z = RoHS Compliant Part.