4T2R Direct RF Transmitter and Observation Receiver

Preliminary Technical Data

AD9986

FEATURES

- Flexible reconfigurable radio common platform design
  - 4D2A (4 × 12 GSPS 16-bit DAC + 2 × 6 GSPS 12-bit ADC)
  - 4D1A (4 × 12 GSPS 16-bit DAC + 1 × 6 GSPS 12-bit ADC)
  - Transmit/receive channel bandwidth up to 1.2 GHz/2.4 GHz (4T2R)
  - Transmit/receive channel bandwidth up to 2.4 GHz/2.4 GHz (2T2R)
  - RF DAC/RF ADC output/input −3 dB bandwidth of 5.2 GHz and 7.5 GHz
  - On-chip PLL with multichip synchronization
    - External RF clock input option
- ADC ac performance at 6 GSPS
  - Full-scale input voltage: 1.475 V p-p
  - Noise density: −153 dBFS/Hz
  - Noise figure: 25.3 dB
  - HD2: −65.2 dBFS at 2.7 GHz
  - HD3: −70.8 dBFS at 2.7 GHz
  - Worst other (excluding HD2 and HD3): −68.5 dBFS at 2.7 GHz
- DAC ac performance at 12 GSPS
  - Full-scale output current range: 7 mA to 40 mA
  - 2-tone IMD3 (−7 dBFS per tone): −78.9 dBc
  - Noise spectral density (NSD), single-tone at 3.7 GHz: −155.1 dBc/Hz
  - Spurious free dynamic range (SFDR), single-tone at 3.7 GHz: −70 dBc
- Versatile digital features
  - Selectable interpolation and decimation filters
  - Configurable digital down conversion (DDC) and digital up conversion (DUC)
    - 8 fine complex DUCs and 4 coarse complex DUCs
    - 8 fine complex DDCs and 4 coarse complex DDCs
    - 48-bit numerically controlled oscillator (NCO) per DUC/DDC
    - Option to bypass fine DUC/DDC
  - Programmable 192 tap programmable filter (PFIR) for receive equalization
    - Supports 4 different profile settings loaded via GPIO
  - Programable delay per data path
  - Receive automatic gain control (AGC) support
    - Fast detect with low latency for fast AGC control
    - Signal monitor for slow AGC control
    - Dedicated AGC support pins
  - Transmit DPD support
    - Fine DUC channel gain control and delay adjust
    - Coarse DDC delay adjust for DPD observation path
- Versatile digital features
  - Supports real or complex digital data (8-bit, 12-bit, or 16-bit)
  - Configurable digital up/down conversion (DDC/DUC)
    - 8 fine complex DUCs and 4 coarse complex DUCs
    - 8 fine complex DDCs and 4 coarse complex DDCs
    - 2 independent NCO per DUC/DDC
    - Option to bypass fine DUC/DDC
- Auxiliary features
    - ADC clock driver with selectable divide ratios
    - PA downstream protection circuitry
    - On-chip temperature sensor
    - Programmable GPIO pins
    - ADC clock driver with selectable divide ratios
    - TDD power savings option
- SERDES JESD204B/C Interface, 16 lanes up to 24.75 Gbps
  - 8 receive lanes for RFDAC
  - 8 transmit lanes for RFADC
  - JESD204B compatible with the maximum 15.5 Gbps lane rate
  - JESD204C compatible with the maximum 24.75 Gbps lane rate
  - Sample/bit repeat mode for receive lane rate matching
- 15 mm × 15 mm BGA with 0.8 mm pitch

APPLICATIONS

- Wireless communications infrastructure
- W-CDMA, LTE, LTE-A, massive MIMO
- Microwave point-to-point, E-band, and 5G mm wave
- Broadband communications systems
- Data over cable service interface specification (DOCSIS) 3.0 cable modem termination system (CMTS)
- Communications test and measurement system

GENERAL DESCRIPTION

The transmit signal front-end (TxFE™) is a highly integrated device with 16-bit, 12 GSPS maximum sample rate RF digital-to-analog converter (DAC) core and 12-bit, 6 GSPS rate RF analog-to-digital converter (ADC) core. The AD9986 is able to support four transmitter channels and two receiver channels with 4D2A configuration. This device is well suited for 2-antenna and 4-antenna transmitter applications requiring wideband ADCs for the digital predistortion (DPD) observation path. It features a sixteen lane 24.75 Gbps JESD204C or 15.5 Gbps JESD204B data transceiver port, an on-chip clock multiplier, and digital signal processing capability targeted at multiband direct-to-RF radio applications. It supports up to a 6 GSPS complex transmit and receive data rate in single channel mode. The maximum radio band spacing supported in multichannel mode is 1.2 GHz.

Rev. PrA Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

FUNCTIONAL BLOCK DIAGRAM

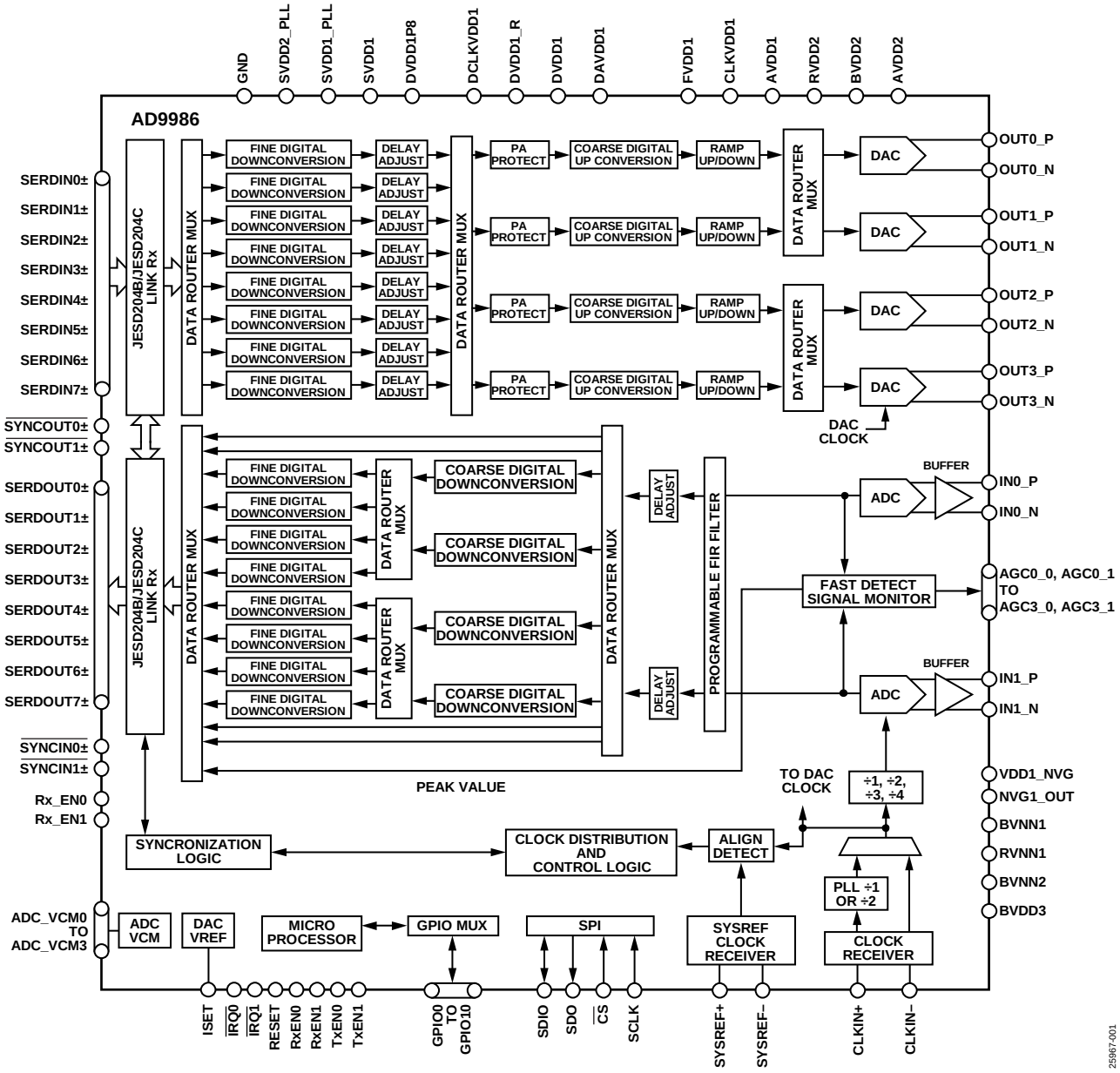


Figure 1.

ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
ISET, DACxP, DACxN, TDP, TDN	−0.3 V to AVDD2 + 0.3 V
VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG	−0.3 V to AVDD2_PLL + 0.3 V
ADC0P, ADC0N, ADC1P, ADC1N	−0.3 V to BVDD2 + 0.3 V
VCM0, VCM1	−0.3 V to RVDD2 + 0.3 V
CLKINP, CLKINN	−0.2 V to PLLCLKVDD1 + 0.2 V
ADCDRVN, ADCDRVP	−0.2 V to CLKVDD1 + 0.2 V
SERDINx±, SERDOUTx±	−0.2 V to SVDD1 + 0.2 V
SYSREFP, SYSREFN, and SYNCxIN±	−0.2 V to +2.5 V
SYNCxOUT±, SYNCxIN±, RESET, TXENx, RXENx, IRQx, CS, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, ADCx_SMON0, ADCx_SMON1, ADCx_FD0, ADCx_FD1, GPIOx	−0.3 V to DVDD1P8 + 0.3 V
AVDD2, AVDD2_PLL, BVDD2, RVDD2, SVDD2_PLL, DVDD1P8	−0.3 V to +2.2 V
PLLCLKVDD1, AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, DAVDD1, DVDD1_RT, DCLKVDD1, SVDD1, SVDD1_PLL	−0.2 V to +1.2 V
VNN1	−1.1 V to +0.2 V
Temperature	
Maximum Junction (T_J)[1]	120°C
Storage Range	−40°C to +150°C

[1] Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9986 reflow profile is in accordance with the JEDEC JESD 20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T_J does not exceed the limits shown in Table 1.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_TOP} is the junction-to-case thermal resistance.

θ_{JB} is the junction-to-board thermal resistance.

Table 2. Thermal Resistance[1]

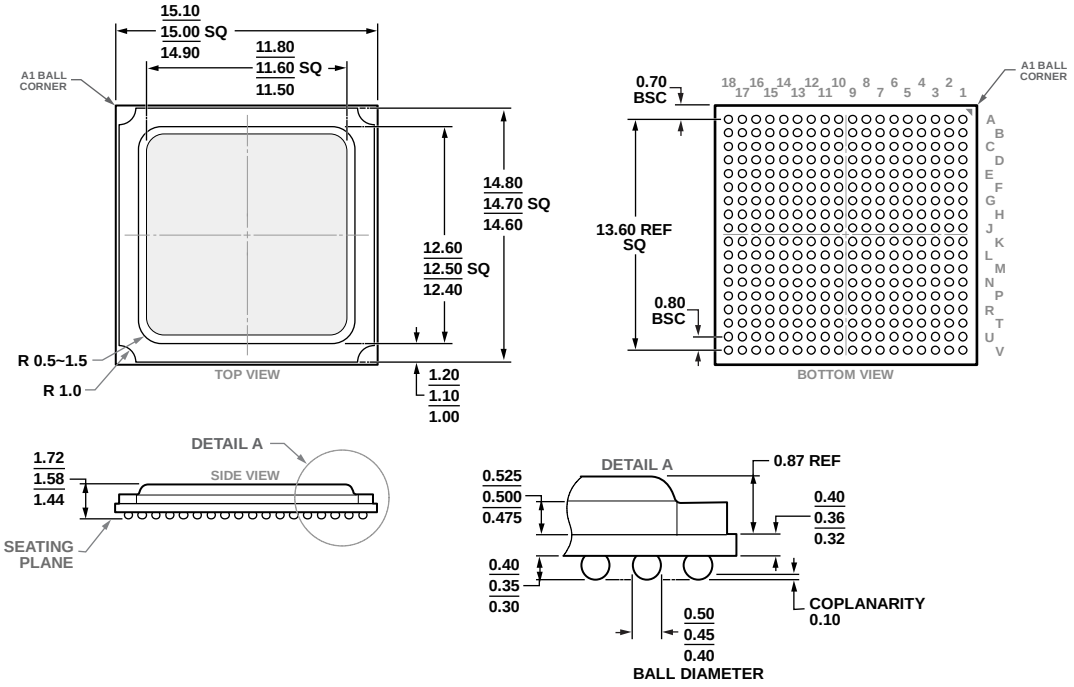
Package Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Unit
BP-324-3	0.0	11.7	0.40	2.3	°C/W

[1] Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-1

Figure 2. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-324-3)
Dimensions shown in millimeters