Mixed-Signal Front End (MxFE®)

AD9960

FEATURES

Receive path includes
- Simultaneous sampling 32 MSPS I/Q SHA
- 64 MSPS 14-bit muxed ADC with 77 dBFS SNR
- Bypassable 2nd order CIC and 64-tap FIR decimation filters

Transmit path includes
- Dual 12-bit, 32 MSPS TxDAC
- Bypassable 64-tap FIR and 3rd order CIC decimation filters

Auxiliary converters includes
- Dual 10-bit voltage output DACs
- Three 10-bit SAR muxed ADCs—10 analog inputs
- Programmable full-scale input/output levels

Flexible DSP and digital interface includes
- Bidirectional 16-bit Tx/Rx data port
- Supports interleaved Rx and Tx I/Q data as well as noninterleaved Tx data

9 programmable GPIOs

3- or 4-wire SPI interface

SPI-configurable registers allow programmability of IC and access to auxiliary converters and GPIOs

Internal clock doubler and timing generation circuitry

80-lead LQFP package

APPLICATIONS

RFID readers

FUNCTIONAL BLOCK DIAGRAM

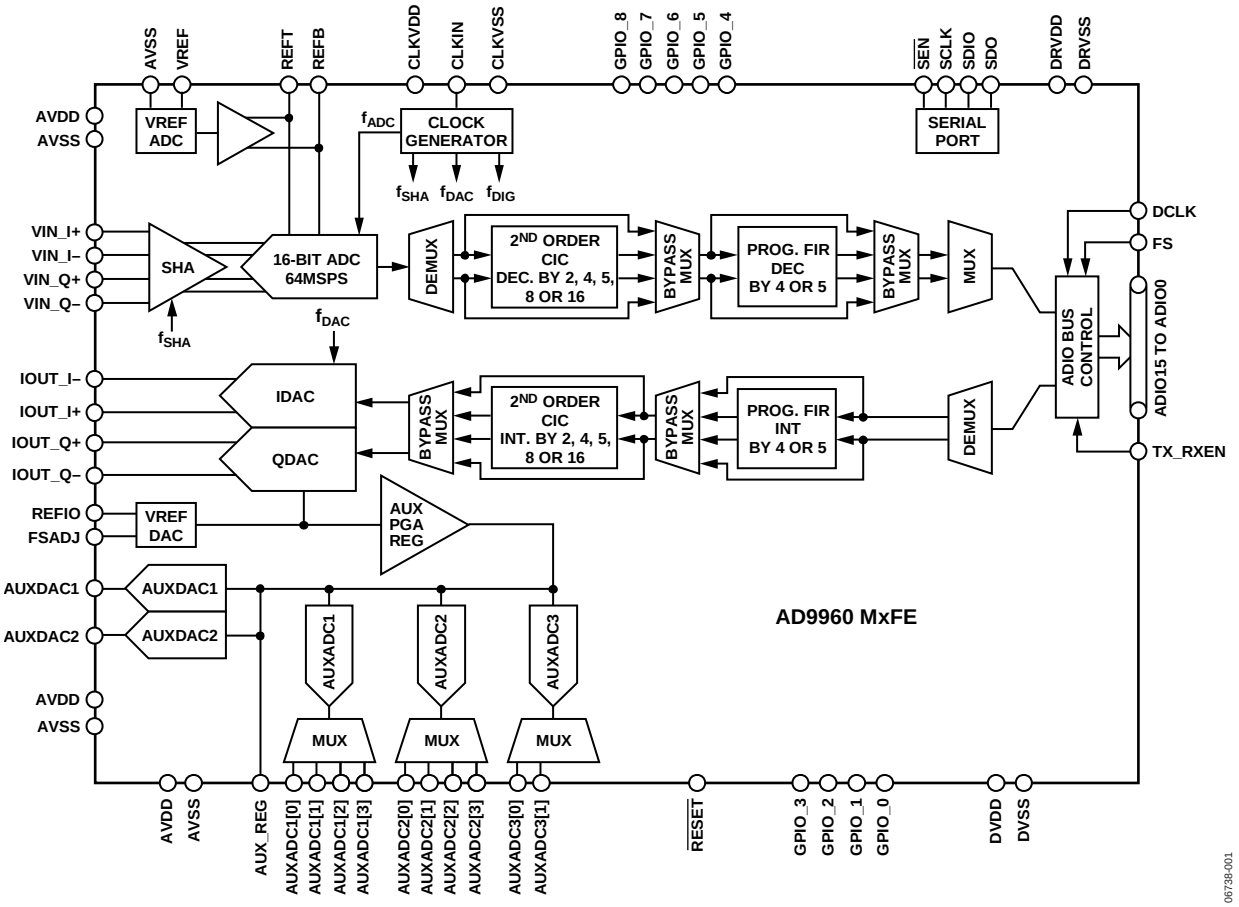

Figure 1.

Rev. 0

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REVISION HISTORY

5/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9960 is a member of the MxFE family, a group of integrated mixed-signal front-end ICs optimized for specific communications markets. The AD9960 has been optimized for high performance, wireless applications using a half-duplex protocol.

In the Rx signal path, the AD9960 integrates a dual simultaneous sampling SHA followed by a 14-bit muxed input ADC with 32 MSPS per channel capabilities. On the Tx signal path, it integrates a dual 12-bit, 32 MSPS TxDAC®. The power bias of the ADC and DACs can be reduced to support low power operation modes. The AD9960 uses a single input clock pin (CLKIN) to generate all internal clocks with an optional clock doubler to generate the ADC sampling clock.

Both the Rx and Tx signal paths provide CIC and programmable FIR filters with selectable decimation/interpolation factors to reduce the DSP processing and analog filtering requirements. A flexible bidirectional 16-bit data port is used to interface to popular DSPs. The bus direction is controlled via the DSP with the AD9960 generating a frame sync pulse indicating when valid interleaved Rx data begins to appear on the bus or when the DSP can place valid complex or real Tx data on to the bus. GPIO pins are available to support different DSP requirements.

The AD9960 also integrates auxiliary functions accessible via serial programmable interface (SPI) registers. Three muxed-input ADCs provide the ability to monitor up to 10 channels, while two voltage DACs can be used for control purposes. The full-scale input/output levels of each of these 10-bit resolution converters are also individually programmable. Also included are nine GPIO pins that are SPI-configurable. A 3- or 4- wire SPI is used to configure the AD9960's many modes of operation.

The AD9960 is packaged in an 80-lead LQFP (low profile quad flat package) and is specified over the −40°C to +85°C temperature range.

SPECIFICATIONS

ANALOG SPECIFICATIONS

T_{MIN} to T_{MAX}, unless otherwise specified; analog and digital supplies = 3.3 V ± 10%; f_{CLKIN} = 32 MHz. TxDAC settings: f_{DAC} = 32 MSPS; 8× interpolation; I_{OUTFS} = 20 mA[1]; differential load resistance of 25 Ω[2]; unless otherwise noted. RxADC settings: f_{ADC} = 64 MSPS[3] ; no decimation, internal VREF; differential 3 V p-p analog inputs; unless otherwise noted.

Table 1. Tx Path Specifications

Parameter	Min	Typ	Max	Unit
Tx PATH GENERAL				
Resolution		12		Bits
Maximum DAC Update Rate	32			MHz
Maximum Full-Scale Output Current	2		20	mA
Gain Mismatch Error	−2		+2	% FS
Offset Mismatch Error	−2		+2	% FS
Voltage Reference (REFIO)		1.23		V
Output Voltage Compliance Range	−1.0		+1.3	V
Tx PATH DYNAMIC PERFORMANCE (I_{OUTFS} = 20 mA; f_{OUT} = 100 kHz)				
SNR	71	73		dBFS
SINAD		70		dB
THD		−79	−71	dBc
SFDR, Wideband (DC to Nyquist)		83		dBc

Table 2. Rx Path Specifications

Parameter	Min	Typ	Max	Unit
Rx PATH GENERAL				
Resolution		14		Bits
Maximum I/Q Channel Sample Rate	32			MSPS
Reference Voltage (VREF)	1.44	1.5	1.55	V
Differential Analog Input Voltage Range	2		3	V p-p
Gain Error (with Internal VREF)	2		2	% FS
Gain Drift (with Internal VREF)		±25		ppm/C
Gain Mismatch Error		±0.1		% FS
Offset Mismatch Error		±0.3		% FS
Aperture Uncertainty (Jitter)		1		ps rms
Input-Referred Noise		150		µV rms
Rx PATH DYNAMIC PERFORMANCE (V_{IN} = −0.5 dBFS; f_{IN} = 1 MHz)				
SNR	71	74		dBc
SINAD	70	72		dBc
THD (2nd to 9th Harmonic)		−79	−71	dBc
SFDR, Wideband (DC to Nyquist)	74	82		dBc

[1] R_{SET} = 1.31 kΩ with internal VREF DAC.
[2] Results in 1 V p-p maximum differential voltage with common-mode voltage set to 0.5 V to replicate dc-coupled input to quadrature modulator.
[3] 2× clock multiplier enabled.

Table 3. Auxiliary ADC and DAC Specifications

Parameter	Min	Typ	Max	Unit
AUXILIARY ADC				
Resolution		10		Bits
ADC Monotonicity		Guaranteed		
Input Range[1]	0		AVDD	V
Conversion Rate				µs
AUXILIARY DAC				
Resolution		10		Bits
DAC Monotonicity		Guaranteed		
Input Range[1]	0		AVDD	
Slew Rate (Normal)		0.45		V/µs
Slew Rate (Boost)		1.7		V/µs
Settling Time (Normal)		300		kHz
Settling Time (Boost)		960		kHz

[1] AUXADC and AUXDAC full-scale span can be set to AVDD supply or programmable regulator voltage (2.52 V, 2.7 V, 3.0 V).

Table 4. Power Specifications

Parameter	Min	Typ	Max	Unit
POWER SUPPLY RANGE				
ADC Supply Voltage (ADCVDD)	3.0	3.3	3.6	V
DAC Supply Voltage (DACVDD)	3.0	3.3	3.6	V
Auxiliary Supply Voltage (AUXVDD)	3.0	3.3	3.6	V
Clock Supply Voltage (CLKVDD)	3.0	3.3	3.6	V
Digital Supply Voltage (DVDD)	2.7	3.3	3.6	V
Driver Supply Voltage (DRVDD)	2.7	3.3	3.6	V
ANALOG SUPPLY CURRENTS				
ADCVDD (Nominal Bias)		104	114	mA
DACVDD (20 mA Full-Scale Outputs)		68	73	mA
AUXVDD		2	3	mA
CLKVDD		2	3.5	mA
DIGITAL SUPPLY CURRENTS[1]				
DVDD (Tx Mode)		116	140	mA
DVDD (Rx Mode)		107	135	mA
DRVDD (Tx Mode)		5		mA
DRVDD (Rx Mode) with C_{LOAD} = 5 pF[2]		5		mA

[1] Rx digital and analog path configured for bypass mode.
[2] DRVDD in Rx mode is dependent on ADIO bus load capacitance.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%.

Table 5. Digital Logic Levels

Parameter	Min	Typ	Max	Unit
CMOS LOGIC INPUTS				
High Level Input Voltage	DRVDD – 0.7			V
Low Level Input Voltage			0.4	V
Input Leakage Current			12	µA
Input Capacitance		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)				
High Level Output Voltage (I_{OH} = 1 mA)	DRVDD – 0.7			V
Low Level Output Voltage (I_{OH} = 1 mA)			0.4	V
Output Rise/Fall Time (High Strength Mode and C_{LOAD} = 5 pF)		0.7/0.7		ns
Output Rise/Fall Time (Low Strength Mode and C_{LOAD} = 5 pF)		1.0/1.0		ns
RESET				
Minimum Low Pulse Width (Relative to f_{ADC})	1			Clock cycles

Table 6. CLKIN Timing Specifications

Parameter	Min	Typ	Max	Unit
INPUT CLOCK				
CLKIN Clock Rate with 2× CLK Multiplier	16		32	MHz
CLKIN Clock Rate without 2× CLK Multiplier	4		64	MHz
CLKIN Pulse Width High	12.5			ns
CLKIN Pulse Width Low	12.5			ns

Table 7. ADIO Port Timing Specifications

Parameter	Min	Typ	Max	Unit
READ OPERATION[1]				
Output Data Rate	2		64	MSPS
Three-State Output Enable Time (t_{PZL})		3		ns
Three-State Output Disable Time (t_{PLZ})		3		ns
Rx Data Valid Time (t_{VT})		1.5		ns
Rx Data Output Delay (t_{OD})		4		ns
WRITE OPERATION				
Tx Data Setup Time (t_{DS})		1		ns
Tx Data Hold Time (t_{DH})		2.5		ns
Latch Enable Time (t_{EN})		3		ns
Latch Disable Time (t_{DIS})		3		ns

[1] C_{LOAD} = 5 pF for digital data outputs.

Table 8. Serial Port Timing Specifications

Parameter	Min	Typ	Max	Unit
WRITE OPERATION				
SCLK Clock Rate (f_{SCLK})			32	MHz
SCLK Clock High (t_{HI})		14		ns
SCLK Clock Low (t_{LOW})		14		ns
SDIO to SCLK Setup Time (t_{DS})		14		ns
SCLK to SDIO Hold Time (t_{DH})		0		ns
$\overline{SEN}$ to SCLK Setup Time (t_S)		14		ns
SCLK to $\overline{SEN}$ Hold Time (t_H)		0		ns
READ OPERATION				
SCLK Clock Rate (f_{SCLK})			32	MHz
SCLK Clock High (t_{HI})		14		ns
SCLK Clock Low (t_{LOW})		14		ns
SDIO to SCLK Setup Time (t_{DS})		14		ns
SCLK to SDIO Hold Time (t_{DH})		0		ns
SCLK to SDIO (or SDO) Data Valid Time (t_{DV})		14		ns
$\overline{SEN}$ to SDIO Output Valid to High-Z (t_{EZ})		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
ELECTRICAL	
AVDD, CLKVDD Voltage	3.9 V maximum
DVDD, DRVDD Voltage	3.9 V maximum
VIN_I+, VIN_I–, VIN_Q+, VIN_Q–	–0.3 V to AVDD + 0.3 V
REFT, REFB	–0.3 V to AVDD + 0.3 V
IOUT_I+, IOUT_I–, IOUT_Q+, IOUT_Q–	–1.5 V to AVDD + 0.3 V
AUXADC	–0.3 V to AVDD + 0.3 V
AUXDAC	–0.3 V to AVDD + 0.3 V
CLKIN	–0.3 V to CLVDD + 0.3 V
REFIO, FSADJ	–0.3 V to AVDD + 0.3 V
Digital Input and Output Voltage	–0.3 V to DRVDD + 0.3 V
Digital Output Current	5 mA maximum
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	–40°C to +85°C
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec)	150°C
Storage Temperature Range (Ambient)	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 10. Thermal Resistance

Package Type	θ_{JA}	Unit
80-Lead LQFP (4-Layer Board)	38.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

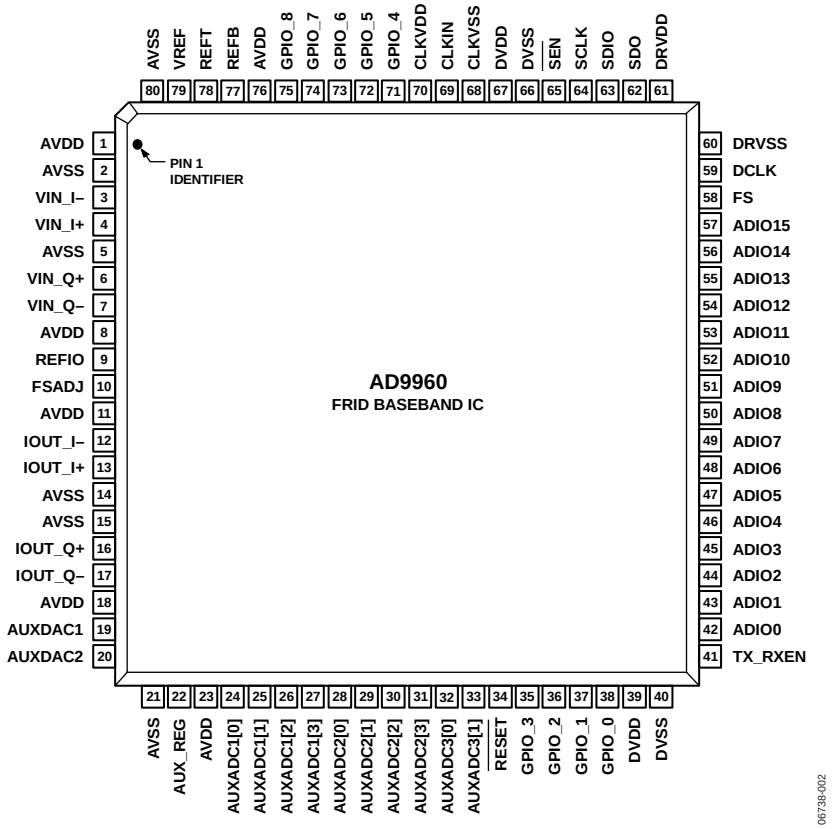

Figure 2. AD9960 Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 11, 18, 23, 76	AVDD	Analog Supply Input
2, 5, 14, 15, 21, 80	AVSS	Analog Supply Return
3, 4	VIN_I–, VIN_I+	I-Channel Differential Voltage Rx Input
6, 7	VIN_Q+, VIN_Q–	Q-Channel Differential Voltage Rx Input
9	REFIO	I and Q TxDACs Reference Input/Output
10	FSADJ	I and Q TxDACs Full-Scale Current Adjust
12, 13	IOUT_I–, IOUT_I+	I TxDAC Differential Current Output
16, 17	IOUT_Q+, IOUT_Q–	Q TxDAC Differential Current Output
19, 20	AUXDAC1, AUXDAC2	Voltage Output of Auxiliary DACs
22	AUX_REG	Regulator Output that Sets Full-Scale Span for All Auxiliary ADCs and DACs
24 to 27	AUXADC1[0] to AUXADC1[3]	Voltage Inputs to Auxiliary 4-Channel Muxed ADC1
28 to 31	AUXADC2[0] to AUXADC2[3]	Voltage Inputs to Auxiliary 4-Channel Muxed ADC2
32 to 33	AUXADC3[0] to AUXADC3[1]	Voltage Inputs to Auxiliary 2-Channel Muxed ADC3
34	$\overline{\text{RESET}}$	Reset Input (Active Low)
35	GPIO_3	General-Purpose Input/Output (or Single-Bit Tx Mode Data Input)
36	GPIO_2	General-Purpose Input/Output (or Single-Bit Tx Mode Clock Output)
37	GPIO_1	General-Purpose Input/Output (or TI DSP Interface Control Output)
38	GPIO_0	General-Purpose Input/Output (or TI DSP Interface Control Output)
39, 67	DVDD	Digital Supply Input
40, 66	DVSS	Digital Supply Return

Pin No.	Mnemonic	Description
41	TX_RXEN	Half-Duplex Tx/Rx Digital Bus Control Input
42	ADIO0	Bit 0 (LSB) of 16-Bit Bidirectional ADIO Buffer
43 to 56	ADIO1 to ADIO14	Bit 1 to Bit 14 of 16-Bit Bidirectional ADIO Buffer
57	ADIO15	Bit 15 (MSB) of 16-Bit Bidirectional ADIO Buffer
58	FS	Frame Sync Pulse Output (indicates start of when valid I/Q is placed on bus for DSP)
59	DCLK	Digital Clock Output to DSP (equal to ADIO data rate)
60	DRVSS	Digital I/O Supply Return
61	DRVDD	Digital I/O Supply Input
62	SDO	Serial Port Data Output
63	SDIO	Serial Port Data Input/Output
64	SCLK	Serial Port Clock Input
65	$\overline{\text{SEN}}$	Serial Port Enable Input (Active Low)
68	CLKVSS	Clock Supply Return
69	CLKIN	Clock Input
70	CLKVDD	Clock Supply Input
71	GPIO_4	General-Purpose Input/Output (or ADC Overload Output)
72 to 75	GPIO_5 to GPIO_8	General-Purpose Input/Outputs
77, 78	REFB, REFT	ADC Reference Decoupling
79	VREF	ADC Reference Input/Output

OUTLINE DIMENSIONS

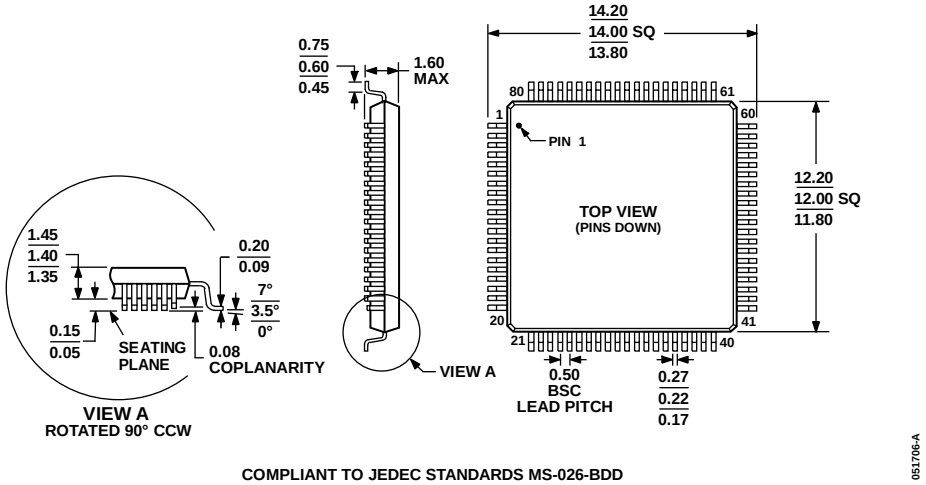

Figure 3. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9960BSTZ[1]	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1
AD9960BSTZRL[1]	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1

[1] Z = RoHS Compliant Part.

NOTES