# Quad, 12-Bit, 4 GSPS RF ADC

Preliminary Technical Data

# AD9209

## FEATURES

- Flexible reconfigurable common platform design
  - Supports single, dual, and quad band
  - Datapaths and DSP blocks are fully bypassable
  - ADC sample rate ratios of 1, 2, 3, and 4
  - On-chip PLL with multichip synchronization
    - External RF clock input option for off-chip PLL
- Maximum ADC sample rate up to 4 GSPS
  - Maximum data rate up to 4 GSPS using JESD204C
  - Useable analog bandwidth to 8 GHz
- Buffered input with −3 dB bandwidth ≥ 7.5 GHz
  - Full-scale of 1.4 V p-p with $R_{IN}$ = 100 Ω
  - Overload protection clamp
  - Supports dc coupled with common-mode feedback
- ADC ac performance at 4 GSPS
  - Noise density: −151.5 dBFS/Hz
  - Noise figure: 26.8 dB
  - HD2: −67 dBFS at 2.7 GHz
  - HD3: −74 dBFS at 2.7 GHz
  - Worst other (excluding HD2 and HD3): −82 dBFS at 2.7 GHz
- Versatile digital features
  - Selectable decimation filters
  - Configurable digital down conversion (DDC)
    - 8 fine complex DDCs and 4 coarse complex DDCs
    - 48-bit numerically controlled oscillator (NCO) per DDC
    - Option to bypass fine and coarse DDC
  - Programmable 192 tap programmable filter (PFIR) for receive equalization
    - Supports 4 different profile settings loaded via GPIO
  - Programable delay per data path
  - Receive automatic gain control (AGC) support
    - Fast detect with low latency for fast AGC control
    - Signal monitor for slow AGC control
    - Dedicated AGC support pins
- Auxiliary features
  - Fast frequency hopping
  - ADC clock driver with selectable divide ratios
  - On-chip temperature monitoring unit
  - Flexible GPIOx pins
- SERDES JESD204B/JESD204C interface, 16 lanes up to 24.75 Gbps
  - 8 lanes per ADCs
  - JESD204B compatible with the maximum 15.5 Gbps lane rate
  - JESD204C compatible with the maximum 24.75 Gbps lane rate
  - Supports real or complex digital data (8-bit, 12-bit, 16-bit, or 24-bit)
- 15 mm × 15 mm, 324-ball BGA with 0.8 mm pitch

## APPLICATIONS

- Wireless communications infrastructure
- Microwave point-to-point, E-band, and 5G mm wave
- Broadband communications systems
- Data over cable service interface specification (DOCSIS) 3.1 and 4.0 cable modem termination system (CMTS)
- Phased array radar and electronic warfare
- Electronic test and measurement systems

## GENERAL DESCRIPTION

The AD9209 is a quad, 12-bit, 4 GSPS analog-to-digital converter (ADC). The ADC input features an on-chip wideband buffer with overload protection. This product is designed to support communications applications capable of direct sampling wideband signals with a range up to 7.5 GHz. An optional low phase noise phase-locked loop (PLL) clock synthesizer is available to generate the ADC sampling clock, simplifying printed circuit board (PCB) distribution of a high frequency clock signal. Alternatively, the CLKIN of the device can be driven directly with the ADC sampling clock (or a higher version up to 12 GHz when the internal clock divider is enabled). An optional CLKOUT buffer is available to transmit the ADC sampling clock to other devices.

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Document Feedback


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# FUNCTIONAL BLOCK DIAGRAM

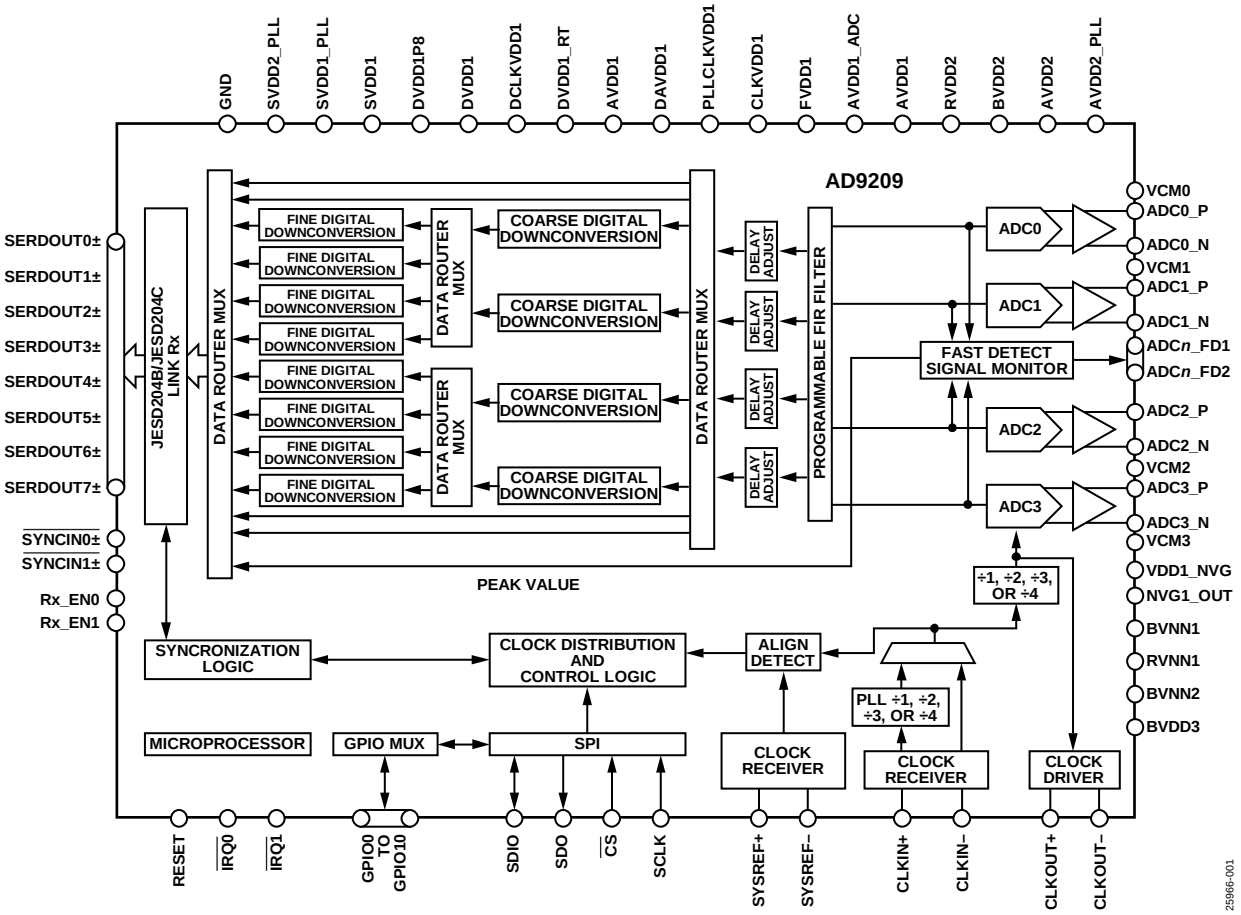



*Figure 1.*

# ABSOLUTE MAXIMUM RATINGS

**Table 1.**

| Parameter | Rating |
|---|---|
| ISET, DACxP, DACxN, TDP, TDN | −0.3 V to AVDD2 + 0.3 V |
| VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG | −0.3 V to AVDD2_PLL + 0.3 V |
| ADC0P, ADC0N, ADC1P, ADC1N, ADC2P, ADC2N, ADC3P, ADC3N | −0.3 V to BVDD2 + 0.3 V |
| VCM0, VCM1 | −0.3 V to RVDD2 + 0.3 V |
| CLKINP, CLKINN | −0.2 V to PLLCLKVDD1 + 0.2 V |
| ADCDRVN, ADCDRVP | −0.2 V to CLKVDD1 + 0.2 V |
| SERDINx±, SERDOUTx± | −0.2 V to SVDD1 + 0.2 V |
| SYSREFP, SYSREFN, and $\overline{\text{SYNCxIN±}}$ | −0.2 V to +2.5 V |
| $\overline{\text{SYNCxOUT±}}$, $\overline{\text{SYNCxIN±}}$, $\overline{\text{RESET}}$, TXENx, RXENx, $\overline{\text{IRQ\_x}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, ADCx_SMON0, ADCx_SMON1, ADCx_FD0, ADCx_FD1, GPIOx | −0.3 V to DVDD1P8 + 0.3 V |
| AVDD2, AVDD2_PLL, BVDD2, RVDD2, SVDD2_PLL, DVDD1P8 | −0.3 V to +2.2 V |
| PLLCLKVDD1, AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, DAVDD1, DVDD1_RT, DCLKVDD1, SVDD1, SVDD1_PLL | −0.2 V to +1.2 V |
| VNN1 | −1.1 V to +0.2 V |
| Temperature | |
| Maximum Junction ($T_J$)[1] | 120°C |
| Storage Range | −40°C to +150°C |

[1] Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## REFLOW PROFILE

The AD9209 reflow profile is in accordance with the JEDEC JESD 20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum $T_J$ does not exceed the limits shown in Table 1.

$\theta_{JA}$ is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

$\theta_{JC\_TOP}$ is the junction-to-case thermal resistance.

$\theta_{JB}$ is the junction-to-board thermal resistance.

**Table 2. Thermal Resistance[1]**

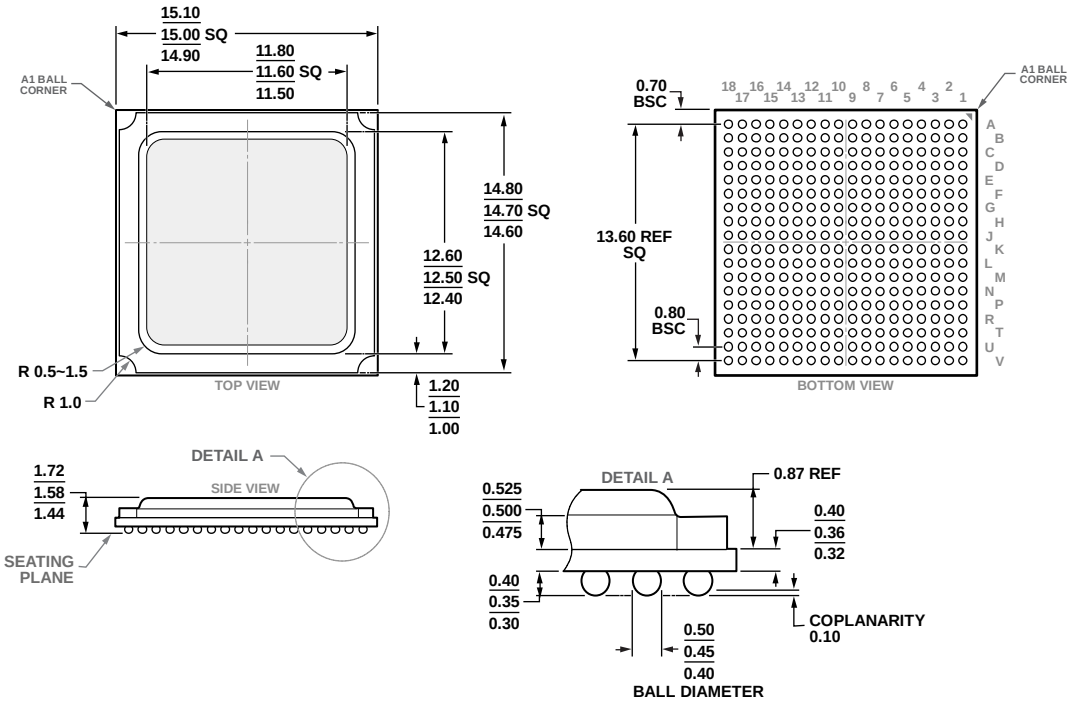
| Package Type | Airflow Velocity (m/sec) | $\theta_{JA}$ | $\theta_{JC\_TOP}$ | $\theta_{JB}$ | Unit |
|---|---|---|---|---|---|
| BP-324-3 | 0.0 | 11.7 | 0.40 | 2.3 | °C/W |

[1] Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-1**

*Figure 2. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]*
*(BP-324-3)*
*Dimensions shown in millimeters*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