

FEATURES**Flexible reconfigurable common platform design**

- 4 DAC cores connected to various DSP and bypass datapaths

- Supports single, dual, and quad band

- Datapaths and DSP blocks are fully bypassable

- On-chip PLL with multichip synchronization

- External RF clock input option for off chip PLL

Maximum DAC sample rate up to 12 GSPS

- Maximum data rate up to 12 GSPS using JESD204C

- Useable analog bandwidth to 8 GHz

DAC ac performance at 12 GSPS

- Full-scale output current range: 7 mA to 40 mA

- Two tone IMD3 (–7 dBFS per tone): –78.9 dBc

- Noise spectral density (NSD), single tone at 3.7 GHz: –155.1 dBc/Hz

- Spurious free dynamic range (SFDR), single tone at 3.7 GHz: –70 dBc

Versatile digital features

- Selectable interpolation filters

- Configurable digital up conversion (DUC)

- 8 fine complex DUCs and 4 coarse complex DUCs

- 48-bit numerically controlled oscillator (NCO) per DUC

- Option to bypass fine and coarse DUC

- Programmable 192 tap PFIR filter for receive equalization

- Supports 4 different profile settings loaded via GPIO

- Programable delay per data path

- Receive automatic gain control (AGC) support

- Fast detect with low latency for fast AGC control

- Signal monitor for slow AGC control

- Dedicated AGC support pins

- Transmit digital predistortion (DPD) support

- Fine DUC channel gain control and delay adjust

Auxiliary features

- Fast frequency hopping

- Direct digital synthesis (DDS)

- Low latency digital loopback mode (receive datapath

- NCOs can be routed to transmit datapaths)

- Power amplifier downstream protection circuitry

- On-chip temperature monitoring unit

- Flexible GPIOx pins

- TDD power savings option

- SERDES JESD204B/JESD204C interface

- 8 lanes up to 24.75 Gbps

- JESD204B compatible with the maximum 15.5 Gbps

- JESD204C compatible with the maximum 24.75 Gbps

- Supports real or complex digital data (8-bit, 12-bit, 16-bit, or 24-bit)

- 15 mm × 15 mm, 324-ball BGA with 0.8 mm pitch

APPLICATIONS

- Wireless communications infrastructure

- Microwave point-to-point, E-band, and 5G mm wave

- Broadband communications systems

- Data over cable service interface specification (DOCSIS) 3.1 and 4.0 cable modem termination system (CMTS)

- Phased array radar and electronic warfare

- Electronic test and measurement systems

GENERAL DESCRIPTION

The AD9177 is a highly integrated device with four, 16-bit, 12 GSPS maximum sample rate, RF digital-to-analog converter (DAC) cores, supporting up to eight baseband channels. The device is well suited for applications requiring wideband DACs to process signal(s) of wide instantaneous bandwidth. The device features an 8 lane, 24.75 Gbps JESD204C or 15.5 Gbps JESD204B data receiver port, an on-chip clock multiplier, and digital signal processing (DSP) features targeted at either wideband or multiband direct to RF applications. The DSP datapaths may be bypassed to allow a direct connection between the DAC cores and the data receiver port. The device also features frequency hopping modes and datapath mux configurations useful for phase array radar systems and electronic warfare applications.

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FUNCTIONAL BLOCK DIAGRAM

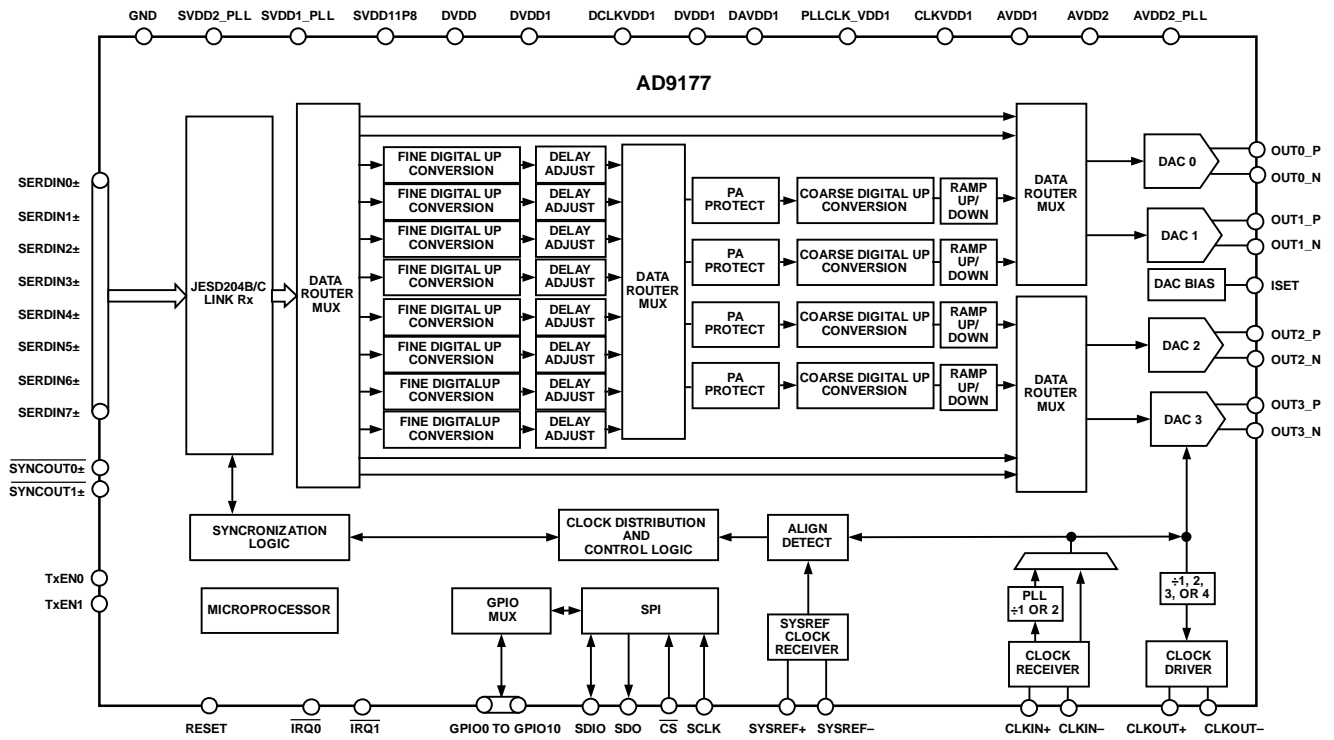


Figure 1.

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ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
ISET, DACxP, DACxN, TDP, TDN	−0.3 V to AVDD2 + 0.3 V
VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG	−0.3 V to AVDD2_PLL + 0.3 V
CLKINP, CLKINN	−0.2 V to PLLCLKVDD1 + 0.2 V
ADCDRVN, ADCDRVp	−0.2 V to CLKVDD1 + 0.2 V
SERDINx±	−0.2 V to SVDD1 + 0.2 V
SYSREFP, SYSREFN	−0.2 V to +2.5 V
SYNCxOUT±, SYNCxIN±, RESET, TXENx, IRQx, CS, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, GPIOx	−0.3 V to DVDD1P8 + 0.3 V
AVDD2, AVDD2_PLL, SVDD2_PLL, DVDD1P8	−0.3 V to +2.2 V
PLLCLKVDD1, AVDD1, CLKVDD1, FVDD1, DAVDD1, DCLKVDD1, SVDD1, SVDD1_PLL	−0.2 V to +1.2 V
Temperature	
Maximum Junction (T _J) ¹	120°C
Storage Range	−40°C to +150°C

¹ Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9177 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T_J does not exceed the limits shown in Table 1.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_TOP} is the junction-to-case thermal resistance.

θ_{JB} is the junction-to-board thermal resistance.

Table 2. Thermal Resistance¹

Package Type	Airflow Velocity (m/sec)	θ _{JA}	θ _{JC_TOP}	θ _{JB}	Unit
BP-324-3	0.0	11.7	0.40	2.3	°C/W

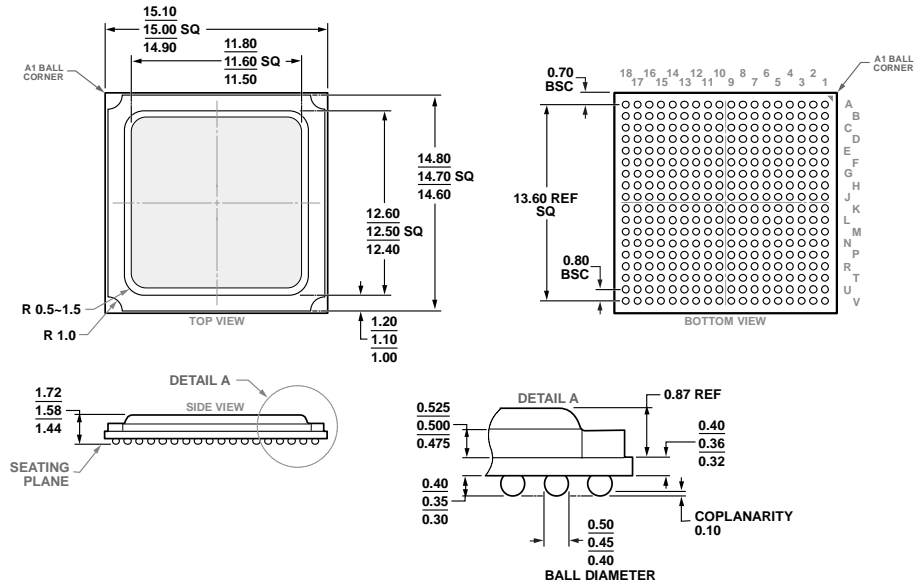
¹ Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-1
 Figure 2. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
 (BP-324-3)
 Dimensions shown in millimeters