

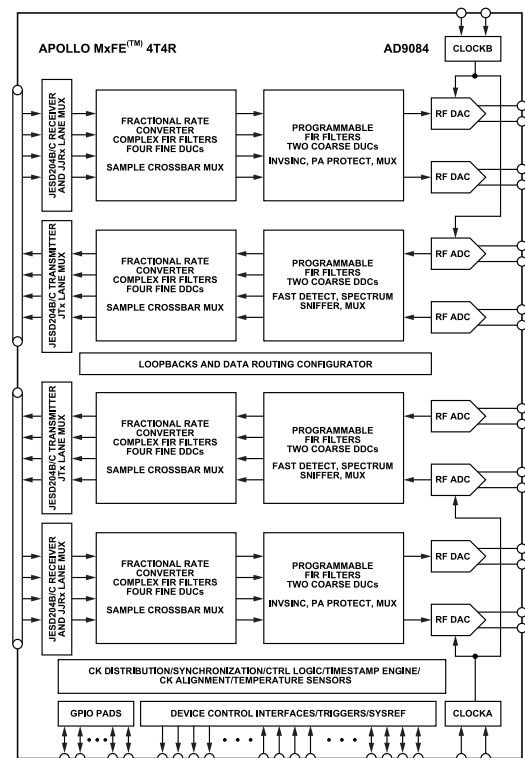
Apollo MxFE Quad, 16-Bit, 28 GSPS RF DAC and Quad, 12-Bit, 20 GSPS RF ADC
FEATURES

- ▶ Flexible reconfigurable common platform design
 - ▶ 4 DACs and 4 ADCs (4D4A)
 - ▶ Usable RF Analog bandwidth up to 18 GHz
 - ▶ Maximum DAC/ADC sample rate up to 28 GSPS/20 GSPS
- ▶ DAC to ADC sample rate ratios of 1 and 2
 - ▶ Clocking
 - ▶ On-chip PLL (7 GHz to 14 GHz)
- ▶ External RFCLK input up to 20 GHz
- ▶ Multichip synchronization via subclass1
- ▶ Single-ended (SE) or differential (DIFF) ADC inputs
 - ▶ Two separate versions, both 50 Ω input impedance
 - ▶ Single-ended version with on-chip wide bandwidth balun
- ▶ Differential ADC AC performance at 20 GSPS
 - ▶ Full-scale input voltage: 500 mV p-p/-2 dBm
 - ▶ Noise density: -150 dBFS/Hz at -20 dBFS at 2 GHz
 - ▶ HD2/HD3: -65 dBFS/-70 dBFS at -7 dBFS at 2 GHz
 - ▶ IMD3: -75 dBFS at -13 dBFS/tone at 2 GHz
- ▶ DAC AC performance at 28 GSPS
 - ▶ Full-scale output power: -2.1 dBm at 2 GHz
 - ▶ IMD3: -75 dBc at -13 dBFS/tone at 2 GHz to 10 GHz
 - ▶ NSD (shuffling disabled): -164 dBFS/Hz at 0 dBFS at 2 GHz
- ▶ Versatile digital features
 - ▶ Supports real or complex digital data (8-, 12-, 16-bit)
 - ▶ Configurable DDC and DUC
 - ▶ 8 fine complex DUCs and 4 coarse complex DUCs
 - ▶ 8 fine complex DDCs and 4 coarse complex DDCs
 - ▶ Option to bypass fine and coarse DUC/DDC
 - ▶ DUC/DDC alias rejection
 - ▶ 85 dB for interpolation filters
 - ▶ 100 dB for decimation filters
 - ▶ Fractional sample rate converter (FSRC)
- ▶ Programmable FIR filters for transmit/receive
- ▶ Multiple loopback (ADC to DAC) supported
 - ▶ ~45 ns without DSP path
- ▶ Dynamic configuration through SPI/HSCI/GPIO
- ▶ Spectrum sniffer/monitor
- ▶ Interfaces
 - ▶ SPI
 - ▶ High-Speed Control Interface (HSCI)
 - ▶ JESD204B/JESD204C: 20 Gbps/32.5 Gbps
- ▶ 24 lanes for Rx, 24 lanes for Tx
- ▶ Receive AGC support

- ▶ Fast detect with low latency for fast AGC control
- ▶ Signal monitor for slow AGC control
- ▶ Auxiliary features
 - ▶ Power amplifier downstream protection circuitry
 - ▶ On-chip temperature monitoring unit
 - ▶ TDD power savings option
- ▶ Total power consumption range dependent on device configuration : 20 W to 30 W
- ▶ 24 mm × 26 mm, 899-ball BGA with 0.8 mm pitch
- ▶ Operating junction temperature (T_J): -40°C to +110°C

APPLICATIONS

- ▶ Radar and communications
 - ▶ L/S/C/X/Ku band radar and electronic warfare
 - ▶ Phase array system
 - ▶ Broadband communications systems
- ▶ Electronic test and measurement systems
- ▶ Satellite communications
- ▶ Microwave point-to-point, X-band and 5G mmWave

FUNCTIONAL BLOCK DIAGRAM

Figure 1. Functional Block Diagram

Rev. PrA

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

Information furnished by Analog Devices is believed to be accurate and reliable "as is". However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

GENERAL DESCRIPTION

The Apollo mixed signal front-end (MxFE[®]) is a highly integrated device with a 16-bit, 28 GSPS maximum sample rate, RF digital-to-analog converter (DAC) core, and 12-bit, 20 GSPS maximum sample rate, RF analog-to-digital converter (ADC) core. The AD9084 supports four transmit channels and four receive channels. The AD9084 is well suited for applications requiring both wideband ADCs and DACs to process signal(s) having wide instantaneous bandwidth. The device features a 48 lane, 32.5 Gbps JESD204C or 20 Gbps JESD204B data transceiver port, an on-chip clock multiplier, and a digital signal processing (DSP) capability targeted

at either wideband or multiband, direct to RF applications. The AD9084 also features a bypass mode that allows the full bandwidth capability of the ADC and/or DAC cores to bypass the DSP data-paths. The device also features low latency loopback and frequency hopping modes targeted at phased array radar systems and electronic warfare applications.

The AD9084 is available in a 24 mm x 26 mm, 899-ball BGA and operates within the -40°C to +110°C junction temperature range. For additional information, contact ApolloSupport@analog.com.

Table 1. Product Listing with Distinguishing Features

Part No.	Tx				Rx				Digital Features						
	DAC Ch	Max DAC Rate (GSPS)	Min Interp Ratio	Max Tx BW (GHz)	ADC Ch	Max ADC Rate (GSPS)	Min Dec Ratio	Max Rx BW (GHz)	Input Network	FSRC	Rx to Tx Loopback	Fast Freq Hopping	PFILT CFIR	Dynamic Config (PFILT CFIR, DDC/DUC)	Spectrum Sniffer
AD9084-DF	4	28	1x	14	4	20	1x	10	DIFF	Yes	Yes	Yes	Yes	Yes	Yes
AD9084-SE	4	28	1x	14	4	14	1x	7	SE	Yes	Yes	Yes	Yes	Yes	Yes
AD9088	8	16	1x	8	8	8	1x	4	SE	No	Yes	Yes	Yes	Yes	Yes

OUTLINE DIMENSIONS

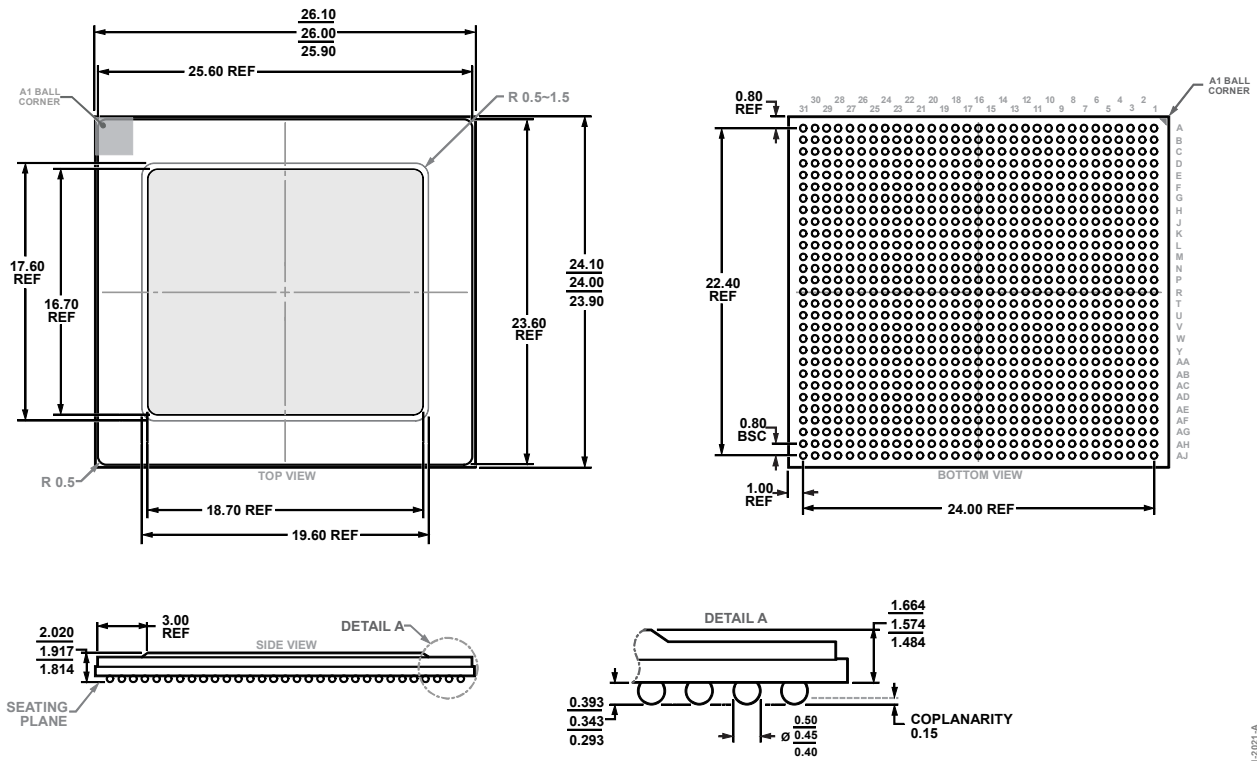


Figure 2. 899-Ball (29 x 31) Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-899-1)
Dimensions shown in millimeters