LC²MOS Quad 14-Bit DACs

AD7834/AD7835

FEATURES

Four 14-bit DACs in one package
AD7834—serial loading
AD7835—parallel 8-bit/14-bit loading
Voltage outputs
Power-on reset function
Maximum/minimum output voltage range of ±8.192 V
Maximum output voltage span of 14 V
Common voltage reference inputs
User-assigned device addressing
Clear function to user-defined voltage
Surface-mount packages
AD7834—28-lead SOIC and PDIP
AD7835—44-lead MQFP and PLCC

APPLICATIONS

Process control
Automatic test equipment
General-purpose instrumentation

GENERAL DESCRIPTION

The AD7834 and AD7835 contain four 14-bit DACs on one monolithic chip. The AD7834 and AD7835 have output voltages in the range ±8.192 V with a maximum span of 14 V.

The AD7834 is a serial input device. Data is loaded in 16-bit format from the external serial bus, MSB first after two leading 0s, into one via DIN, SCLK, and $\overline{\text{FSYNC}}$. The AD7834 has five dedicated package address pins, PA0 to PA4, that can be wired to AGND or V_{CC} to permit up to 32 AD7834s to be individually addressed in a multipackage application.

The AD7835 can accept either 14-bit parallel loading or double-byte loading, where right-justified data is loaded in one 8-bit byte and one 6-bit byte. Data is loaded from the external bus into one of the input latches under the control of the $\overline{\text{WR}}$, $\overline{\text{CS}}$, $\overline{\text{BYSHF}}$, and DAC channel address pins, A0 to A2.

With each device, the $\overline{\text{LDAC}}$ signal is used to update all four DAC outputs simultaneously, or individually, on reception of new data. In addition, for each device, the asynchronous $\overline{\text{CLR}}$ input can be used to set all signal outputs, $V_{OUT}1$ to $V_{OUT}4$, to the user-defined voltage level on the device sense ground pin, DSG. On power-on, before the power supplies have stabilized, internal circuitry holds the DAC output voltage levels to within ±2 V of the DSG potential. As the supplies stabilize, the DAC output levels move to the exact DSG potential (assuming $\overline{\text{CLR}}$ is exercised).

The AD7834 is available in a 28-lead 0.3" SOIC package and a 28-lead 0.6" PDIP package, and the AD7835 is available in a 44-lead MQFP package and a 44-lead PLCC package.

FUNCTIONAL BLOCK DIAGRAMS

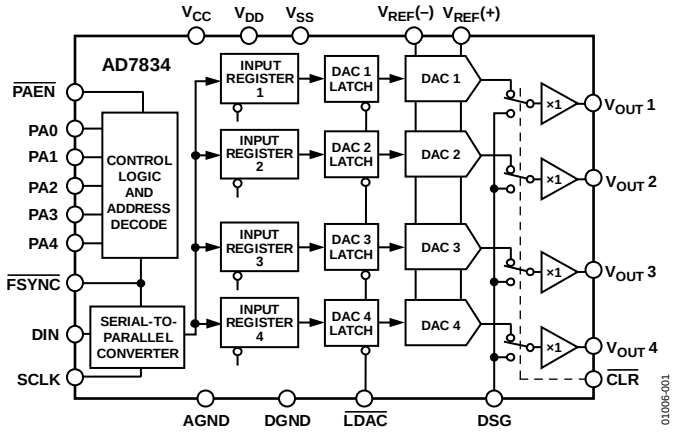

Figure 1. AD7834

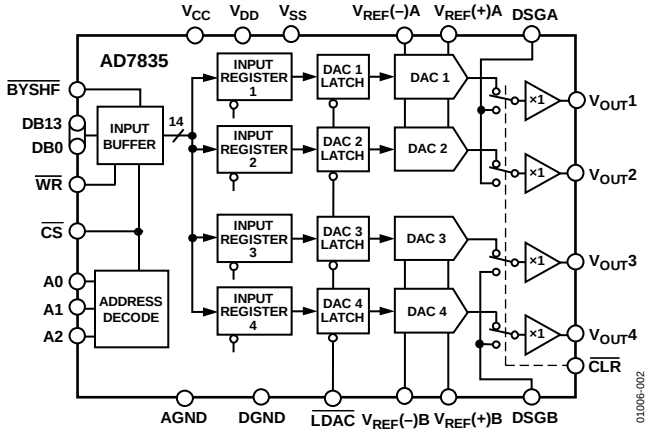

Figure 2. AD7835

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REVISION HISTORY

8/07—Rev. C to Rev. D

Changes to Table 5 ... 7
Added Table 6 ... 7
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7/05—Rev. B to Rev. C

Updated Format ... Universal
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7/03—Rev. A to Rev. B

Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5 V ± 5%; V_{DD} = 15 V ± 5%; V_{SS} = −15 V ± 5%; AGND = DGND = 0 V; T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A	B	S	Unit	Test Conditions/Comments
ACCURACY					
Resolution	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed monotonic over temperature.
Full-Scale Error					$V_{REF}(+)$ = +7 V, $V_{REF}(-)$ = −7 V.
T_{MIN} to T_{MAX}	±5	±5	±8	mV max	
Zero-Scale Error	±4	±4	±5	mV max	$V_{REF}(+)$ = +7 V, $V_{REF}(-)$ = −7 V.
Gain Error	±0.5	±0.5	±0.5	mV typ	$V_{REF}(+)$ = +7 V, $V_{REF}(-)$ = −7 V.
Gain Temperature Coefficient[2]	4	4	4	ppm FSR/°C typ	
	20	20	20	ppm FSR/°C max	
DC Crosstalk[2]	50	50	50	µV max	See the Terminology section. R_L = 10 kΩ.
REFERENCE INPUTS					
DC Input Resistance	30	30	30	MΩ typ	
Input Current	±1	±1	±1	µA max	Per input.
$V_{REF}(+)$ Range	0/8.192	0/8.192	0/8.192	V min/max	
$V_{REF}(-)$ Range	−8.192/0	−8.192/0	−8.192/0	V min/max	
$V_{REF}(+) - V_{REF}(-)$	5/14	7/14	5/14	V min/max	For specified performance. Can go as low as 0 V, but performance is not guaranteed.
DEVICE SENSE GROUND INPUTS					
Input Current	±2	±2	±2	µA max	Per input. V_{DSG} = −2 V to +2 V.
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	µA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
POWER REQUIREMENTS					
V_{CC}	5.0	5.0	5.0	V nom	±5% for specified performance.
V_{DD}	15.0	15.0	15.0	V nom	±5% for specified performance.
V_{SS}	−15.0	−15.0	−15.0	V nom	±5% for specified performance.
Power Supply Sensitivity					
ΔFull Scale/ΔV_{DD}	110	110	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	100	100	dB typ	
I_{CC}	0.2	0.2	0.5	mA max	V_{INH} = V_{CC}, V_{INL} = DGND.
	3	3	3	mA max	AD7834: V_{INH} = 2.4 V min, V_{INL} = 0.8 V max.
	6	6	6	mA max	AD7835: V_{INH} = 2.4 V min, V_{INL} = 0.8 V max.
I_{DD}	13	13	15	mA max	AD7834: outputs unloaded.
	15	15	15	mA max	AD7835: outputs unloaded.
I_{SS}	13	13	15	mA max	Outputs unloaded.

[1] Temperature range for A, B, and C versions is −40°C to +85°C.
[2] Guaranteed by design.

V_{CC} = 5 V ± 5%; V_{DD} = 12 V ± 5%; V_{SS} = −12 V ± 5%; AGND = DGND = 0 V; T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A	B	S	Unit	Test Conditions/Comments
ACCURACY					
Resolution	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed monotonic over temperature.
Full-Scale Error					$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = −5 V.
T_{MIN} to T_{MAX}	±5	±5	±8	mV max	
Zero-Scale Error	±4	±4	±5	mV max	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = −5 V.
Gain Error	±0.5	±0.5	±0.5	mV typ	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = −5 V.
Gain Temperature Coefficient[2]	4	4	4	ppm FSR/°C typ	
	20	20	20	ppm FSR/°C max	
DC Crosstalk[2]	50	50	50	µV max	See the Terminology section. R_L = 10 kΩ.
REFERENCE INPUTS					
DC Input Resistance	30	30	30	MΩ typ	
Input Current	±1	±1	±1	µA max	Per input.
$V_{REF}(+)$ Range	0/8.192	0/8.192	0/8.192	V min/max	
$V_{REF}(-)$ Range	−5/0	−5/0	−5/0	V min/max	
$V_{REF}(+) - V_{REF}(-)$	5/13.192	7/13.192	5/13.192	V min/max	For specified performance. Can go as low as 0 V, but performance is not guaranteed.
DEVICE SENSE GROUND INPUTS					
Input Current	±2	±2	±2	µA max	Per input. V_{DSG} = −2 V to +2 V.
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	µA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
POWER REQUIREMENTS					
V_{CC}	5.0	5.0	5.0	V nom	±5% for specified performance.
V_{DD}	15.0	15.0	15.0	V nom	±5% for specified performance.
V_{SS}	−15.0	−15.0	−15.0	V nom	±5% for specified performance.
Power Supply Sensitivity					
ΔFull Scale/ΔV_{DD}	110	110	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	100	100	dB typ	
I_{CC}	0.2	0.2	0.5	mA max	V_{INH} = V_{CC}, V_{INL} = DGND.
	3	3	3	mA max	AD7834: V_{INH} = 2.4 V min, V_{INL} = 0.8 V max.
	6	6	6	mA max	AD7835: V_{INH} = 2.4 V min, V_{INL} = 0.8 V max.
I_{DD}	13	13	15	mA max	AD7834: outputs unloaded.
	15	15	15	mA max	AD7835: outputs unloaded.
I_{SS}	13	13	15	mA max	Outputs unloaded.

[1] Temperature range for A, B, and C versions is −40°C to +85°C.
[2] Guaranteed by design.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance and are not subject to production testing.

Table 3.

Parameter	A	B	S	Unit (typ)	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time	10	10	10	µs	Full-scale change to ±1/2 LSB. DAC latch contents alternately loaded with all 0s and all 1s.
Digital-to-Analog Glitch Impulse	120	120	120	nV-s	Measured with $V_{REF}(+) = V_{REF}(-) = 0$ V. DAC latch alternately loaded with all 0s and all 1s.
DC Output Impedance	0.5	0.5	0.5	Ω	See the Terminology section.
Channel-to-Channel Isolation	100	100	100	dB	See the Terminology section; applies to the AD7835 only.
DAC-to-DAC Crosstalk	25	25	25	nV-s	See the Terminology section.
Digital Crosstalk	3	3	3	nV-s	Feedthrough to DAC output under test due to change in digital input code to another converter.
Digital Feedthrough—AD7834	0.2	0.2	0.2	nV-s	Effect of input bus activity on DAC output under test.
Digital Feedthrough—AD7835	1.0	1.0	1.0	nV-s	
Output Noise Spectral Density at 1 kHz	40	40	40	nV/√Hz	All 1s loaded to DAC. $V_{REF}(+) = V_{REF}(-) = 0$ V.

TIMING SPECIFICATIONS

V_{CC} = 5 V ± 5%; V_{DD} = 11.4 V to 15.75 V; V_{SS} = −11.4 V to −15.75 V; AGND = DGND = 0 V[1].

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
AD7834-SPECIFIC			
t_1[2]	100	ns min	SCLK cycle time
t_2[2]	50	ns min	SCLK low
t_3[2]	30	ns min	SCLK high time
t_4	30	ns min	$\overline{FSYNC}$, $\overline{PAEN}$ setup time
t_5	40	ns min	$\overline{FSYNC}$, $\overline{PAEN}$ hold time
t_6	30	ns min	Data setup time
t_7	10	ns min	Data hold time
t_8	0	ns min	$\overline{LDAC}$ to $\overline{FSYNC}$ setup time
t_9	40	ns min	$\overline{LDAC}$ to $\overline{FSYNC}$ hold time
t_{21}	20	ns min	Delay between write operations
AD7835-SPECIFIC			
t_{11}	15	ns min	A0, A1, A2, $\overline{BYSHF}$ to $\overline{CS}$ setup time
t_{12}	15	ns min	A0, A1, A2, $\overline{BYSHF}$ to $\overline{CS}$ hold time
t_{13}	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_{14}	0	ns min	$\overline{CS}$ to $\overline{WR}$ hold time
t_{15}	40	ns min	$\overline{WR}$ pulse width
t_{16}	40	ns min	Data setup time
t_{17}	10	ns min	Data hold time
t_{18}	0	ns min	$\overline{LDAC}$ to $\overline{CS}$ setup time
t_{19}	0	ns min	$\overline{CS}$ to $\overline{LDAC}$ setup time
t_{20}	0	ns min	$\overline{LDAC}$ to $\overline{CS}$ hold time
GENERAL			
t_{10}	40	ns min	$\overline{LDAC}$, $\overline{CLR}$ pulse width

[1] All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and time from a voltage level of 1.6 V.
[2] Rise and fall times should be no longer than 50 ns.

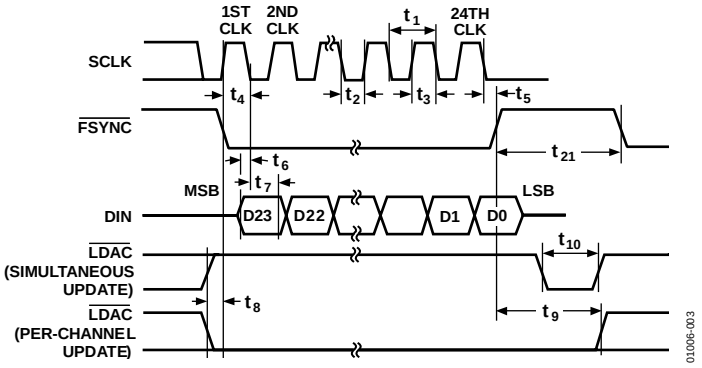

Figure 3. AD7834 Timing Diagram

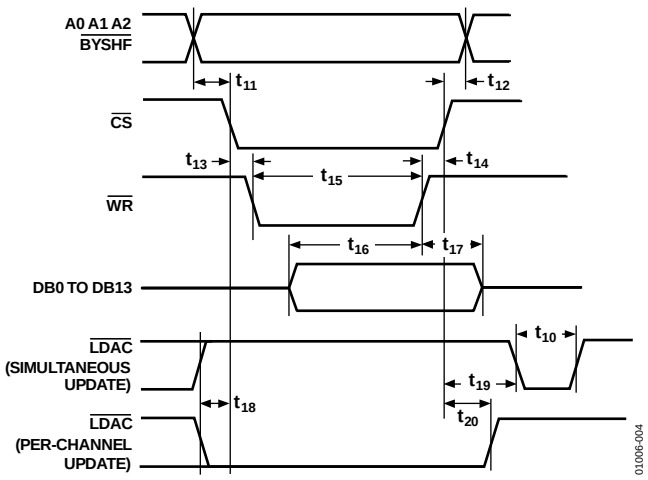

Figure 4. AD7835 Timing Diagram