Data Sheet

AD5529R

16-Channel, 16-Bit High-Voltage Output DAC

FEATURES

- 16-bit resolution, ±1LSB_{16} DNL, ±1LSB_{16} INL
- Independently programmable output ranges: 0V to 5V, 0V to 10V, 0V to 20V, 0V to 40V, ±5V, ±10V, ±15V, and ±20V
- Configurable grouping of supplies
- 4.096V internal voltage reference, 8ppm/°C typical
- Function generation with toggle, sinusoidal dither, and ramp waveforms
- Output voltage, current, and die temperature monitors
- Outputs drive ±25mA with 0.5V headroom
- 4.3mm × 4.3mm, 60-ball WLCSP

APPLICATIONS

- Optical networking
- Instrumentation
- Data acquisition
- Automatic test equipment
- Process control and industrial automation

GENERAL DESCRIPTION

The AD5529R is a 16-channel, 16-bit voltage output digital-to-analog converter (DAC) with an integrated precision reference. The AD5529R operates from both unipolar and bipolar supplies. It is guaranteed monotonic and has built in rail-to-rail output buffers that can source or sink up to 25mA.

The internal 4.096V precision reference sets the accuracy of the output voltage.

Four toggle pins support multiple digital functions such as toggle, sinusoidal dither, and ramps at multiple frequencies. An analog multiplexer simplifies measurement of DAC output voltages, load currents, and junction temperatures. The analog multiplexer can be used in applications where closed-loop systems are required.

The AD5529R features programmable offset and gain registers, which help to offload tasks from the external digital controller, enhancing overall system efficiency and performance.

The serial-peripheral interface (SPI) allows 3- and 4-wire connection and operates on logic levels from 1.98V down to 1.08V.

The SPI interface supports in-frame target addressing, which allows up to four AD5529R devices to share the same SPI interface.

FUNCTIONAL BLOCK DIAGRAM

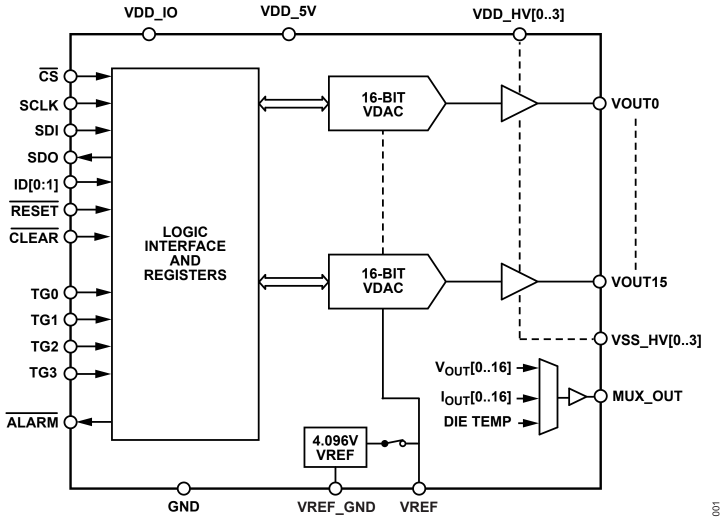

Figure 1. AD5529R Block Diagram

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.935.5565 |

TABLE OF CONTENTS

TABLE OF CONTENTS

REVISION HISTORY

4/2026—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

VDD_HVx = 7V to 45V, VSS_HVx = −22.5V to −0.5V, VSS_HV0 ≤ VSS_HV[1:3], and VDD_HVx − VSS_HVx < 45V, VDD_5V = 4.75V to 5.25V, VDD_IO = 1.08V to 1.98V. Unless otherwise noted, $-40°C \leq T_A \leq 125°C$ for min and max values, $T_A = 25°C$ typical values, outputs unloaded, all output ranges, external reference = 4.096V.

Table 1. Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	
INL			±1	LSB	All ranges, except 0V to 40V
			±2	LSB	0V to 40V range
DNL			±1	LSB	Guaranteed monotonic
TUE			±0.3	%FSR	0V to 5V, 0V to 10V, ±5V ranges
			±0.35	%FSR	0V to 20V, 0V to 40V, ±10V, ±15V, ±20 ranges
Gain Error			±0.3	%FSR	0V to 5V, 0V to 10V, ±5V ranges
			±0.35	%FSR	0V to 20V, 0V to 40V, ±10V, ±15V, ±20 ranges
Gain Error Temperature Drift		4		ppmFSR/°C	0V to 5V, 0V to 10V, ±5V ranges
		4.5		ppmFSR/°C	0V to 20V, 0V to 40V, ±10V, ±15V, ±20 ranges
Bipolar Zero Error			±0.25	%FSR	
Bipolar Zero Error Temperature Drift		0.7		ppmFSR/°C	
Zero-Scale Error					
			±0.25	%FSR	All unipolar ranges
			±0.33	%FSR	All bipolar ranges
Zero-Scale Error Temperature Drift		1.3		ppmFSR/°C	All unipolar ranges
		2.6		ppmFSR/°C	All bipolar ranges
OUTPUT CHARACTERISTICS					
Pull-Down Resistance		28		kΩ	Pull-down present when the channel is disabled
Output Voltage Ranges	−20		+20	V	
	−15		+15	V	
	−10		+10	V	
	−5		+5	V	
	0		40	V	
	0		20	V	
	0		10	V	
	0		5	V	
Headroom and Footroom[1]	0.5			V	I_{OUT} = ±25mA
	0.35			V	I_{OUT} = ±15mA
Output Current			±25	mA	
Short-Circuit Current[2]		±45		mA	
Maximum Capacitive Load[1]		1		nF	$R_L = \infty$
Load Regulation		120		µV/mA	±10V range, $-10mA \leq I_{OUT} \leq +10mA$
DC Crosstalk		5		µV	DAC code = midscale, due to single channel, full-scale output change, internal reference
REFERENCE OUTPUT					
Output Voltage[3]	4.091		4.101	V	At 25°C
External Load Current		5		mA	Source only
Voltage Reference Temperature Drift[4]		8	13	ppm/°C	−40°C to +125°C
Load Regulation		215		µV/mA	
Noise Spectral Density		180		nV/√Hz	At 1kHz
0.1Hz to 10Hz Noise		8.5		µV RMS	

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Long-Term Drift		110		ppm	T_A = 25°C, 1000hours
REFERENCE INPUT					
Input Voltage Range[1]	4.056	4.096	4.136	V	
Input Current		60		µA	All channels enabled
POWER SUPPLY					
VDD_HVx	7		45	V	
VSS_HVx	−22.5		0	V	For unipolar range, VSS_HV ≤ −0.5V
VDD_HVx to VSS_HVx			<45	V	Any VDD_HVx to any VSS_HVx
VDD_5V	4.75		5.25	V	
VDD_IO	1.08		1.98	V	
SUPPLY CURRENT					
VDD_HV		13		mA	±15V range, all channels enabled, code = full-scale
		100		µA	All channels disabled
VSS_HV		−13		mA	±15V range, all channels enabled, code = zero-scale
		−66		µA	All channels disabled
VDD_5V		33		mA	All channels enabled, ±20V range, code = zero-scale
		22		mA	All channels enabled, 0V to 40V range, code = full-scale
		350	600	µA	All channels disabled
VDD_IO		1	20	µA	No SDO line activity
MONITOR MUX					
Output Voltage Range	0		VREF	V	
Buffer Output Impedance		150		mΩ	
Output Current Limit		±12.5		mA	
Mux Switching Glitch[5]		0.85		mV	R_L = 2kΩ, C_L = 220pF
Current Monitor Error		±0.5		mA	I_{OUT} = 25mA, for no calibration and for calibration-adjusted formula
Voltage Monitor Error					
No Calibration		±2		%FSR	
Calibration-Adjusted Formula		±0.1		%FSR	
Temperature Monitor Error[6]		6.8		°C	Single measurement
Temperature Monitor Slope		7.7		mV/°C	
AC PERFORMANCE					
Settling Time					¼ to ¾ scale step, settled to ±1LSB$_{16}$ R_L = 2kΩ, C_L = 220pF
		7		µs	0V to 5V range
		12		µs	0V to 10V range, ±5V range
		13		µs	0V to 20V range, ±10V range
		18		µs	0V to 40V range, ±20V range
		16		µs	±15V range
Slew Rate		3		V/µs	
Output Noise Spectral Density					0V to 5V range, code = midscale
		130		nV/√Hz	At f = 1kHz
		67		nV/√Hz	At f = 10kHz
		6		µV RMS	0.1Hz to 10Hz
Digital-to Analog Glitch		1.30		nV × s	0V to 5V range, R_L = 2kΩ, C_L = 220pF
Glitch Impulse Peak Amplitude		1.90		mV	0V to 5V range, R_L = 2kΩ, C_L = 220pF
Digital Feedthrough		±0.2		nV × s	0V to 5V range, R_L = 2kΩ, C_L = 220pF
Digital Crosstalk		±0.2		nV × s	0V to 5V range, R_L = 2kΩ, C_L = 220pF
Analog Crosstalk		0.55		nV × s	0V to 5V range, R_L = 2kΩ, C_L = 220pF

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC-to-DAC Crosstalk		±0.45		nV × s	0V to 5V range, R_L = 2kΩ, C_L = 220pF
LOGIC INPUTS AND OUTPUTS					All digital pins
Input Low Voltage			0.3 × VDD_IO	V	
Input High Voltage	0.7 × VDD_IO			V	
Output Low Voltage			0.2 × VDD_IO	V	
Output High Voltage	0.8 × VDD_IO			V	
Pin Capacitance		3		pF	
Digital Input Leakage[7]					
		10		nA	All digital inputs except ID0, ID1
		200		nA	ID0, ID1
Digital High-Z Output Leakage[8]		10		nA	

[1] Guaranteed by design and characterization not production tested.

[2] The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature may impair device reliability.

[3] Output voltage includes the effects of preconditioning drift and soldering.

[4] Voltage reference temperature coefficient is calculated as per the box method. For more details, see the Terminology section.

[5] The peak voltage glitch seen on the VOUTn channels when a different channel is monitored through MUX_PARAM_SEL.

[6] See Figure 37.

[7] TG[0 to 3], $\overline{\text{RESET}}$, $\overline{\text{CLEAR}}$, $\overline{\text{CS}}$, SDI, ID[0 to 1], SCLK.

[8] SDO and $\overline{\text{ALARM}}$.

SPECIFICATIONS

TIMING CHARACTERISTICS

VDD_IO = 1.08V to 1.98V, −40°C ≤ T_A ≤ +125°C, T_A = 25°C, unless otherwise noted.

Table 2. AD5529R Timing Specifications[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_1 (Write)	20[2]			ns	SCLK cycle time (write)
t_1 (Read)	40[3]			ns	SCLK cycle time (read), 1.62V ≤ VDD_IO ≤ 1.98V
	50[4]			ns	SCLK cycle time (read), 1.08V ≤ VDD_IO < 1.62V
t_2		$t_1/2$		ns	SCLK high time
t_3		$t_1/2$		ns	SCLK low time
t_4	8			ns	SCLK rising edge to CSB falling edge
t_5	8			ns	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_6	8			ns	SCLK rising edge to CSB rising edge
t_7	8			ns	$\overline{CS}$ rising edge to SCLK rising edge
t_8	4.5			ns	Data setup time
t_9	3.5			ns	Data hold time
t_{10}	20			ns	$\overline{CS}$ high time
t_{11}			21	ns	SCLK falling edge to SDO data available, 1.08V ≤ VDD_IO < 1.62V
			13	ns	SCLK falling edge to SDO data available, 1.62V ≤ VDD_IO ≤ 1.98V
t_{12}	2			ns	SCLK falling edge to SDO data remains valid
t_{13}			16	ns	$\overline{CS}$ rising edge to SDO disabled
t_{14}			16	ns	SCLK falling edge to SDO enabled, 1.08V ≤ VDD_IO < 1.62V
			10	ns	SCLK falling edge to SDO enabled, 1.62V ≤ VDD_IO ≤ 1.98V
t_{reset}	20			ns	Minimum reset low width
t_{clear}	20			ns	Minimum clear low width
t_{L1}[5]	200			ns	Toggle period between pulses
t_{L2}	280			ns	Time to start toggle pulse
t_{L3}	100			ns	Toggle pulse width
t_{L4}/t_{L5}		240		ns	Toggle active edge to output response time rising/falling (output starts to change)
t_{vout_async}		340		ns	Asynchronous write till output response time

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[1] All input signals are specified with $t_R = t_F$ = 1ns/V (10% to 90% of IOVCC) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

[2] Equivalent to 50MHz for write operation only.

[3] Equivalent to 25MHz for read operation only.

[4] Equivalent to 20MHz for read operation only.

[5] Measured with DAC Deglitcher disabled.

SPECIFICATIONS

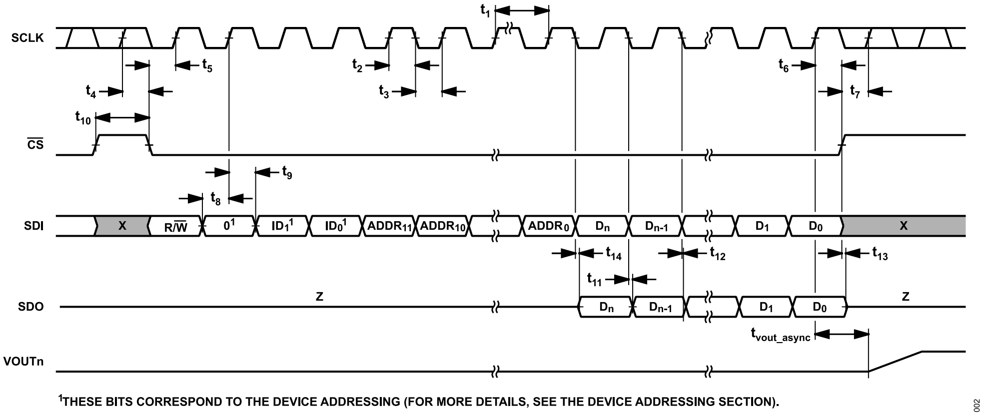


Figure 2. Serial Write and Read Operation

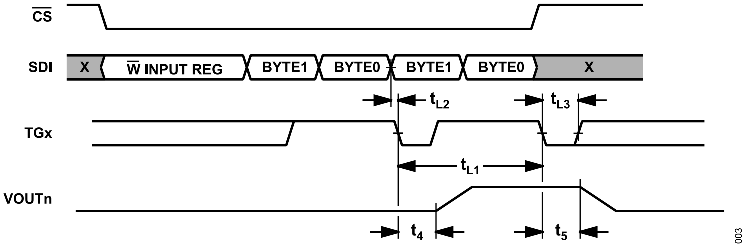


Figure 3. LDAC Timing

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
VDD_HV0/1/2/3 to GND	−0.3V to +50V
VSS_HV0/1/2/3 to GND	−25V to +0.3V
VDD_HVX to VSS_HVX	−0.3V to +50V
VSS_HV0 to VSS_HV1/2/3	−25V to +0.3V, VSS_HV0 must always be equal or lower than VSS_HV[1:3]
VDD_5V to GND	−0.3V to +6V
VDD_IO to GND	−0.3 to +2.2V
VREF to GND	−0.3 to +6V, or −0.3V to +VDD_5V, whichever is lower
Digital Inputs to GND[1]	−0.3V to +VDD_IO
Digital Outputs to GND[2]	−0.3V to +VDD_IO
MUX_OUT to GND	−0.3V to +VDD_5V, or −0.3V to +6V, whichever is lower
VREF_GND to GND	−0.3V to +0.3V
Temperature	
Operating Junction	−40°C to +125°C
Storage Range	−65°C to +150°C
Absolute Maximum Junction	150°C
Reflow Soldering Peak	260°C

[1] Digital inputs include $\overline{\text{CS}}$, SDI, SCLK, LDAC/TOGGLE[3:0], $\overline{\text{RESET}}$, and $\overline{\text{CLEAR}}$.

[2] Digital outputs include SDO and $\overline{\text{ALARM}}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JB} is the junction-to-board thermal resistance.

θ_{JC} is the junction-to-case thermal resistance.

Ψ_{JT} is the junction-to-top thermal characterization parameter.

Ψ_{JB} is the junction-to-board thermal characterization parameter.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
WLCSP CB-60-1[1]	43	13.4	1.31	3.94	13	°C/W

[1] Simulation values on JEDEC 2S2P board with 4 thermal vias, still air (0m/sec airflow).

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD5529R

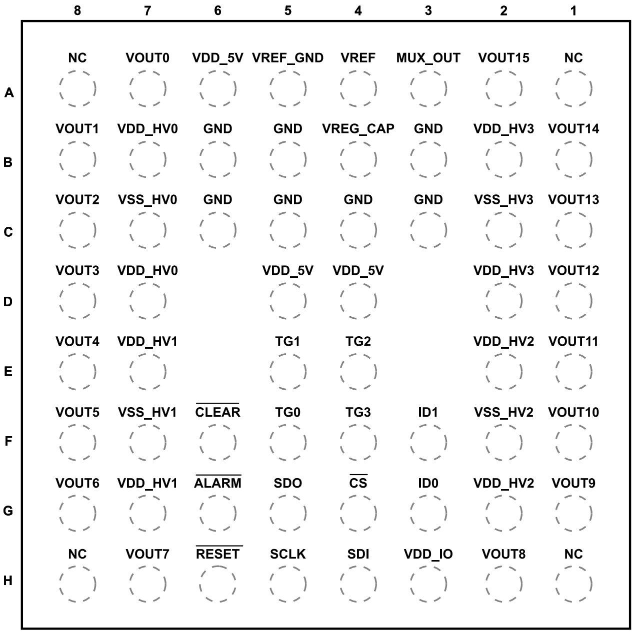
Table 5. AD5529R, 60-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	3500	2
FICDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.

004

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions, 60-Ball WLCSP

Pin Number	Mnemonic	Type[1]	Description
H3	VDD_IO	S	Logic Power Supply. VDD_IO must be between 1.08V and 1.98V. Decouple the VDD_IO supply with a 0.1µF capacitor to GND. This pin supplies power to the serial interface circuit blocks on the device.
A6, D4, D5	VDD_5V	S	Power Supply Input. These devices operate from 4.75V to 5.25V. Decouple the VDD_5V supply with a 10µF capacitor in parallel with a 0.1µF capacitor to GND.
B7, D7	VDD_HV0	S	Analog Positive Supply for DAC Outputs of Channel 0, Channel 1, Channel 2, and Channel 3. Bypass the VDD_HV0 pin to GND with a 10µF capacitor.
E7, G7	VDD_HV1	S	Analog Positive Supply for DAC Outputs of Channel 4, Channel 5, Channel 6, and Channel 7. Bypass the VDD_HV1 pin to GND with a 10µF capacitor.
G2, E2	VDD_HV2	S	Analog Positive Supply for DAC Outputs of Channel 8, Channel 9, Channel 10, and Channel 11. Bypass the VDD_HV2 pin to GND with a 10µF capacitor.
D2, B2	VDD_HV3	S	Analog Positive Supply for DAC Outputs of Channel 12, Channel 13, Channel 14, and Channel 15. Bypass the VDD_HV3 pin to GND with a 10µF capacitor.
C7	VSS_HV0	S	Analog Negative Supply for DAC Outputs of Channel 0, Channel 1, Channel 2, and Channel 3. Bypass VSS_HV0 to GND with a 10µF capacitor unless VSS_HV0 is connected to GND.
F7	VSS_HV1	S	Analog Negative Supply for DAC Outputs of Channel 4, Channel 5, Channel 6, and Channel 7. Bypass VSS_HV1 to GND with a 10µF capacitor unless VSS_HV1 is connected to GND.
F2	VSS_HV2	S	Analog Negative Supply for DAC Outputs of Channel 8, Channel 9, Channel 10, and Channel 11. Bypass VSS_HV2 to GND with a 10µF capacitor unless VSS_HV2 is connected to GND.
C2	VSS_HV3	S	Analog Negative Supply for DAC Outputs of Channel 12, Channel 13, Channel 14, and Channel 15. Bypass VSS_HV3 to GND with a 10µF capacitor unless VSS_HV3 is connected to GND.
A5	REF_GND	S	Analog Ground for Internal Reference. REFGND must be connected to GND using a low-impedance connection.
B3, B5, B6, C3, C4, C5, C6	GND	S	Ground Reference Point for All Circuitry on the Device.
A7	VOUT0	AO	Analog Output Voltage from DAC 0.
B8	VOUT1	AO	Analog Output Voltage from DAC 1.
C8	VOUT2	AO	Analog Output Voltage from DAC 2.
D8	VOUT3	AO	Analog Output Voltage from DAC 3.
E8	VOUT4	AO	Analog Output Voltage from DAC 4.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions, 60-Ball WLCSP (Continued)

Pin Number	Mnemonic	Type[1]	Description
F8	VOUT5	AO	Analog Output Voltage from DAC 5.
G8	VOUT6	AO	Analog Output Voltage from DAC 6.
H7	VOUT7	AO	Analog Output Voltage from DAC 7.
H2	VOUT8	AO	Analog Output Voltage from DAC 8.
G1	VOUT9	AO	Analog Output Voltage from DAC 9.
F1	VOUT10	AO	Analog Output Voltage from DAC 10.
E1	VOUT11	AO	Analog Output Voltage from DAC 11.
D1	VOUT12	AO	Analog Output Voltage from DAC 12.
C1	VOUT13	AO	Analog Output Voltage from DAC 13.
B1	VOUT14	AO	Analog Output Voltage from DAC 14.
A2	VOUT15	AO	Analog Output Voltage from DAC 15.
A3	MUX_OUT	AO	Monitor Multiplexer Analog Output. This pin is used to monitor internal die temperature, output voltages, and output current of a selected channel (see the Monitor Multiplexer section).
A4	VREF	AI/O	Reference Voltage. When using the internal reference, this is the reference output pin. When using an external reference of 4.096V, this is the input pin.
G4	$\overline{\text{CS}}$	DI	Chip-Select Active-Low Control Input. Frame synchronization signal for the input data.
H4	SDI	DI/O	Serial Data Input. Logic input. Data to be written to the device is provided on this input and is clocked into the register on the rising edge of SCLK. This pin becomes bidirectional in SPI 3-wire mode configuration.
G5	SDO	DO	Serial Data Output. Logic output. A readback operation provides data on this output pin as a serial data stream. Data is clocked out on the falling edge of SCLK and is valid on the rising edge of SCLK. This pin becomes high-impedance when SPI 3-wire mode is selected.
H5	SCLK	DI	Serial Clock Input.
F5	TG0	DI	TOGGLE0 Pin. Pulsing this pin low or high based on trigger edge settings allows all the selected DAC to be updated, which allows the selected DAC outputs to update synchronously for any of the digital function generation. When not used, this pin must be connected to either VDD_IO or GND (see the Hardware Trigger section).
H6	$\overline{\text{RESET}}$	DI	Asynchronous Reset. Active-low logic input, falling edge sensitive, resets all registers to their default values (see the Hardware Reset section).
F6	$\overline{\text{CLEAR}}$	DI	Active-Low Asynchronous Clear Input. A logic low at this level-triggered input clears the DAC registers to their 0V output codes (see the CLEAR Function section).
E5	TG1	DI	TOGGLE1 Pin. Pulsing this pin low or high based on trigger edge settings allows all the selected DAC to be updated, which allows the selected DAC outputs to update synchronously for any of the digital function generation. When not used, this pin can be connected to either VDD_IO or GND (see the Hardware Trigger section).
E4	TG2	DI	TOGGLE2 Pin. Pulsing this pin low or high based on trigger edge settings allows all the selected DAC to be updated, which allows the selected DAC outputs to update synchronously for any of the digital function generation. When not used, this pin can be connected to either VDD_IO or GND (see the Hardware Trigger section).
F4	TG3	DI	TOGGLE3 Pin. Pulsing this pin low or high based on trigger edge settings allows all the selected DAC to be updated, which allows the selected DAC outputs to update synchronously for any of the digital function generation. When not used, this pin can be connected to either VDD_IO or GND (see the Hardware Trigger section).
G6	$\overline{\text{ALARM}}$	DO	Alarm Indicator. Logic output. $\overline{\text{ALARM}}$ is an open-drain, N channel output that pulls low when a fault condition occurs. The $\overline{\text{ALARM}}$ pin, once triggered, does not clear until the condition that triggered the alarm is gone and the bit in the status/alarm register is set. A pull-up resistor of ≥10kΩ is recommended (see the ALARM Function section).
G3	ID0	DI	Device ID Bit 0. This pin must be connected to either VDD_IO or GND (see the Device Addressing section).
F3	ID1	DI	Device ID Bit 1. This pin must be connected to either VDD_IO or GND (see the Device Addressing section).
B4	VREG_CAP	AI	An external 100nF capacitor to GND must be connected to this pin.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions, 60-Ball WLCSP (Continued)

Pin Number	Mnemonic	Type[1]	Description
A1, A8, H1, H8	No Connect	N/A	Do not connect this pin. Leave these pins floating.

[1] AO is analog output pin, AI/O is analog input or output pin, S is supply pin, DI is digital input pin, DO is digital output pin, DI/O is digital input or output pin, and N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, T_A = 25°C, VDD_5V = 5V, VDD_IO = 1.8V, outputs unloaded, external reference with 1µF external capacitor, VDD_HVx and VSS_HVx set depending on range as VDD_HVx = MAX (7, FS + 0.5V), VSS_HVx = ZS − 0.5V.

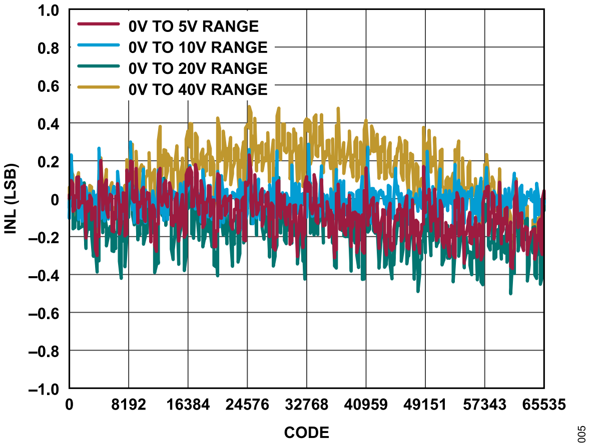


Figure 5. INL vs. Code, Unipolar Ranges

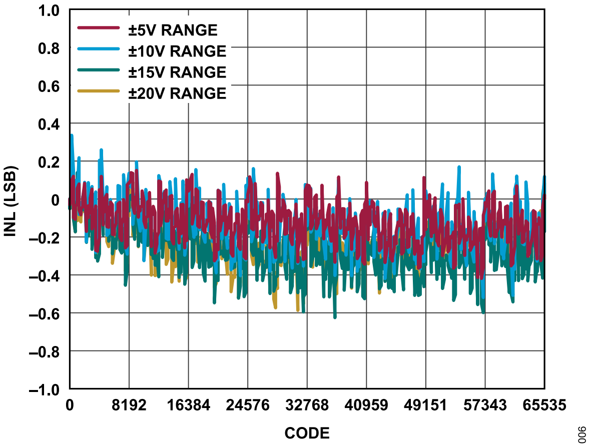


Figure 6. INL vs. Code, Bipolar Ranges

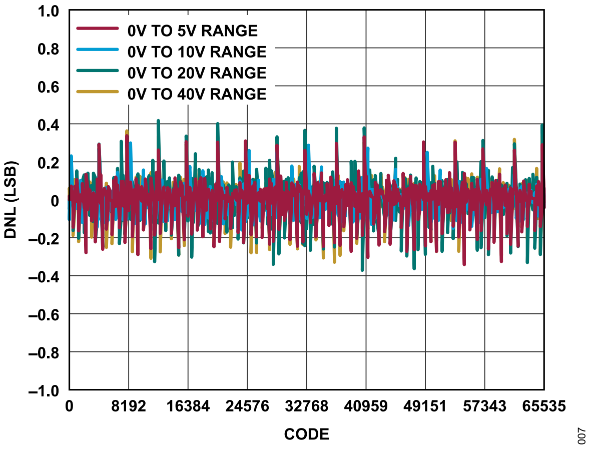


Figure 7. DNL vs. Code, Unipolar Ranges

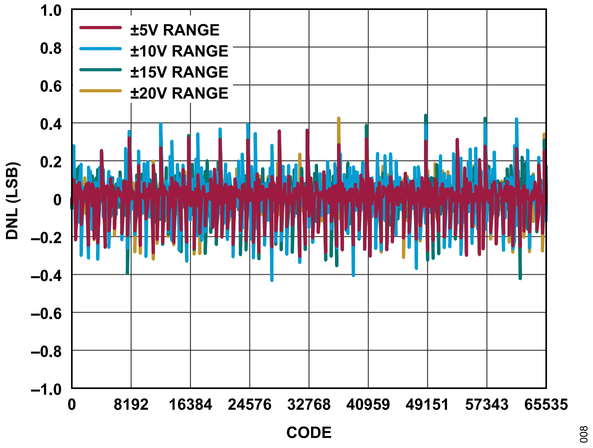


Figure 8. DNL vs. Code, Bipolar Ranges

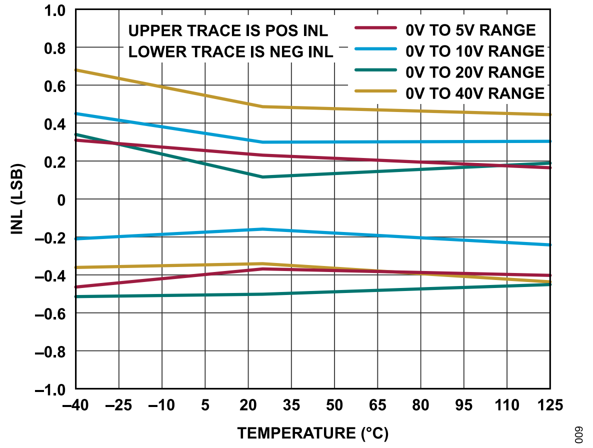


Figure 9. INL vs. Temperature, Unipolar Ranges

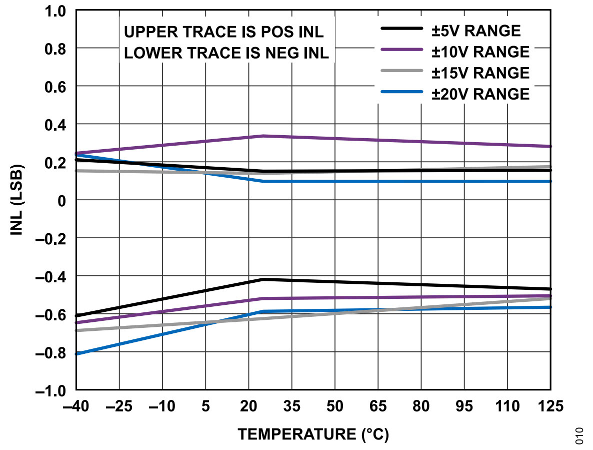


Figure 10. INL vs. Temperature, Bipolar Ranges

TYPICAL PERFORMANCE CHARACTERISTICS

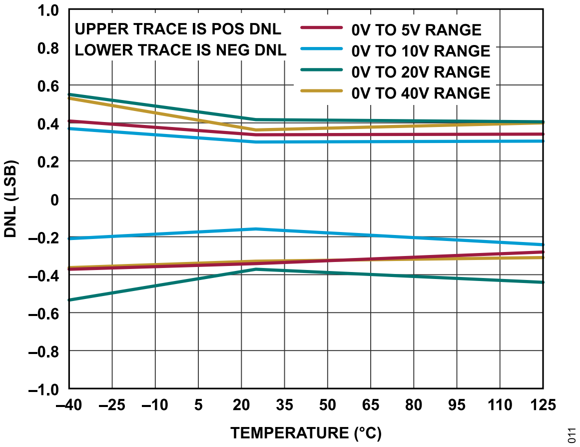


Figure 11. DNL vs. Temperature, Unipolar Ranges

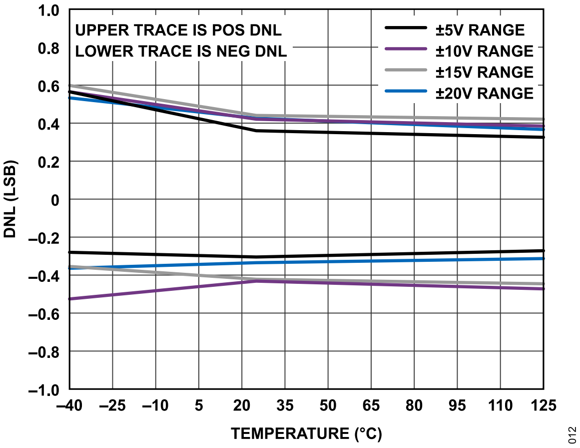


Figure 12. DNL vs. Temperature, Bipolar Ranges

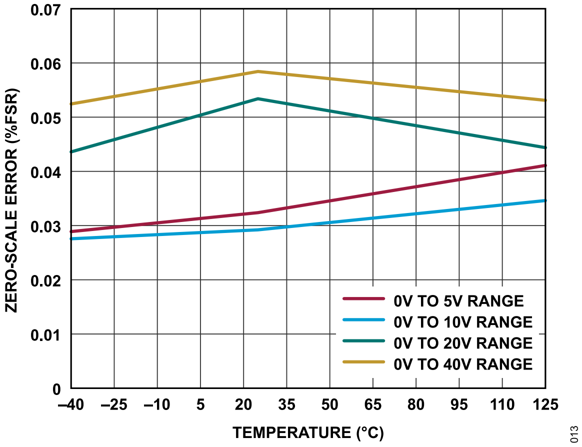


Figure 13. Zero-Scale Error vs. Temperature

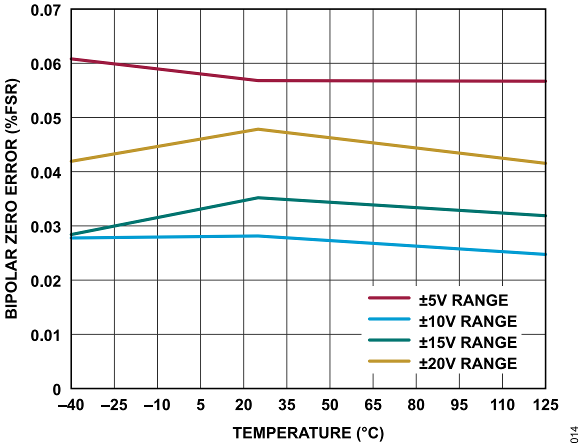


Figure 14. Bipolar Zero Error vs. Temperature

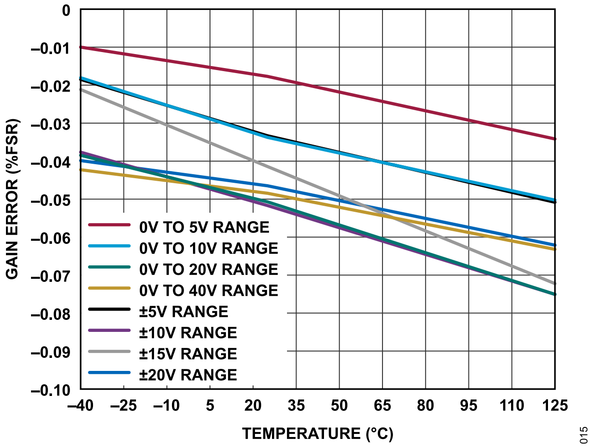


Figure 15. Gain Error vs. Temperature

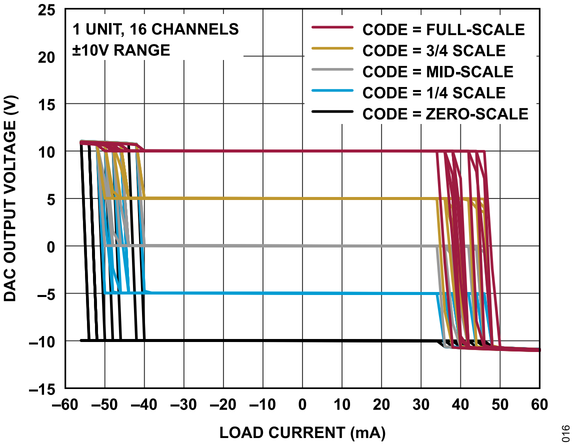


Figure 16. DAC Output Source and Sink Capability

TYPICAL PERFORMANCE CHARACTERISTICS

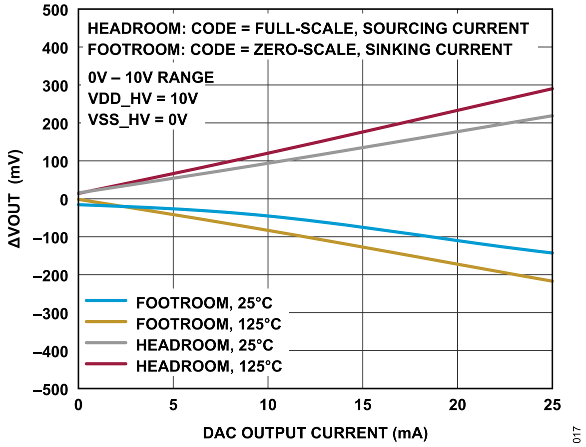


Figure 17. Headroom and Footroom vs. Output Load Current, 0V to 10V Range

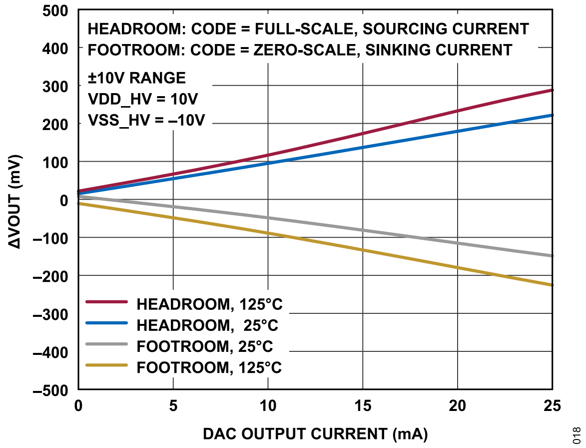


Figure 18. Headroom and Footroom vs. Output Load Current, ±10V Range

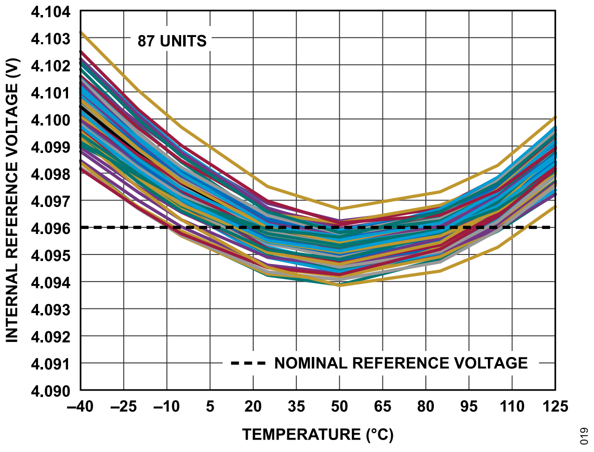


Figure 19. Internal Reference Temperature Drift

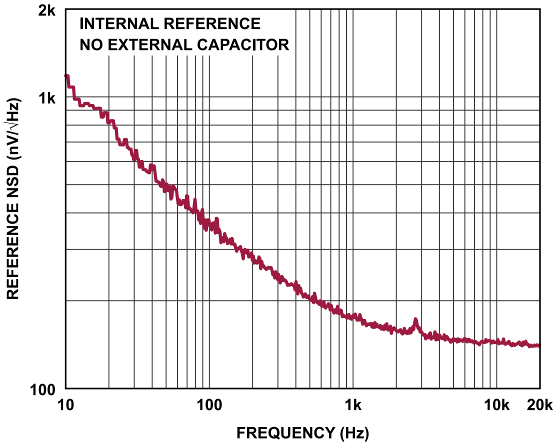


Figure 20. Internal Reference Noise Spectral Density

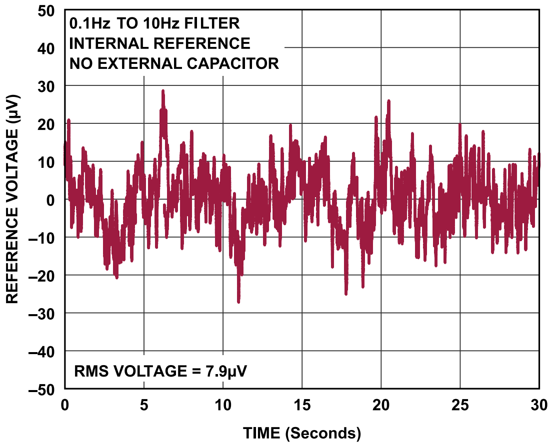


Figure 21. Internal Reference Noise

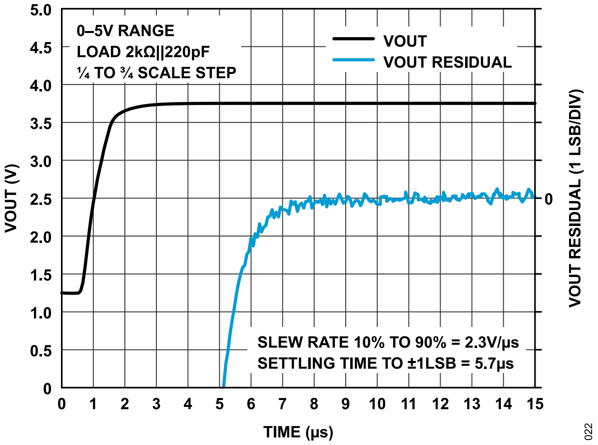


Figure 22. Settling Behavior, Rising Edge, 0V to 5V Range

TYPICAL PERFORMANCE CHARACTERISTICS

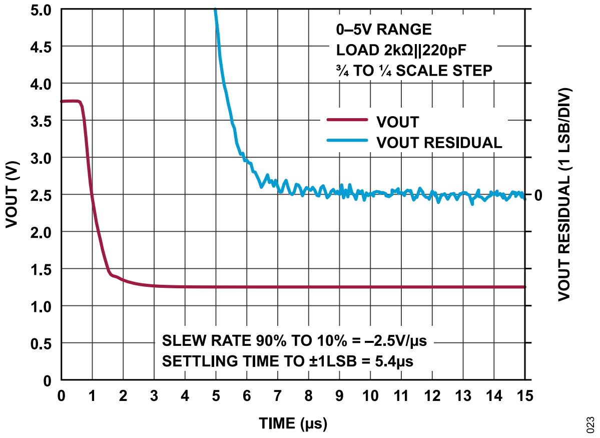


Figure 23. Settling Behavior, Falling Edge, 0V to 5V Range

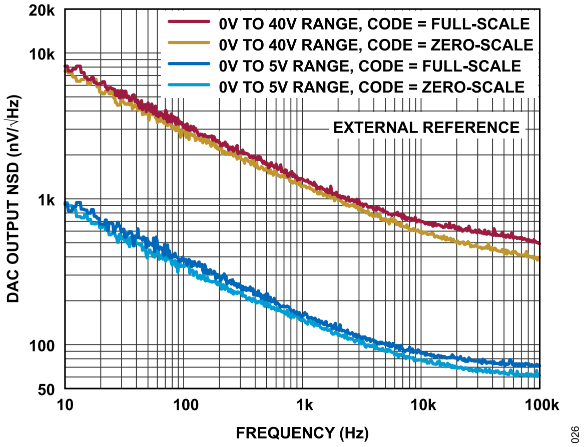


Figure 26. DAC Output Noise Spectral Density

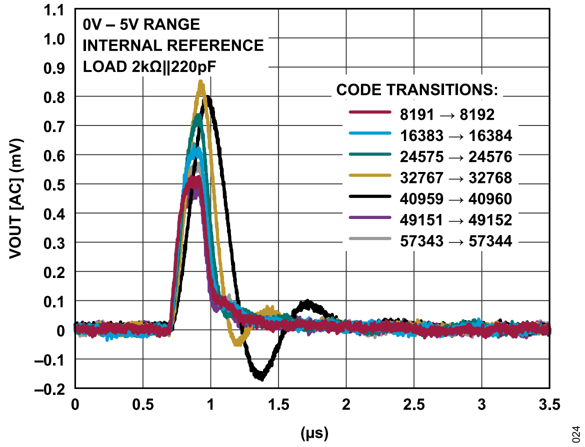


Figure 24. Glitch Amplitude, 0V to 5V Range

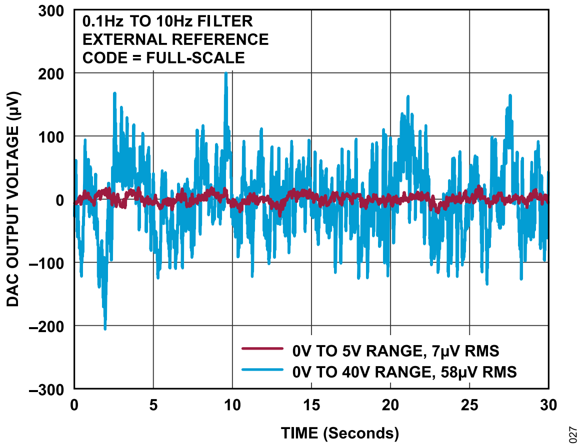


Figure 27. DAC Output Noise

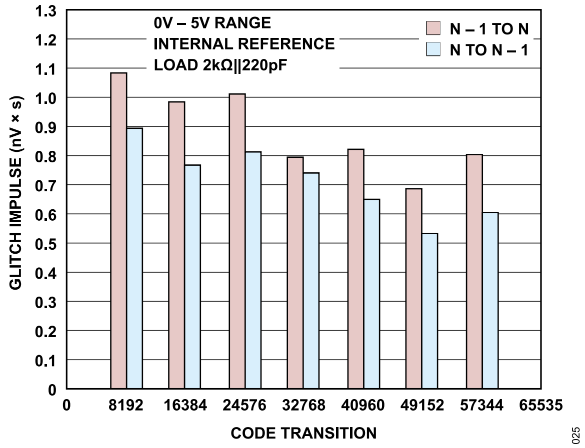


Figure 25. Glitch Impulse, 0V to 5V Range

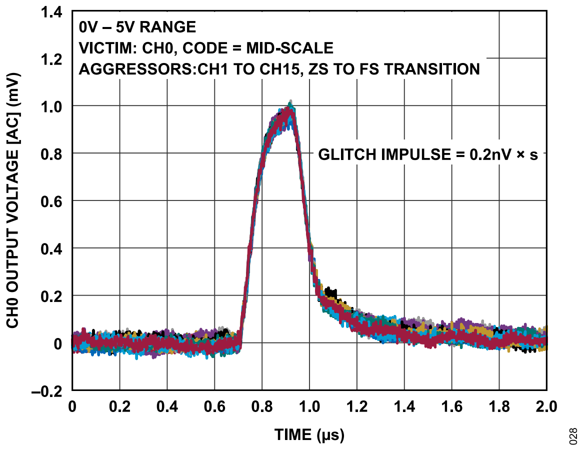


Figure 28. DAC-to-DAC Crosstalk

TYPICAL PERFORMANCE CHARACTERISTICS

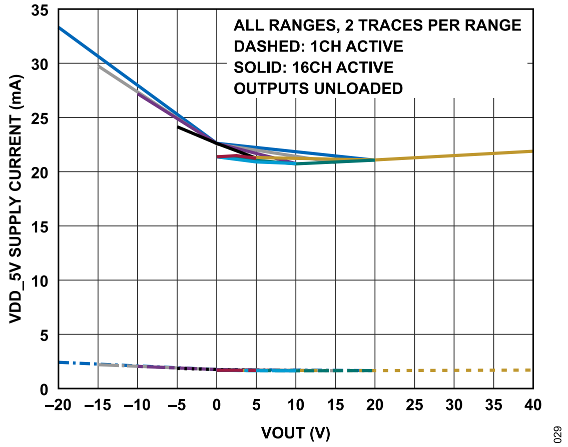


Figure 29. VDD_5V Supply Current vs. V_{OUT}

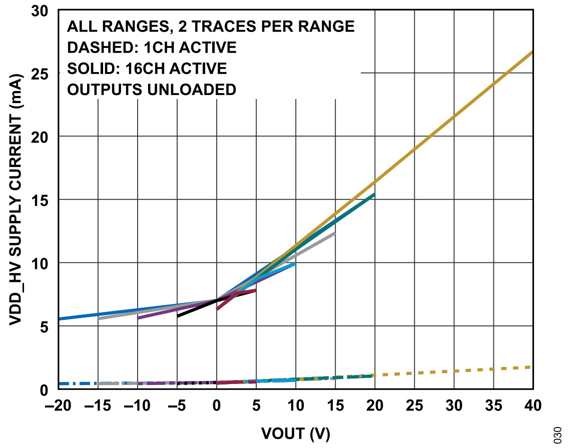


Figure 30. VDD_HV Supply Current vs. V_{OUT}

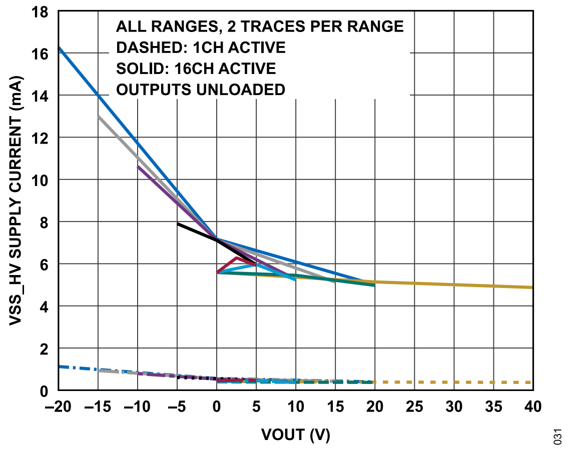


Figure 31. VSS_HV Supply Current vs. V_{OUT}

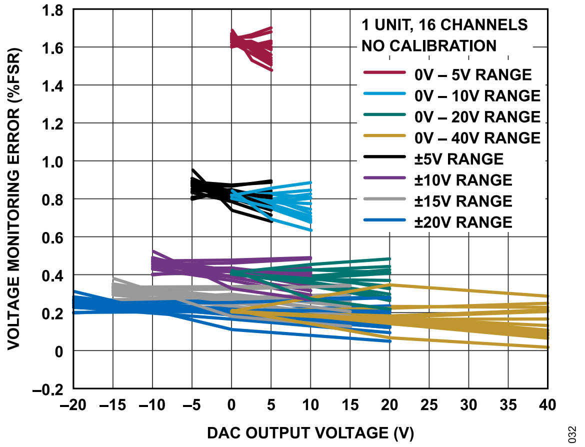


Figure 32. DAC Output Voltage Monitoring Error vs. DAC Output Voltage, No Calibration

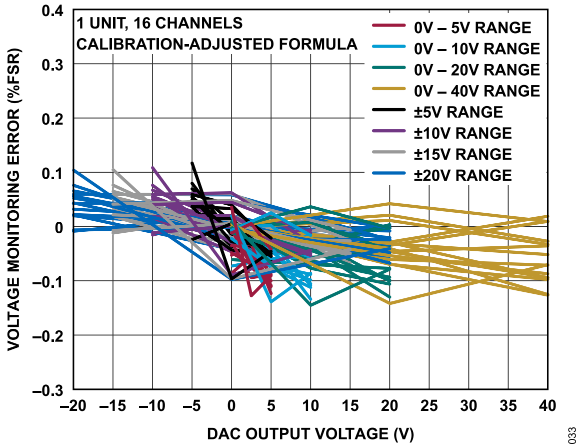


Figure 33. DAC Output Voltage Monitoring Error vs. DAC Output Voltage, Calibration-Adjusted Formula

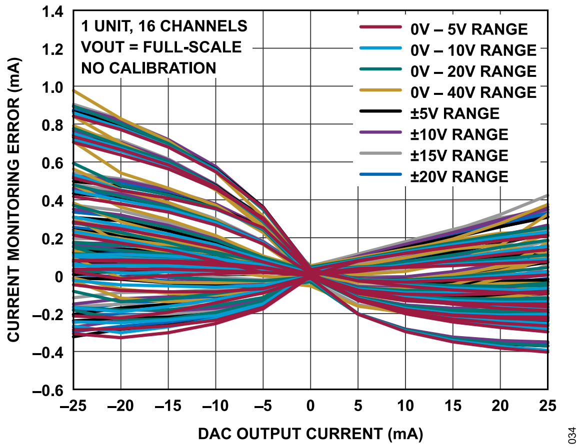


Figure 34. DAC Output Current Monitoring Error vs. DAC Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

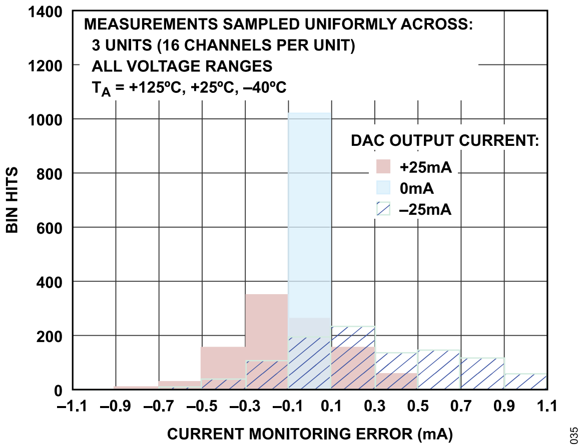


Figure 35. DAC Output Current Monitoring Error, Histogram

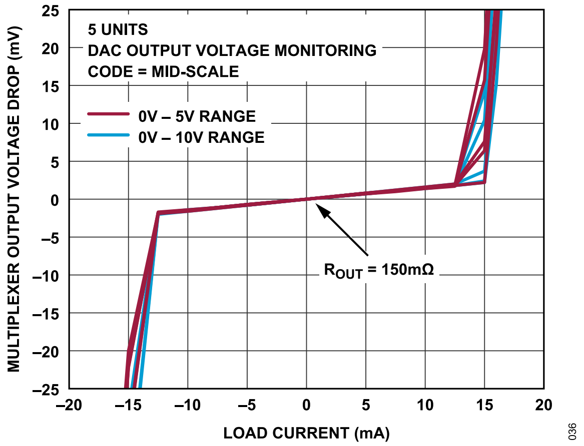


Figure 36. Multiplexer Output Buffer Load Regulation

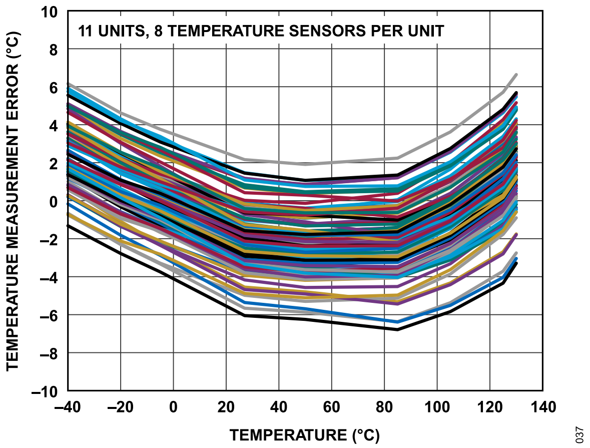


Figure 37. Temperature Sensor Error

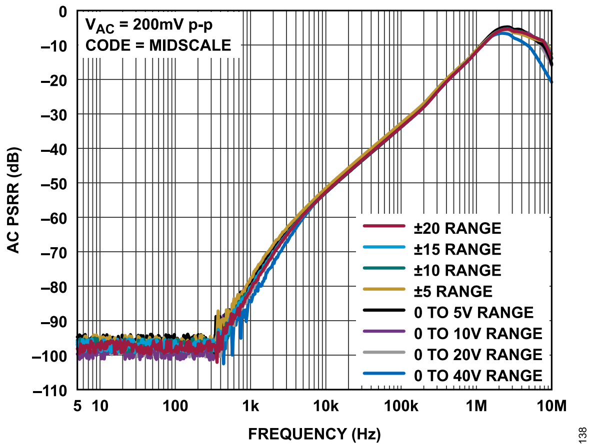


Figure 38. AC PSRR, VDD_HVx Rail

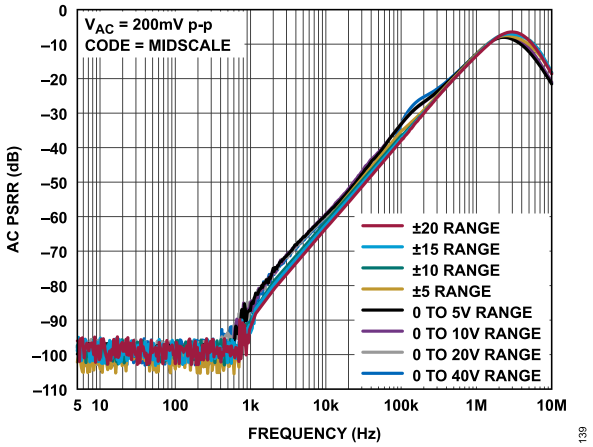


Figure 39. AC PSRR, VSS_HVx Rail

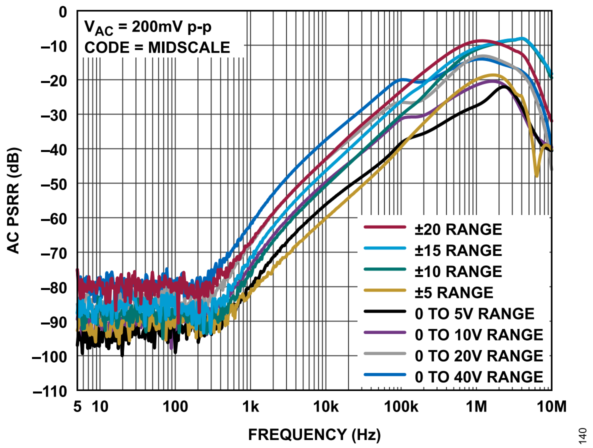


Figure 40. AC PSRR, VDD_5V Rail

TERMINOLOGY

Total Unadjusted Error (TUE)

Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, zero-scale error or bipolar zero-error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in %FSR. TUE equals the root square of the INL square, plus the gain error square, and the offset error square.

Integral Nonlinearity (INL)

Integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Zero code error is expressed in %FSR.

Zero-Scale Error Temperature Drift

Zero code error temperature drift is a measure of the change in zero code error with a change in temperature across a specified temperature range. It is calculated via the Box Method according to the following formula[1]:

$$ZSE\_TempDrift\left({}^{ppmFSR}\!/_{{}^\circ C}\right) = \frac{ZSE_{MAX} - ZSE_{MIN}}{T_{MAX} - T_{MIN}} \times 10^4$$

Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0V when the DAC register is loaded with the midscale code. Bipolar zero error is expressed in %FSR.

Bipolar Zero Error Temperature Drift

Bipolar zero error temperature drift is a measure of the change in bipolar zero error with a change in temperature across a specified temperature range. It is calculated by the box method according to the following formula[1]:

$$BZE\_TempDrift\left({}^{ppmFSR}\!/_{{}^\circ C}\right) = \frac{BZE_{MAX} - BZE_{MIN}}{T_{MAX} - T_{MIN}} \times 10^4$$

Gain Error

Gain error is a measure of the deviation in slope of the DAC transfer characteristic from the ideal slope. It is expressed as %FSR and calculated by the following formula:

$$GainError\left(\%FSR\right) = \frac{VOUT\_Span_{MEASURED} - VOUT\_Span_{IDEAL}}{VOUT\_Span_{IDEAL}} \times 10^2$$

Gain Error Temperature Drift

Gain error temperature drift is a measure of the change in gain error with a change in temperature across a specified temperature range. It is calculated by the box method according to the following formula[1]:

$$GE\_TempDrift\left({}^{ppmFSR}\!/_{{}^\circ C}\right) = \frac{GE_{MAX} - GE_{MIN}}{T_{MAX} - T_{MIN}} \times 10^4$$

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV × s, and is measured when the digital input code is changed by 1LSB at the major carry transition, that is, 0x7FFF to 0x800.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV × s, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

DC Crosstalk

DC crosstalk is the DC change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on the aggressor DAC channel while maintaining the victim DAC channel at midscale. It is expressed in µV.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC channel in response to a code change in the input register of another DAC channel. It is measured with a full-scale code change (all 0s to all 1s and vice versa) on the aggressor DAC channel input register while maintaining the victim DAC channel at midscale. It is expressed in nV × s.

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[1] Note that 1ppmFSR/°C = 10^{-4}%FSR/°C.

TERMINOLOGY

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC channel in response to a synchronous update in the output of another DAC channel done by a hardware trigger. It is measured by loading one of the input registers of the aggressor channel with a full-scale code change (all 0s to all 1s and vice versa), then triggering the output update by a hardware trigger when in synchronous mode, while maintaining the victim DAC at midscale. The glitch impulse is measured in nV × s.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC channel in response to an asynchronous update to the output of another DAC channel done by the SPI interface. It is measured by writing all 1s (or all 0s) to the aggressor channel input register, and then triggering an output update via writing all 0s (or all 1s) to the aggressor channel input register, while maintaining the victim DAC channel at midscale. The glitch impulse is measured in nV × s.

VOLTAGE REFERENCE TEMPERATURE DRIFT

Voltage reference temperature drift is a measure of the change in the reference output voltage with a change in temperature across a specified temperature range. The temperature drift is calculated using the box method, and specified relative to the nominal reference voltage, using the following formula:

$$VREF\_TempDrift\ (ppm/℃) = \frac{VREF_{MAX} - VREF_{MIN}}{VREF_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

$VREF_{MAX}$ and $VREF_{MIN}$ are the respective maximum and minimum reference output voltage values measured over the temperature range. $VREF_{NOMINAL}$ is the nominal reference output voltage, 4.096V.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5529R is a 16-channel, 16-bit voltage-output DAC that supports both bipolar operation and unipolar output ranges when powered from bipolar VDD_HV/VSS_HV analog supplies, with digital supply voltages from 1.08V to 1.98V. The AD5529R has an integrated 4.096V on-chip precision reference.

The AD5529R offers a versatile serial interface compatible with 3-wire and 4-wire SPI. The SPI interface supports in-frame target addressing, which allows multiple devices to share the same SPI bus. For more details, see the SPI Interface section.

DAC Channels

The AD5529R contains 16 buffered voltage output DAC channels output buffers capable of sourcing or sinking up to 25mA. A simplified block diagram of a DAC channel is shown in Figure 41. DAC channel includes programmable output range selection by the Output Range Register with one register per channel. A total of eight output voltage ranges are supported, spanning both unipolar and bipolar operation.

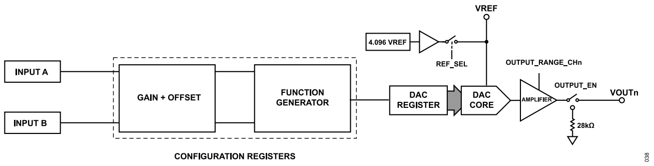

Figure 41. DAC Channel Block Diagram

Transfer Function

The ideal output voltage of DAC channel n is given by:

$$V_{OUTn} = A \times \frac{D}{2^{16}} + B$$

where:

D represents the decimal value of the straight binary code written to the DAC register (ranging from 0 to 65,535).

Parameters A and B are range dependent and defined in Table 7.

Table 7. A and B Values for Different Ranges

Output Range (V)	A	B
0 to 5	5	0
0 to 10	10	0
0 to 20	20	0
0 to 40	40	0
±5	10	−5
±10	20	−10
±15	30	−15
±20	40	−20

DAC Output Ranges and Supply Rails

Each DAC channel can be independently configured to one of eight possible output voltage ranges through its Output Range Register: 0V to 5V, 0V to 10V, 0V to 20V, 0V to 40V, −5V to +5V, −10V to +10V, −15V to +15V, −20V to +20V.

The AD5529R has four sets of DAC output supply rails, each powering four DAC outputs, with the correspondence specified in Table 8.

Table 8. Supply Rail Correspondence to DAC Channels

Supply Rail Pins	DAC Channels
VDD_HV0, VSS_HV0	VOUT0 to VOUT3
VDD_HV1, VSS_HV1	VOUT4 to VOUT7
VDD_HV2, VSS_HV2	VOUT8 to VOUT11
VDD_HV3, VSS_HV3	VOUT12 to VOUT15

The voltage level of each supply rail must be chosen to fulfill the most restrictive headroom (highest voltage) for the positive rail and most restrictive footroom (lowest voltage) for the negative rail from the four corresponding channels. The requirement for each channel depends on the selected output range. Table 9 lists the recommended supply voltage for each range, where the 500mV headroom and footroom requirements along with a minimum of 7V for the positive rail are taken into account.

Table 9. Recommended Supply Voltages for Each DAC Output Range

DAC Output Range (V)	Negative Rail Voltage (V)	Positive Rail Voltage (V)
0 to 5	−0.5	7
0 to 10	−0.5	10.5
0 to 20	−0.5	20.5
0 to 40	−0.5	40.5
−5 to +5	−5.5	7
−10 to +10	−10.5	10.5
−15 to +15	−15.5	15.5
−20 to +20	−20.5	20.5

While Table 9 values ensure specified performance across the full ±25mA current source and sink range, the following considerations apply:

- Headroom and footroom can be relaxed for DAC current demands below the rated ±25mA (for typical behavior, see Figure 17 and Figure 18).
- For unipolar ranges, it is possible to supply the negative rail at 0V at the expense nonlinearity (in the form of a dead band) at the lower end of the range.
- For the 0V to 5V and −5V to +5V ranges, while the DAC outputs can operate with a positive rail supply voltage between 5.5V and 7V, data sheet specifications and dynamic performance cannot be guaranteed.

THEORY OF OPERATION

DAC Output Enable/Disable

After power up, hardware reset, or software reset all DAC outputs are disabled. A disabled DAC output is actively pulled to ground by an internal resistance of 28kΩ. Note that this means that while AD5529R is unpowered, the pull-down resistance is not present. When a channel is disabled, its associated output amplifier and reference buffer are disabled, which leads to significantly reduced power consumption.

Each DAC channel output can be individually enabled or disabled by setting its corresponding bit to 1 or 0 respectively in the Output Enable Register.

MONITOR MULTIPLEXER

The AD5529R includes a buffered monitor multiplexer that drives a voltage signal on the MUX_OUT pin. This signal can represent one of the following measurements:

- Output voltage of a selected channel
- Output current of a selected channel
- Temperature from one of the eight internal sensors
- Calibration signal for the output voltage or the output current measurements

The monitoring functionality is controlled through the MUX Out Select Register. The multiplexer output is disabled by default, placing the output buffer in a high-impedance state. The output buffer is enabled by setting the MUX_OUT_EN bit to 1. Bit field MUX_PARAM_SEL controls which signal is transmitted over MUX_OUT, for more details, see the MUX Out Select Register section.

Output Voltage Monitoring

When the multiplexer output is enabled, and the bit field MUX_PARAM_SEL is set to a value corresponding to voltage monitor for Channel n, the voltage at the output of channel n (V_{VOUTn}) can be monitored by measuring the voltage at the MUX_OUT pin (V_{MUX_OUT}) and then performing the following calculation:

$$V_{VOUTn} = 21 \times V_{MUX\_OUT} - 10 \times V_{REF}$$

Table 10. DAC Output Voltage Encoding in Multiplexer Output

DAC Output Voltage (V)	V_{MUX_OUT} (V)
40	3.855
20	2.903
15	2.665
10	2.427
5	2.189
0	1.950
−5	1.712
−10	1.474
−15	1.236
−20	0.988

Output Current Monitoring

When the multiplexer output is enabled, and the bit field MUX_PARAM_SEL is set to a value corresponding to current monitor for Channel n, the current at the output of channel n (I_{VOUTn}) can be monitored by measuring the voltage at the MUX_OUT pin (V_{MUX_OUT}) and then performing the following calculation:

$$I_{VOUTn} = \frac{V_{MUX\_OUT} - \frac{V_{REF}}{2}}{60\Omega}$$

Positive values for I_{VOUTn} correspond to the channel sourcing current, while negative values correspond to sinking.

Table 11. DAC Output Current Encoding in Multiplexer Output

DAC Output Current (mA)	V_{MUX_OUT} (V)
25	3.548
1	2.108
0	2.048
−1	1.988
−25	0.548

Temperature Monitoring

The AD5529R has eight on-chip temperature sensors. Each sensor is adjacent to two contiguous DAC outputs: temp sensor number 0 covers channels 0 and 1, temp sensor number 1 covers channels 2 and 3, and so on. These temperature sensors provide the temperature alarm and shutdown functionality (for more details, see the Temperature Alarm section), and they can also be accessed by the user by the monitor multiplexer. When the multiplexer output is enabled, and the bit field MUX_PARAM_SEL is set to a value corresponding to temp sensor number n output, the temperature of sensor n ($Temp_n$) can be monitored by measuring the voltage at the MUX_OUT pin (V_{MUX_OUT}) and then performing the following calculation (with V_{MUX_OUT} in units of Volts):

$$Temp_n[°C] = \frac{1000}{7.695} \times \left(V_{MUX\_OUT} - 2.036\right)$$

Table 12. Sensor Temperature Encoding in Multiplexer Output

Sensor Temperature (°C)	V_{MUX_OUT} (V)
150	3.190
125	2.998
25	2.228
0	2.036
−40	1.728

THEORY OF OPERATION

Calibration Signals

It is possible to increase the accuracy of DAC output voltage and output current monitoring by making corrections to the calculations based on the value of internal calibration signals. There are two internal calibration signals that are shared across all channels, one for output voltage monitoring ($V_{cal\_voltage}$) and one for output current monitoring ($V_{cal\_current}$). $V_{cal\_voltage}$ or $V_{cal\_current}$ can be output through the monitoring multiplexer by setting the corresponding value in the MUX_PARAM_SEL bit field in the MUX Out Select Register. This allows the user to measure and store the value of the calibration signals.

Once the value of the voltage or current calibration signal has been measured and stored, the regular multiplexer voltage or current monitoring function can be used in conjunction with the following calibration-adjusted formulas to monitor the output voltage or output current with improved accuracy:

$$V_{VOUTn}\left(calibrated\right) = 21 \times \left(V_{MUX\_OUT} - V_{cal\_voltage}\right) + \frac{V_{REF}}{2}$$

$$I_{VOUTn}\left(calibrated\right) = \frac{V_{MUX\_OUT} - V_{cal\_current}}{60\Omega}$$

The calibration signals $V_{cal\_voltage}$ and $V_{cal\_current}$ have values in the range of 2.048V ± 3mV. The output voltage monitoring has the highest potential for accuracy improvement with calibration, where the typical uncalibrated error of ±2%FSR can be reduced to ±0.1%FSR with the calibration correction.

VOLTAGE REFERENCE

The AD5529R has an on-chip, buffered, 4.096V, 8ppm/°C typical reference. The reference output is available at the VREF pin, which can typically supply external loads of up to +5mA.

The external 4.096V reference is enabled by default. If the internal reference is required instead, it can be selected by configuring the Reference Source Select Register.

GAIN AND OFFSET CORRECTION

The gain and offset correction feature allows the AD5529R to apply a digital correction to the code stored in DAC_INPUT_A_CHn and DAC_INPUT_B_CHn, which results in a gain/offset corrected code being exercised at the DAC output:

$$CORRECTED\_CODE = DAC\_INPUT\_CODE \times G + C$$

Each channel has independent gain/offset correction registers, and the correction is applied in all operating modes with the following two exceptions:

- **Synchronous/Asynchronous Mode**: Only the adjusted DAC_INPUT_A_CHn is used (digital functions disabled).
- **Dither Mode**: The unadjusted DAC_INPUT_B_CHn value is used to directly control the sine-wave amplitude.

If the correction results in a value greater than the maximum code or in a negative value, the corrected code is clamped to either 0xFFFF or 0x0000, respectively. Note that applying digital offset correction always results in a loss of dynamic range at the DAC output. For gain correction, a gain correction factor <1 also results in a loss of dynamic range, while a factor >1 results in an effective increase in INL. For the AD5529R, the intended use of the gain/offset correction feature is the calibration of small system errors, where the loss of dynamic range and small degradation of INL result in a favorable trade-off vs. the improvement in overall accuracy. Specifically, the reduced gain error correction range allowed by the feature is mathematically guaranteed to incur in <0.5LSB increased linearity error.

The offset correction applied to a channel is controlled by its 16-bit Digital Offset Correction Register. The value of the register in two's complement corresponds to the number of codes to add (C in the formula for the corrected code). This results in an offset correction range capability between −32768 and +32767 codes.

The gain correction applied to a channel is controlled by its Digital Gain Correction Register. Each LSB change in the Digital Gain Correction Register corresponds to an increase/decrease of the DAC input code of:

$$\Delta\%_{\Delta 1LSB} = \pm 2^{-15} \times 100 \approx \pm 0.0030518\%$$

This results in a maximum code adjustment range allowed by the feature of approximately +0.388% to −0.391%, with the encoding of the gain correction factor (G in the formula for the corrected code) as per Table 13.

Table 13. Encoding of Gain Correction Factor in Digital Gain Correction Register

CAL_GAIN_CH Field Value	Gain Correction Factor (G)	Code Adjustment (Δ%)
0b11111111	1.0038757	+0.3875732%
0b11111110	1.0038452	+0.3845215%
...	...	...
0b10000001	1.0000305	+0.0030518%
0b10000000 (default)	1	+0% (no gain correction)
0b01111111	0.9999695	-0.0030518%
...	...	...
0b00000001	0.9961243	−0.3875732%
0b00000000	0.9960938	−0.3906250%

The straight binary value to be written in the Digital Gain Correction Register to achieve a required gain correction factor G can be calculated using the following formula:

$$CAL\_GAIN\_CH = 128 + \left(G - 1\right) \times 2^{15}$$

Note that the relationship between the code adjustment (Δ%) and the gain correction factor G is:

$$\Delta\% = (G - 1) \times 100$$

THEORY OF OPERATION

DAC UPDATES

The AD5529R supports two DAC update mechanisms, asynchronous and synchronous. The update behavior is configured in the Sync-Async Load Register, which determines whether the DAC output updates immediately following a register write or waits for a trigger event. The default is asynchronous. When operating in synchronous mode, the trigger source is selected (hardware or software) by the Hardware-Software Trigger Register. A flow diagram is shown in Figure 42.

The Secondary DAC Input Register is reserved for use with the function generator and does not affect standard DAC output updates.

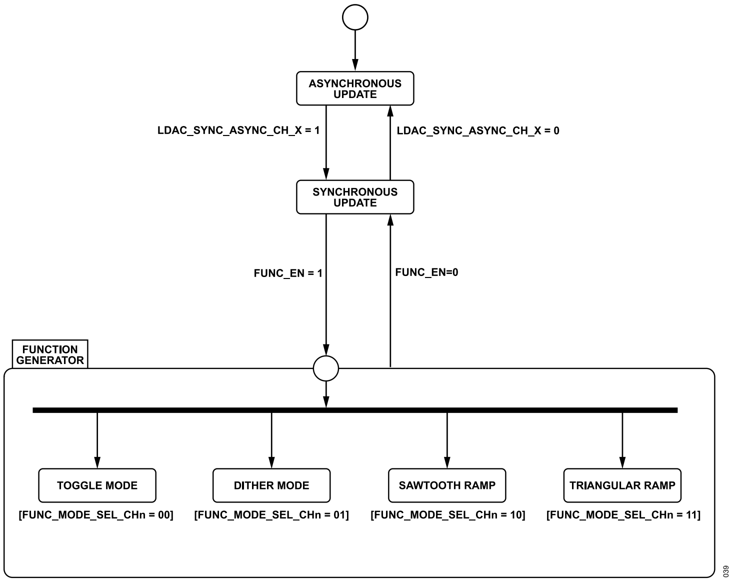

Figure 42. DAC Updates Flowchart

Software Triggers

The AD5529R supports two software triggered LDAC mechanisms.

The Individual Channel Software LDAC Register allows a trigger event to be generated on a per-channel basis, which enables the channels to update their outputs independently.

Multichannel Software LDAC Register provides a simultaneous update mechanism for multiple channels.

Hardware Trigger

The Hardware trigger for the AD5529R allows DAC output updates to be controlled using external toggle pins TG[0 to 3]. For each DAC channel, the LDAC Hardware Pin and Edge Select Register defines which toggle pin is used as the hardware trigger source and which signal transition initiates the update.

Synchronous Updates

To perform a synchronous update on a single channel, equivalent to a traditional LDAC operation on the AD5529R, do the following steps:

1. Disable all digital functions for the required channel by clearing the corresponding bits in the Function Enable Register.
2. Enable synchronous mode, configure the channel for synchronous operation by setting the corresponding bit high in the Sync-Async Load Register.
3. Select the trigger source, in the Hardware-Software Trigger Register, select whether the synchronous update is triggered by a hardware or software source.
4. Configure the hardware trigger source by programming the LDAC Hardware Pin and Edge Select Register. Select the required toggle pin and the triggering edge.
5. Load the required code to update to in Primary DAC Input Register.
6. Apply the selected trigger source by asserting the corresponding channel bit in the Individual Channel Software LDAC Register for a software trigger or by toggling the configured TG pin for a hardware trigger.
7. Repeat steps 5 and 6 as required.

For multichannel synchronous updates, the procedure is as follows:

1. Disable all digital functions for the required channel by clearing the corresponding bits in the Function Enable Register.
2. Select the channels to be updated simultaneously by programming the Multi Input Channel Select Register.
3. For a simultaneous multi DAC update using a hardware trigger, ensure that all channels selected in the MULTI_INPUT_SEL register are configured with the same trigger source in the LDAC_HW_SRC_CH register.
4. Load the required DAC code by writing to the Multichannel Input Register.
5. Apply the selected trigger source by asserting the appropriate bit in the Multichannel Software LDAC Register or by applying the required edge on the configured TG pin for a hardware trigger.
6. Repeat steps 4 and 5 as required.

Table 14 and Table 15 summarize the register configuration and trigger requirements for performing synchronous DAC output updates using hardware and software triggers.

THEORY OF OPERATION

Table 14. AD5529R Hardware Triggers

LDAC_SYNC_ASYNC	LDAC_HW_SW	LDAC_HW_SRC_CH	Actions to Update the Output
(1) SYNC	Hardware LDAC	Select appropriate TGPx source and edge polarity	Generate an edge transition (rising, falling, or any) on the selected toggle pin for the chosen channel.

Table 15. AD5529R Software Triggers

LDAC_SYNC_ASYNC	LDAC_HW_SW	LDAC_HW_SRC_CH	MULTI_INPUT_SEL	Actions to Update the Output	
(1) SYNC	Software LDAC	DONT CARE	Channel included	Assert the channel's bit in the SW_LDAC register.	Assert the channel's bit in the MULTI_SW_LDAC register.
(1) SYNC	Software LDAC	DONT CARE	Channel not included	Assert the channel's bit in the SW_LDAC register.	

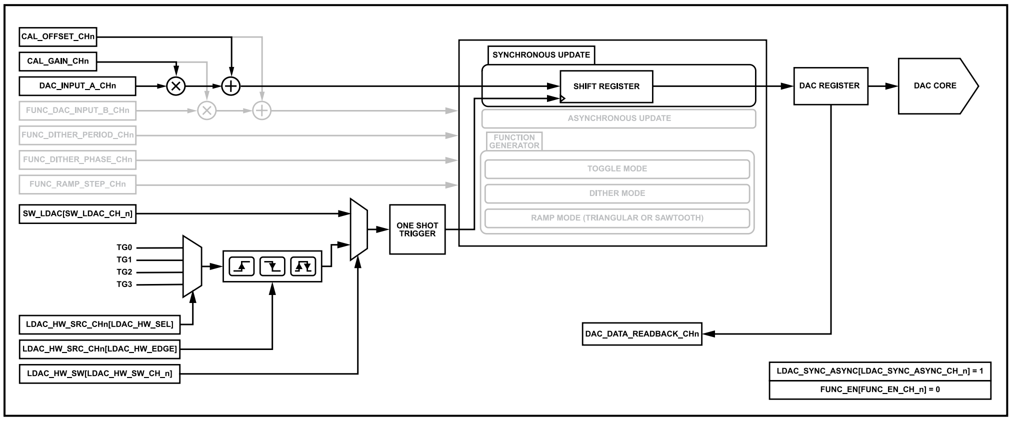

Figure 43. Synchronous Block Diagram

Asynchronous Updates

In the AD5529R, asynchronous DAC updates allow the DAC output to update automatically following a write to the DAC input register, without requiring a trigger event. This update mode is intended for low latency operation and supports multiple write paths that result in an immediate output update. Table 16 summarizes the register write paths that result in an asynchronous DAC update.

Table 16. Asynchronous DAC Updates

LDAC_SYNC_ASYNC	MULTI_INPUT_SEL	Actions to Update the Output
(0) ASYNC	Channel included	Write to the MULTI_INPUT_A register.
(0) ASYNC	Channel not included	Write to channel's DAC_INPUT_A register.

THEORY OF OPERATION

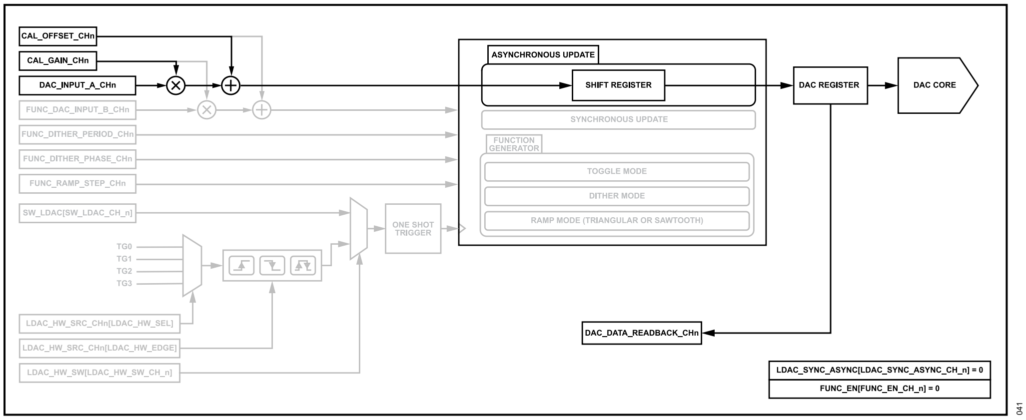

Figure 44. Asynchronous Block Diagram

Digital Functions

The AD5529R provides several digital functions that reduce external controller overhead by performing common operations internally. The dither, toggle, and ramp functions are mutually exclusive on a per-channel basis, with only one function selectable for each channel at any time by the Function Mode Select Register. These functions cannot be enabled simultaneously on the same channel. Each channel includes a dedicated register in the memory map for configuring operation in toggle, dither, or ramp mode. The digital functions for all channels are disabled by default.

Each channel supports five selectable clock sources for the digital functions, four hardware toggle pins TG[3:0], and one software toggle. The clock source is selected on a per-channel basis by programming the Hardware-Software Trigger Register to choose between hardware or software toggle operation. When hardware toggle is selected, the specific toggle pin and its active edge are configured using the LDAC Hardware Pin and Edge Select Register, with the TG[3:0] pins supporting toggle frequencies up to 5MHz for all digital functions. When software toggle is selected, updates are triggered by asserting the corresponding channel bits in the Individual Channel Software LDAC Register, with the maximum toggle rate limited by the SPI write latency associated with repeated writes to the register.

Digital functions cannot be enabled on a channel that is configured for asynchronous updates. To enable a digital function, the channel must first be configured for synchronous update mode by programming the Sync-Async Load Register. Once the channel is set to synchronous operation, the function generator may be enabled.

A block diagram of the digital functions is shown in Figure 45.

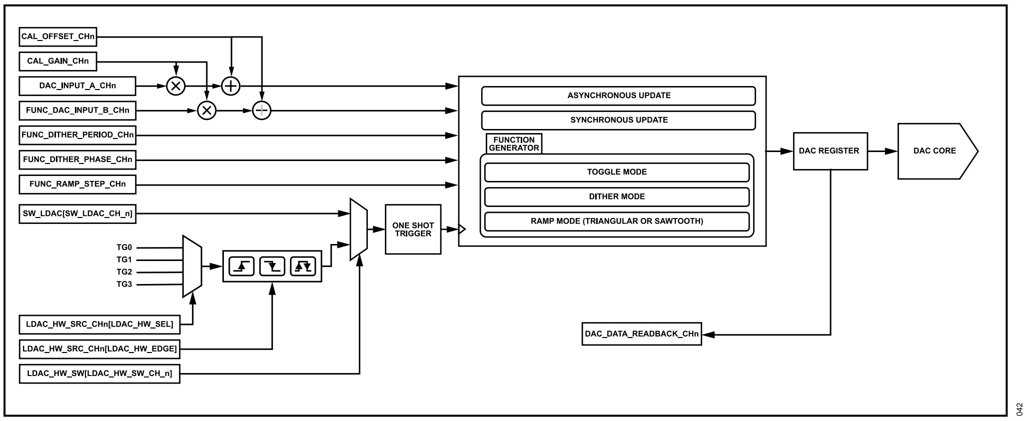

Figure 45. Digital Functions Diagram

THEORY OF OPERATION

Toggle Function

In toggle mode, the DAC output alternates between the values programmed in Primary DAC Input Register and Secondary DAC Input Register, which produce a square-wave type output at the applied trigger rate. A simplified block-level representation of the toggle function is shown in Figure 46. It is enabled by writing 0x0000 to the Function Mode Select Register.

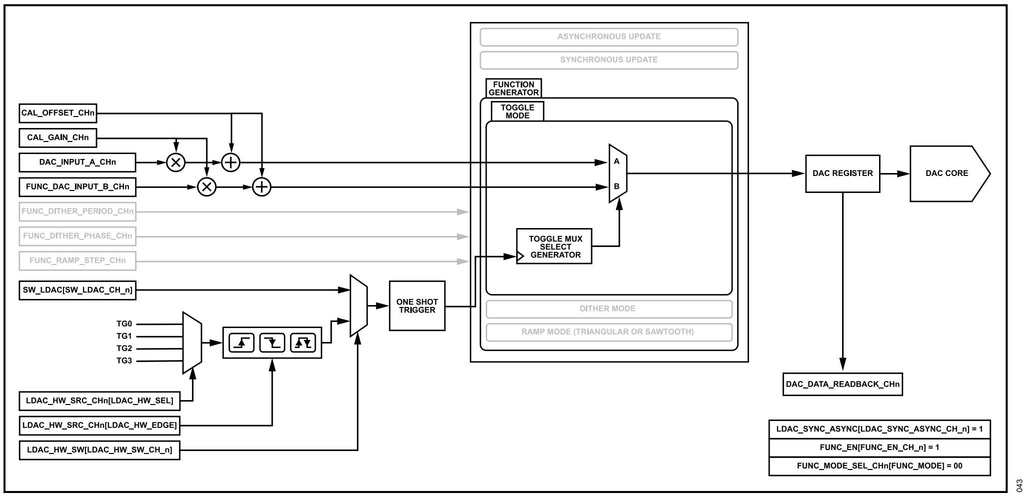

Figure 46. Toggle Block Diagram

The recommended sequence to enter toggle mode is as follows:

1. Configure the trigger type by programming the Hardware-Software Trigger Register to select either a hardware toggle or a software toggle.
2. Configure the trigger mechanism. If hardware toggle is selected (LDAC_HW_SW = 0), select the required toggle pin and triggering edge polarity (rising, falling, or either) in the LDAC Hardware Pin and Edge Select Register. If software toggle is selected (LDAC_HW_SW = 1), configure software triggering by the Individual Channel Software LDAC Register.
3. Write the two DAC codes to be toggled between into Primary DAC Input Register and Secondary DAC Input Register.
4. Enable the channel output through the Output Enable Register.
5. Apply the pre configured toggle source.

Figure 47 shows the programming flow for toggle mode.

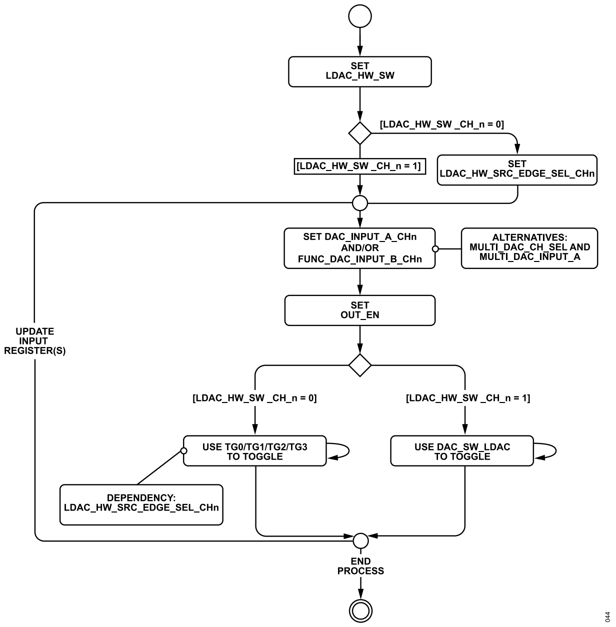

Figure 47. Toggle Flow Diagram

THEORY OF OPERATION

Updates to Primary DAC Input Register and Secondary DAC Input Register are edge triggered. The DAC only updates on the selected trigger edge, so the opposite edge produces no change. Because of this, two trigger edges may be required for the new code to fully propagate, which ensures the output moves only between valid A and B codes.

An example of toggling on the rising edge and any edge are shown in Figure 49 and Figure 48.

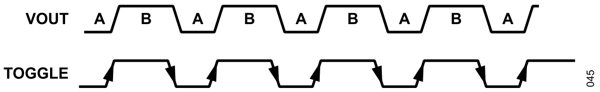

Figure 48. Toggling on Both Edges

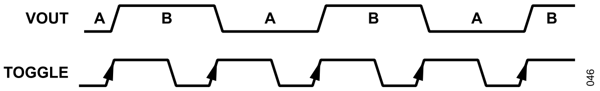

Figure 49. Toggling on the Rising Edge

THEORY OF OPERATION

Dither Function

A dither signal generator injects a digital dither signal into the DAC signal path. The AD5529R generates a sinusoidal output with the transfer function, as shown in Figure 50:

$$D\left(n\right) = \sin\left(\frac{(2\times\pi\times \mathrm{n})}{N} + \varphi\right)$$

where:

n = 0, 1, 2 … N-1.

N is the signal period.

φ is the initial signal phase.

The dither clock source and the parameters *N* and *φ* are programmable per-channel, which allows independent control of dither frequency and relative alignment across all AD5529R channels. For each channel of the AD5529R, the user can choose any of the four TG[0:3] pins or the software toggle bit as the dither clock.

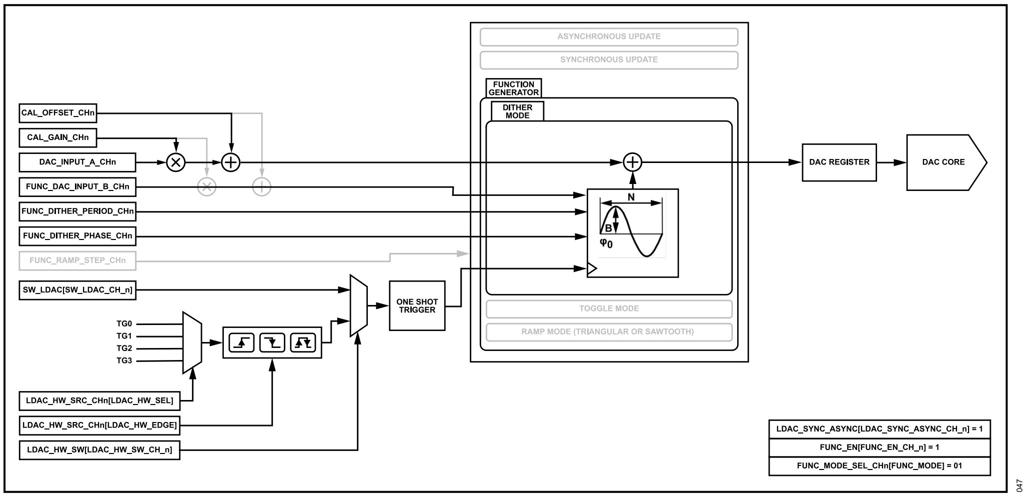

Figure 50. Dither Block Diagram

Before entering the digital DAC signal path, the sinusoidal dither D(n) is combined with the programmed offset and amplitude values held in Input Register A and Input Register B. This operation produces the final DAC data value, as shown in the following equation:

$$DAC\_REGISTER = DAC\_INPUT\_A\_CHn \quad + \\ FUNC\_DAC\_INPUT\_B[13{:}0] \times D(n)$$

Only DAC_INPUT_A_CHn is gain and offset adjusted when in dither mode.

To limit the dither amplitude to ¼ of the configured range, only the lower 14 bits of FUNC_DAC_INPUT_B are used.

The dither signal frequency can be set per-channel by writing to the Dither Period Select Register, with the following options, as shown in Table 17.

Table 17. Dither Period

DITHER_PERIOD[2:0]	N	Output Signal Frequency
000	128	$f_{TOGGLE}/128$
001	64	$f_{TOGGLE}/64$
010	32	$f_{TOGGLE}/32$
011	16	$f_{TOGGLE}/16$
100	8	$f_{TOGGLE}/8$
101	4	$f_{TOGGLE}/4$
110	2	$f_{TOGGLE}/2$

THEORY OF OPERATION

The lookup table for the sine function for the seven different N options is shown in Table 18.

Table 18. Dither Signal Generator Lookup Table Using DITHER_PERIOD[2:0] Bits

Dither Sample	fclk/2	fclk/4	fclk/8	fclk/16	fclk/32	fclk/64	fclk/128
0		=	=	=	=	=	0.0
1							0.04907
2						=	0.09790
3							0.14673
4					=	=	0.19507
5							0.24292
6						=	0.29028
7							0.33691
8				=	=	=	0.38257
9							0.42749
10						=	0.47144
11							0.51416
12					=	=	0.55566
13							0.59570
14						=	0.63428
15							0.67163
16			=	=	=	=	0.70703
17							0.74097
18						=	0.77295
19							0.80322
20					=	=	0.83154
21							0.85767
22						=	0.88184
23							0.90405
24				=	=	=	0.92383
25							0.94165
26						=	0.95703
27							0.96997
28					=	=	0.98071
29							0.98926
30						=	0.99512
31							0.99878
32	=	=	=	=	=	=	1

THEORY OF OPERATION

Blank cells indicate no additional values required for N.

No other setting is allowed. Figure 51 shows this mechanism.

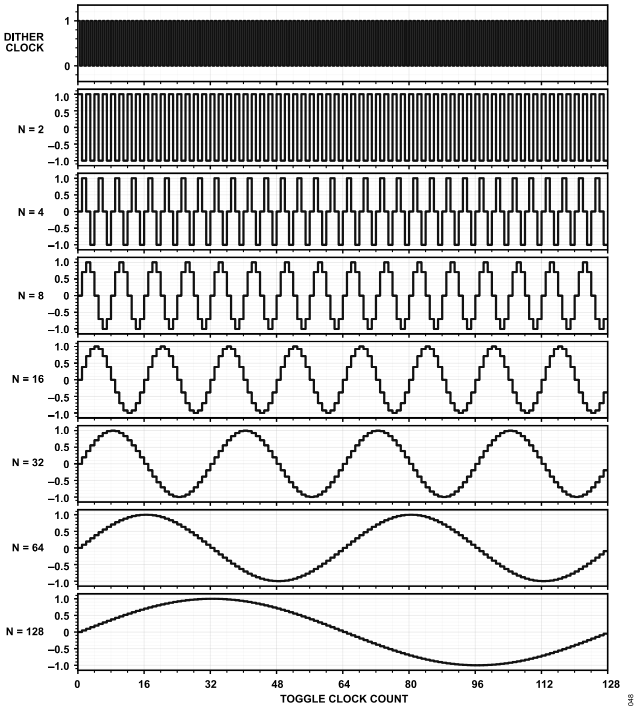

Figure 51. Sinusoidal Waveforms for Various Values of Dither Period N

For example, a toggle frequency of 500kHz is used along with a DITHER_PERIOD of N = 8:

$$Dither\ Output\ Frequency = \frac{500kHz}{8} = 62.5kHz$$

The number of discrete update points and the magnitude of each point, D(n), are determined by the programmed dither frequency. Each point is updated on the selected edge of the dither clock, with one update occurring per dither clock period.

The dither phase (φ, initial phase angle) can be set per-channel by writing to the Dither Phase Select Register[1:0] bits. The four options supported are shown in Table 19:

Table 19. Dither Initial Phase

DITHER_PHASE[1:0]	Initial Dither Phase (φ)
00	0°
01	90°
10	180°
11	270°

Note that if the initial dither phase (φ) is set to 90° or 270°, the first N/4 clock does not produce dither outputs. This is to avoid the transient that occurs upon transitioning to the first point of the dither. The output stays at DAC_INPUT_A_CHn.

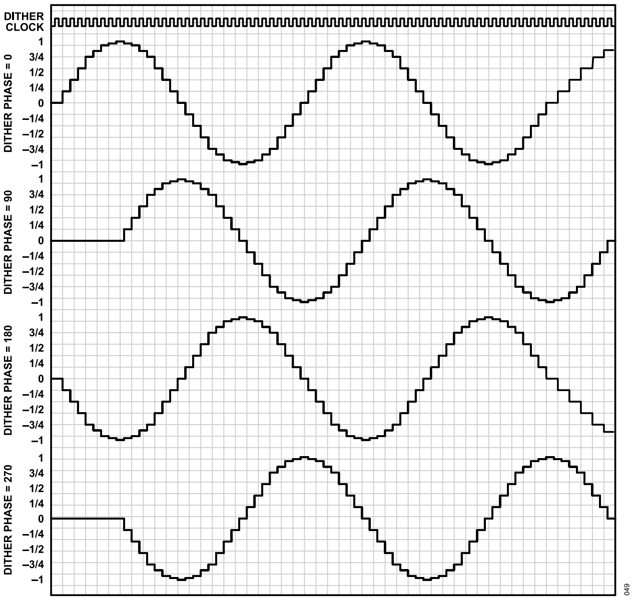

Figure 52. Dither Waveform for Different Values of φ

To start the dither mode, program the device as follows:

1. Select the required dither trigger source in the Hardware-Software Trigger Register. If a hardware trigger is selected, configure the toggle pin and trigger edge (rising, falling, or either) in LDAC Hardware Pin and Edge Select Register. If a software trigger is selected, configure the Individual Channel Software LDAC Register.
2. Program dither DC level and amplitude. Write the required DC value of the dither waveform to Primary DAC Input Register. Write the required dither amplitude to Secondary DAC Input Register.
3. Configure dither parameters. Set the dither period using Dither Period Select Register[2:0]. Set the initial dither phase using Dither Period Select Register[1:0].
4. Enable the output of the required channels by configuring the Output Enable Register.
5. Apply the selected trigger to start dither operation.

Exiting dither mode, to exit the dither mode, do the following steps:

1. Disable dither function by setting the required channels bit low in the FUNC_EN register.
2. Dither keeps running until users apply enough dither clocks to finish a dither period, when D(n) = 0.

THEORY OF OPERATION

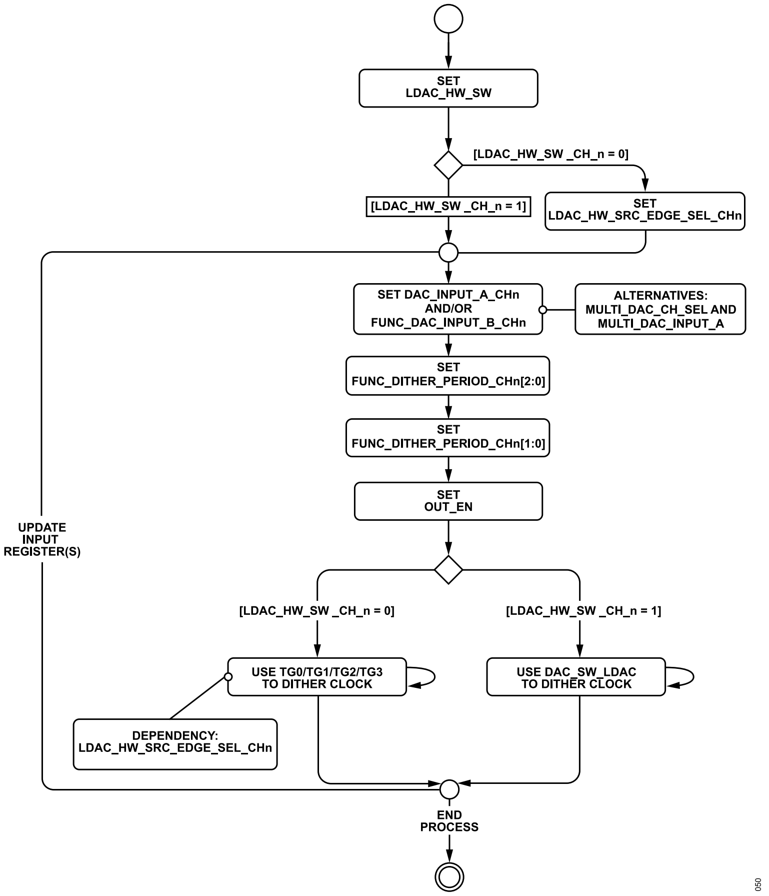

Figure 53. Dither Flow Diagram

THEORY OF OPERATION

Ramp Function

Ramp function mode enables generation of a ramp waveform by applying a clock to the toggle pins, which eliminates the need for continuous SPI communication and offloading this task from the external controller. Two ramp shapes are supported, sawtooth and triangular. The required ramp shape is selected using the Function Mode Select Register. The ramp function always starts at the Primary DAC Input Register code and descends if > Secondary DAC Input Register code or ascend based on if its < Secondary DAC Input Register code. If DAC_INPUT_A_CHn = FUNC_DAC_INPUT_B_CHn, no ramp is generated. A ramp block diagram is shown in Figure 54.

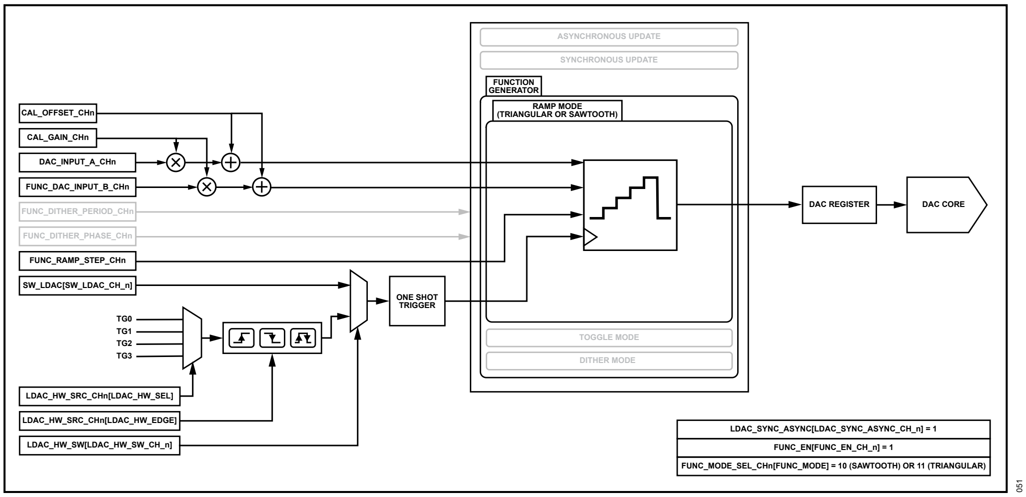

Figure 54. Ramp Block Diagram

THEORY OF OPERATION

Figure 55 and Figure 56 show sawtooth ramp operation for two different step configurations. When the programmed step size results in an integer number of output updates between start and end, the ramp transitions with uniform step sizes (see Figure 56). When the step size does not divide evenly into the start to end range, the final step is reduced in magnitude to reach the programmed end value, as shown in Figure 55.

- Primary DAC Input Register = d100
- Secondary DAC Input Register = d800
- Ramp Step Register = d130

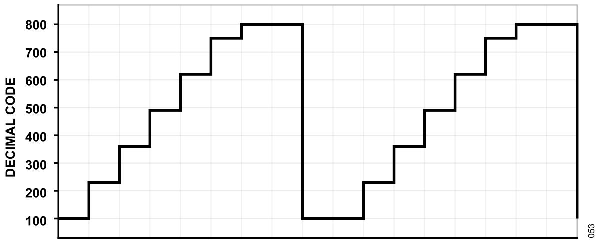

Figure 55. Sawtooth Ramp with Truncated Final Step

- Primary DAC Input Register = d100
- Secondary DAC Input Register = d800
- Ramp Step Register = d140

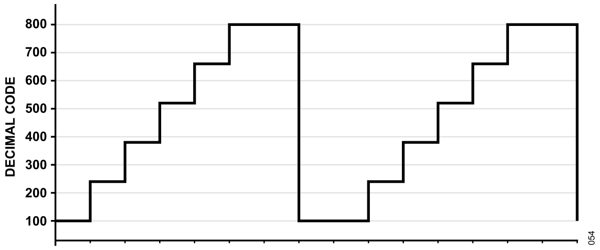

Figure 56. Sawtooth Ramp with Uniform Step Size

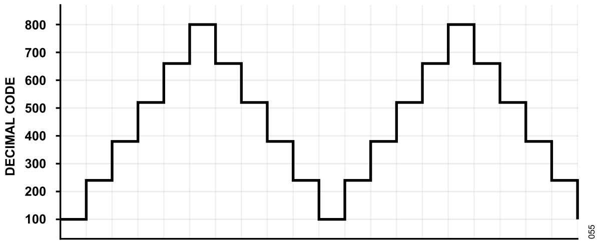

Figure 57. Triangle Ramp with Uniform Step Size

The voltage change per ramp step is given by the product of the programmed ramp step and the DAC LSB voltage, which is defined by the selected output range:

$$\Delta V_{STEP} = \frac{Range\ \ Span(V)}{2^{16}} \times FUNC\_RAMP\_STEP$$

To start ramp mode, program the device as follows:

1. Select the required ramp clock source using the Hardware-Software Trigger Register. If a hardware clock source is selected, configure the toggle pin (TG[3:0]) and trigger edge polarity in LDAC Hardware Pin and Edge Select Register. If a software trigger is selected, configure the Individual Channel Software LDAC Register.
2. Program ramp start and end values, write the ramp start value to Primary DAC Input Register. Write the ramp end value to Secondary DAC Input Register.
3. Program the ramp step size by writing to the Ramp Step Register. This setting defines the increment applied between the programmed ramp start and end values.
4. Enable the output of the required channels by configuring the Output Enable Register.
5. Apply the selected hardware or software clock source to begin ramp operation.

Figure 58 shows the ramp flow diagram.

Exiting the ramp function, to exit the ramp function, do the following steps:

1. Disable the ramp function by setting the required channels bit low in the FUNC_EN register.
2. The ramp function keeps running until there is enough dither clocks applied to reach the Primary DAC Input Register code.

THEORY OF OPERATION

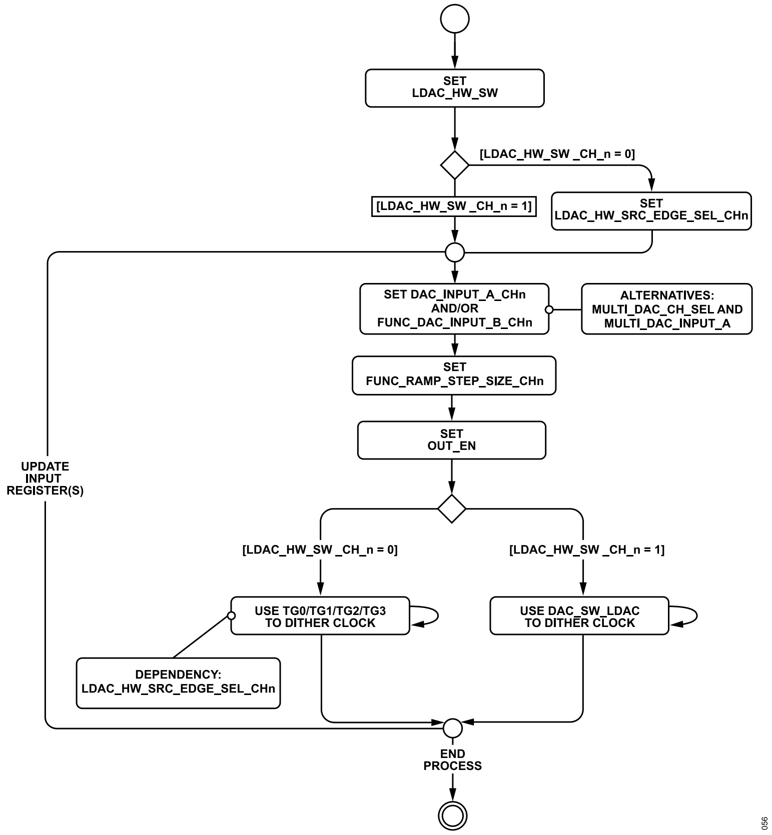

Figure 58. Ramp Flow Diagram

THEORY OF OPERATION

Function Restart

The function generator restart behavior is determined by how the corresponding bit in the Function Enable Register is controlled. Each bit independently enables or disables the function generator for its associated channel.

FUNC_EN Bit Cleared and Held Cleared

Clearing the FUNC_EN bit disables the function generator. When the bit is held low, the device continues to advance through the remaining toggle events of the current waveform period. The output returns to the DAC_INPUT_A_CHn code only after the required number of toggle pulses have been applied. No further waveform activity occurs while FUNC_EN remains low (see Figure 59).

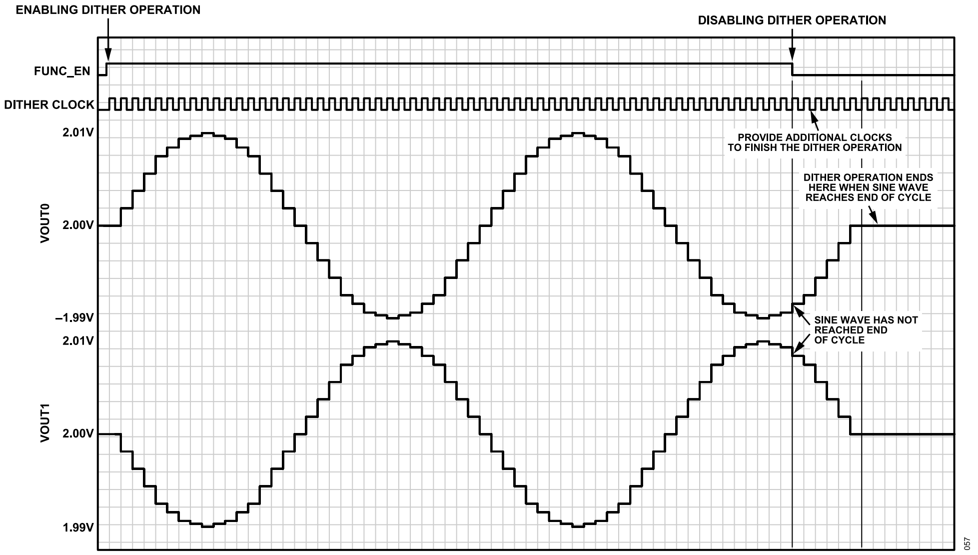

Figure 59. Ending Dither Waveform Output

FUNC_EN Bit Cleared and Then Set Again

Momentarily clearing and then resetting a channel's FUNC_EN bit forces an immediate restart of that channel's function generator. In this condition, the AD5529R skips any remaining toggle events associated with the active period and drives the output directly back to the programmed DAC_INPUT_A_CHn code (see Figure 60).

All previously configured function generator parameters for that channel remain unaffected.

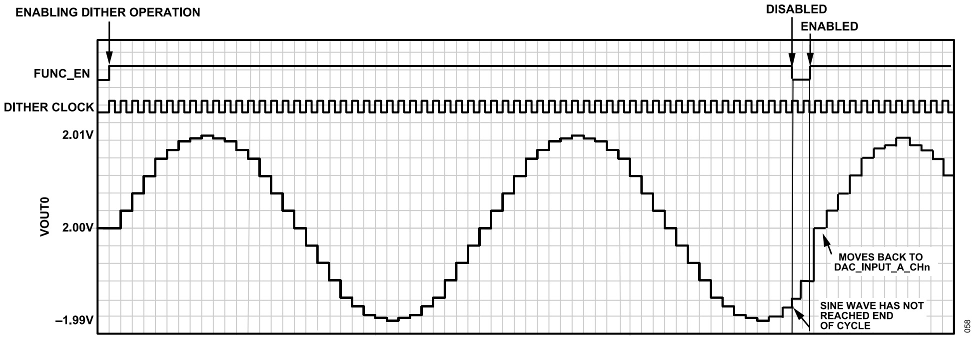

Figure 60. Restarting Dither Waveform Output

THEORY OF OPERATION

Function Generator Flags

The AD5529R includes several status and interrupt flags to indicate the operating state and completion of the function generator.

Function Generator Busy Live Flags Register: This is a live status flag that indicates whether the function generator on a given channel is active. The flag asserts when a function is enabled and remains asserted for the duration of the function generator operation. The flag deasserts immediately if the channel is switched to asynchronous update mode. If a function is disabled while the channel is not at an endpoint, FGEN_BUSY remains asserted until sufficient toggle events occur to complete the current function period and return the output to Primary DAC Input Register, after which the flag deasserts. Performing a function restart followed by disabling the function generator also causes FGEN_BUSY to deassert.

Function Interrupt Status Register: This is a per-channel sticky status flag that asserts when a falling edge is detected on the corresponding channel's FGEN_BUSY flag, which indicates completion of a function generator operation. The flag does not assert if the function generator is disabled as a result of switching the channel to asynchronous update mode. If the function generator is never enabled for a channel, the corresponding FUNC_INT_STAT bit remains low.

Function Interrupt Enable Register: This register allows each channel to be selected as a contributor to the global function complete interrupt. Setting a bit means that the channel's function-complete status can feed into the ALL_FUNC_INT_STAT register.

Function Interrupt Status Register: This register contains a single global sticky flag. It sets when all channels selected in the FUNC_INT_EN register have completed their function generator cycles. The bit can be routed to the $\overline{\text{ALARM}}$ pin. It is cleared using write 1 to clear, and only the channels that contribute to it are affected while ALL_FUNC_INT_EN is enabled.

Combined Function Generators Status Register: This register enables the global ALL_FUNC_INT_STAT interrupt path. When enabled, the value of ALL_FUNC_INT_STAT can drive the $\overline{\text{ALARM}}$ pin. For more details, see the $\overline{\text{ALARM}}$ Function section.

OVERTEMPERATURE SHUTDOWN

The AD5529R provides overtemperature protection using one temperature sensor per DAC channel pair. When the measured junction temperature reaches 130°C, both channels associated with the sensor are forced into power-down, and the DAC cores and output stages for the pair are disabled. Temperature sensing for that pair remains disabled until the channels are reenabled. If the over temperature condition persists when the pair is reactivated, the temperature sensor immediately reasserts shutdown.

To enable overtemperature shutdown for a DAC pair, do the following steps:

- Enable the temperature sensor associated with the DAC pair in the Temperature Sensors Enable Register. The default is disabled.
- Set the corresponding shutdown enable bits in the Disable Channel by Temp Sensor Shutdown Register.

Once both the temperature sensor and shutdown-enable bits are configured, the DAC pair is protected and automatically shuts down when the monitored temperature reaches 130°C.

During an overtemperature event, the device applies the same power-down path used by the Output Enable Register, pulling the output pin toward GND through an effective resistance of approximately 28kΩ, and the digital logic updates the corresponding Output Enable Register fields to indicate that power-down has been asserted for the affected channels.

$\overline{\text{ALARM}}$ FUNCTION

The AD5529R asserts the $\overline{\text{ALARM}}$ pin low, if configured to do so, when any of the following conditions occur:

1. Overtemperature alert: When $T_J > 110°C$.
2. Overtemperature shutdown: When $T_J \geq 130°C$.
3. SPI_CRC error: If enabled. If a CRC error occurs at the end of a frame, and no more frames occur, then the bit does not get set until the next SPI frame.
4. Digital functions completion.

If multiple events are configured to assert the $\overline{\text{ALARM}}$ pin, the user must read back the status registers to identify the source.

Figure 61 shows the conditions that drive the $\overline{\text{ALARM}}$ pin.

THEORY OF OPERATION

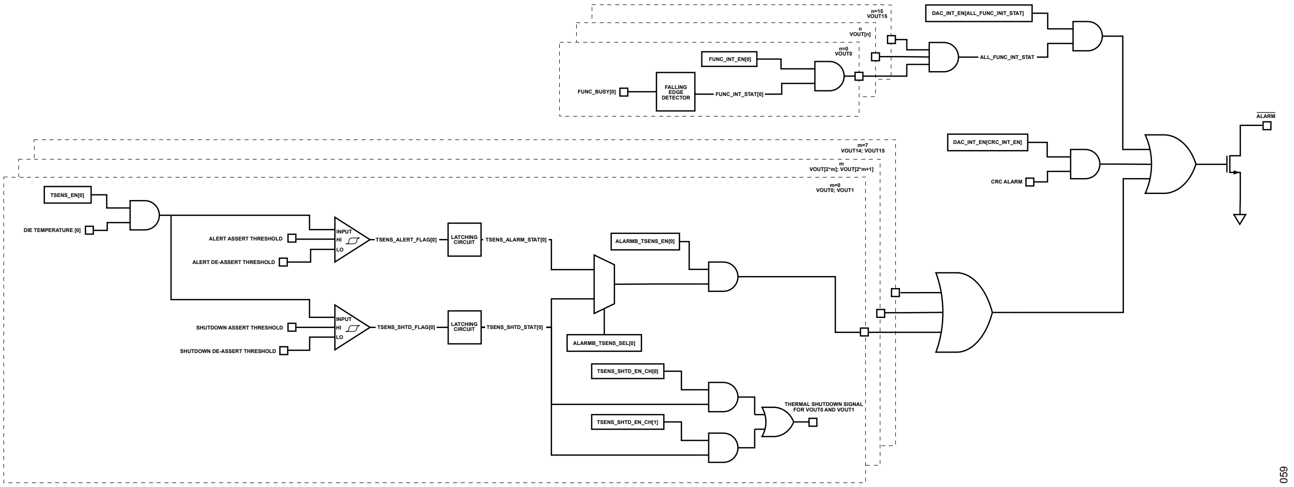

Figure 61. ALARM Block Diagram

Temperature Alarm

The AD5529R includes a set of registers that control temperature sensing, status reporting, and alarm generation.

Temperature Sensors Enable Register: Enables or disables the temperature sensors. Each bit controls the power state of an individual temperature sensor, which must be powered up for temperature status reporting or alarm functions to operate. Each temperature sensor monitors two DAC output amplifiers, and all sensors are powered down by default.

Temperature Sensors Alert Live Flags Register and Temperature Sensors Shutdown Live Flags Register: These registers report the status of the two temperature flags available in the AD5529R. The alert flag asserts when a temperature sensor exceeds 110°C, and the shutdown flag asserts when a temperature sensor exceeds 130°C. Both this flags can be read live in these register locations.

Temperature Sensors Status to ALARM Pin Enable Register: Enables the latched temperature alert and shutdown status for each temperature sensor to assert the ALARM pin.

Alert/Shutdown Status Signals to ALARM Pin Select Register: This register decides which temperature sensor latched status (alert or shutdown, 110°C or 130°C) are redirected to the ALARM pin.

After ALARM is asserted, users must read the TSENS_ALERT/SHTD_STAT registers to determine the cause of the fault. The latched flag/shutdown signals can only be cleared after writing 1 to the latched flag/shutdown status bits.

Digital Functions Completion

The AD5529R can indicate when all digital functions on the enabled channels have completed. The ALL_FUNC_INT_STAT register reports the completion status of the digital functions. When the ALL_FUNC_INT_EN[0] bit in the DAC Interrupts Enable Register is set, this status flag is permitted to drive the ALARM pin.

CRC Alarm

The AD5529R can be configured to assert the ALARM pin when an SPI CRC error occurs by enabling the CRC_INIT_EN bit in the DAC Interrupts Enable Register. When CRC checking is enabled, a CRC error flag is generated if a frame fails the CRC check. If the CRC error occurs at the end of an SPI frame and no subsequent frames are received, the error flag is not set until the next SPI frame.

Hardware Reset

RESET is an active low signal, falling edge sensitive. Asserting RESET places the device in the power-on-reset (POR) state. While RESET is held low, all SPI transactions toggle pulses are ignored, and the SDO output remains in a high-Z state.

When RESET is released, the digital core performs its initialization sequence and resets all AD5529R registers to their default values.

CLEAR FUNCTION

The CLEAR function resets only the DAC data registers and does not affect any device configuration settings. This differs from a full device RESET, which reinitializes the entire device and restores all registers to their default values. The AD5529R CLEAR pin is active low. When asserted, all powered-up DAC channels are loaded with their default clear codes based on their programmed output range:

- Unipolar Ranges: Outputs return to zero scale (0V).
- Bipolar Ranges: Outputs return to midscale (0V).

All configuration registers retain their previously programmed settings after a CLEAR event. If the CLEAR pin is unused, it must be connected to VDD_IO.

Software Reset

If using the software reset, this can be done by setting the SW_RESET and RESET_SW bits in the INTERFACE_CONFIG_A register. Both bit fields must be written during the same data phase to

THEORY OF OPERATION

successfully initiate a software reset. Following the reset command, the device runs the POR sequence and initializes the digital core, which returns all DAC registers to their default values except for INTERFACE_CONFIG_A.

SPI INTERFACE

The AD5529R uses a 4-wire serial interface ($\overline{\text{CS}}$, SCLK, SDI, and SDO) that is compatible with classic SPI, QSPI™, and MICROWIRE® interface standards, as well as most DSPs. Data is sampled by the AD5529R on the positive (rising) edge of the clock. This corresponds to either SPI mode 0 or mode 3. The AD5529R supports also a 3-wire bidirectional ($\overline{\text{CS}}$, SCLK, and SDIO) serial interface. Also, the AD5529R supports multidevice addressing, up to four devices can be connected sharing the SPI interface. Several AD5529R can be placed in the same bus with their registers being placed in different addresses in the 16-bit address range.

The interface allows device addressing during the 16-bit instruction phase. This phase consists of the R/W bit, followed by 3 bits [0, ID1, ID0], and then a 12-bit register address. Figure 63 shows a classic read to a single byte register.

The $\overline{\text{CS}}$ pin frames data during a SPI transaction. A falling edge on $\overline{\text{CS}}$ enables the digital interface and initiates an SPI transaction. Each SPI transaction consists of at least one instruction phase and data phase. For all SPI transactions, data is aligned most significant bit (MSB) first. If $\overline{\text{CS}}$ goes high during a SPI transaction, then it terminates part or all the data transfer and disables the digital interface. If $\overline{\text{CS}}$ goes high after one or more registers are written, those completed registers are written or read, but any partial written register is aborted.

In multidevice addressing mode, only the addressed device drives SDO pin during the data phase. SDO pin is never driven during the instruction phase.

Instruction Phase

The instruction phase comprises a read/write (R/W) bit, followed by a 3-bit device ID field and a register address word. Driving the R/W bit low selects a write operation, while driving it high selects a read operation. The register address field defines the target register. The three MSBs of the address must be [0, ID1, ID0], where ID1 and ID0 correspond to the logic levels applied to the ID1 and ID0 address pins of the addressed device. This addressing scheme allows up to four AD5529R devices to share a common SPI bus. The register address word is 12-bit in length by default.

Data Phase

The data phase immediately follows the instruction phase. The data phase can include the data for a single-byte register, a multibyte register, or multiple registers. For multibyte registers all bytes must be entered during the CS frame, if the data phase of a SPI write transaction does not include entire bytes of data for the register being updated, the contents of the register are not updated, and the Interface_Status_A Register [Register_Partial_Access_Err] bit is set. Figure 62 shows a classic write to a multibyte register.

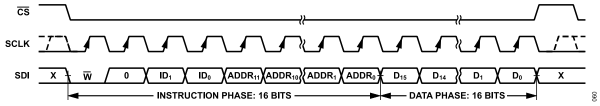

Figure 62. SPI Write Sequence

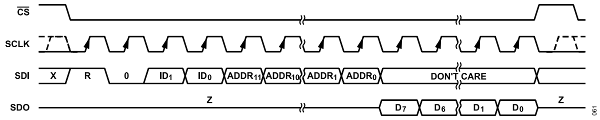

Figure 63. SPI Read Sequence

Multibyte Registers

Besides the 1-byte registers, there are registers with 2 bytes of data stored in jumps of two addresses and are referred to as multibyte registers. When writing to a multibyte register, all bytes must be accessed in a single SPI transaction. For this reason, the Interface_Config_C [Strict_Register_Access] bit is read only and set to 1.

A write transaction to a multibyte register takes effect after the 16th SCLK edge of the data phase, unless CRC is enabled, in which case, the write happens after 8th edge of the CRC phase.

The address of a multibyte register always depends on the Interface_Config_A [Addr_Direction] bit. With addresses descending, the first byte accessed in the data phase must be the most significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next lowest address. With addresses ascending, the first byte accessed in the data phase must be the least significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next highest address.

If a SPI write transaction to a multibyte register is attempted on a per byte basis, the register contents are not updated on the device, and the Interface_Status_A [Partial_Register_Access] bit is set. For example, the DAC_INPUT_A_CHn register is two bytes long, and the addresses of its least significant byte and most significant byte are 0x0148 and 0x0149, respectively.

Address direction is selected with the Interface_Config_A [Addr_Direction] bit, if this bit is set to 0, the address decrements after each byte is accessed. If this bit is set to 1, the address increments after each byte is accessed. This bit is the only one, in the entire register map, that does not reset with a software reset. Figure 64 shows a write to a multibyte register where the Addr_Ascension is selected as decrement.

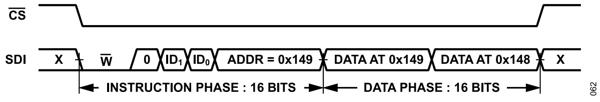

Figure 64. SPI Multibyte Write, Descending Address

THEORY OF OPERATION

Streaming Mode

When the Interface_Config_B [Access_Mode] bit is set to 0, single instruction mode is disabled, and streaming mode is enabled. In streaming mode, multiple registers with adjacent addresses can be accessed with a single instruction phase and data phase, which allow efficient access of contiguous regions of memory (for example, during initial device configuration). The streaming mode is selected by default.

When in streaming mode, each SPI frame consists of a single instruction phase and the following data phase contains data for multiple registers with adjacent addresses. A starting register address is specified by the digital host in the instruction phase, and this address is automatically incremented or decremented (based on the address direction setting) after each byte of data is accessed. The data phase can therefore be multiple bytes long, and each consecutive byte of read or write data corresponds to the next highest or lowest register address (for ascending and descending address direction, respectively).

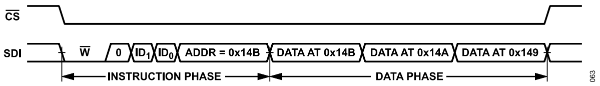

Figure 65. SPI Streaming Mode

When writing to a multibyte register in streaming mode with address ascending, the user must address the least significant byte of the register in the instruction phase and provide data starting from the least significant byte in the data phase. When writing to a multibyte register in streaming mode with the address descending, the user must start addressing the most significant byte of the register in the instruction phase and provide data starting from the most significant byte in the data phase.

When reading from a multibyte register in streaming mode with address descending, read back the data starting from the most significant byte. When reading from a multibyte register in streaming mode with address ascending, read back data starting from the least significant byte.

The STREAM_MODE register can be used to specify a set of consecutive registers to loop through in the data phase. Looping allows the digital host to repeatedly read from or write to a set of registers as efficiently as possible.

If address direction is set to descending, the address decrements until it reaches address 0x00. On the subsequent byte access, the address is set to the highest valued byte address available.

If address direction is set to ascending, the address increments until it reaches the highest valued byte address available. On the subsequent byte access, the address is reset to 0x00.

If STREAM_MODE is set to a value other than 0, looping is enabled, and the value in STREAM_MODE sets the number of bytes to be accessed in a single data phase before the byte address resets to the one specified in the instruction phase.

The value of the STREAM_MODE[LOOP_COUNT] register can be kept or returned to the default value of 0 when the frame transaction is completed, that is, $\overline{\text{CS}}$ brought high. The way that the STREAM_ MODE behaves is controlled by the bit TRANSFER_REGISTER[STREAM_LENGTH_KEEP_VALUE].

THEORY OF OPERATION

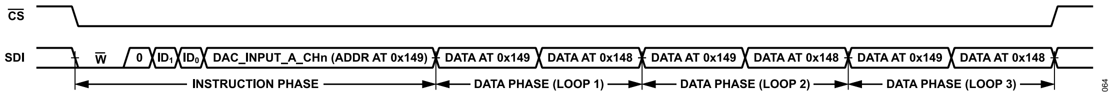

Figure 66. SPI Streaming Mode LOOP_COUNT = 2

Single Instruction Mode

When the Interface_Config_B [Access_Mode] bit is set to 1, streaming mode is disabled, and single instruction mode is enabled. In single instruction mode, the data phase consists of data for a single register, and each data phase must be followed by a new instruction phase (even if $\overline{\text{CS}}$ remains low). Single instruction mode allows the digital host to quickly read from and write to registers with nonadjacent addresses in a single SPI frame, whereas streaming mode only allows either reading or writing to contiguous registers without pulsing $\overline{\text{CS}}$ high to initiate a new instruction phase.

When accessing multibyte registers in single instruction mode, data phase should cover all the bytes in a multibyte register, and the register address is still dependent on the Interface_Config_A [Addr_Direction] bit.

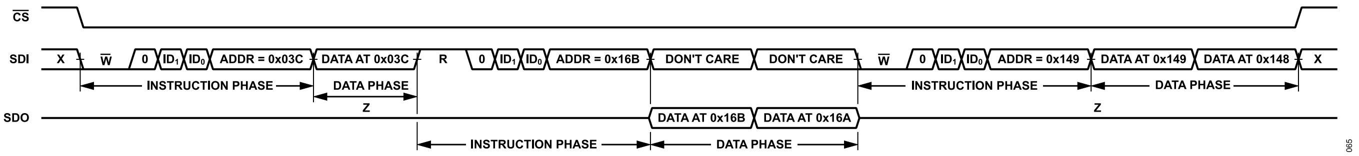

Figure 67. SPI Single Instruction Mode

Device Addressing

The AD5529R provides two device-address pins (ID[1:0]) on the WLCSP package to support multiple devices operating on the same SPI bus. With four unique address combinations, up to four AD5529R devices can share the interface, which allow a host controller to access as many as 64 independently configurable DAC channels.

The logic levels applied to ID0 and ID1 define the device address, as shown in Table 20.

During SPI communication, the instruction phase includes two address bits that must match the logic levels on the ID[1:0] pins for a device to accept the command. Only the addressed device responds to SPI read and write operations. A typical four-device SPI connection using AD5529R WLCSP devices is shown in Figure 68.

Table 20. Device Addressing Truth Table

Address Pins ID[1:0]	Device Identity	Address Bits, [14:12], in Instruction Phase
0 0	0	0 0 0
0 1	1	0 0 1
1 0	2	0 1 0
1 1	3	0 1 1

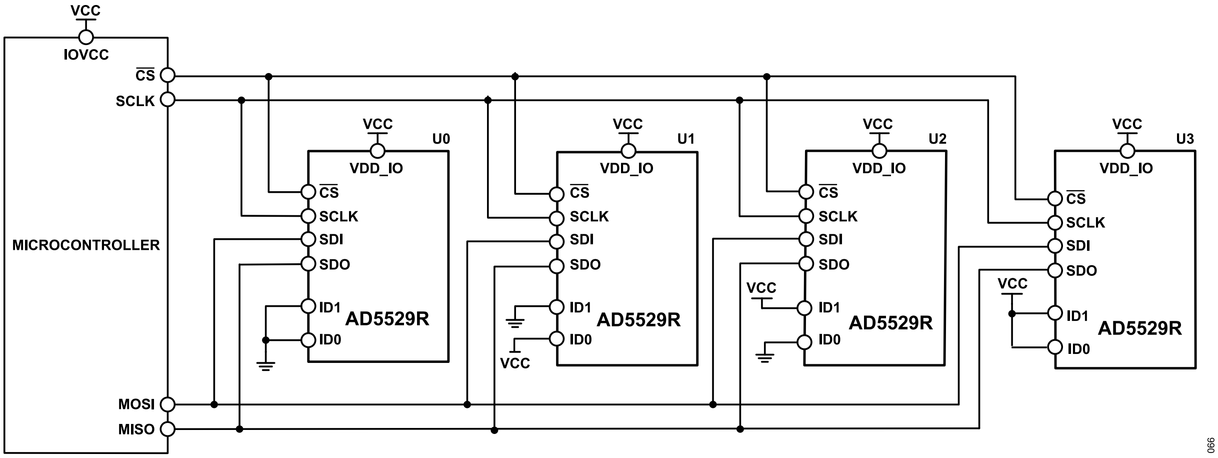

Figure 68. AD5529R WLCSP Daisy-Chain Configuration

THEORY OF OPERATION

CRC Error Detection

The AD5529R DACs feature optional cyclic redundancy checks (CRCs) to provide error detection for SPI transactions between the digital host and the DAC (target). The CRC error detection is disabled by default. The CRC error detection allows the SPI host and targets to detect bit transfer errors with significant reliability. The CRC algorithm involves using a seed value and polynomial division to generate a CRC code. The controller and target both calculate the CRC code independently to determine the validity of transferred data.

This DAC uses the CRC-8 standard with the following polynomial:

$$x^8 + x^2 + x + 1 \tag{1}$$

CRC error detection is enabled with the CRC_EN and CRC_EN_B bits in the INTERFACE_CONFIG_C register. The value of CRC_EN is only updated if CRC_EN_B is set to the CRC_EN inverted value in the same register write instruction. Therefore, to enable the CRC, the CRC_EN must therefore be set to 0b01 while CRC_EN_B is set to 0b10 in the same write transaction.

To disable the CRC, the CRC_EN must be set to 0b00 and the CRC_EN_B is set to 0b11 in the same write transaction.

Writing inverted values to two separate fields reduces the chances of CRC being enabled in error. The $\overline{\text{CS}}$ must be brought high at the end of the enable/disable write. The first CRC code must be included after the register write/read data, immediately following the register write transaction enabling the CRC. A register write transaction that disables the CRC must still include the CRC code on SDI, but the following transaction does not require the CRC code.

Figure 69 and Figure 70 show how a CRC code is appended to the write or read, respectively, for the digital host or DAC to validate the data. For register writes, the digital host must generate the CRC using the calculation described in Equation 1. For register reads, the host must also send the correct CRC byte that is checked by the DAC. The first byte of data sent contributes to the CRC calculation. Therefore, a value of 0x00 is recommended. In the same read transaction, the DAC provides the CRC code for the digital host to verify.

When accessing multibyte registers with the CRC error detection enabled, the CRC code is placed after all bytes of register data. When the CRC error detection is enabled, the DAC does not update its register contents in response to a register write transaction unless it receives a valid CRC code at the end of the register data on the SDI. If the CRC code is invalid, or the digital host fails to transmit the CRC code, the AD5529R do not update the register contents, and the CRC_ERR flag in the INTERFACE_ STATUS_A register is set. The CRC_ERR flag is write-1-to-clear (R/W1C) and the correct CRC is required for the write to clear to take effect.

Table 1 shows the seed value used in the CRC code calculation and how it is transmitted for both single instruction mode and streaming mode. When using single instruction mode, every CRC code in a SPI frame uses 0xA5 as the seed value to prevent stuck at fault conditions for Address 0x0000.

When using the streaming mode, the first CRC code in a SPI frame also uses 0xA5 as the seed value, but subsequent CRC codes in the same frame are calculated using the LSB of the register address being accessed in the SPI transaction as the seed value.

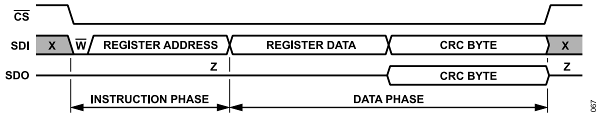

Figure 69. SPI Write with CRC Enabled

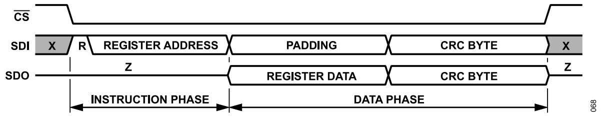

Figure 70. SPI Read with CRC Enabled

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

The pin configurations of the AD5529R are arranged in a way that facilitates optimal layout. Most digital high-speed lines are located on one side of the chip, with the analog functions of each DAC distributed along the other three sides. This arrangement allows the routing of digital lines straight away from the analog functions.

The following are some PCB design recommendations to obtain the best for the AD5529R:

- Ensure that power supply lines have as large a trace as possible to provide a low-impedance path to reduce glitch effects.
- A low-impedance analog ground plane and star grounding techniques are recommended. It is advised to keep the ground layer continuous to minimize ground resistance.
- Shield clocks and other fast switching digital signals from other parts of the signal by using a digital ground.
- Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at 45° or 90° angles to each other to reduce feedthrough affects on the board.
- For clock rates around the device maximum of 50MHz, it is advised to add series resistors near the source I/O pins. Values from 22Ω to 100Ω are commonly used and help to improve signal integrity by reducing ringing and reflections caused from fast signal transitions.

When using the WLCSP package, follow the layout guidelines in Application Note AN-617: *Wafer Level Chip Scale Package*.

SUPPLY SETUP

Figure 71 shows a compliant voltage supply configuration. In this example, the four negative rails are biased at –20V (VSS_HV0), 0V (VSS_HV1), –15V (VSS_HV2), and –5V (VSS_HV3). The arrangement satisfies the requirement that VSS_HV0 be maintained equal to, or more negative than, VSS_HV1, VSS_HV2, and VSS_HV3. There are no specific requirements on the power-up sequence other than ensuring that all Absolute Maximum Ratings are respected even on a transient basis. Note that this typically implies powering VSS_HV0 before VSS_HV1, VSS_HV2, and VSS_HV3.

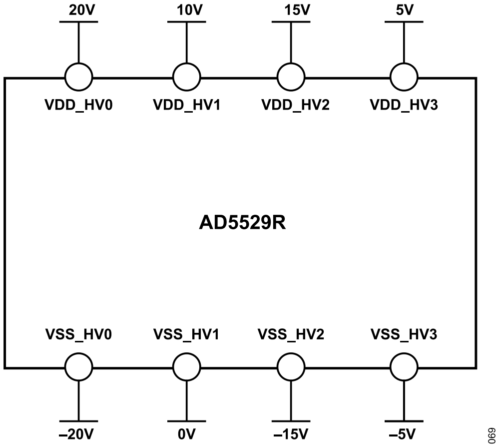

Figure 71. AD5529R VSS_HVX Supply Setup

CHANNEL DIAGNOSTICS IN SYSTEMS WHERE MULTIPLE AD5529RS SHARE SPI AND MUXOUT

In systems using multiple AD5529R, the architecture supports both the sharing of SPI lines and a single MUXOUT pin across up to four WLCSP devices. To avoid contention on the shared MUXOUT line, the AD5529R incorporates internal control logic that guarantees only one device drives the pin at any given time.

Whenever the MUX_OUT_SEL register is written, all devices momentarily place their MUXOUT pins into a high-impedance (Hi-Z) state. The device whose Device ID (ID0/ID1 pins) matches the addressed write transaction then drives the MUXOUT pin, while all nonaddressed devices remain in Hi-Z. This sequence occurs on every MUXOUT register write, which ensures deterministic, contention free operation. This mechanism is not relevant for single device configurations but is required for multidevice AD5529R systems sharing a common MUXOUT node.

DAC HOTPATH

The DAC hotpath is a dedicated register region that optimizes DAC updates in multidevice configurations where several AD5529R devices share a common SPI bus. It reduces the number of SPI frames required to write DAC data and supports synchronized output updates across devices. In single device systems, the hotpath offers no advantage over the standard register map and can be disregarded.

The DAC hotpath region refers to Multi Device SW LDAC Mode 0 Register to Input Device 3 Register inclusive.

APPLICATIONS INFORMATION

Software Trigger Control

The Multi Device SW LDAC Mode 0 Register provides per device software trigger control in multidevice configurations. The register contains four bits, with each bit corresponding to one device.

1. Writing a 1 to a bit triggers an update event for that device.
2. Writing 0x000F triggers an update event on all devices.

This allows selective or simultaneous DAC updates across multiple devices with a single SPI transaction

The Multi Device SW LDAC Mode 1 Register generates a software trigger event on all devices, but only for the selected channel. Setting a bit high in this register updates the corresponding channel number across every DAC connected to the SPI bus. This is useful when the same channel must be updated simultaneously on all devices.

DAC Updates

The AD5529R hotpath alias register map provides two mechanisms for updating the DAC_INPUT_A registers.

Per-Channel DAC Update

The INPUT_DEV[0 to 3]_CH registers provide a direct write path to the DAC_INPUT_A register of an individual channel. Each register is connected to a specific device address in the hotpath map, so a write updates only the channel associated with that dedicated die register, independent of the device address field in the SPI frame.

Multichannel DAC Update

The MULTI_INPUT_DEV_[0 to 3] registers provide a mechanism to update DAC_INPUT_A across multiple channels simultaneously. Channels that respond to this write are selected by the MULTI_INPUT_SEL register. A single write updates all selected channels on the addressed die with the same DAC code.

A summary is shown in Table 21.

Table 21. DAC Update Methods

Method	MULTI_INPUT_SEL	Actions to Update the Output
INPUT_DEV[0 to 3]_CH	Not used	Writing to this register updates only the addressed channel on the device whose ID0/ID1 pins match the hotpath address.
MULTI_INPUT_DEV_[0 to 3]	Channels selected	Writing to this register updates all channels selected in MULTI_INPUT_SEL with the same DAC code on the device whose ID0/ID1 pins match the hotpath address.

REGISTER SUMMARY

This section contains details about the functions of each of the bit fields. The access column in the register tables specifies whether the bit fields are read-only (R), read/write (R/W), write-1-to-clear (R/W1C), or register always reads as zero (R0/W) bits.

Table 22. AD5529R Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			RESET_SW	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	RESERVED							0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	STATUS_BIT_3	STATUS_BIT_2	STATUS_BIT_1	STATUS_BIT_0	RESERVED		OPERATING_MODE		0xF0	R
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x08	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x40	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x41	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x85	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x0F	TRANSFER_CONFIG	[7:0]	RESERVED					KEEP_STREAM_LENGTH_VAL	RESERVED		0x00	R/W
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		STRICT_REGISTER_ACCESS	RESERVED	ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x2F	R/W
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	REGISTER_PARTIAL_ACCESS_ERR	ADDRESS_INVALID_ERR	0x00	R/W
0x014	MULTI_INPUT_SEL	[15:8]	INPUT_SEL_CH_15	INPUT_SEL_CH_14	INPUT_SEL_CH_13	INPUT_SEL_CH_12	INPUT_SEL_CH_11	INPUT_SEL_CH_10	INPUT_SEL_CH_9	INPUT_SEL_CH_8	0x0000	R/W
		[7:0]	INPUT_SEL_CH_7	INPUT_SEL_CH_6	INPUT_SEL_CH_5	INPUT_SEL_CH_4	INPUT_SEL_CH_3	INPUT_SEL_CH_2	INPUT_SEL_CH_1	INPUT_SEL_CH_0		
0x016	LDAC_SYNC_ASYNC	[15:8]	LDAC_SYNC_ASYNC_CH_15	LDAC_SYNC_ASYNC_CH_14	LDAC_SYNC_ASYNC_CH_13	LDAC_SYNC_ASYNC_CH_12	LDAC_SYNC_ASYNC_CH_11	LDAC_SYNC_ASYNC_CH_10	LDAC_SYNC_ASYNC_CH_9	LDAC_SYNC_ASYNC_CH_8	0x0000	R/W
		[7:0]	LDAC_SYNC_ASYNC_CH_7	LDAC_SYNC_ASYNC_CH_6	LDAC_SYNC_ASYNC_CH_5	LDAC_SYNC_ASYNC_CH_4	LDAC_SYNC_ASYNC_CH_3	LDAC_SYNC_ASYNC_CH_2	LDAC_SYNC_ASYNC_CH_1	LDAC_SYNC_ASYNC_CH_0		
0x018	LDAC_HW_SW	[15:8]	LDAC_HW_SW_CH_15	LDAC_HW_SW_CH_14	LDAC_HW_SW_CH_13	LDAC_HW_SW_CH_12	LDAC_HW_SW_CH_11	LDAC_HW_SW_CH_10	LDAC_HW_SW_CH_9	LDAC_HW_SW_CH_8	0x0000	R/W
		[7:0]	LDAC_HW_SW_CH_7	LDAC_HW_SW_CH_6	LDAC_HW_SW_CH_5	LDAC_HW_SW_CH_4	LDAC_HW_SW_CH_3	LDAC_HW_SW_CH_2	LDAC_HW_SW_CH_1	LDAC_HW_SW_CH_0		
0x01A to 0x038 by 2	LDAC_HW_SRC_CHn	[15:8]	RESERVED						LDAC_HW_SEL_CH		0x0000	R/W
		[7:0]	RESERVED						LDAC_HW_EDGE_SEL_CH			
0x03A	OUT_EN	[15:8]	OUT_EN_CH_15	OUT_EN_CH_14	OUT_EN_CH_13	OUT_EN_CH_12	OUT_EN_CH_11	OUT_EN_CH_10	OUT_EN_CH_9	OUT_EN_CH_8	0x0000	R/W

REGISTER SUMMARY

Table 22. AD5529R Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
		[7:0]	OUT_EN_CH_7	OUT_EN_CH_6	OUT_EN_CH_5	OUT_EN_CH_4	OUT_EN_CH_3	OUT_EN_CH_2	OUT_EN_CH_1	OUT_EN_CH_0		
0x03C to 0x05A by 2	OUT_RANGE_CHn	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					OUT_RANGE_CH				
0x05C to 0x07A by 2	CAL_GAIN_CHn	[15:8]	RESERVED								0x0080	R/W
		[7:0]	CAL_GAIN_CH									
0x07C to 0x09A by 2	CAL_OFFSET_CHn	[15:8]	CAL_OFFSET_CH[15:8]								0x0000	R/W
		[7:0]	CAL_OFFSET_CH[7:0]									
0x09C	FUNC_EN	[15:8]	FUNC_EN_CH_15	FUNC_EN_CH_14	FUNC_EN_CH_13	FUNC_EN_CH_12	FUNC_EN_CH_11	FUNC_EN_CH_10	FUNC_EN_CH_9	FUNC_EN_CH_8	0x0000	R/W
		[7:0]	FUNC_EN_CH_7	FUNC_EN_CH_6	FUNC_EN_CH_5	FUNC_EN_CH_4	FUNC_EN_CH_3	FUNC_EN_CH_2	FUNC_EN_CH_1	FUNC_EN_CH_0		
0x09E to 0x0BC by 2	FUNC_MODE_SEL_CHn	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						FUNC_MODE_CH			
0x0BE to 0x0DC by 2	FUNC_DAC_INPUT_B_CHn	[15:8]	DAC_INPUT_B_CH[15:8]								0x0000	R/W
		[7:0]	DAC_INPUT_B_CH[7:0]									
0x0DE to 0x0FC by 2	FUNC_DITHER_PERIOD_CHn	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED					DITHER_PERIOD_CH				
0x0FE to 0x11C by 2	FUNC_DITHER_PHASE_CHn	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						DITHER_PHASE_CH			
0x11E to 0x13C by 2	FUNC_RAMP_STEP_CHn	[15:8]	RESERVED								0x0000	R/W

REGISTER SUMMARY

Table 22. AD5529R Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
		[7:0]	RAMP_STEP_CH									
0x13E	FUNC_INT_EN	[15:8]	FUNC_INT_EN_CH_15	FUNC_INT_EN_CH_14	FUNC_INT_EN_CH_13	FUNC_INT_EN_CH_12	FUNC_INT_EN_CH_11	FUNC_INT_EN_CH_10	FUNC_INT_EN_CH_9	FUNC_INT_EN_CH_8	0x0000	R/W
		[7:0]	FUNC_INT_EN_CH_7	FUNC_INT_EN_CH_6	FUNC_INT_EN_CH_5	FUNC_INT_EN_CH_4	FUNC_INT_EN_CH_3	FUNC_INT_EN_CH_2	FUNC_INT_EN_CH_1	FUNC_INT_EN_CH_0		
0x140	MUX_OUT_SEL	[15:8]	RESERVED								0x003F	R/W
		[7:0]	MUX_OUT_EN	RESERVED	MUX_PARAM_SEL							
0x142	MULTI_SW_LDAC	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED							MULTI_SW_LDAC		
0x144	MULTI_INPUT	[15:8]	MULTI_INPUT[15:8]								0x0000	R/W
		[7:0]	MULTI_INPUT[7:0]									
0x146	SW_LDAC	[15:8]	DAC_SW_LDAC_CH_15	DAC_SW_LDAC_CH_14	DAC_SW_LDAC_CH_13	DAC_SW_LDAC_CH_12	DAC_SW_LDAC_CH_11	DAC_SW_LDAC_CH_10	DAC_SW_LDAC_CH_9	DAC_SW_LDAC_CH_8	0x0000	R/W
		[7:0]	DAC_SW_LDAC_CH_7	DAC_SW_LDAC_CH_6	DAC_SW_LDAC_CH_5	DAC_SW_LDAC_CH_4	DAC_SW_LDAC_CH_3	DAC_SW_LDAC_CH_2	DAC_SW_LDAC_CH_1	DAC_SW_LDAC_CH_0		
0x148 to 0x166 by 2	DAC_INPUT_A_CHn	[15:8]	DAC_INPUT_A_CH[15:8]								0x0000	R/W
		[7:0]	DAC_INPUT_A_CH[7:0]									
0x168	FUNC_INT_STAT	[15:8]	FUNC_INT_STAT_CH_15	FUNC_INT_STAT_CH_14	FUNC_INT_STAT_CH_13	FUNC_INT_STAT_CH_12	FUNC_INT_STAT_CH_11	FUNC_INT_STAT_CH_10	FUNC_INT_STAT_CH_9	FUNC_INT_STAT_CH_8	0x0000	R/W
		[7:0]	FUNC_INT_STAT_CH_7	FUNC_INT_STAT_CH_6	FUNC_INT_STAT_CH_5	FUNC_INT_STAT_CH_4	FUNC_INT_STAT_CH_3	FUNC_INT_STAT_CH_2	FUNC_INT_STAT_CH_1	FUNC_INT_STAT_CH_0		
0x16A to 0x188 by 2	DAC_DATA_READBACK_CHn	[15:8]	DAC_DATA_READBACK_CH[15:8]								0x0000	R
		[7:0]	DAC_DATA_READBACK_CH[7:0]									
0x18A	TSENS_EN	[15:8]	RESERVED								0x0000	R/W
		[7:0]	TEMPSENS_PDB_TS_7	TEMPSENS_PDB_TS_6	TEMPSENS_PDB_TS_5	TEMPSENS_PDB_TS_4	TEMPSENS_PDB_TS_3	TEMPSENS_PDB_TS_2	TEMPSENS_PDB_TS_1	TEMPSENS_PDB_TS_0		
0x18C	TSENS_ALERT_FLAG	[15:8]	RESERVED								0x0000	R
		[7:0]	TEMPSENS_ALERT_FLAG_TS_7	TEMPSENS_ALERT_FLAG_TS_6	TEMPSENS_ALERT_FLAG_TS_5	TEMPSENS_ALERT_FLAG_TS_4	TEMPSENS_ALERT_FLAG_TS_3	TEMPSENS_ALERT_FLAG_TS_2	TEMPSENS_ALERT_FLAG_TS_1	TEMPSENS_ALERT_FLAG_TS_0		
0x18E	TSENS_SHTD_FLAG	[15:8]	RESERVED								0x0000	R
		[7:0]	TEMPSENS_SHUTDOWN_FLAG_TS_7	TEMPSENS_SHUTDOWN_FLAG_TS_6	TEMPSENS_SHUTDOWN_FLAG_TS_5	TEMPSENS_SHUTDOWN_FLAG_TS_4	TEMPSENS_SHUTDOWN_FLAG_TS_3	TEMPSENS_SHUTDOWN_FLAG_TS_2	TEMPSENS_SHUTDOWN_FLAG_TS_1	TEMPSENS_SHUTDOWN_FLAG_TS_0		

REGISTER SUMMARY

Table 22. AD5529R Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x190	TSENS_ALERT_STAT	[15:8]	RESERVED								0x0000	R/W
		[7:0]	TEMPSENS_ALERT_STATUS_TS_7	TEMPSENS_ALERT_STATUS_TS_6	TEMPSENS_ALERT_STATUS_TS_5	TEMPSENS_ALERT_STATUS_TS_4	TEMPSENS_ALERT_STATUS_TS_3	TEMPSENS_ALERT_STATUS_TS_2	TEMPSENS_ALERT_STATUS_TS_1	TEMPSENS_ALERT_STATUS_TS_0		
0x192	TSENS_SHTD_STAT	[15:8]	RESERVED								0x0000	R/W
		[7:0]	TEMPSENS_SHUTDOWN_STATUS_TS_7	TEMPSENS_SHUTDOWN_STATUS_TS_6	TEMPSENS_SHUTDOWN_STATUS_TS_5	TEMPSENS_SHUTDOWN_STATUS_TS_4	TEMPSENS_SHUTDOWN_STATUS_TS_3	TEMPSENS_SHUTDOWN_STATUS_TS_2	TEMPSENS_SHUTDOWN_STATUS_TS_1	TEMPSENS_SHUTDOWN_STATUS_TS_0		
0x194	ALARMB_TSENS_EN	[15:8]	RESERVED								0x0000	R/W
		[7:0]	ALARMB_TEMPSENS_EN_TS_7	ALARMB_TEMPSENS_EN_TS_6	ALARMB_TEMPSENS_EN_TS_5	ALARMB_TEMPSENS_EN_TS_4	ALARMB_TEMPSENS_EN_TS_3	ALARMB_TEMPSENS_EN_TS_2	ALARMB_TEMPSENS_EN_TS_1	ALARMB_TEMPSENS_EN_TS_0		
0x196	ALARMB_TSENS_SEL	[15:8]	RESERVED								0x0000	R/W
		[7:0]	ALARMB_TEMPSENS_SEL_TS_7	ALARMB_TEMPSENS_SEL_TS_6	ALARMB_TEMPSENS_SEL_TS_5	ALARMB_TEMPSENS_SEL_TS_4	ALARMB_TEMPSENS_SEL_TS_3	ALARMB_TEMPSENS_SEL_TS_2	ALARMB_TEMPSENS_SEL_TS_1	ALARMB_TEMPSENS_SEL_TS_0		
0x198	TSENS_SHTD_EN_CH	[15:8]	TEMPSENS_SHUTDOWN_EN_CH_15	TEMPSENS_SHUTDOWN_EN_CH_14	TEMPSENS_SHUTDOWN_EN_CH_13	TEMPSENS_SHUTDOWN_EN_CH_12	TEMPSENS_SHUTDOWN_EN_CH_11	TEMPSENS_SHUTDOWN_EN_CH_10	TEMPSENS_SHUTDOWN_EN_CH_9	TEMPSENS_SHUTDOWN_EN_CH_8	0x0000	R/W
		[7:0]	TEMPSENS_SHUTDOWN_EN_CH_7	TEMPSENS_SHUTDOWN_EN_CH_6	TEMPSENS_SHUTDOWN_EN_CH_5	TEMPSENS_SHUTDOWN_EN_CH_4	TEMPSENS_SHUTDOWN_EN_CH_3	TEMPSENS_SHUTDOWN_EN_CH_2	TEMPSENS_SHUTDOWN_EN_CH_1	TEMPSENS_SHUTDOWN_EN_CH_0		
0x19A	DAC_DIS_DEGLITCH_CH	[15:8]	DAC_DIS_DEGLITCH_CH_15	DAC_DIS_DEGLITCH_CH_14	DAC_DIS_DEGLITCH_CH_13	DAC_DIS_DEGLITCH_CH_12	DAC_DIS_DEGLITCH_CH_11	DAC_DIS_DEGLITCH_CH_10	DAC_DIS_DEGLITCH_CH_9	DAC_DIS_DEGLITCH_CH_8	0x0000	R/W
		[7:0]	DAC_DIS_DEGLITCH_CH_7	DAC_DIS_DEGLITCH_CH_6	DAC_DIS_DEGLITCH_CH_5	DAC_DIS_DEGLITCH_CH_4	DAC_DIS_DEGLITCH_CH_3	DAC_DIS_DEGLITCH_CH_2	DAC_DIS_DEGLITCH_CH_1	DAC_DIS_DEGLITCH_CH_0		
0x19C	DAC_INT_EN	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED						CRC_INT_EN	ALL_FUNC_INT_EN		
0x19E	ALL_FUNC_INT_STAT	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED							ALL_FUNC_INT_STAT		
0x1A0	FUNC_BUSY	[15:8]	FUNC_BUSY_CH_15	FUNC_BUSY_CH_14	FUNC_BUSY_CH_13	FUNC_BUSY_CH_12	FUNC_BUSY_CH_11	FUNC_BUSY_CH_10	FUNC_BUSY_CH_9	FUNC_BUSY_CH_8	0x0000	R
		[7:0]	FUNC_BUSY_CH_7	FUNC_BUSY_CH_6	FUNC_BUSY_CH_5	FUNC_BUSY_CH_4	FUNC_BUSY_CH_3	FUNC_BUSY_CH_2	FUNC_BUSY_CH_1	FUNC_BUSY_CH_0		
0x1A2	REF_SEL	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED							REF_SEL		
0x1A4	INIT_CRC_ERR_STAT	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED							INIT_ERR		

REGISTER SUMMARY

Table 22. AD5529R Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x1A8	MULTI_DEV_SW_LDAC_0	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED				MULTI_SW_LDAC_DEV_3	MULTI_SW_LDAC_DEV_2	MULTI_SW_LDAC_DEV_1	MULTI_SW_LDAC_DEV_0		
0x1AA	MULTI_INPUT_DEV_0	[15:8]	MULTI_INPUT_DEV_0[15:8]								0x0000	R/W
		[7:0]	MULTI_INPUT_DEV_0[7:0]									
0x1AC	MULTI_INPUT_DEV_1	[15:8]	MULTI_INPUT_DEV_1[15:8]								0x0000	R/W
		[7:0]	MULTI_INPUT_DEV_1[7:0]									
0x1AE	MULTI_INPUT_DEV_2	[15:8]	MULTI_INPUT_DEV_2[15:8]								0x0000	R/W
		[7:0]	MULTI_INPUT_DEV_2[7:0]									
0x1B0	MULTI_INPUT_DEV_3	[15:8]	MULTI_INPUT_DEV_3[15:8]								0x0000	R/W
		[7:0]	MULTI_INPUT_DEV_3[7:0]									
0x1B2	MULTI_DEV_SW_LDAC_1	[15:8]	MULTI_SW_LDAC_CH_15	MULTI_SW_LDAC_CH_14	MULTI_SW_LDAC_CH_13	MULTI_SW_LDAC_CH_12	MULTI_SW_LDAC_CH_11	MULTI_SW_LDAC_CH_10	MULTI_SW_LDAC_CH_9	MULTI_SW_LDAC_CH_8	0x0000	R/W
		[7:0]	MULTI_SW_LDAC_CH_7	MULTI_SW_LDAC_CH_6	MULTI_SW_LDAC_CH_5	MULTI_SW_LDAC_CH_4	MULTI_SW_LDAC_CH_3	MULTI_SW_LDAC_CH_2	MULTI_SW_LDAC_CH_1	MULTI_SW_LDAC_CH_0		
0x1B4 to 0x1D2 by 2	INPUT_DEV_0_CHn	[15:8]	INPUT_DEV_0_CH[15:8]								0x0000	R/W
		[7:0]	INPUT_DEV_0_CH[7:0]									
0x1D4 to 0x1F2 by 2	INPUT_DEV_1_CHn	[15:8]	INPUT_DEV_1_CH[15:8]								0x0000	R/W
		[7:0]	INPUT_DEV_1_CH[7:0]									
0x1F4 to 0x212 by 2	INPUT_DEV_2_CHn	[15:8]	INPUT_DEV_2_CH[15:8]								0x0000	R/W
		[7:0]	INPUT_DEV_2_CH[7:0]									
0x214 to 0x232 by 2	INPUT_DEV_3_CHn	[15:8]	INPUT_DEV_3_CH[15:8]								0x0000	R/W
		[7:0]	INPUT_DEV_3_CH[7:0]									

REGISTER DETAILS: BASE DEVICE AND INTERFACE AND CONFIGURATION

INTERFACE CONFIGURATION A REGISTER

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

Interface Configuration Settings.

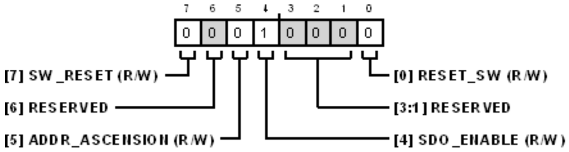

Figure 72. Interface Configuration A Register

Table 23. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET	First of Two of SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the part. All registers except for this register are reset to their default values.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_ASCENSION	Determines Sequential Addressing Behavior. 0: Address is decremented by one when streaming. 1: Address is incremented by one when streaming.	0x0	R/W
4	SDO_ENABLE	SDO Pin Enable.	0x1	R/W
[3:1]	RESERVED	Reserved.	0x0	R
0	RESET_SW	Second of Two of SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the part. All registers except for this register are reset to their default values.	0x0	R/W

INTERFACE CONFIGURATION B REGISTER

Address: 0x01, Reset: 0x00, Name: INTERFACE_CONFIG_B

Additional Interface Configuration Settings

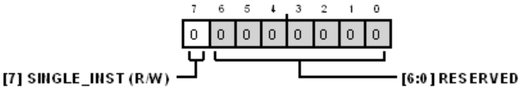

Figure 73. Interface Configuration B Register

Table 24. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Select Streaming or Single Instruction Mode. 0: Streaming mode is enabled. The address increments/decrements as successive data bytes are received. 1: Single instruction mode is enabled.	0x0	R/W
[6:0]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS: BASE DEVICE AND INTERFACE AND CONFIGURATION

DEVICE CONFIGURATION REGISTER

Address: 0x02, Reset: 0xF0, Name: DEVICE_CONFIG

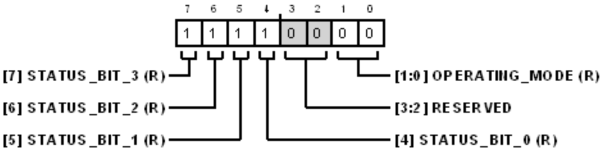

Figure 74. Device Configuration Register

Table 25. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
7	STATUS_BIT_3	Device Status Bit 3.	0x1	R
6	STATUS_BIT_2	Device Status Bit 2.	0x1	R
5	STATUS_BIT_1	Device Status Bit 1.	0x1	R
4	STATUS_BIT_0	Device Status Bit 0.	0x1	R
[3:2]	RESERVED	Reserved.	0x0	R
[1:0]	OPERATING_MODE	Operating Mode, Read Only.	0x0	R

CHIP TYPE REGISTER

Address: 0x03, Reset: 0x08, Name: CHIP_TYPE

The chip type is used to identify the family of ADI devices a given device belongs to. It should be used in conjunction with the Product ID to uniquely identify a given product.

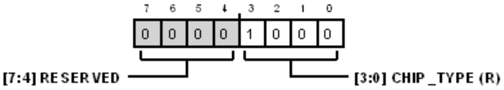

Figure 75. Chip Type Register

Table 26. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision DAC.	0x8	R

PRODUCT ID LOW REGISTER

Address: 0x04, Reset: 0x4A, Name: PRODUCT_ID_L

Low Byte of the Product ID.

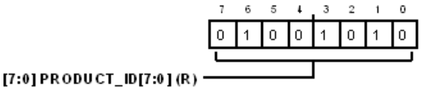

Figure 76. Product ID Low Register

Table 27. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	This is Device Chip Type/Family. The product ID should be used in conjunction with chip type to identify a product.	0x4A	R

REGISTER DETAILS: BASE DEVICE AND INTERFACE AND CONFIGURATION

PRODUCT ID HIGH REGISTER

Address: 0x05, Reset: 0x41, Name: PRODUCT_ID_H

High Byte of the Product ID.

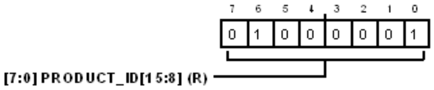

Figure 77. Product ID High Register

Table 28. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	This is Device Chip Type/Family. The product ID should be used in conjunction with chip type to identify a product.	0x41	R

CHIP GRADE REGISTER

Address: 0x06, Reset: 0x00, Name: CHIP_GRADE

Identifies product variations and device revisions.

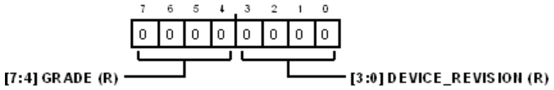

Figure 78. Chip Grade Register

Table 29. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	This is the Device Performance Grade.	0x0	R
[3:0]	DEVICE_REVISION	This is the Device Hardware Revision.	0x0	R

SCRATCH PAD REGISTER

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

This may be used to test writes and reads.

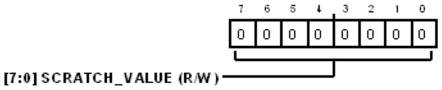

Figure 79. Scratch Pad Register

Table 30. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

SPI REVISION REGISTER

Address: 0x0B, Reset: 0x85, Name: SPI_REVISION

Indicates the SPI interface revision.

REGISTER DETAILS: BASE DEVICE AND INTERFACE AND CONFIGURATION

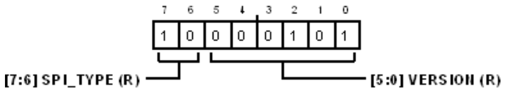

Figure 80. SPI Revision Register

Table 31. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	Always Reads as 0x2. 10:	0x2	R
[5:0]	VERSION	SPI Version. 100: Revision 1.2. 101: Revision 1.3.	0x5	R

VENDOR ID LOW REGISTER

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

Low Byte of the Vendor ID.

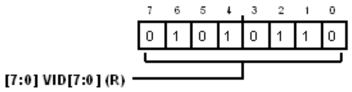

Figure 81. Vendor ID Low Register

Table 32. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Analog Devices Vendor ID.	0x56	R

VENDOR ID HIGH REGISTER

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

High Byte of the Vendor ID.

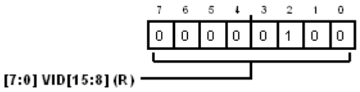

Figure 82. Vendor ID High Register

Table 33. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Analog Devices Vendor ID.	0x4	R

STREAM MODE REGISTER

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

Defines the length of the loop when streaming data.

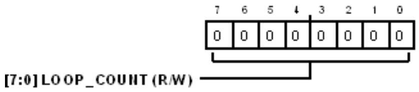

Figure 83. Stream Mode Register

REGISTER DETAILS: BASE DEVICE AND INTERFACE AND CONFIGURATION

Table 34. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Sets the Data Byte Count Before Looping to Start Address. When streaming data, a nonzero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes may be written using this approach. A value of 0x00, disables the loop back, so that addressing wraps around at the upper/lower limits of memory.	0x0	R/W

TRANSFER CONFIG REGISTER

Address: 0x0F, Reset: 0x00, Name: TRANSFER_CONFIG

Controls how data moves between controller and target registers.

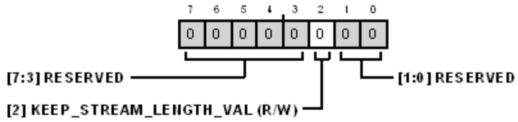

Figure 84. Transfer Config Register

Table 35. Bit Descriptions for TRANSFER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	KEEP_STREAM_LENGTH_VAL	When set, the loop counter does not reset on CSB rising edge.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

INTERFACE CONFIGURATION C REGISTER

Address: 0x10, Reset: 0x2F, Name: INTERFACE_CONFIG_C

Additional Interface Configuration Settings.

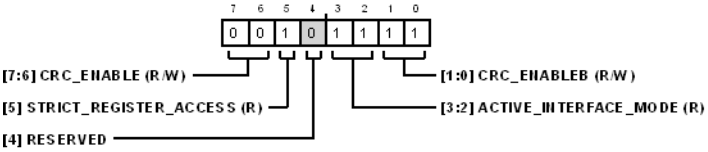

Figure 85. Interface Configuration C Register

Table 36. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_ENABLE	CRC Enable. This is written to enable/disable the use of CRC on the interface. The CRC_EnableB bit field must also be written with the inverted value of this bit field for the CRC to be enabled. 0: CRC disabled. 1: CRC enabled.	0x0	R/W
5	STRICT_REGISTER_ACCESS	Multibyte Registers Must Be Read/Written in Full. When this mode is enabled, all bytes of a multibyte register must be read/written in full. 0: Normal mode, no access restrictions. 1: Strict mode, multibyte registers require all bytes accessed.	0x1	R
4	RESERVED	Reserved.	0x0	R
[3:2]	ACTIVE_INTERFACE_MODE	This is the active mode the SPI interface is operating in. 00: 11:	0x3	R

REGISTER DETAILS: BASE DEVICE AND INTERFACE AND CONFIGURATION

Table 36. Bit Descriptions for INTERFACE_CONFIG_C (Continued)

Bits	Bit Name	Description	Reset	Access
[1:0]	CRC_ENABLEB	Inverted CRC Enable. This must be written with the inverted value of the CRC_ENABLE.	0x3	R/W

INTERFACE STATUS A REGISTER

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

Status bits are set to 1 to indicate an active condition. They may be cleared by writing a 1 to the corresponding bit location.

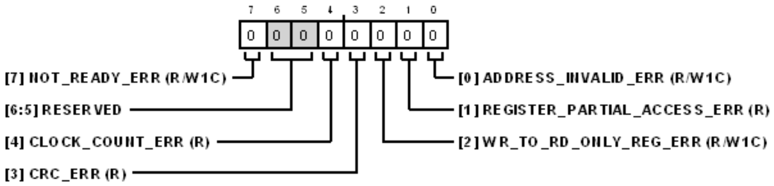

Figure 86. Interface Status A Register

Table 37. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
7	NOT_READY_ERR	Device Not Ready for Transaction. This error bit is set if the user attempts to execute a SPI transaction before the completion of digital initialization.	0x0	R/W1C
[6:5]	RESERVED	Reserved.	0x0	R
4	CLOCK_COUNT_ERR	Incorrect Number of Clocks Detected in a Transaction. This bit is set if the number of clocks received in a given SPI frame, defines as from CSB going low to CSB going high is not a multiple of 8-bits.	0x0	R
3	CRC_ERR	Invalid/No CRC Received. This is set when the controller fails to send a CRC or when the device calculates and checks the CRC and finds the CRC value is incorrect.	0x0	R
2	WR_TO_RD_ONLY_REG_ERR	Attempt to Write Read-Only Register. This is set when a write to a register that is read-only is attempted by the SPI controller.	0x0	R/W1C
1	REGISTER_PARTIAL_ACCESS_ERR	Fewer Than Expected Number of Bytes Read/Written. This bit is only valid when Strict register access is enabled.	0x0	R
0	ADDRESS_INVALID_ERR	Attempt to Read/Write Nonexistent Register Address. This bit is set when the user tries to access register addresses outside allowed memory map space	0x0	R/W1C

REGISTER DETAILS: COMMON DAC REGISTER MAPS

MULTI INPUT CHANNEL SELECT REGISTER

Address: 0x014, Reset: 0x0000, Name: MULTI_INPUT_SEL

This register is used to select which DAC_INPUT_A_CHn is updated by a write operation to MULTI_INPUT.

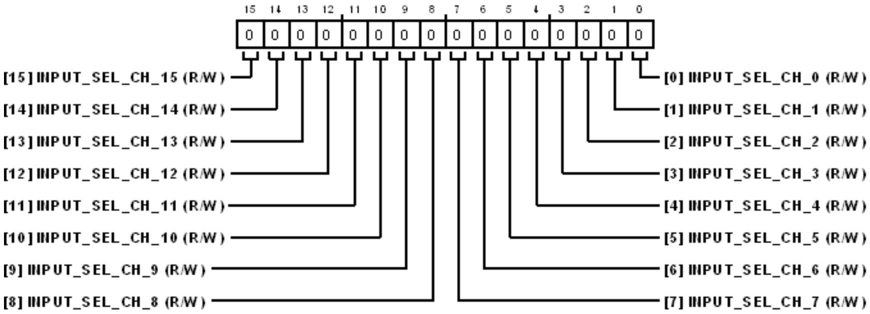

Figure 87. Multi Input Channel Select Register

Table 38. Bit Descriptions for MULTI_INPUT_SEL

Bits	Bit Name	Description	Reset	Access
15	INPUT_SEL_CH_15	Channel 15 Multi Input Update Enable.	0x0	R/W
14	INPUT_SEL_CH_14	Channel 14 Multi Input Update Enable.	0x0	R/W
13	INPUT_SEL_CH_13	Channel 13 Multi Input Update Enable.	0x0	R/W
12	INPUT_SEL_CH_12	Channel 12 Multi Input Update Enable.	0x0	R/W
11	INPUT_SEL_CH_11	Channel 11 Multi Input Update Enable.	0x0	R/W
10	INPUT_SEL_CH_10	Channel 10 Multi Input Update Enable.	0x0	R/W
9	INPUT_SEL_CH_9	Channel 9 Multi Input Update Enable.	0x0	R/W
8	INPUT_SEL_CH_8	Channel 8 Multi Input Update Enable.	0x0	R/W
7	INPUT_SEL_CH_7	Channel 7 Multi Input Update Enable.	0x0	R/W
6	INPUT_SEL_CH_6	Channel 6 Multi Input Update Enable.	0x0	R/W
5	INPUT_SEL_CH_5	Channel 5 Multi Input Update Enable.	0x0	R/W
4	INPUT_SEL_CH_4	Channel 4 Multi Input Update Enable.	0x0	R/W
3	INPUT_SEL_CH_3	Channel 3 Multi Input Update Enable.	0x0	R/W
2	INPUT_SEL_CH_2	Channel 2 Multi Input Update Enable.	0x0	R/W
1	INPUT_SEL_CH_1	Channel 1 Multi Input Update Enable.	0x0	R/W
0	INPUT_SEL_CH_0	Channel 0 Multi Input Update Enable. 0: Channel not included in multi DAC updates. 1: Channel included in multi DAC updates.	0x0	R/W

SYNC-ASYNC LOAD REGISTER

Address: 0x016, Reset: 0x0000, Name: LDAC_SYNC_ASYNC

This register is used to select between synchronous and asynchronous mode of updating the DAC Register, hence, the output of the DAC. This is set on a per-channel basis corresponding to the selected bit field.

REGISTER DETAILS: COMMON DAC REGISTER MAPS

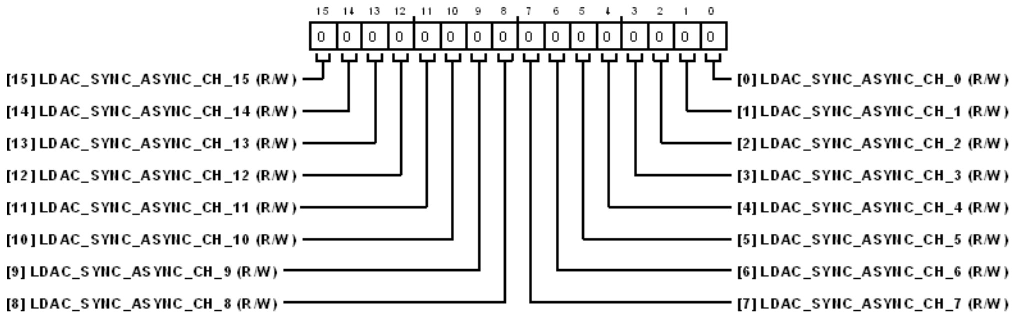

Figure 88. Sync-Async Load Register

Table 39. Bit Descriptions for LDAC_SYNC_ASYNC

Bits	Bit Name	Description	Reset	Access
15	LDAC_SYNC_ASYNC_CH_15	Channel 15 Synchronous or Asynchronous Update.	0x0	R/W
14	LDAC_SYNC_ASYNC_CH_14	Channel 14 Synchronous or Asynchronous Update.	0x0	R/W
13	LDAC_SYNC_ASYNC_CH_13	Channel 13 Synchronous or Asynchronous Update.	0x0	R/W
12	LDAC_SYNC_ASYNC_CH_12	Channel 12 Synchronous or Asynchronous Update.	0x0	R/W
11	LDAC_SYNC_ASYNC_CH_11	Channel 11 Synchronous or Asynchronous Update.	0x0	R/W
10	LDAC_SYNC_ASYNC_CH_10	Channel 10 Synchronous or Asynchronous Update.	0x0	R/W
9	LDAC_SYNC_ASYNC_CH_9	Channel 9 Synchronous or Asynchronous Update.	0x0	R/W
8	LDAC_SYNC_ASYNC_CH_8	Channel 8 Synchronous or Asynchronous Update.	0x0	R/W
7	LDAC_SYNC_ASYNC_CH_7	Channel 7 Synchronous or Asynchronous Update.	0x0	R/W
6	LDAC_SYNC_ASYNC_CH_6	Channel 6 Synchronous or Asynchronous Update.	0x0	R/W
5	LDAC_SYNC_ASYNC_CH_5	Channel 5 Synchronous or Asynchronous Update.	0x0	R/W
4	LDAC_SYNC_ASYNC_CH_4	Channel 4 Synchronous or Asynchronous Update.	0x0	R/W
3	LDAC_SYNC_ASYNC_CH_3	Channel 3 Synchronous or Asynchronous Update.	0x0	R/W
2	LDAC_SYNC_ASYNC_CH_2	Channel 2 Synchronous or Asynchronous Update.	0x0	R/W
1	LDAC_SYNC_ASYNC_CH_1	Channel 1 Synchronous or Asynchronous Update.	0x0	R/W
0	LDAC_SYNC_ASYNC_CH_0	Channel 0 Synchronous or Asynchronous Update. 0: DAC output is updated by a write to DAC_INPUT. 1: DAC output is updated by an LDAC event.	0x0	R/W

HARDWARE-SOFTWARE TRIGGER REGISTER

Address: 0x018, Reset: 0x0000, Name: LDAC_HW_SW

This register selects the source of the DAC update, either by hardware (HW) LDAC or software (SW) LDAC. LDAC_SYNC_ASYNC[LDAC_SYNC_ASYNC_CH_n] must be set to synchronous mode or 0b1. This is set on a per-channel basis corresponding to the selected bit field.

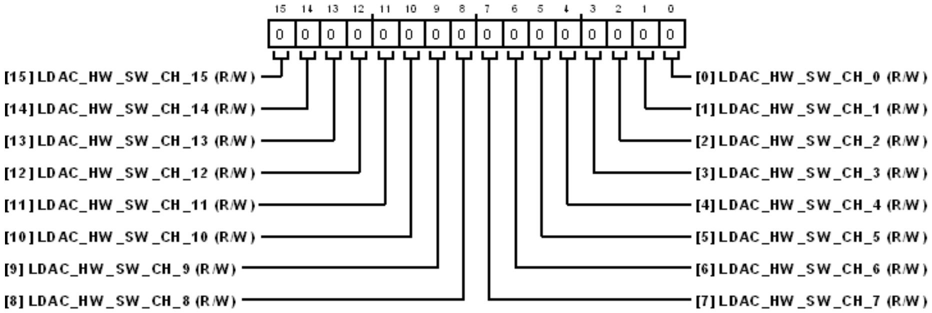

Figure 89. Hardware-Software Trigger Register

REGISTER DETAILS: COMMON DAC REGISTER MAPS

Table 40. Bit Descriptions for LDAC_HW_SW

Bits	Bit Name	Description	Reset	Access
15	LDAC_HW_SW_CH_15	Channel 15 Hardware or Software LDAC.	0x0	R/W
14	LDAC_HW_SW_CH_14	Channel 14 Hardware or Software LDAC.	0x0	R/W
13	LDAC_HW_SW_CH_13	Channel 13 Hardware or Software LDAC.	0x0	R/W
12	LDAC_HW_SW_CH_12	Channel 12 Hardware or Software LDAC.	0x0	R/W
11	LDAC_HW_SW_CH_11	Channel 11 Hardware or Software LDAC.	0x0	R/W
10	LDAC_HW_SW_CH_10	Channel 10 Hardware or Software LDAC.	0x0	R/W
9	LDAC_HW_SW_CH_9	Channel 9 Hardware or Software LDAC.	0x0	R/W
8	LDAC_HW_SW_CH_8	Channel 8 Hardware or Software LDAC.	0x0	R/W
7	LDAC_HW_SW_CH_7	Channel 7 Hardware or Software LDAC.	0x0	R/W
6	LDAC_HW_SW_CH_6	Channel 6 Hardware or Software LDAC.	0x0	R/W
5	LDAC_HW_SW_CH_5	Channel 5 Hardware or Software LDAC.	0x0	R/W
4	LDAC_HW_SW_CH_4	Channel 4 Hardware or Software LDAC.	0x0	R/W
3	LDAC_HW_SW_CH_3	Channel 3 Hardware or Software LDAC.	0x0	R/W
2	LDAC_HW_SW_CH_2	Channel 2 Hardware or Software LDAC.	0x0	R/W
1	LDAC_HW_SW_CH_1	Channel 1 Hardware or Software LDAC.	0x0	R/W
0	LDAC_HW_SW_CH_0	Channel 0 Hardware or Software LDAC. 0: Hardware LDAC selected. 1: Software LDAC selected.	0x0	R/W

LDAC HARDWARE PIN AND EDGE SELECT REGISTER

Address: 0x01A to 0x038 (Increments of 2), Reset: 0x0000, Name: LDAC_HW_SRC_CHn

This register selects the HW LDAC source and the edge of the LDAC update for CHn.

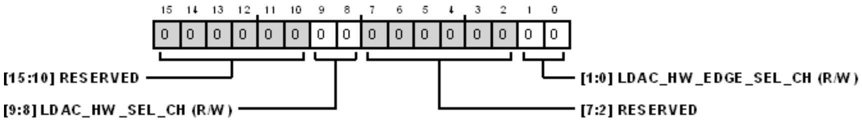

Figure 90. LDAC Hardware Pin and Edge Select Register

Table 41. Bit Descriptions for LDAC_HW_SRC_CHn

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
[9:8]	LDAC_HW_SEL_CH	Hardware LDAC Pin Selection. 00: LDAC/Toggle Pin 0 Used. 01: LDAC/Toggle Pin 1 Used. 10: LDAC/Toggle Pin 2 Used. 11: LDAC/Toggle Pin 3 Used.	0x0	R/W
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	LDAC_HW_EDGE_SEL_CH	Hardware LDAC Edge Selection. 00: Trigger rising edge. 01: Trigger falling edge. 10: Trigger at any edge. 11: Reserved.	0x0	R/W

REGISTER DETAILS: COMMON DAC REGISTER MAPS

OUTPUT ENABLE REGISTER

Address: 0x03A, Reset: 0x0000, Name: OUT_EN

This register enables or disables the selected DAC output. This is set on a per-channel basis corresponding to the selected bit field.

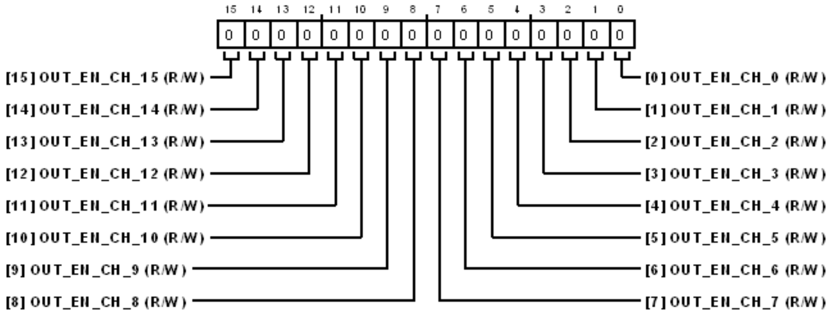

Figure 91. Output Enable Register

Table 42. Bit Descriptions for OUT_EN

Bits	Bit Name	Description	Reset	Access
15	OUT_EN_CH_15	Channel 15 Output Enable.	0x0	R/W
14	OUT_EN_CH_14	Channel 14 Output Enable.	0x0	R/W
13	OUT_EN_CH_13	Channel 13 Output Enable.	0x0	R/W
12	OUT_EN_CH_12	Channel 12 Output Enable.	0x0	R/W
11	OUT_EN_CH_11	Channel 11 Output Enable.	0x0	R/W
10	OUT_EN_CH_10	Channel 10 Output Enable.	0x0	R/W
9	OUT_EN_CH_9	Channel 9 Output Enable.	0x0	R/W
8	OUT_EN_CH_8	Channel 8 Output Enable.	0x0	R/W
7	OUT_EN_CH_7	Channel 7 Output Enable.	0x0	R/W
6	OUT_EN_CH_6	Channel 6 Output Enable.	0x0	R/W
5	OUT_EN_CH_5	Channel 5 Output Enable.	0x0	R/W
4	OUT_EN_CH_4	Channel 4 Output Enable.	0x0	R/W
3	OUT_EN_CH_3	Channel 3 Output Enable.	0x0	R/W
2	OUT_EN_CH_2	Channel 2 Output Enable.	0x0	R/W
1	OUT_EN_CH_1	Channel 1 Output Enable.	0x0	R/W
0	OUT_EN_CH_0	Channel 0 Output Enable. 0: Output is disabled. 1: Output is enabled.	0x0	R/W

OUTPUT RANGE REGISTER

Address: 0x03C to 0x05A (Increments of 2), Reset: 0x0000, Name: OUT_RANGE_CHn

This register selects the voltage range of the DAC output for CHn. The supply voltages must be wider than the output range to allow for adequate footroom and headroom.

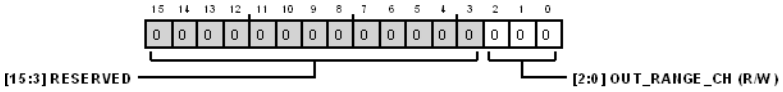

Figure 92. Output Range Register

REGISTER DETAILS: COMMON DAC REGISTER MAPS

Table 43. Bit Descriptions for OUT_RANGE_CHn

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	OUT_RANGE_CH	Output Range Selector. 000: From 0V to 5V output. 001: From 0V to 10V output. 010: From 0V to 20V output. 011: From 0V to 40V output. 100: From −5V to +5V output. 101: From −10V to +10V output. 110: From −15V to +15V output. 111: From −20V to +20V output.	0x0	R/W

DIGITAL GAIN CORRECTION REGISTER

Address: 0x05C to 0x07A (Increments of 2), Reset: 0x0080, Name: CAL_GAIN_CHn

This register stores the gain correction coefficient for CHn.

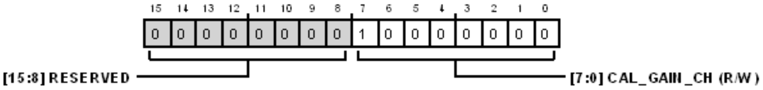

Figure 93. Digital Gain Correction Register

Table 44. Bit Descriptions for CAL_GAIN_CHn

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CAL_GAIN_CH	Digital Gain Correction Value.	0x80	R/W

DIGITAL OFFSET CORRECTION REGISTER

Address: 0x07C to 0x09A (Increments of 2), Reset: 0x0000, Name: CAL_OFFSET_CHn

This register stores the offset correction coefficient for CHn.

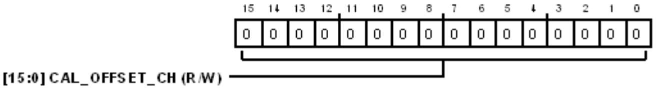

Figure 94. Digital Offset Correction Register

Table 45. Bit Descriptions for CAL_OFFSET_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	CAL_OFFSET_CH	Digital Offset Correction Value.	0x0	R/W

FUNCTION ENABLE REGISTER

Address: 0x09C, Reset: 0x0000, Name: FUNC_EN

This register enables or disables the digital function. This is set on a per-channel basis corresponding to the selected bit field.

REGISTER DETAILS: COMMON DAC REGISTER MAPS

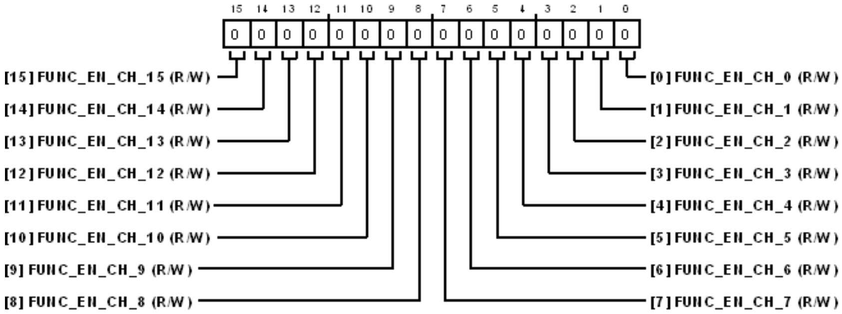

Figure 95. Function Enable Register

Table 46. Bit Descriptions for FUNC_EN

Bits	Bit Name	Description	Reset	Access
15	FUNC_EN_CH_15	Channel 15 Function Generator Enable.	0x0	R/W
14	FUNC_EN_CH_14	Channel 14 Function Generator Enable.	0x0	R/W
13	FUNC_EN_CH_13	Channel 13 Function Generator Enable.	0x0	R/W
12	FUNC_EN_CH_12	Channel 12 Function Generator Enable.	0x0	R/W
11	FUNC_EN_CH_11	Channel 11 Function Generator Enable.	0x0	R/W
10	FUNC_EN_CH_10	Channel 10 Function Generator Enable.	0x0	R/W
9	FUNC_EN_CH_9	Channel 9 Function Generator Enable.	0x0	R/W
8	FUNC_EN_CH_8	Channel 8 Function Generator Enable.	0x0	R/W
7	FUNC_EN_CH_7	Channel 7 Function Generator Enable.	0x0	R/W
6	FUNC_EN_CH_6	Channel 6 Function Generator Enable.	0x0	R/W
5	FUNC_EN_CH_5	Channel 5 Function Generator Enable.	0x0	R/W
4	FUNC_EN_CH_4	Channel 4 Function Generator Enable.	0x0	R/W
3	FUNC_EN_CH_3	Channel 3 Function Generator Enable.	0x0	R/W
2	FUNC_EN_CH_2	Channel 2 Function Generator Enable.	0x0	R/W
1	FUNC_EN_CH_1	Channel 1 Function Generator Enable.	0x0	R/W
0	FUNC_EN_CH_0	Channel 0 Function Generator Enable. 0: Function generator disabled. 1: Function generator enabled.	0x0	R/W

FUNCTION MODE SELECT REGISTER

Address: 0x09E to 0x0BC (Increments of 2), Reset: 0x0000, Name: FUNC_MODE_SEL_CHn

This register selects the function generator mode for CHn. FUNC_EN[FUNC_EN_CH_n] must be enabled.

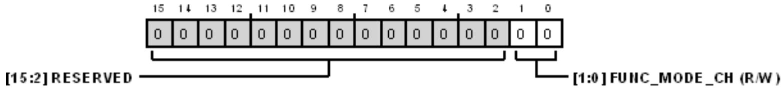

Figure 96. Function Mode Select Register

Table 47. Bit Descriptions for FUNC_MODE_SEL_CHn

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	FUNC_MODE_CH	Function Generator Mode Selector. 00: Toggle mode. 01: Dither mode. 10: Sawtooth ramp mode.	0x0	R/W

REGISTER DETAILS: COMMON DAC REGISTER MAPS

Table 47. Bit Descriptions for FUNC_MODE_SEL_CHn (Continued)

Bits	Bit Name	Description	Reset	Access
		11: Triangular ramp mode.		

SECONDARY DAC INPUT REGISTER

Address: 0x0BE to 0x0DC (Increments of 2), Reset: 0x0000, Name: FUNC_DAC_INPUT_B_CHn

This register is the INPUT_B register used for digital function generation.

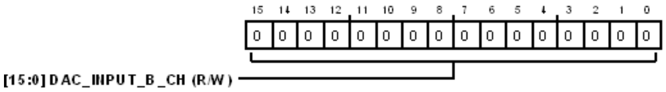

Figure 97. Secondary DAC Input Register

Table 48. Bit Descriptions for FUNC_DAC_INPUT_B_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_INPUT_B_CH	Secondary DAC Input Code for Function Generator.	0x0	R/W

DITHER PERIOD SELECT REGISTER

Address: 0x0DE to 0x0FC (Increments of 2), Reset: 0x0000, Name: FUNC_DITHER_PERIOD_CHn

This register serves as the period divider for the dither function of channel n, where n is the channel number.

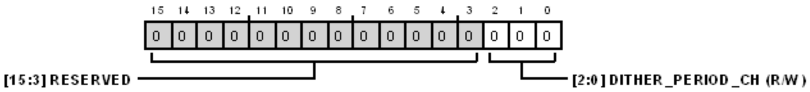

Figure 98. Dither Period Select Register

Table 49. Bit Descriptions for FUNC_DITHER_PERIOD_CHn

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	DITHER_PERIOD_CH	Dither Function Period Setting. 000: Dither period of 128/F_{TOGGLE}. 001: Dither period of 64/F_{TOGGLE}. 010: Dither period of 32/F_{TOGGLE}. 011: Dither period of 16/F_{TOGGLE}. 100: Dither period of 8/F_{TOGGLE}. 101: Dither period of 4/F_{TOGGLE}. 110: Dither period of 2/F_{TOGGLE}.	0x0	R/W

DITHER PHASE SELECT REGISTER

Address: 0x0FE to 0x11C (Increments of 2), Reset: 0x0000, Name: FUNC_DITHER_PHASE_CHn

This register serves as the initial phase for the Dither function of channel n, where n is the channel number.

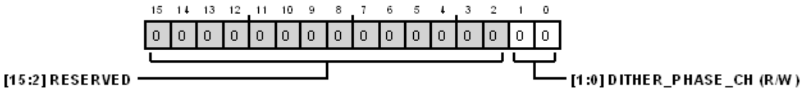

Figure 99. Dither Phase Select Register

REGISTER DETAILS: COMMON DAC REGISTER MAPS

Table 50. Bit Descriptions for FUNC_DITHER_PHASE_CHn

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	DITHER_PHASE_CH	Dither Function Phase Setting. 00: 0° (0 Radians). 01: 90° or π/2 radians delay with request to a 0° sine. 10: 180° or π radians delay with request to a 0° sine. 11: 270° or 3π/2 radians delay with request to a 0° sine.	0x0	R/W

RAMP STEP REGISTER

Address: 0x11E to 0x13C (Increments of 2), Reset: 0x0000, Name: FUNC_RAMP_STEP_CHn

This register defines the step size for the ramp function.

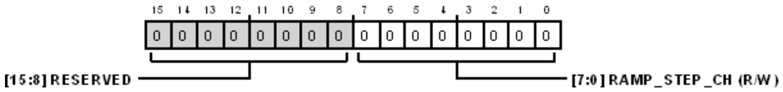

Figure 100. Ramp Step Register

Table 51. Bit Descriptions for FUNC_RAMP_STEP_CHn

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	RAMP_STEP_CH	Ramp Functions Step − Actual Step is Value + 1.	0x0	R/W

FUNCTION INTERRUPT ENABLE REGISTER

Address: 0x13E, Reset: 0x0000, Name: FUNC_INT_EN

Each bit is an enable signal that allows the contribution of each channel's FUNC_INT_STAT to the ALL_FUNC_INT_STAT register. This is set on a per-channel basis corresponding to the selected bit field.

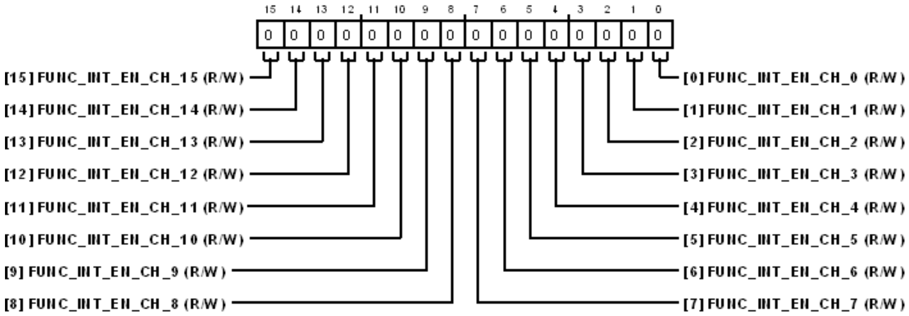

Figure 101. Function Interrupt Enable Register

Table 52. Bit Descriptions for FUNC_INT_EN

Bits	Bit Name	Description	Reset	Access
15	FUNC_INT_EN_CH_15	Channel 15 Function Generator Interrupt Enable.	0x0	R/W
14	FUNC_INT_EN_CH_14	Channel 14 Function Generator Interrupt Enable.	0x0	R/W
13	FUNC_INT_EN_CH_13	Channel 13 Function Generator Interrupt Enable.	0x0	R/W
12	FUNC_INT_EN_CH_12	Channel 12 Function Generator Interrupt Enable.	0x0	R/W
11	FUNC_INT_EN_CH_11	Channel 11 Function Generator Interrupt Enable.	0x0	R/W
10	FUNC_INT_EN_CH_10	Channel 10 Function Generator Interrupt Enable.	0x0	R/W

REGISTER DETAILS: COMMON DAC REGISTER MAPS

Table 52. Bit Descriptions for FUNC_INT_EN (Continued)

Bits	Bit Name	Description	Reset	Access
9	FUNC_INT_EN_CH_9	Channel 9 Function Generator Interrupt Enable.	0x0	R/W
8	FUNC_INT_EN_CH_8	Channel 8 Function Generator Interrupt Enable.	0x0	R/W
7	FUNC_INT_EN_CH_7	Channel 7 Function Generator Interrupt Enable.	0x0	R/W
6	FUNC_INT_EN_CH_6	Channel 6 Function Generator Interrupt Enable.	0x0	R/W
5	FUNC_INT_EN_CH_5	Channel 5 Function Generator Interrupt Enable.	0x0	R/W
4	FUNC_INT_EN_CH_4	Channel 4 Function Generator Interrupt Enable.	0x0	R/W
3	FUNC_INT_EN_CH_3	Channel 3 Function Generator Interrupt Enable.	0x0	R/W
2	FUNC_INT_EN_CH_2	Channel 2 Function Generator Interrupt Enable.	0x0	R/W
1	FUNC_INT_EN_CH_1	Channel 1 Function Generator Interrupt Enable.	0x0	R/W
0	FUNC_INT_EN_CH_0	Channel 0 Function Generator Interrupt Enable. 0: Channel does not contribute to All Funct Disabled interrupt. 1: Channel contributes to All Funct Disabled interrupt.	0x0	R/W

MUX OUT SELECT REGISTER

Address: 0x140, Reset: 0x003F, Name: MUX_OUT_SEL

This register enables or disables the MUXOUT pin. Additionally, it selects whether voltage, current, temperature, or calibration data is present at the MUXOUT analog output pin.

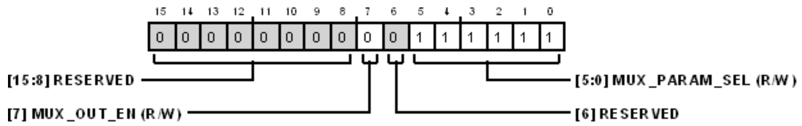

Figure 102. MUX Out Select Register

Table 53. Bit Descriptions for MUX_OUT_SEL

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	MUX_OUT_EN	MUX Output Enable Bit. 0: Disabled. 1: Enabled.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
[5:0]	MUX_PARAM_SEL	MUX Parameter Selector. 000000: Voltage monitor for Channel 0. 000001: Voltage monitor for Channel 1. 000010: Voltage monitor for Channel 2. 000011: Voltage monitor for Channel 3. 000100: Voltage monitor for Channel 4. 000101: Voltage monitor for Channel 5. 000110: Voltage monitor for Channel 6. 000111: Voltage monitor for Channel 7. 001000: Voltage monitor for Channel 8. 001001: Voltage monitor for Channel 9. 001010: Voltage monitor for Channel 10. 001011: Voltage monitor for Channel 11. 001100: Voltage monitor for Channel 12. 001101: Voltage monitor for Channel 13. 001110: Voltage monitor for Channel 14.	0x3F	R/W

REGISTER DETAILS: COMMON DAC REGISTER MAPS

Table 53. Bit Descriptions for MUX_OUT_SEL (Continued)

Bits	Bit Name	Description	Reset	Access
		001111: Voltage monitor for Channel 15. 010000: Current monitor for Channel 0. 010001: Current monitor for Channel 1. 010010: Current monitor for Channel 2. 010011: Current monitor for Channel 3. 010100: Current monitor for Channel 4. 010101: Current monitor for Channel 5. 010110: Current monitor for Channel 6. 010111: Current monitor for Channel 7. 011000: Current monitor for Channel 8. 011001: Current monitor for Channel 9. 011010: Current monitor for Channel 10. 011011: Current monitor for Channel 11. 011100: Current monitor for Channel 12. 011101: Current monitor for Channel 13. 011110: Current monitor for Channel 14. 011111: Current monitor for Channel 15. 100000: Temp sensor number 0 output. 100001: Temp sensor number 1 output. 100010: Temp sensor number 2 output. 100011: Temp sensor number 3 output. 100100: Temp sensor number 4 output. 100101: Temp sensor number 5 output. 100110: Temp sensor number 6 output. 100111: Temp sensor number 7 output. 101000: Voltage monitor output calibration mode. All values from 6'b101000 to 6'b101111 yield Vmon Cal. 110000: Current monitor output calibration mode. All values from 6'b110000 to 6'b110111 yield Imon Cal. 111000: MUX output set to high-Z. All values from 6'b111000 to 6'b111111 yield high-Z.		

MULTICHANNEL SOFTWARE LDAC REGISTER

Address: 0x142, Reset: 0x0000, Name: MULTI_SW_LDAC

Software LDAC trigger for all channels. When the bit field is set high, the DAC registers of all 16 channels get updated with respective input register data. LDAC_HW_SW[LDAC_HW_SW_CH_n] must be set to 1.

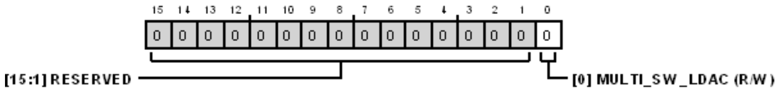

Figure 103. Multichannel Software LDAC Register

Table 54. Bit Descriptions for MULTI_SW_LDAC

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	MULTI_SW_LDAC	Multichannel Software LDAC Trigger Bit.	0x0	R/W

MULTICHANNEL INPUT REGISTER

Address: 0x144, Reset: 0x0000, Name: MULTI_INPUT

REGISTER DETAILS: COMMON DAC REGISTER MAPS

A write to this register also gets written to INPUT_CHn registers selected by MULTI_INPUT_SEL register.

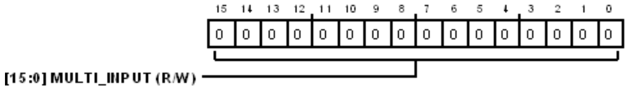

Figure 104. Multichannel Input Register

Table 55. Bit Descriptions for MULTI_INPUT

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_INPUT	Multichannel Input Register Code.	0x0	R/W

INDIVIDUAL CHANNEL SOFTWARE LDAC REGISTER

Address: 0x146, Reset: 0x0000, Name: SW_LDAC

Software LDAC trigger for individually selected channels. When a bit field is set high, the DAC register of the corresponding channel gets updated with Input register data. LDAC_HW_SW[LDAC_HW_SW_CH_n] must be set to 1.

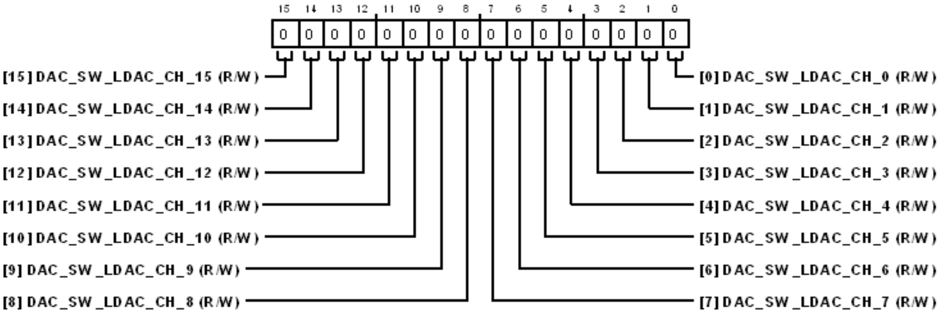

Figure 105. Individual Channel Software LDAC Register

Table 56. Bit Descriptions for SW_LDAC

Bits	Bit Name	Description	Reset	Access
15	DAC_SW_LDAC_CH_15	Channel 15 Software LDAC Trigger.	0x0	R/W
14	DAC_SW_LDAC_CH_14	Channel 14 Software LDAC Trigger.	0x0	R/W
13	DAC_SW_LDAC_CH_13	Channel 13 Software LDAC Trigger.	0x0	R/W
12	DAC_SW_LDAC_CH_12	Channel 12 Software LDAC Trigger.	0x0	R/W
11	DAC_SW_LDAC_CH_11	Channel 11 Software LDAC Trigger.	0x0	R/W
10	DAC_SW_LDAC_CH_10	Channel 10 Software LDAC Trigger.	0x0	R/W
9	DAC_SW_LDAC_CH_9	Channel 9 Software LDAC Trigger.	0x0	R/W
8	DAC_SW_LDAC_CH_8	Channel 8 Software LDAC Trigger.	0x0	R/W
7	DAC_SW_LDAC_CH_7	Channel 7 Software LDAC Trigger.	0x0	R/W
6	DAC_SW_LDAC_CH_6	Channel 6 Software LDAC Trigger.	0x0	R/W
5	DAC_SW_LDAC_CH_5	Channel 5 Software LDAC Trigger.	0x0	R/W
4	DAC_SW_LDAC_CH_4	Channel 4 Software LDAC Trigger.	0x0	R/W
3	DAC_SW_LDAC_CH_3	Channel 3 Software LDAC Trigger.	0x0	R/W
2	DAC_SW_LDAC_CH_2	Channel 2 Software LDAC Trigger.	0x0	R/W
1	DAC_SW_LDAC_CH_1	Channel 1 Software LDAC Trigger.	0x0	R/W
0	DAC_SW_LDAC_CH_0	Channel 0 Software LDAC Trigger.	0x0	R/W

PRIMARY DAC INPUT REGISTER

Address: 0x148 to 0x166 (Increments of 2), Reset: 0x0000, Name: DAC_INPUT_A_CHn

REGISTER DETAILS: COMMON DAC REGISTER MAPS

This register serves as the INPUT_A register for each DAC.

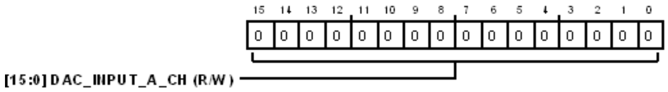

Figure 106. Primary DAC Input Register

Table 57. Bit Descriptions for DAC_INPUT_A_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_INPUT_A_CH	Primary DAC Input Code.	0x0	R/W

FUNCTION INTERRUPT STATUS REGISTER

Address: 0x168, Reset: 0x0000, Name: FUNC_INT_STAT

This register reports the current status of the digital function.

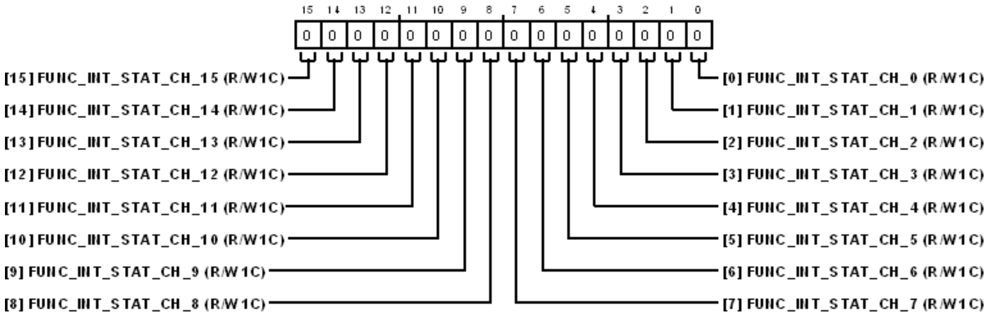

Figure 107. Function Interrupt Status Register

Table 58. Bit Descriptions for FUNC_INT_STAT

Bits	Bit Name	Description	Reset	Access
15	FUNC_INT_STAT_CH_15	Channel 15 Function Generator Status.	0x0	R/W1C
14	FUNC_INT_STAT_CH_14	Channel 14 Function Generator Status.	0x0	R/W1C
13	FUNC_INT_STAT_CH_13	Channel 13 Function Generator Status.	0x0	R/W1C
12	FUNC_INT_STAT_CH_12	Channel 12 Function Generator Status.	0x0	R/W1C
11	FUNC_INT_STAT_CH_11	Channel 11 Function Generator Status.	0x0	R/W1C
10	FUNC_INT_STAT_CH_10	Channel 10 Function Generator Status.	0x0	R/W1C
9	FUNC_INT_STAT_CH_9	Channel 9 Function Generator Status.	0x0	R/W1C
8	FUNC_INT_STAT_CH_8	Channel 8 Function Generator Status.	0x0	R/W1C
7	FUNC_INT_STAT_CH_7	Channel 7 Function Generator Status.	0x0	R/W1C
6	FUNC_INT_STAT_CH_6	Channel 6 Function Generator Status.	0x0	R/W1C
5	FUNC_INT_STAT_CH_5	Channel 5 Function Generator Status.	0x0	R/W1C
4	FUNC_INT_STAT_CH_4	Channel 4 Function Generator Status.	0x0	R/W1C
3	FUNC_INT_STAT_CH_3	Channel 3 Function Generator Status.	0x0	R/W1C
2	FUNC_INT_STAT_CH_2	Channel 2 Function Generator Status.	0x0	R/W1C
1	FUNC_INT_STAT_CH_1	Channel 1 Function Generator Status.	0x0	R/W1C
0	FUNC_INT_STAT_CH_0	Channel 0 Function Generator Status. 0: Function generator never used or it is still busy. 1: Function generator finished its operation.	0x0	R/W1C

REGISTER DETAILS: COMMON DAC REGISTER MAPS

DAC DATA READBACK REGISTER

Address: 0x16A to 0x188 (Increments of 2), Reset: 0x0000, Name: DAC_DATA_READBACK_CHn

In direct-load mode (functions disabled), this register contains the Gain/Offset corrected DAC_INPUT_A code going to the analog domain. If synchronous updates are used, an LDAC event is required for the DAC output to update with this code after it is modified. If asynchronous updates are used, this register is updated together with output of the DAC.

With functions enabled (only synchronous updates allowed), this register contains the next code that is applied to the DAC when an LDAC event is detected. That is: Toggle mode: DAC_INPUT_A if output is currently B, and DAC_INPUT_B if output is currently A (Gain/Offset Corrected). Dither mode: Sine point n+1 if output is currently at sine point n. Sawtooth mode: Ramp point n+1 if output is currently at ramp point n, and DAC_INPUT_A when endpoint DAC_INPUT_B is reached (to generate Sawtooth step). Triangular mode: Ramp point n+1 if output is currently at ramp point n.

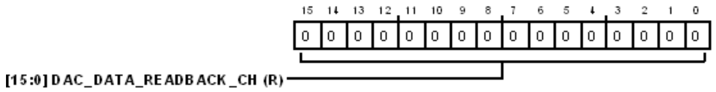

Figure 108. DAC Data Readback Register

Table 59. Bit Descriptions for DAC_DATA_READBACK_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_DATA_READBACK_CH	Digital Code Driving the DAC.	0x0	R

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

TEMPERATURE SENSORS ENABLE REGISTER

Address: 0x18A, Reset: 0x0000, Name: TSENS_EN

This register enables or disables the temperature sensor.

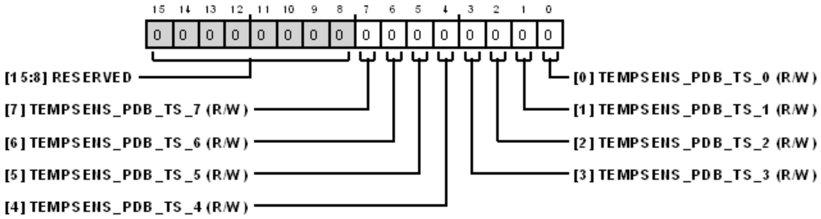

Figure 109. Temperature Sensors Enable Register

Table 60. Bit Descriptions for TSENS_EN

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	TEMPSENS_PDB_TS_7	Temp Sensor 7 Power Down.	0x0	R/W
6	TEMPSENS_PDB_TS_6	Temp Sensor 6 Power Down.	0x0	R/W
5	TEMPSENS_PDB_TS_5	Temp Sensor 5 Power Down.	0x0	R/W
4	TEMPSENS_PDB_TS_4	Temp Sensor 4 Power Down.	0x0	R/W
3	TEMPSENS_PDB_TS_3	Temp Sensor 3 Power Down.	0x0	R/W
2	TEMPSENS_PDB_TS_2	Temp Sensor 2 Power Down.	0x0	R/W
1	TEMPSENS_PDB_TS_1	Temp Sensor 1 Power Down.	0x0	R/W
0	TEMPSENS_PDB_TS_0	Temp Sensor 0 Power Down. 0: Temp Sensor powered down. 1: Temp Sensor powered up.	0x0	R/W

TEMPERATURE SENSORS ALERT LIVE FLAGS REGISTER

Address: 0x18C, Reset: 0x0000, Name: TSENS_ALERT_FLAG

This register reports when a temperature sensor exceeds 110°C.

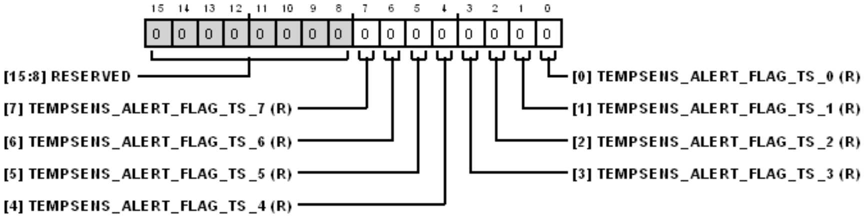

Figure 110. Temperature Sensors Alert Live Flags Register

Table 61. Bit Descriptions for TSENS_ALERT_FLAG

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	TEMPSENS_ALERT_FLAG_TS_7	Temp Sensor 7 Live Alert Signal.	0x0	R
6	TEMPSENS_ALERT_FLAG_TS_6	Temp Sensor 6 Live Alert Signal.	0x0	R
5	TEMPSENS_ALERT_FLAG_TS_5	Temp Sensor 5 Live Alert Signal.	0x0	R
4	TEMPSENS_ALERT_FLAG_TS_4	Temp Sensor 4 Live Alert Signal.	0x0	R
3	TEMPSENS_ALERT_FLAG_TS_3	Temp Sensor 3 Live Alert Signal.	0x0	R

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

Table 61. Bit Descriptions for TSENS_ALERT_FLAG (Continued)

Bits	Bit Name	Description	Reset	Access
2	TEMPSENS_ALERT_FLAG_TS_2	Temp Sensor 2 Live Alert Signal.	0x0	R
1	TEMPSENS_ALERT_FLAG_TS_1	Temp Sensor 1 Live Alert Signal.	0x0	R
0	TEMPSENS_ALERT_FLAG_TS_0	Temp Sensor 0 Live Alert Signal.	0x0	R

TEMPERATURE SENSORS SHUTDOWN LIVE FLAGS REGISTER

Address: 0x18E, Reset: 0x0000, Name: TSENS_SHTD_FLAG

This register reports when a temperature sensor exceeds 130°C and shuts down the DAC or DACs output associated with that sensor.

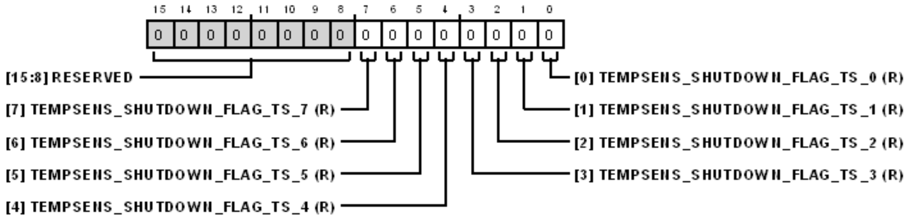

Figure 111. Temperature Sensors Shutdown Live Flags Register

Table 62. Bit Descriptions for TSENS_SHTD_FLAG

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	TEMPSENS_SHUTDOWN_FLAG_TS_7	Temp Sensor 7 Live Shutdown Signal.	0x0	R
6	TEMPSENS_SHUTDOWN_FLAG_TS_6	Temp Sensor 6 Live Shutdown Signal.	0x0	R
5	TEMPSENS_SHUTDOWN_FLAG_TS_5	Temp Sensor 5 Live Shutdown Signal.	0x0	R
4	TEMPSENS_SHUTDOWN_FLAG_TS_4	Temp Sensor 4 Live Shutdown Signal.	0x0	R
3	TEMPSENS_SHUTDOWN_FLAG_TS_3	Temp Sensor 3 Live Shutdown Signal.	0x0	R
2	TEMPSENS_SHUTDOWN_FLAG_TS_2	Temp Sensor 2 Live Shutdown Signal.	0x0	R
1	TEMPSENS_SHUTDOWN_FLAG_TS_1	Temp Sensor 1 Live Shutdown Signal.	0x0	R
0	TEMPSENS_SHUTDOWN_FLAG_TS_0	Temp Sensor 0 Live Shutdown Signal.	0x0	R

TEMPERATURE SENSORS ALERT STATUS REGISTER

Address: 0x190, Reset: 0x0000, Name: TSENS_ALERT_STAT

This register reports when a temperature sensor exceeds 110°C.

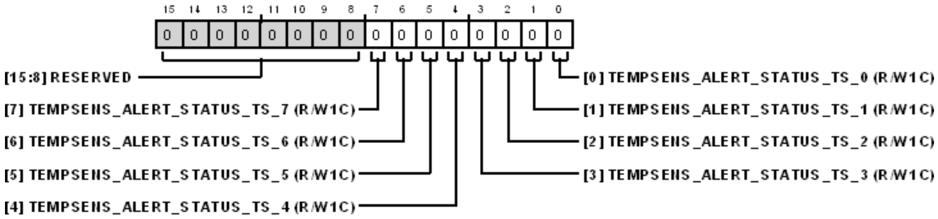

Figure 112. Temperature Sensors Alert Status Register

Table 63. Bit Descriptions for TSENS_ALERT_STAT

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	TEMPSENS_ALERT_STATUS_TS_7	Temp Sensor 7 Latched Alert Signal.	0x0	R/W1C

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

Table 63. Bit Descriptions for TSENS_ALERT_STAT (Continued)

Bits	Bit Name	Description	Reset	Access
6	TEMPSENS_ALERT_STATUS_TS_6	Temp Sensor 6 Latched Alert Signal.	0x0	R/W1C
5	TEMPSENS_ALERT_STATUS_TS_5	Temp Sensor 5 Latched Alert Signal.	0x0	R/W1C
4	TEMPSENS_ALERT_STATUS_TS_4	Temp Sensor 4 Latched Alert Signal.	0x0	R/W1C
3	TEMPSENS_ALERT_STATUS_TS_3	Temp Sensor 3 Latched Alert Signal.	0x0	R/W1C
2	TEMPSENS_ALERT_STATUS_TS_2	Temp Sensor 2 Latched Alert Signal.	0x0	R/W1C
1	TEMPSENS_ALERT_STATUS_TS_1	Temp Sensor 1 Latched Alert Signal.	0x0	R/W1C
0	TEMPSENS_ALERT_STATUS_TS_0	Temp Sensor 0 Latched Alert Signal.	0x0	R/W1C

TEMPERATURE SENSORS SHUTDOWN STATUS REGISTER

Address: 0x192, Reset: 0x0000, Name: TSENS_SHTD_STAT

This register reports when a temperature sensor exceeds 130°C and shuts down the DAC or DACs output associated with that sensor.

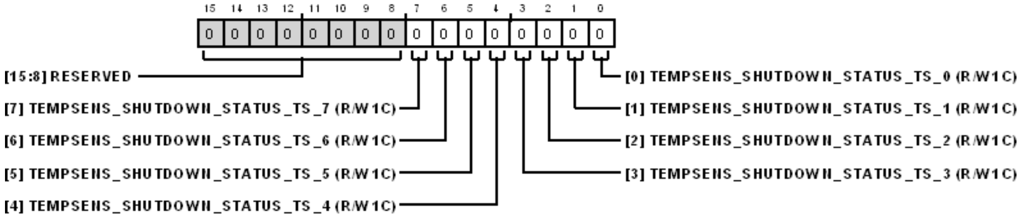

Figure 113. Temperature Sensors Shutdown Status Register

Table 64. Bit Descriptions for TSENS_SHTD_STAT

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	TEMPSENS_SHUTDOWN_STATUS_TS_7	Temp Sensor 7 Latched Shutdown Signal.	0x0	R/W1C
6	TEMPSENS_SHUTDOWN_STATUS_TS_6	Temp Sensor 6 Latched Shutdown Signal.	0x0	R/W1C
5	TEMPSENS_SHUTDOWN_STATUS_TS_5	Temp Sensor 5 Latched Shutdown Signal.	0x0	R/W1C
4	TEMPSENS_SHUTDOWN_STATUS_TS_4	Temp Sensor 4 Latched Shutdown Signal.	0x0	R/W1C
3	TEMPSENS_SHUTDOWN_STATUS_TS_3	Temp Sensor 3 Latched Shutdown Signal.	0x0	R/W1C
2	TEMPSENS_SHUTDOWN_STATUS_TS_2	Temp Sensor 2 Latched Shutdown Signal.	0x0	R/W1C
1	TEMPSENS_SHUTDOWN_STATUS_TS_1	Temp Sensor 1 Latched Shutdown Signal.	0x0	R/W1C
0	TEMPSENS_SHUTDOWN_STATUS_TS_0	Temp Sensor 0 Latched Shutdown Signal.	0x0	R/W1C

TEMPERATURE SENSORS STATUS TO $\overline{\text{ALARM}}$ PIN ENABLE REGISTER

Address: 0x194, Reset: 0x0000, Name: ALARMB_TSENS_EN

This register enables/disables the alarm and shutdown report through the pin for the specific temperature sensor.

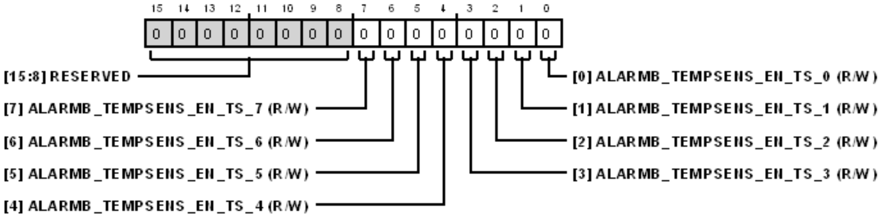

Figure 114. Temperature Sensors Status to $\overline{\text{ALARM}}$ Pin Enable Register

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

Table 65. Bit Descriptions for ALARMB_TSENS_EN

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	ALARMB_TEMPSENS_EN_TS_7	Temp Sensor 7 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
6	ALARMB_TEMPSENS_EN_TS_6	Temp Sensor 6 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
5	ALARMB_TEMPSENS_EN_TS_5	Temp Sensor 5 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
4	ALARMB_TEMPSENS_EN_TS_4	Temp Sensor 4 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
3	ALARMB_TEMPSENS_EN_TS_3	Temp Sensor 3 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
2	ALARMB_TEMPSENS_EN_TS_2	Temp Sensor 2 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
1	ALARMB_TEMPSENS_EN_TS_1	Temp Sensor 1 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
0	ALARMB_TEMPSENS_EN_TS_0	Temp Sensor 0 Shtdw/Alert Enable to Drive $\overline{\text{ALARM}}$ Pin. 0: Disabled. 1: Enabled.	0x0	R/W

ALERT/SHUTDOWN STATUS SIGNALS TO $\overline{\text{ALARM}}$ PIN SELECT REGISTER

Address: 0x196, Reset: 0x0000, Name: ALARMB_TSENS_SEL

This register enables/disables the alarm and shutdown report through the pin for the specific temperature sensor.

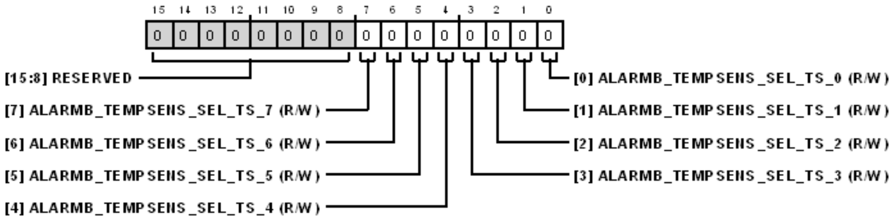

Figure 115. Alert/Shutdown Status Signals to $\overline{\text{ALARM}}$ Pin Select Register

Table 66. Bit Descriptions for ALARMB_TSENS_SEL

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	ALARMB_TEMPSENS_SEL_TS_7	Temp Sensor 7 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
6	ALARMB_TEMPSENS_SEL_TS_6	Temp Sensor 6 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
5	ALARMB_TEMPSENS_SEL_TS_5	Temp Sensor 5 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
4	ALARMB_TEMPSENS_SEL_TS_4	Temp Sensor 4 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
3	ALARMB_TEMPSENS_SEL_TS_3	Temp Sensor 3 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
2	ALARMB_TEMPSENS_SEL_TS_2	Temp Sensor 2 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
1	ALARMB_TEMPSENS_SEL_TS_1	Temp Sensor 1 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin.	0x0	R/W
0	ALARMB_TEMPSENS_SEL_TS_0	Temp Sensor 0 Shtdw/Alert Selector to Drive $\overline{\text{ALARM}}$ Pin. 0: Shutdown status signal selected. 1: Alert status signal selected.	0x0	R/W

DISABLE CHANNEL BY TEMP SENSOR SHUTDOWN REGISTER

Address: 0x198, Reset: 0x0000, Name: TSENS_SHTD_EN_CH

This register enables/disables the shutdown for the specific channel.

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

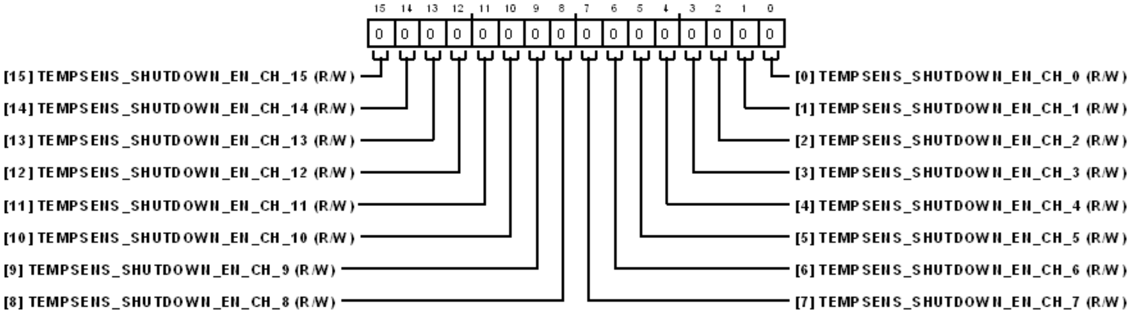

Figure 116. Disable Channel by Temp Sensor Shutdown Register

Table 67. Bit Descriptions for TSENS_SHTD_EN_CH

Bits	Bit Name	Description	Reset	Access
15	TEMPSENS_SHUTDOWN_EN_CH_15	Channel 15 Shutdown by Temp Sensor 7.	0x0	R/W
14	TEMPSENS_SHUTDOWN_EN_CH_14	Channel 14 Shutdown by Temp Sensor 7.	0x0	R/W
13	TEMPSENS_SHUTDOWN_EN_CH_13	Channel 13 Shutdown by Temp Sensor 6.	0x0	R/W
12	TEMPSENS_SHUTDOWN_EN_CH_12	Channel 12 Shutdown by Temp Sensor 6.	0x0	R/W
11	TEMPSENS_SHUTDOWN_EN_CH_11	Channel 11 Shutdown by Temp Sensor 5.	0x0	R/W
10	TEMPSENS_SHUTDOWN_EN_CH_10	Channel 10 Shutdown by Temp Sensor 5.	0x0	R/W
9	TEMPSENS_SHUTDOWN_EN_CH_9	Channel 9 Shutdown by Temp Sensor 4.	0x0	R/W
8	TEMPSENS_SHUTDOWN_EN_CH_8	Channel 8 Shutdown by Temp Sensor 4.	0x0	R/W
7	TEMPSENS_SHUTDOWN_EN_CH_7	Channel 7 Shutdown by Temp Sensor 3.	0x0	R/W
6	TEMPSENS_SHUTDOWN_EN_CH_6	Channel 6 Shutdown by Temp Sensor 3.	0x0	R/W
5	TEMPSENS_SHUTDOWN_EN_CH_5	Channel 5 Shutdown by Temp Sensor 2.	0x0	R/W
4	TEMPSENS_SHUTDOWN_EN_CH_4	Channel 4 Shutdown by Temp Sensor 2.	0x0	R/W
3	TEMPSENS_SHUTDOWN_EN_CH_3	Channel 3 Shutdown by Temp Sensor 1.	0x0	R/W
2	TEMPSENS_SHUTDOWN_EN_CH_2	Channel 2 Shutdown by Temp Sensor 1.	0x0	R/W
1	TEMPSENS_SHUTDOWN_EN_CH_1	Channel 1 Shutdown by Temp Sensor 0.	0x0	R/W
0	TEMPSENS_SHUTDOWN_EN_CH_0	Channel 0 Shutdown by Temp Sensor 0. 0: The Temp Sensor does not disable this channel. 1: The Temp Sensor disables this channel.	0x0	R/W

DISABLE DEGLITCHING BY CHANNEL REGISTER

Address: 0x19A, Reset: 0x0000, Name: DAC_DIS_DEGLITCH_CH

This register enables or disables the output deglitcher of the corresponding DAC.

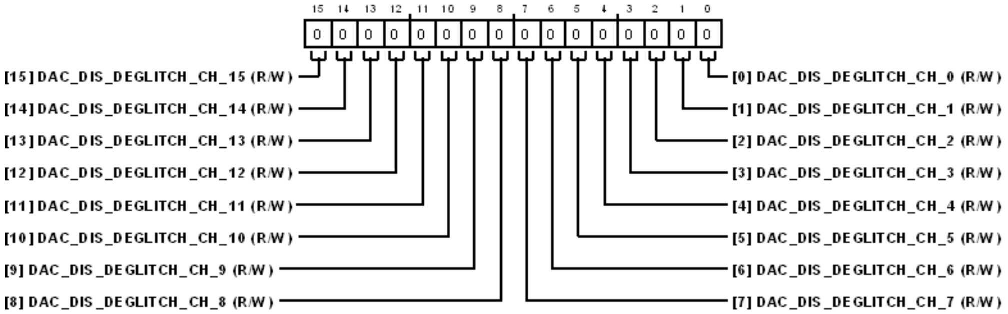

Figure 117. Disable Deglitching by Channel Register

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

Table 68. Bit Descriptions for DAC_DIS_DEGLITCH_CH

Bits	Bit Name	Description	Reset	Access
15	DAC_DIS_DEGLITCH_CH_15	Channel 15 DAC Deglitcher Disable.	0x0	R/W
14	DAC_DIS_DEGLITCH_CH_14	Channel 14 DAC Deglitcher Disable.	0x0	R/W
13	DAC_DIS_DEGLITCH_CH_13	Channel 13 DAC Deglitcher Disable.	0x0	R/W
12	DAC_DIS_DEGLITCH_CH_12	Channel 12 DAC Deglitcher Disable.	0x0	R/W
11	DAC_DIS_DEGLITCH_CH_11	Channel 11 DAC Deglitcher Disable.	0x0	R/W
10	DAC_DIS_DEGLITCH_CH_10	Channel 10 DAC Deglitcher Disable.	0x0	R/W
9	DAC_DIS_DEGLITCH_CH_9	Channel 9 DAC Deglitcher Disable.	0x0	R/W
8	DAC_DIS_DEGLITCH_CH_8	Channel 8 DAC Deglitcher Disable.	0x0	R/W
7	DAC_DIS_DEGLITCH_CH_7	Channel 7 DAC Deglitcher Disable.	0x0	R/W
6	DAC_DIS_DEGLITCH_CH_6	Channel 6 DAC Deglitcher Disable.	0x0	R/W
5	DAC_DIS_DEGLITCH_CH_5	Channel 5 DAC Deglitcher Disable.	0x0	R/W
4	DAC_DIS_DEGLITCH_CH_4	Channel 4 DAC Deglitcher Disable.	0x0	R/W
3	DAC_DIS_DEGLITCH_CH_3	Channel 3 DAC Deglitcher Disable.	0x0	R/W
2	DAC_DIS_DEGLITCH_CH_2	Channel 2 DAC Deglitcher Disable.	0x0	R/W
1	DAC_DIS_DEGLITCH_CH_1	Channel 1 DAC Deglitcher Disable.	0x0	R/W
0	DAC_DIS_DEGLITCH_CH_0	Channel 0 DAC Deglitcher Disable. 0: DAC deglitching enabled. 1: DAC deglitching disabled.	0x0	R/W

DAC INTERRUPTS ENABLE REGISTER

Address: 0x19C, Reset: 0x0000, Name: DAC_INT_EN

This register has two functions: Enable/disable CRC error reporting on the ALARM pin and no function routed to the $\overline{\text{ALARM}}$ pin.

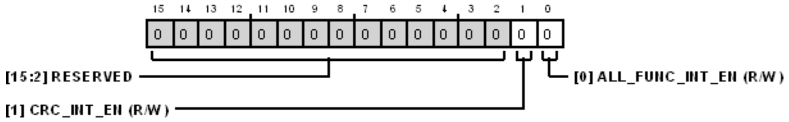

Figure 118. DAC Interrupts Enable Register

Table 69. Bit Descriptions for DAC_INT_EN

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	CRC_INT_EN	Enable CRC Error Interrupt on $\overline{\text{ALARM}}$ Pin.	0x0	R/W
0	ALL_FUNC_INT_EN	All Function Disabled Interrupt Enabled and Driving $\overline{\text{ALARM}}$. 0: Signal ALL_FUNC_INT_STAT not routed to $\overline{\text{ALARM}}$ pin. 1: Signal ALL_FUNC_INT_STAT routed to $\overline{\text{ALARM}}$ pin.	0x0	R/W

COMBINED FUNCTION GENERATORS STATUS REGISTER

Address: 0x19E, Reset: 0x0000, Name: ALL_FUNC_INT_STAT

This register indicates when all digital functions complete their cycle and finish their operations.

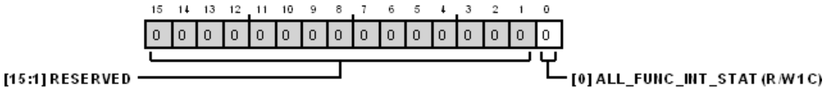

Figure 119. Combined Function Generators Status Register

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

Table 70. Bit Descriptions for ALL_FUNC_INT_STAT

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	ALL_FUNC_INT_STAT	All Functions Disabled Interrupt Status. 0: Not all the function generators have finished yet. 1: All function generators have finished operation.	0x0	R/W1C

FUNCTION GENERATOR BUSY LIVE FLAGS REGISTER

Address: 0x1A0, Reset: 0x0000, Name: FUNC_BUSY

This register indicates when a digital function for a specific channel is still busy.

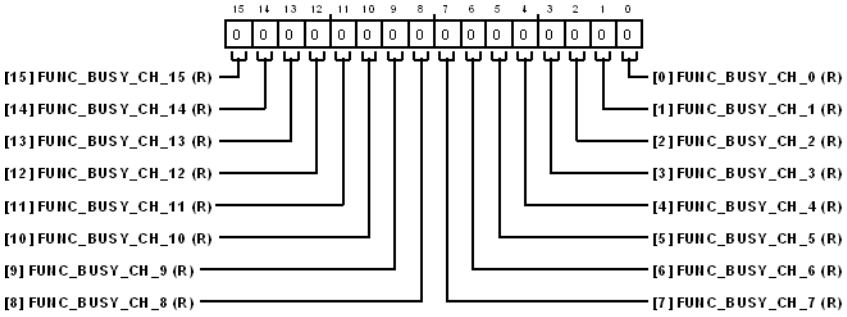

Figure 120. Function Generator Busy Live Flags Register

Table 71. Bit Descriptions for FUNC_BUSY

Bits	Bit Name	Description	Reset	Access
15	FUNC_BUSY_CH_15	Channel 15 Function Generator Busy Live Flag.	0x0	R
14	FUNC_BUSY_CH_14	Channel 14 Function Generator Busy Live Flag.	0x0	R
13	FUNC_BUSY_CH_13	Channel 13 Function Generator Busy Live Flag.	0x0	R
12	FUNC_BUSY_CH_12	Channel 12 Function Generator Busy Live Flag.	0x0	R
11	FUNC_BUSY_CH_11	Channel 11 Function Generator Busy Live Flag.	0x0	R
10	FUNC_BUSY_CH_10	Channel 10 Function Generator Busy Live Flag.	0x0	R
9	FUNC_BUSY_CH_9	Channel 9 Function Generator Busy Live Flag.	0x0	R
8	FUNC_BUSY_CH_8	Channel 8 Function Generator Busy Live Flag.	0x0	R
7	FUNC_BUSY_CH_7	Channel 7 Function Generator Busy Live Flag.	0x0	R
6	FUNC_BUSY_CH_6	Channel 6 Function Generator Busy Live Flag.	0x0	R
5	FUNC_BUSY_CH_5	Channel 5 Function Generator Busy Live Flag.	0x0	R
4	FUNC_BUSY_CH_4	Channel 4 Function Generator Busy Live Flag.	0x0	R
3	FUNC_BUSY_CH_3	Channel 3 Function Generator Busy Live Flag.	0x0	R
2	FUNC_BUSY_CH_2	Channel 2 Function Generator Busy Live Flag.	0x0	R
1	FUNC_BUSY_CH_1	Channel 1 Function Generator Busy Live Flag.	0x0	R
0	FUNC_BUSY_CH_0	Channel 0 Function Generator Busy Live Flag. 0: Function generator is free. 1: Function generator is busy.	0x0	R

REFERENCE SOURCE SELECT REGISTER

Address: 0x1A2, Reset: 0x0000, Name: REF_SEL

This register selects between the internal and external reference voltages.

REGISTER DETAILS: PRODUCT-SPECIFIC DAC REGISTER MAP

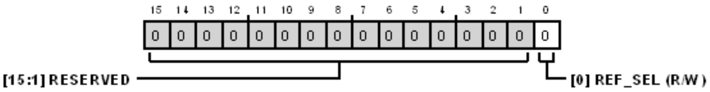

Figure 121. Reference Source Select Register

Table 72. Bit Descriptions for REF_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	REF_SEL	Reference Select. 0: External reference selected. 1: Internal reference selected.	0x0	R/W

INITIALIZATION CRC ERROR STATUS REGISTER

Address: 0x1A4, Reset: 0x0000, Name: INIT_CRC_ERR_STAT

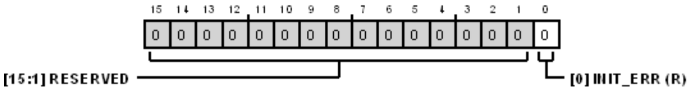

Figure 122. Initialization CRC Error Status Register

Table 73. Bit Descriptions for INIT_CRC_ERR_STAT

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	INIT_ERR	Internal CRC Initialization Error Status Flag. Set to 1'b1 if an internal CRC error is detected during power up. 0: Internal Refresh OK. The internal refresh sequence did not detect any errors. 1: Internal Refresh Error. The internal refresh sequence detected errors.	0x0	R

REGISTER DETAILS: HOTPATH DAC REGISTER MAP

MULTI DEVICE SW LDAC MODE 0 REGISTER

Address: 0x1A8, Reset: 0x0000, Name: MULTI_DEV_SW_LDAC_0

This register sends a software LDAC update to the selected devices that share the SPI lines but have different addresses, using the ID0 and ID1 pins. The selection is done on a per-device basis corresponding to the configured bit field.

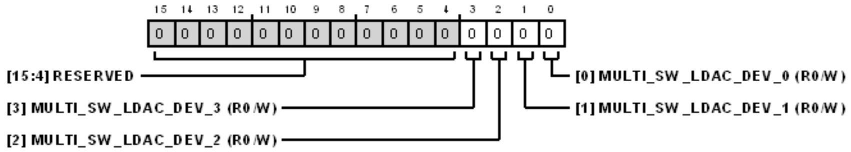

Figure 123. Multi Device SW LDAC Mode 0 Register

Table 74. Bit Descriptions for MULTI_DEV_SW_LDAC_0

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	MULTI_SW_LDAC_DEV_3	Multi SW LDAC Trigger Device 3.	0x0	R0/W
2	MULTI_SW_LDAC_DEV_2	Multi SW LDAC Trigger Device 2.	0x0	R0/W
1	MULTI_SW_LDAC_DEV_1	Multi SW LDAC Trigger Device 1.	0x0	R0/W
0	MULTI_SW_LDAC_DEV_0	Multi SW LDAC Trigger Device 0.	0x0	R0/W

MULTI INPUT DEVICE 0 REGISTER

Address: 0x1AA, Reset: 0x0000, Name: MULTI_INPUT_DEV_0

This register updates the input registers for the channels at Device ID = 0, as selected in MULTI_INPUT_SEL. This works similarly to MULTI_INPUT.

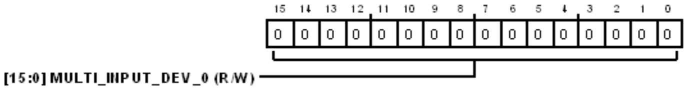

Figure 124. Multi Input Device 0 Register

Table 75. Bit Descriptions for MULTI_INPUT_DEV_0

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_INPUT_DEV_0	Multi Input Device 0.	0x0	R/W

MULTI INPUT DEVICE 1 REGISTER

Address: 0x1AC, Reset: 0x0000, Name: MULTI_INPUT_DEV_1

This register updates the input registers for the channels at Device ID = 1, as selected in MULTI_INPUT_SEL. This works similarly to MULTI_INPUT.

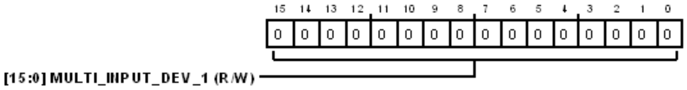

Figure 125. Multi Input Device 1 Register

Table 76. Bit Descriptions for MULTI_INPUT_DEV_1

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_INPUT_DEV_1	Multi Input Device 1.	0x0	R/W

REGISTER DETAILS: HOTPATH DAC REGISTER MAP

MULTI INPUT DEVICE 2 REGISTER

Address: 0x1AE, Reset: 0x0000, Name: MULTI_INPUT_DEV_2

This register updates the input registers for the channels at Device ID = 2, as selected in MULTI_INPUT_SEL. This works similarly to MULTI_INPUT.

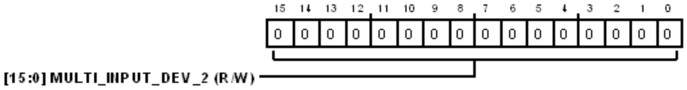

Figure 126. Multi Input Device 2 Register

Table 77. Bit Descriptions for MULTI_INPUT_DEV_2

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_INPUT_DEV_2	Multi Input Device 2.	0x0	R/W

MULTI INPUT DEVICE 3 REGISTER

Address: 0x1B0, Reset: 0x0000, Name: MULTI_INPUT_DEV_3

This register updates the input registers for the channels at Device ID = 3, as selected in MULTI_INPUT_SEL. This works similarly to MULTI_INPUT.

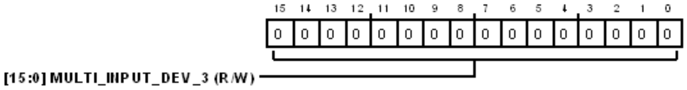

Figure 127. Multi Input Device 3 Register

Table 78. Bit Descriptions for MULTI_INPUT_DEV_3

Bits	Bit Name	Description	Reset	Access
[15:0]	MULTI_INPUT_DEV_3	Multi Input Device 3.	0x0	R/W

MULTI DEVICE SW LDAC MODE 1 REGISTER

Address: 0x1B2, Reset: 0x0000, Name: MULTI_DEV_SW_LDAC_1

Software LDAC trigger for individually selected channels on all devices. When a bit field is set high, the DAC register of the corresponding channel gets updated with input register data. LDAC_HW_SW[LDAC_HW_SW_CH_n] must be set to 1.

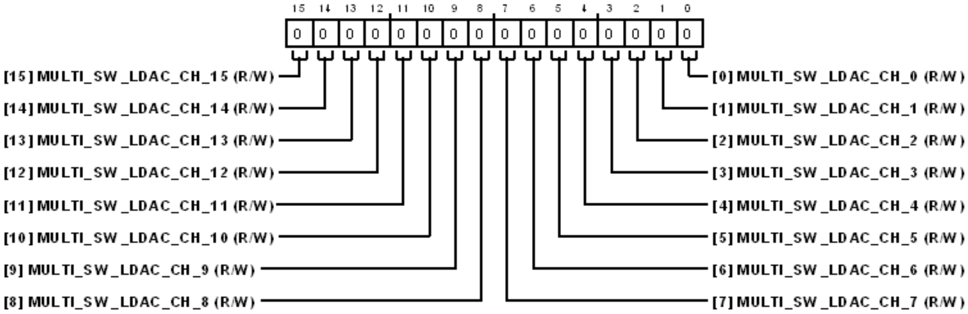

Figure 128. Multi Device SW LDAC Mode 1 Register

Table 79. Bit Descriptions for MULTI_DEV_SW_LDAC_1

Bits	Bit Name	Description	Reset	Access
15	MULTI_SW_LDAC_CH_15	Multi Device SW LDAC Trigger Channel 15.	0x0	R/W

REGISTER DETAILS: HOTPATH DAC REGISTER MAP

Table 79. Bit Descriptions for MULTI_DEV_SW_LDAC_1 (Continued)

Bits	Bit Name	Description	Reset	Access
14	MULTI_SW_LDAC_CH_14	Multi Device SW LDAC Trigger Channel 14.	0x0	R/W
13	MULTI_SW_LDAC_CH_13	Multi Device SW LDAC Trigger Channel 13.	0x0	R/W
12	MULTI_SW_LDAC_CH_12	Multi Device SW LDAC Trigger Channel 12.	0x0	R/W
11	MULTI_SW_LDAC_CH_11	Multi Device SW LDAC Trigger Channel 11.	0x0	R/W
10	MULTI_SW_LDAC_CH_10	Multi Device SW LDAC Trigger Channel 10.	0x0	R/W
9	MULTI_SW_LDAC_CH_9	Multi Device SW LDAC Trigger Channel 9.	0x0	R/W
8	MULTI_SW_LDAC_CH_8	Multi Device SW LDAC Trigger Channel 8.	0x0	R/W
7	MULTI_SW_LDAC_CH_7	Multi Device SW LDAC Trigger Channel 7.	0x0	R/W
6	MULTI_SW_LDAC_CH_6	Multi Device SW LDAC Trigger Channel 6.	0x0	R/W
5	MULTI_SW_LDAC_CH_5	Multi Device SW LDAC Trigger Channel 5.	0x0	R/W
4	MULTI_SW_LDAC_CH_4	Multi Device SW LDAC Trigger Channel 4.	0x0	R/W
3	MULTI_SW_LDAC_CH_3	Multi Device SW LDAC Trigger Channel 3.	0x0	R/W
2	MULTI_SW_LDAC_CH_2	Multi Device SW LDAC Trigger Channel 2.	0x0	R/W
1	MULTI_SW_LDAC_CH_1	Multi Device SW LDAC Trigger Channel 1.	0x0	R/W
0	MULTI_SW_LDAC_CH_0	Multi Device SW LDAC Trigger Channel 0.	0x0	R/W

INPUT DEVICE 0 REGISTER

Address: 0x1B4 to 0x1D2 (Increments of 2), Reset: 0x0000, Name: INPUT_DEV_0_CHn

This register updates DAC_INPUT_A_CH of Device ID = 0.

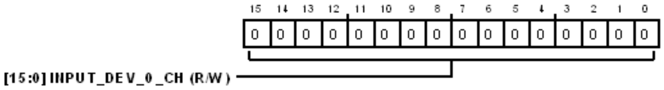

Figure 129. Input Device 0 Register

Table 80. Bit Descriptions for INPUT_DEV_0_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	INPUT_DEV_0_CH	Input A Device 0 Code.	0x0	R/W

INPUT DEVICE 1 REGISTER

Address: 0x1D4 to 0x1F2 (Increments of 2), Reset: 0x0000, Name: INPUT_DEV_1_CHn

This register updates DAC_INPUT_A_CH of Device ID = 1.

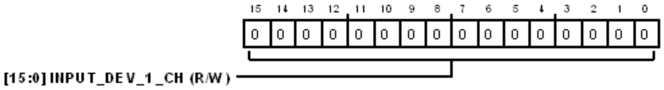

Figure 130. Input Device 1 Register

Table 81. Bit Descriptions for INPUT_DEV_1_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	INPUT_DEV_1_CH	Input A Device 1 Code.	0x0	R/W

REGISTER DETAILS: HOTPATH DAC REGISTER MAP

INPUT DEVICE 2 REGISTER

Address: 0x1F4 to 0x212 (Increments of 2), Reset: 0x0000, Name: INPUT_DEV_2_CHn

This register updates DAC_INPUT_A_CH of Device ID = 2.

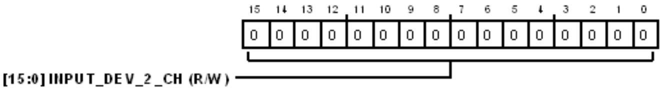

Figure 131. Input Device 2 Register

Table 82. Bit Descriptions for INPUT_DEV_2_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	INPUT_DEV_2_CH	Input A Device 2 Code.	0x0	R/W

INPUT DEVICE 3 REGISTER

Address: 0x214 to 0x232 (Increments of 2), Reset: 0x0000, Name: INPUT_DEV_3_CHn

This register updates DAC_INPUT_A_CH of Device ID = 3.

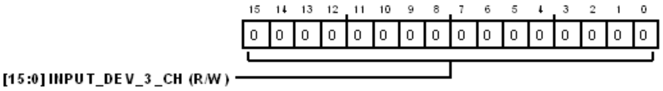

Figure 132. Input Device 3 Register

Table 83. Bit Descriptions for INPUT_DEV_3_CHn

Bits	Bit Name	Description	Reset	Access
[15:0]	INPUT_DEV_3_CH	Input A Device 3 Code.	0x0	R/W

OUTLINE DIMENSIONS

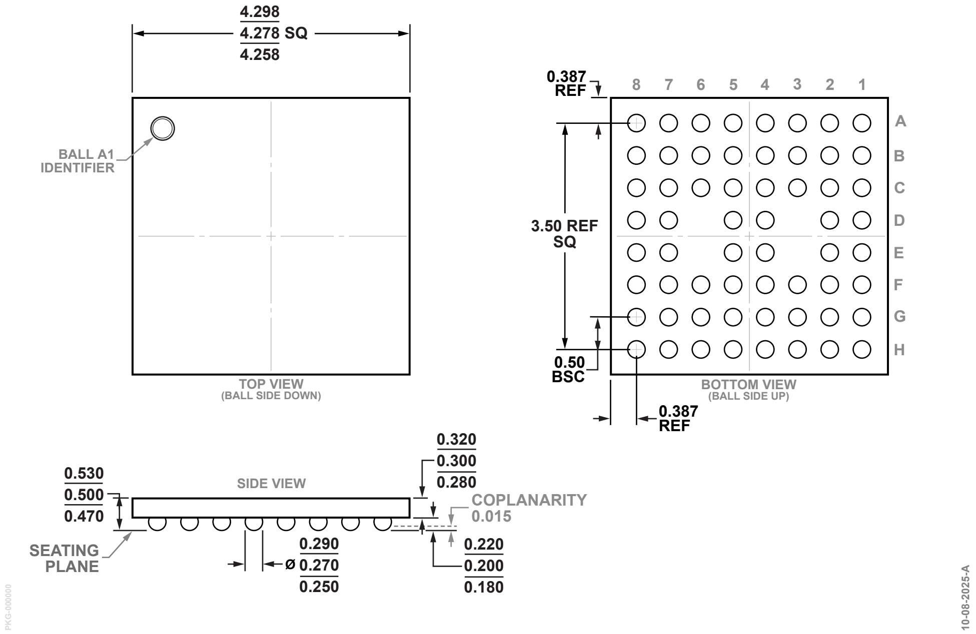

Figure 133. 60-Ball Wafer Level Chip-Scale Package [WLCSP]
(CB-60-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD5529RBCBZ16-RL	−40°C to +125°C	60-Ball [WLCSP]	Reel, 5000	CB-60-1
AD5529RBCBZ16-RL7	−40°C to +125°C	60-Ball [WLCSP]	Reel7, 1500	CB-60-1

[1] Z = RoHS Compliant Part.

Updated: April 30, 2026

EVALUATION BOARDS

Model[1]	Description
EVAL-AD5529R-ARDZ	Evaluation Board

[1] Z = RoHS Compliant Part.